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PREFACE

This issue of international journal "Electronics" includes 10 the most interesting papers selected from the 4th Symposium on Industrial Electronics – INDEL 2002, and 3 regular papers.

The 4th Symposium on Industrial Electronics – INDEL 2002 was held in Banjaluka from November 14-16,2002. At the conference 98 authors and coauthors from 21 institutions both from academia and industry presented 55 papers. All papers are presented in conference proceedings. The main topics of the conference are: Analog and Digital Circuits, Power Electronics, Signal Processing, Materials and Components, Program Support for Control and Model, Identification and Process Control. The aim of the conference is the presentation of the development and research results in the areas related to the conference topics.

Special plenary session devoted to the jubilee: "40 years of Faculty of Electrical Engineering in Banjaluka" was held during the conference.

I would like to express my gratitude to the authors and invite all researches, who are interested in the field on Industrial Electronics, to present their development and research results in the next issue of international journal "Electronics".

Also, I would like to invite all readers of the "Electronics" journal to take active participation at the next 5th Symposium on Industrial Electronics – INDEL 2004, which will be organized in Banjaluka, Republic of Srpska in October/November 2004.

Prof. dr Branko Dokić, Editor

3D-SIMULATION OF ELECTRICAL AND THERMAL CHARACTERISTICS OF ELECTRIC CONTACTS

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Abstract – *Basic features expected from electric contacts in circuit applications are low and stable contact resistance, high electric and heat conductivity, good resistance to welding and wear. In order to fulfill all these requirements contact material should be selected carefully. This paper deals with the simulation of electrical and thermal characteristics of contacts. For various materials, types of contacts and loads the distributions of electric potential, current density and Joule's heat were generated, along with the contact temperature dependences on load levels. Simulated characteristics have been analyzed from the point of view of the evaluation contact material proper to given load.*

1. INTRODUCTION

In spite of an intensive development of semiconductor devices and their often exploitation in electric circuit control, switches and relays still play an important role. They are used in a variety of applications, covering a broad spectrum of industrial activity including electronic and electric industry, manufacture of household appliances, automotive and aerospace engineering. Their function is based on the mechanical action of metal parts known as electric contacts.

Due to versatility of switches and relays, electric contacts are available in different sizes, forms (rivets, profiles, blanks, disks, buttons, etc.) and types (solid and clad). Solid contacts are entirely made of highly conductive materials (precious metals or their alloys), while clad ones are mostly produced of copper with their tops being plated by alloy of precious metals.

The most troublesome aspect of contact evaluation is in choosing the material and predicting performance under a multiplicity of operating conditions. To a large extent, difficulty results from a lack of information on the parameters affecting contact performance. Additional problems can arise during the contact operation as a consequence of improper material selection. They are associated with material transfer and pitting, arc erosion, sticking and welding, and lead to reducing of contact durability. In elimination of some of above-mentioned problems simulation of contact characteristics is used as a powerful CAD-CAE tool.

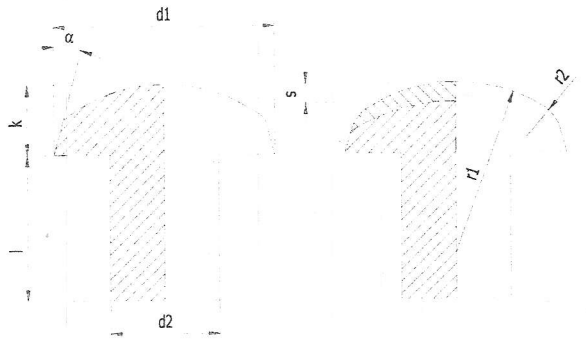
This contribution presents the results of 3D simulation of electrical and thermal characteristics of rivet contacts. Simulation is carried out on solid and clad types of contacts by involving different materials and loads. Distributions of electric potential, current density and Joule's heat, as well as the contact temperature dependences on loads are generated for each contact type considered.

2. SIMULATION PROCEDURE

Three-dimensional simulation of contact characteristics was performed by numerical treatment of the complex physical problems. Software solves Maxwell's equations simultaneously with equations describing heat conduction/convection. It is based on the finite elements analysis (FEA) and utilizes different adaptive grid refinement techniques to reach the fastest solution. Through the graphical user interface the shapes and dimensions of contacts are defined along with material parameters (physical, electrical and thermal ones), and load conditions (the values of electric potential on both contact surfaces).

3. CONTACT PARAMETERS

For the simulation purpose rivet contacts were selected, since this form is commonly used in different applications. Their cross-section for solid and clad type is shown in Fig.1, while dimensions are listed in Table 1.



(a) (b)

Fig. 1. *Cross-section of solid (a) and clad (b) rivet electric contact*

Table 1. *Dimensions of rivet contact [1]*

Contact dimension	Value (mm)
Head diameter - d_1	3
Total head height – k	0.7
Shank diameter - d_2	1.5
Contact layer height – s	0.35
Shank length – l	1.5
Head and contact rounding radii – r_1 and r_2	0.5 and 0.1
Head taper angle - α	15°

Contact materials (kind and composition) were chosen according to data from catalogues of the major world manufacturers [2-4]. Silver with purity of 99.99% was selected to be material for solid contacts, while copper and one of the following alloys: 90%Ag-10%Ni, 90%Ag-10%CdO, 60%Ag-40%Pd were used as materials for clad contacts. Ag-Ni and Ag-CdO alloys are very close to the pure silver in electrical and thermal conductivity, but they exhibit better mechanical properties. Ag-Pd alloy is high in hardness making the contact resistive to deformation and arc erosion. Its high melting point provides good resistance to material transport. On the other hand, Ag-Pd alloy is less conductive (electrically and thermally) than Ag-Ni and Ag-CdO alloys. Values of the physical, electrical and thermal parameters of used materials are summarized in Table 2.

Table 2: *Physical, electrical and thermal parameters of contact materials* [2-4]

Material	Melting point (K)	Specific electrical resistivity (Ωm)	Temperature coefficient of specific electrical resistivity (K^{-1})	Thermal conductivity (W/mK)
Cu	1356	$1.69 \cdot 10^{-8}$	$4.29 \cdot 10^{-3}$	401
Ag	1234	$1.62 \cdot 10^{-8}$	$4.10 \cdot 10^{-3}$	419
90%Ag-10%Ni	1234	$1.89 \cdot 10^{-8}$		390
90%Ag-10%CdO	1234	$2.08 \cdot 10^{-8}$		330
60%Ag-40%Pd	1450	$22 \cdot 10^{-8}$		50

During the simulation, contacts were biased in the following manner: one contact surface was kept at the zero potential, while the other was supplied by the potential that, for different contacts, had taken value from the range of $1 \cdot 10^{-5} \div 5 \cdot 10^{-3}$ V. According to these potential differences and resistivity of materials, currents in contacts were ranged from 0.28A up to 83.9A.

In order to obtain thermal characteristics more accurately, temperature dependence of electrical resistivity was taken into account in all calculations. For heat transmission between contact and surroundings convection regime was assumed, since in that case contacts were treated in an isolated state (without assemblies). Thus, convection coefficient of 28.4W/m^{2}K (valid for air-metal system) and ambient temperature of 300 K were used in thermal simulation.

4. RESULTS

Fig. 2 shows how distribution of the electric potential throughout the solid Ag (Fig. 2a), clad Cu/Ag-Ni (Fig. 2b) and clad Cu/Ag-Pd (Fig. 2c) contact. Presented distributions were generated at potential difference of $2 \cdot 10^{-4}$V, i.e. for currents of 11.4A, 10.8A and 5.6A, respectively.

As can be seen from the Fig. 2, potential distribution in solid Ag contact is very similar to that in clad Cu/Ag-Ni contact. Large difference in electric potential appears only in the case of clad Cu/Ag-Pd contact, which is attributed to the conductivity of involved alloy. Electrical and thermal conductivity of Ag-Pd alloy is one order of magnitude lower than that of other materials considered (see Table 2).

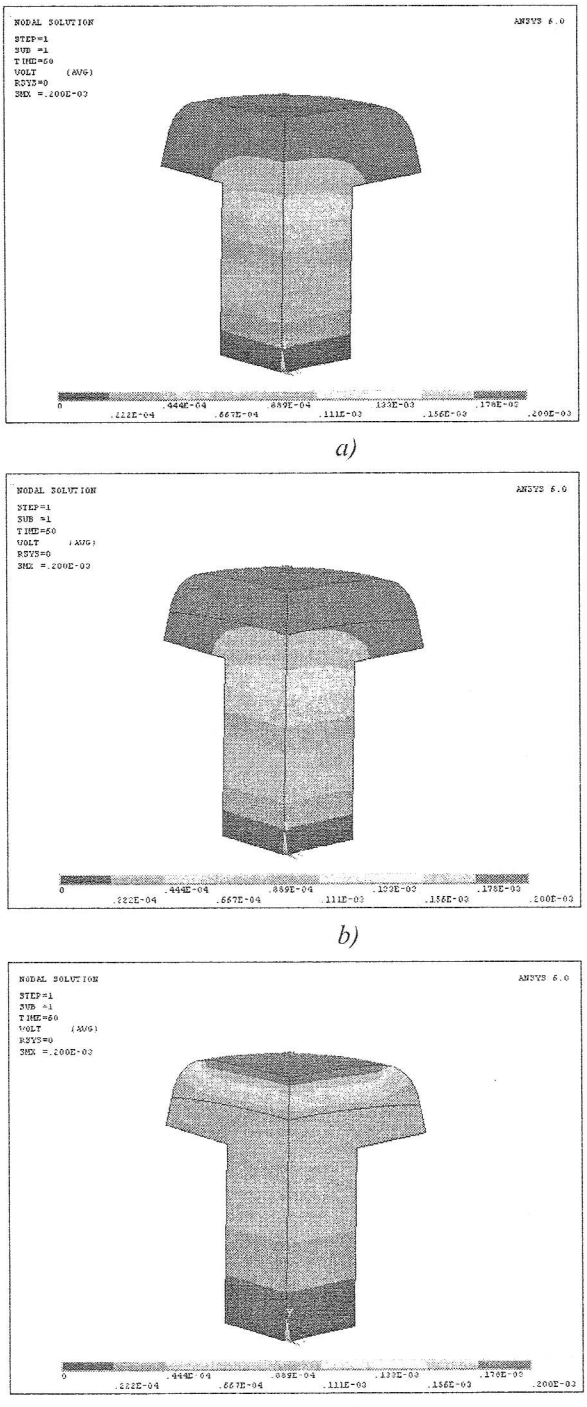


Fig. 2. *Distribution of electric potential in: a) solid Ag, b) clad Cu/Ag-Ni and c) clad Cu/Ag-Pd contacts*

Distribution of the current density in clad Cu/Ag-Ni contact (obtained at load voltage of $2 \cdot 10^{-4}$V) is shown in Fig. 3, using vector representation. Regions of contact where current density reaches the maximum can be easily determined from this figure. In rivet contacts the most critical region is the junction between head and shank where the contact geometry changes abruptly. For the contact presented in Fig. 3 maximum value of current density is $8.7 \cdot 10^6$A/m^2.

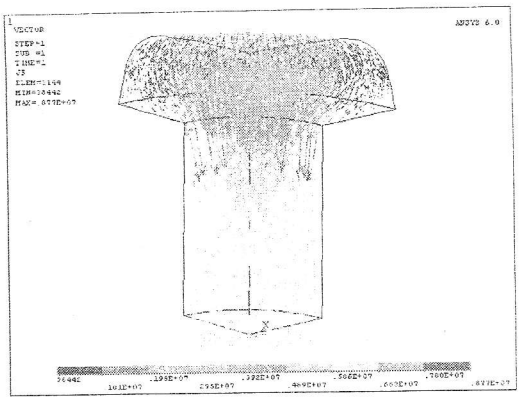


Fig. 3. Distribution of current density in Cu/Ag-Ni contact

Joule's heat generated in contact is directly related to the distribution of the current density, and its values inside the clad Cu/Ag-Ni contact are presented in Fig. 4. It is evident that head-shank junction represents "hot" area in the contact volume. In this area it is reasonable to expect initialization of different thermally activated degradation processes, among which material migration is the most dangerous for reliability of contacts.

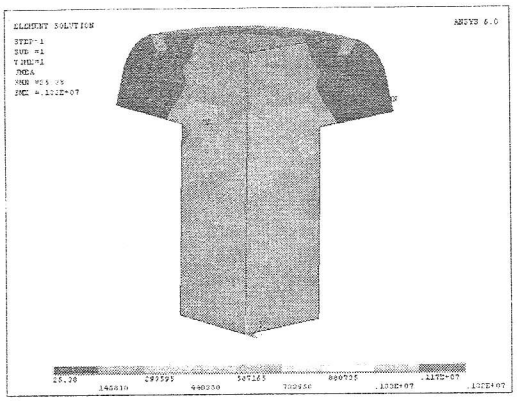


Fig. 4. Distribution of Joule's heat in clad Cu/Ag-Ni contact

In spite of the observed effect of heat accumulation, we have not found any significant difference in the temperature of various parts of contacts. As can be seen in Fig. 5, temperature is uniformly distributed throughout clad Cu/Ag-Ni contact. Reason for this is probably high conductivity of contact material contributing to the fast heat transmission and/or contact assembly omission contributing to the uniformity of surroundings.

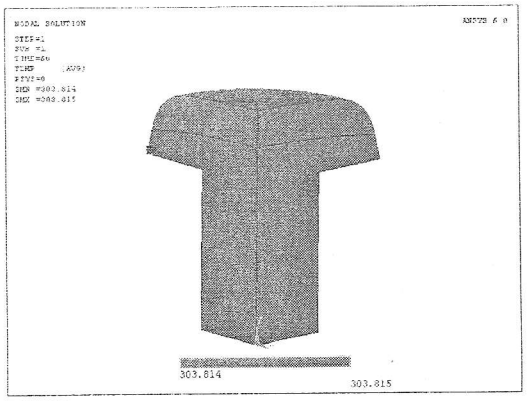


Fig. 5. Distribution of temperature in clad Cu/Ag-Ni contact

Dependencies of the contact temperatures on the current intensity are shown in Fig. 6 for different contact materials. One can see that for Ag, Cu/Ag-Ni and Cu/Ag-CdO contacts the temperature values are very close to each other for the whole range of currents used in the simulation. On the other hand, in Cu/Ag-Pd contact the temperatures reach the higher values, and differences become more significant (even over 200K) as current increases.

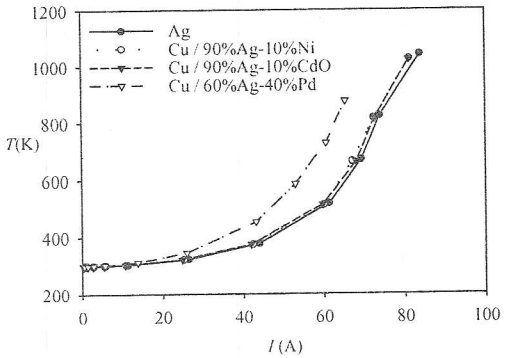


Fig. 6. Contact temperature vs. current intensity

Results from Fig. 6 could be useful in definition of contact applications from the aspect of their limiting by allowed current levels. Namely, only current levels at which temperature of contact does not exceed the melting point of contact material are allowed. Dependencies from Fig. 6 could be also useful in selection of an alternative contact material. When two materials have similar electrical and thermal characteristics, as it is the case with Ag-Ni and Ag-CdO alloys, appropriate material can be selected on the basis of any other property, for instance by ecological suitability. So, due to high toxicity of CdO, Ag-CdO alloy can be replaced by Ag-Ni alloy without any significant change in contact characteristics.

5. CONCLUSION

In the procedure of contact development simulation of electrical and thermal characteristics plays an important role. At specified geometry and contacting mode, simulation provides the data necessary to choose suitable contact material. On the other hand, at pre-set contact material, it enables definition of the limiting electrical conditions for the contact exploitation. On the basis of the simulation results some changes in contact geometry can be also suggested.

Finally, simulation of the contact characteristics can be helpful in considering some problems related to their reliability.

6. REFERENCES

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Acknowledgment

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VHDL-AMS COMPILER FOR ALECSIS SIMULATION ENVIRONMENT

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Abstract: *Mixed-signal and mixed-domain simulator Alecsis with its own object-oriented HDL, AleC++ provides a comprehensive design environment for verification of complex electronic circuits and non-electrical systems. In order to exploit good features of standardization VHDL-AMS compiler for Alecsis has developed. Basic principles of the compiler and its integration into Alecsis are described in this paper.*

Keywords: *electronic circuit, verification, simulation, HDL, compiler.*

1. INTRODUCTION

Modern application-specific integrated circuits (ASICs) and system-on-a chip (SoC) designs frequently contain both analog and digital subsystems, embedded software, and sometimes are used with optical, magnetic and/or micromechanical devices. Therefore, we have not only analogue/digital (mixed-signal) designs, but also mixed-domain integrated systems, where different physical processes interact. For development of such systems a powerful simulator and appropriate modeling language are needed with the ability to describe and analyze all these kinds of subsystems in the most efficient way. Recent development in the field of mixed-signal hardware description languages (HDLs) has been determined by the strong need for standardization. IEEE VHDL 1076.1-1999. (informally known as VHDL-AMS where AMS stands for analog and mixed-signal) [3], [5] and Verilog-AMS standards have been issued and they are intended to be universal tools for modeling and documentation of both analog and digital devices and physical models from other domains (mixed-domain models). However, in the industrial community it is already clear that standardization is not going to solve all problems, such as, for example, the fact that VHDL-AMS and Verilog-AMS can not be used for hardware/software co-simulation necessary in SoC design. One convenient solution is to enable the simulator to accept and integrate models developed in different languages. Such language-neutral simulation environment let designers use codes (descriptions) already written in standard HDLs which are portable between different EDA tools, while taking good features of the other language(s) to describe and test the components which can not be described in standard HDLs. Finally, the whole complex system can be verified using only one simulation tool. Mixed-language simulators are already available in the market (ADVance MS rom Mentor Graphics, SMASH from Dolphin Integration etc.). This paper describes one such approach. It discusses a method of co-simulation with our Alecsis simulator/language environment and VHDL-AMS pre-developed models.

Alecsis (Analogue and Logic Electronic Circuit Simulation System) [1] is a mixed-signal and mixed-domain simulator with its own object-oriented HDL named AleC++ suited for modeling and simulation of both digital and especially complex analogue models. Developed as a

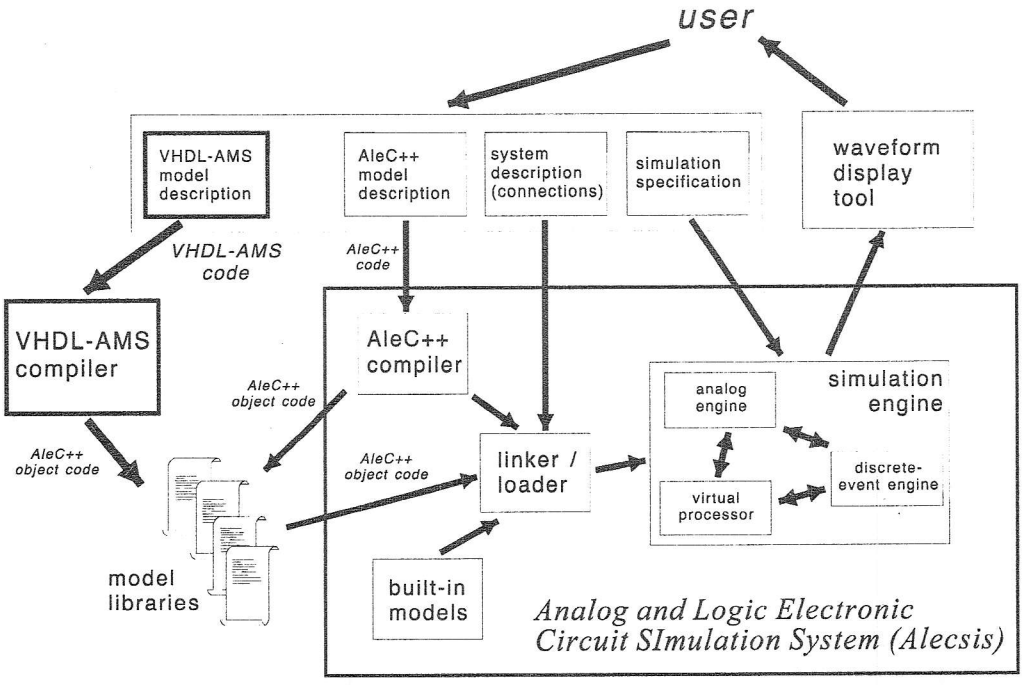

Figure 1. Organization of Alecsis simulator, with VHDL-AMS compiler.

superset of C++, AleC++ supports the good features of object-orientation that enables modeling in a natural way. As Alecsis can interpret C/C++ routines while executing hardware models, it is very convenient for descriptions of systems with embedded software. However, having in mind the importance of standard languages (great number of designers that use it, portable models, growing number of already developed models) and convenience of using mixed-language simulation environment we are developing VHDL-AMS compiler for Alecsis. The compiler enables accepting

of VHDL-AMS code and Alecsis simulation with as low designer intervention as possible.

Short description of Alecsis structure and the concept of integration of VHDL-AMS compiler into Alecsis simulation environment will be given at the beginning. After that the principles of mixed-language simulation will be explained, as well as AleC++ and VHDL-AMS code interaction. The fourth section gives an example of co-simulation and the last one is the conclusion.

7. ALECSIS SIMULATOR/VHDL-AMS COMPILER INTEGRATION

Since AleC++, the hardware description language of simulator Alecsis, is based on the programming language C++, a straightforward solution would be to compile the HDL code into appropriate object code, link it into the simulation kernel and directly execute (compiled simulation). However, the simulation process is simpler if the model code needs not to be compiled and linked to the simulation engine every time it is modified. For that reason interpreted simulation can be used in which model code is captured by the front-end analyzer and transformed into a suitable form for the simulator to execute. This transformation process is called elaboration and it generates a program to be interpreted by the simulator. The drawback of such approach is lack of code optimization, so the model interpretation is slow. Since model code is executed many times during the simulation run, the code optimization is of great importance.

Alecsis combines good features of both approaches. From the user's point of view AleC++ models can be used both in an interpreted and compiled simulation. However, even if the user chooses interpreted mode, the code is firstly compiled into AleC++ object code (internal binary format of the simulator Alecsis) and optimization is performed. AleC++ object code is used as an intermediate code for communication between different HDLs. After that the virtual processor interprets the generated object code. In compiled mode, the result of compilation is stored in the model libraries in AleC++ object code format. These compiled models can be later used in system description or in description of other models, and all global symbols will be resolved by the linker/loader before the simulation starts.

The simplest way to achieve AleC++/VHDL-AMS co-simulation is to use the existing simulation kernel of Alecsis simulator and to develop a new compiler for VHDL-AMS language [4]. Figure 1 shows the co-simulation concept. The structure of VHDL-AMS compiler is shown in Figure 2.

At first the compiler front-end analyses VHDL-AMS source code and generates the intermediate data structures. It consists of two usual building blocks: lexical analyzer (scanner) and syntax analyzer (parser) [2]. The lexical analyzer

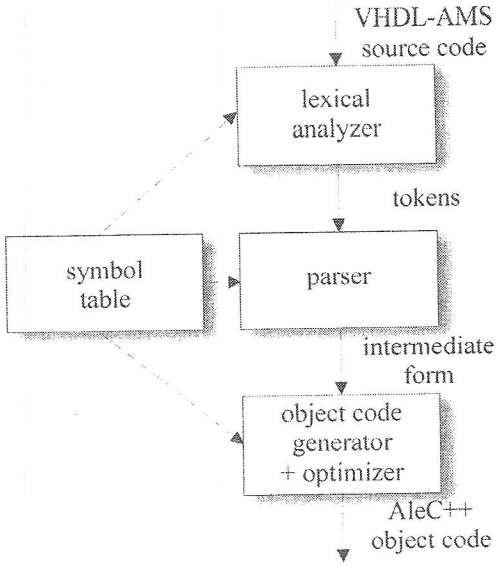

Figure 2. VHDL-AMS compiler structure

carries out the simplest level of structural analysis and groups the individual characters of the source code text into the logical entities having a collective meaning (tokens). The syntax analyzer then groups the simple elements identified by the scanner into the larger language constructs, such as entities, architectures, statements, loops and functions. The parser constructs binary trees followed by an intermediate form (called "three-address code" [2]). Also, in this phase the semantic analysis is performed which determines type of variables, signals, terminals and quantities, the size of arrays and so on. A symbol table is used to keep track of scope and binding information about names (see Figure 2). The compiler back-end takes generated intermediate data structures and produces AleC++ object code. The code optimisation is performed in this phase, too. It eliminates the unnecessary instructions, groups some instructions into one, discards the dead code (code that never executes), find the most frequently used variables and put them into registers etc. Alecsis implements only the local (peephole) optimisation that improves the quality of the generated object code while preserving pretty short compilation time. In this type of optimization, compiler does not analyze the whole code but only 2-3 successive instructions and tries to perform optimization on them. It can significantly reduce the simulation time while compilation is still pretty fast.

Due to similarities between AleC++ and VHDL-AMS, as it will be shown in the following section, the code generation phase developed for AleC++ language is used nearly complete without changes for VHDL-AMS compiler, too.

Compiled VHDL-AMS models can be used in the same manner as any other AleC++ model. The only exception is that simulation control parameters must be obtained from AleC++ file. They include control of numerical integration, iterative processes and sparse matrix solving. Therefore, VHDL-AMS models can not be used in the interpreted mode.

8. VHDL-AMS AND ALEC++ MIXED-LANGUAGE SIMULATION

Two problems must be solved in order to make AleC++/VHDL-AMS mixed-language simulation possible:on what level would be the code combining allowed and if the

synchronizing primitives are needed. Since the objective of co-simulation here is to enable reuse of models developed in the other HDL there is no need for code combining inside a

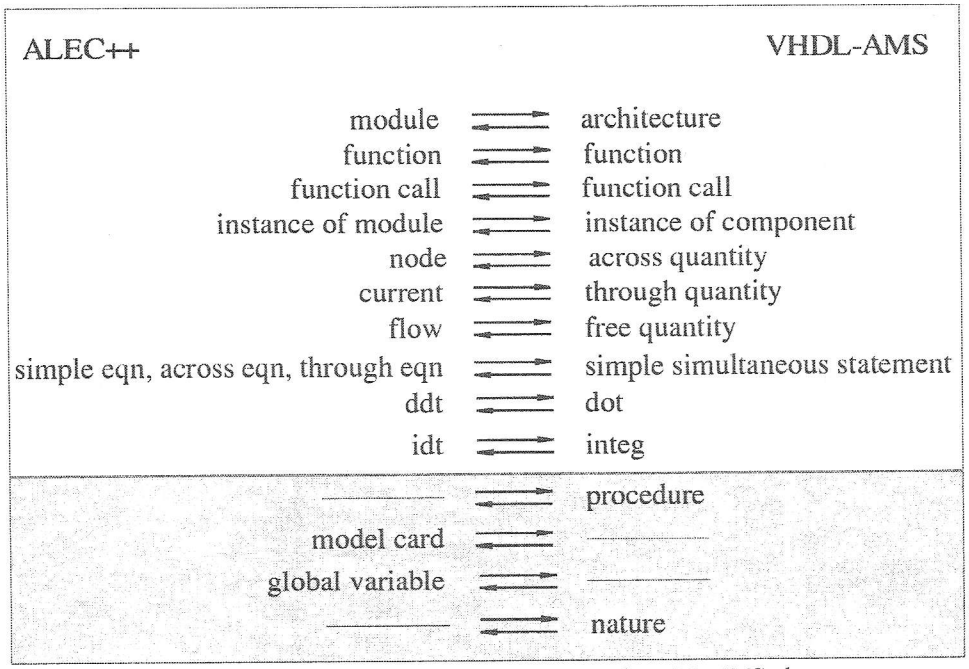

Figure 3. Correspondence between AleC++ and VHDL-AMS elements. Shadowed items do not have appropriate counterparts

single language object (e.g. function, instance of component)

Since AleC++ resembles the semantics of standard HDLs such as VHDL-AMS, the correspondence between language elements can be easily established (Figure 3). It enables VHDL-AMS compiler to form appropriate data structures that can be translated into AleC++ object code and use of almost completely unchanged the back-end of the existing AleC++ compiler. A VHDL-AMS model consists of an *entity* describing the interface and one or more *architectures* containing the implementation of the model. When that model is instantiated in a structural description, the designer specifies which of several architectures to use for each instance. Every architecture with appropriate entity in VHDL-AMS corresponds to one module in AleC++ and they are compiled into the library object of the same kind. Another basic language construct in both languages is *function*. Code combining under this level is forbidden. That means that it is not allowed to describe one process or equation in VHDL-AMS and another in AleC++ inside the same module/architecture. The mixed-language simulation is enabled through the instantiation of the subsystems (components in VHDL-AMS and modules in AleC++) and calling functions described in the other HDL. Thus, it is possible in VHDL-AMS descriptions to use components and call functions implemented in AleC++ and vice versa.

For describing of continuous systems VHDL-AMS uses the theory of differential and algebraic equations to represent the unknowns in the system of DAE's. Also, special kind of quantities called *branch quantities* are used for representing the unknowns in the equations describing conservative systems (systems obeying Kirchhoff's laws). There are two types of branch quantities: *across quantities* (for effort like effects such as voltage or pressure) and *through quantities* (for flow like effects such as current or fluid flow rate). AleC++ uses a similar language element called *link* to describe quantities that appears on a module terminal and represent the unknowns in the behavioral system descriptions. There are five types of links in AleC++: *node*, *current*, *flow*, *charge*, and *signal*. In terms of across and through quantities node is across and current is through quantity. The flows represent general analog quantities and correspond to free quantities in VHDL-AMS. For notating DAE's a new class of statements known as simple simultaneous statements is introduced in VHDL-AMS. AleC++ has similar language constructs for writing equations. Three forms of describing equations are used: one for non-conservative and two for conservative systems with across and through quantities. Since the way of writing equations is almost the same in both languages VHDL-AMS compiler can easily determine contributions of the equations from VHDL-AMS model to the matrix of the system of equations describing the whole design. The compiler at first identifies the different unknown quantities in the VHDL-AMS model and from each equation determines contributions to the system matrix. If only one equation contributes to the specified matrix row then the equation appears as is in the system of equations. However, other equations in the same or some other VHDL-AMS or AleC++ model can contribute to the same row. All these contributions are added to appropriate row following the concept of "stamps" commonly used in electronic circuit simulation. It is necessary in Alecsis to explicitly specify to which matrix row the equation contributes. In equations using free quantities that information can be provided as the equation's label. Branch quantities are declared with respect to two terminals. They hold no values but can be used to determine matrix rows to which equations containing branch quantities contribute. VHDL-AMS does not specify a technique for

solution of the system of equations leaving the selection of the method to the implementer of a simulator.

VHDL-AMS provides conditional and selected forms of the simultaneous statement that allow changing set of equations in the model. Since AleC++ has similar constructs, VHDL-AMS compiler can easily translate those statements into the corresponding object code.

Both languages support signal attributes for derivative and integration over time used in differential equations. AleC++ also supports second-order time derivative attribute and it is implemented in VHDL-AMS compiler, too.

Through the instantiation, ports of the component are bound and parameters are passed to it. The interconnection of quantities via component instantiations and port maps associates unknowns in different equations and implicitly creates additional equations constraining the paired quantities to have the same value. Also, through the function call actual arguments are passed to the function. Ports and parameters passed to the subsystem or function may belong to different types. Since, both languages, AleC++ and VHDL-AMS, have very complex and powerful data type system it is very important to establish the data type correspondence. Due to the same machine representation it is easy to accomplish that. The type *real* in VHDL-AMS corresponds to *double* in AleC++, and *integer* in VHDL-AMS to *int* in AleC++. Enumeration types exist in both languages, just like vectors, while *record* in VHDL-AMS relates to *struct* in AleC++. The designer has to take care about this data type correspondence when uses mixed-language descriptions. Besides, if the designer creates new data type, the same name and the equivalent description has to be used in both languages. As opposed to earlier language versions VHDL-AMS introduces a new two-level type system: the types already inherent within VHDL'93 and the natures. Natures represent distinct energy domains (electrical, thermal etc.). Its declaration consists of specifying nature's "across" and "through" types. Therefore, type information in the intermediate structures is represented by type symbol and nature symbol instances. All instances of object (except for terminals), literal, subtype and subprogram symbols are linked to their corresponding type symbol and all instances of terminals and subnature symbols are linked to their corresponding nature symbol. Furthermore, nature symbol instances are linked to the symbol instances denoting their across and through types. Since a branch quantity is declared with reference to two terminals, and terminal is declared to be of some nature, the type of branch quantities is derived form the nature of their terminals.

Thanks to the fact that both languages produce the object code of the same format, the simulation engine and virtual processor do not know which compiler has prepared the information. Since the interference boundary of the two languages is limited to library objects, no additional synchronization mechanism is needed.

9. CO-SIMULATION EXAMPLE

An example of a mechanical model describing oscillating mass is given in order to illustrate AleC++/VHDL-AMS mixed-language description and simulation of non-electrical systems (Figure 4). Its architecture is described in VHDL-AMS and defines mechanical equilibrium as a single differential equation using a simple simultaneous statement. Entities for calculating velocity and acceleration are not necessary for simulation, but are used just to print out the appropriate results. These models are instantiated and appropriate simulation control parameters are given in AleC++ file. VHDL-AMS models have to be compiled first into the AleC++ object code, and then the whole system is simulated using Alecsis.

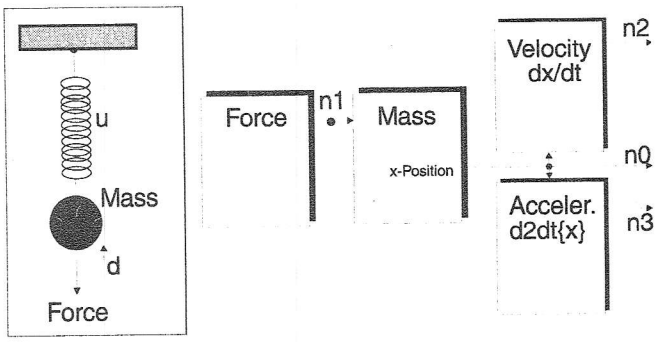

Figure 4. Architecture of oscillating mass

VHDL-AMS code describing the oscillating mass and additional entities for acceleration and velocity is given in Figure 5 and the corresponding AleC++ code for the model verification is shown in Figure 6.

```
entity mass_e is
 generic (m,u,d: real);
 port (quantity x: out real;
       quantity force: in real
 );
end entity mass_e;
architecture mass of mass_e is
begin
  x:   m*x'dot'dot + d*x'dot + u*x -
1*force == 0;
end architecture mass;

entity velocity_e is
 port (quantity x: real;
       quantity v: real
 );
end entity velocity_e;
architecture velocity of velocity_e
is
begin
       v:  1*v - 1*x'dot == 0;
end architecture velocity;
entity acceleration_e is
 port (quantity x: real;
       quantity a: real
 );
end entity acceleration_e;
architecture acceleration of
acceleration_e is
begin
a:  1*a - 1*x'dot'dot == 0;
end architecture acceleration;
```

Figure 5. VHDL-AMS model of the oscillating mass

```
#include <alec.h>
#define Period 15. s
module mass(flow x, force)
action(double m, double u, double d);
module velocity(flow x, v);
module acceleration(flow x, a);
library "mass";
library "velocity";
library "acceleration";
module Force (flow force) {
action (double force_value) {

          double force_out;
       process per_moment {
       force_out = force_value*exp(-now);

       eqn force: {force} = force_out;
            }
      }
}
root eq() {
  flow n0, n1, n2, n3;

  mass p;
      Force F;
      velocity V;
      acceleration A;

  p(n1,n0) {m=1; u=1; d=0.35;}
      F (n0) {force_value=10;}
      V (n1,n2);
      A (n1,n3);

  timing {tstop = Period; a_step =
Period/1000;}


  plot { flow n1;flow n2;flow n3; }

}
```

Figure 6. AleC++ code for the model verification

The mixed-language simulation results are shown in Figure 7.

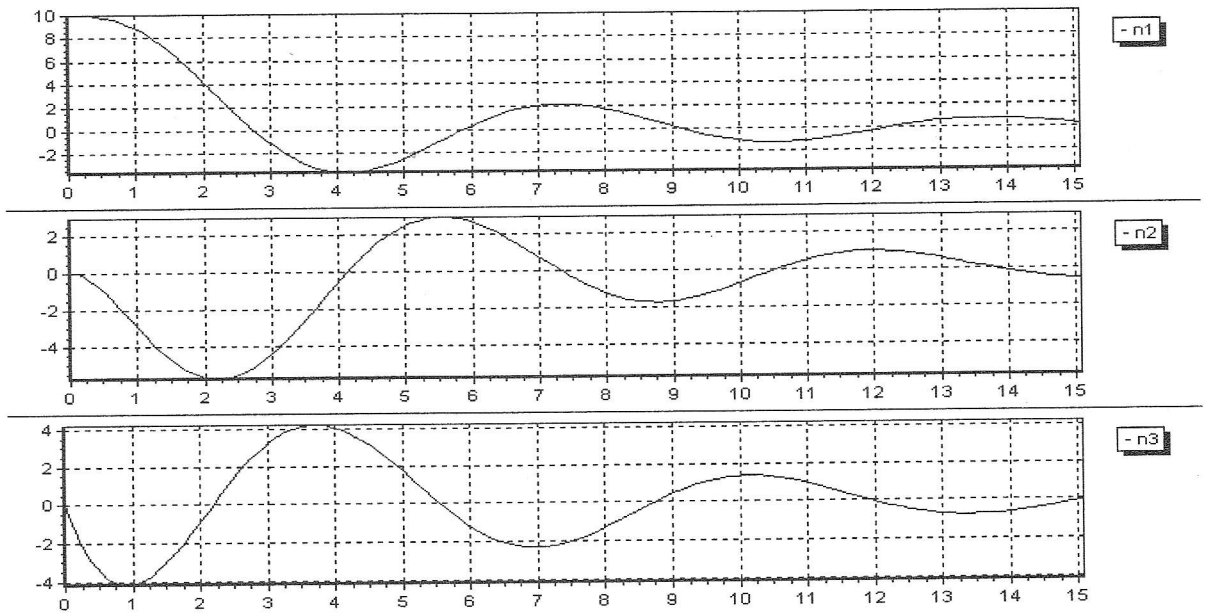

Figure 7. Simulation results of the oscillating mass. Traced signals are position, velocity and acceleration of the mass

A simple example of a summer/limiter is given in order to illustrate AleC++/VHDL-AMS mixed-language description and simulation of electronic circuits. Its architecture is described in VHDL-AMS and defines input/output transform as a single algebraic equation using a simple simultaneous statement. The role of the limiter is to clip the summer output if it exceeds a certain range. This model is instantiated and appropriate simulation control parameters are given in an AleC++ file. VHDL-AMS model has to be compiled first into the AleC++ object code, and then the whole system is simulated using Alecsis. VHDL-AMS code describing the summer/limiter is shown in Fig. 8 and the corresponding code for the circuit verification is shown in Fig. 9.

```
entity summer_limiter is
 generic (gain1 : real; -- gain of input 1
          gain2 : real; -- gain of input 2
          max_output:   real;   --   maximum
output
          min_output:   real;   --   minimum
output
       );

       port (quantity input1, input2 :
            in real; -- two input ports
         quantity output : out real --
output port
         );
     end entity summer_limiter;

     architecture        summer        of
summer_limiter is
```

```
    quantity sum: real;

    begin
      -- state defining equation

  sum: 1*sum - gain1*input1 -
                    gain2*input2 == 0.0;

  if (sum > max_limit) use

        output: 1*output == max_limit;
      elsif (sum < min_limit) use
        output: 1*output == min_limit;
      else
        output: 1*output - 1*sum == 0;

  end use;

end architecture summer;
```

Figure 8. VHDL-AMS code describing the circuit

```
    module summer (flow input1, input2,
output) action (double gain1, double
gain2, double max_limit, double
min_limit);

    library "summer";

    root summer_test() {
      flow in1, in2, outlim;

      summer sum;

      sum(in1, in2, outlim) {gain1=1.0;
      gain2=1.0;          max_limit=0.0;
min_limit=-2.0;}

      timing
{tstop=Period;a_step=Period/1000; }

      plot {flow in1; flow in2; flow
outlim;}

      /* sinusoidal excitation for
input1 and input 2 */

      action {
        double excit_out;
        process per_moment {
          excit_out =
          1.0*sin(twopi*1000*now+3.141);
          eqn in1: {in1} = excit_out;
          eqn in2: {in2} = excit_out;
        }
      }
}
```

Figure 9. Code for the circuit verification

The mixed-language simulation results are shown in Figure 10.

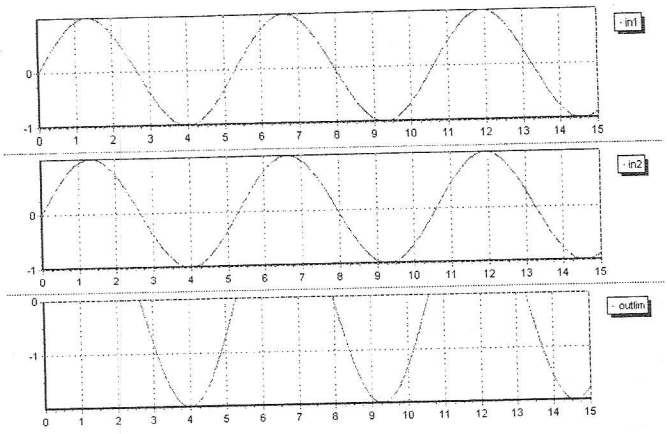

Figure 10. Simulation results of the summer/limiter

10. CONCLUSION

AleC++ is an HDL that has all properties of a programming language, too. This gives designers freedom in modeling very complex systems that are not conveniently covered by standard HDLs. However, having in mind the opportunities that standardization brings, a separate VHDL-AMS compiler for Alecsis simulator has been developed. In this sense, mixed-language descriptions and simulations are possible enabling one part of the design to be modeled in AleC++ and exploiting its important advantages, while the other part (pre-developed models in VHDL-AMS) may be given in standardized form. It gives designers the comprehensive environment they need to develop analog/mixed-signal circuits and SoC while they still can exploit the power of using portable models already developed in standard HDLs.

The implementation of frequency-domain simulation in Alecsis is under development and appropriate VHDL-AMS constructs for small-signal frequency-domain and noise simulation will be incorporated into the compiler in the near future.

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HOP RATE ESTIMATION OF FREQUENCY HOPPERS BASED ON SPATIO-TIME-FREQUENCY SIGNAL ANALYSIS

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Abstract: An algorithm for estimation of hop duration of the frequency hopping signals is proposed. The algorithm can be applied when many hoppers share the same frequency sub band. The algorithm is based on spatio-time-frequency signal analisys.

Keywords: frequency hopping, antenna array, MUSIC method, spectrum segmentation

1. INTRODUCTION

Frequency Hopping (FH) signals are the Low Probability of Intercept (LPD) class of signals. Signal intelligence of frequency hopping transmissions is a very complex technical problem since many narrow bands and wide bands as well as many frequency hoppers can share the same frequency sub band, and then there is no apriory information about the number and parameters of active emitters. In this situation, the required information are provided by parameter estimation of received signals.

The main task of modern communication intelligence sistems is detection of frequency hoppers, transmitter location, and separation of the classical narrow-band and frequency hopping emitters amongselves.

An algorithm for hop duration estimation is proposed which is based on spatio-time-frequency signal analysis, in situation when many frequency hoppers with different hop rate share the same frequency sub-band.

12. SPATIAL MATHEMATICAL MODEL OF SIGNAL SUPERPOSITION ON ANTENNA ARRAY

Radio signal $u(t)$ in given frequency sub-band $\Delta\omega_{BW}$ and observation interval ΔT is the result of superposition of radio signals of many active transmitters $\{u_k(t)\}, k=1,..,K$ and noise $n(t)$, and it can be expressed in analytical form as:

$$u(t)=\sum_{k=1}^{K}u_k(t)+n(t)=\sum_{k=1}^{K}s_k(t)\exp(j\omega_{Ck}t)+n(t), \quad (1)$$

The processes of detection, parameter estimation of superposed radio signals and information signal separations are based on analysis of the signal $u(t)$, which is available on the given frequency sub band $\Delta\omega_{BW}$ and time interval ΔT in situation when there are no *a priory* information about the number, statistical and spectral parameters of superposed signals.

Generalized spatial model of the superposed signal can be expressed in time domain in a form [1]:

$$\mathbf{x}(n)=\sum_{h=-H/2}^{H/2}[\mathbf{A}(\omega_c,\omega_h)\mathbf{F}(\Omega_h)+\mathbf{N}(\Omega_h)]\exp(j2\pi\Omega_h n), \quad (2)$$

where $\mathbf{x}(n)=[x_1(n)\ \ x_2(n)\ \ ...\ \ x_L(n)]^T$ denotes the vector with the time samples of the *IQ* demodulated signal on antenna array of arbitrary but known geometry and $\Omega_h \in [-0.5,0.5]$ is the normalised frequency. Spatial model of the signal on antenna array in frequency domain can be expressed in the next matrix form:

$$\mathbf{X}(\Omega_h)=\mathbf{A}(\omega_C,\omega_h)\mathbf{F}(\Omega_h)+\mathbf{N}(\Omega_h), \quad (3)$$

where $\mathbf{X}(\Omega_h)=[X_1(\Omega_h)\ \ X_2(\Omega_h)\ \ ...\ \ X_L(\Omega_h)]^T$ is a vector with spectral samples of the signals on antenna array. $\mathbf{F}(\Omega_h)=[F_1(\Omega_h)\ \ F_2(\Omega_h)\ \ ...\ \ F_L(\Omega_h)]^T$ is a vector with spectral samples of IQ demodulated/down converted signals on antenna array. $\mathbf{N}(\Omega_h)=[N_1(\Omega_h)\ \ N_2(\Omega_h)\ \ ...\ \ N_L(\Omega_h)]^T$ is a vector with spectral samples of noise on antenna array. $F_k(\Omega_h)$ is a shifted spectrum of the complex envelope of the *k*th superposed signal and it can be expressed like:

$$\begin{aligned}F_k(\Omega_h)&=\sum_{n=1}^{N}s_k(n\Delta t)\exp[j(\omega_{Ck}-\omega_C)n\Delta t]\exp(j2\pi\omega_h n\Delta t)=\\&\sum_{n=1}^{N}s_k(n\Delta t)\exp[j2\pi\Omega_{Ck}n]\exp(j2\pi\Omega_h n)=\\&\sum_{n=1}^{N}f_k(n\Delta t)\exp(j2\pi\Omega_h n).\end{aligned} \quad (4)$$

The vector $\mathbf{F}_k(\Omega_h)$ contains the information about spectral bandwidths and central frequencies of superposed signal. Spectral components of the $\mathbf{F}_k(\Omega_h)$ are symmetrically distributed around the normalized central frequencies:

$$\left\{\Omega_{Ck}=\frac{\omega_{Ck}-\omega_C}{\Delta\omega_{BW}}=\frac{f_{Ck}-f_C}{\Delta f_{BW}}\right\}, k=1,..,K$$

From the known central frequency of selected frequency sub-band and estimated normalized central frequencies $\{\Omega_{Ck}\}, k=1,..,K$, the central frequencies of radio signals $\{\omega_{Ck}\}, k=1,..,K$ can be further simply calculated.

The matrix $\mathbf{A}(\omega_C,\omega_n)$ has the *LxK* dimension. The columns of this matrix are the so called steering vectors of superposed radio signals which can be expressed in the next normalized form:

$$\left[\exp\left(j2\pi\left(\frac{\omega_C+\omega_h}{\omega_A}\right)\mathbf{v}_k^T\frac{\mathbf{r}_1}{\lambda_A}\right)\ \ ...\ \ \exp\left(j2\pi\left(\frac{\omega_C+\omega_h}{\omega_A}\right)\mathbf{v}_k^T\frac{\mathbf{r}_L}{\lambda_A}\right)\right]^T \quad (5)$$

where $\mathbf{r}_l \in R^3$ is a vector of location of the *l*th antenna in real 3-D space, $\mathbf{v}_k \in R^3$ is a unit vector which denotes the direction of arrival (DOA) of the *k*th radio signal on antenna array and it can be expressed in spherical

coordinate as the function of direction of arrival (azimuth θ_κ and elevation φ_κ) in the next form:

$$\mathbf{v}_k = [\sin(\theta_k)\cos(\varphi_k) \quad \cos(\theta_k)\cos(\varphi_k) \quad \sin(\varphi_k)] \quad (6)$$

In order to formulate the spatial model of superposition of the frequency hoppers, firstly it is needed to formulate the mathematical model of the frequency hopping signal in referent point in the space. Energy spectrum representation of the frequency hopping signal in time-frequency domain in given frequency sub-band and $\Delta\omega_{BW}$ and observation interval ΔT is presented in the Fig.1. The main parameters, which are relevant for the formulation of mathematical model, are defined in the Fig.1, too.

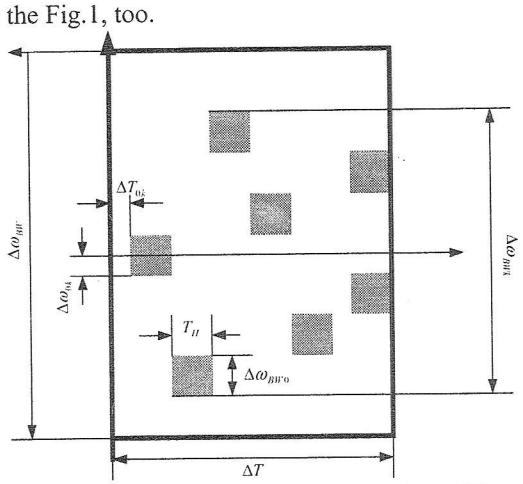


Fig.1 Energy spectrum representation of the frequency hopping signal

Parameter $\Delta\omega_{BWk}$ denotes the bandwidth of the hopping of the qth signal during the observation interval ΔT, and $\Delta\omega_{BW0}$ is the spectral bandwidth of the elementary hop. Parameters $\Delta\omega_{0k}$, ΔT_{0k} denote frequency and time shift respectively, related to the origin of coordinate system.

Those parameters are defined due to the fact that the hoppers of different radio networks are asynchronous, or due to the fact that the channel raster is not the same in different hoppers. The quantity $M_h = \Delta\omega_{BW}/\Delta\omega_{BW0}$ denotes the number of all possible frequency channels in frequency sub band $\Delta\omega_{BW}$; $N_h = \Delta T/T_H$ denotes the number of all hops in time observation interval ΔT.

The complex envelope of the frequency hopping signal $s_k(t)$ can be expressed in discrete time-frequency domain in such a form, [3,4]:

$$s_k(n) = \sum_{v=1}^{N_h} \exp\left[j2\left(\gamma_{kv} \frac{\Delta\omega_{BW0} - \Delta\omega_{0k}}{\Delta\omega_{BW}} \right) n \right] \cdot \cdot \sum_{h=-H/2}^{H/2} S_{kv}(\Omega_h) \exp[-j2\pi\Omega_h((v-1)n_h - n_k)] \exp(j2\pi\Omega_h n). \quad (7)$$

In equation above, n_h denotes the number of time samples in one hop, n_k denotes the number of time samples for which the beginning of the first hop is shifted in contrast to кординантни почетак, $v = 1,..,N_h$ denotes the ordering number of the hop, $\gamma_{kv} \in (-M_h/2, M_h/2)$ denotes code sequence of the hopper and $S_{kv}(\Omega_h)$ is a complex envelope of the *vth* hop.

13. SPECTRUM SEGMENTATION

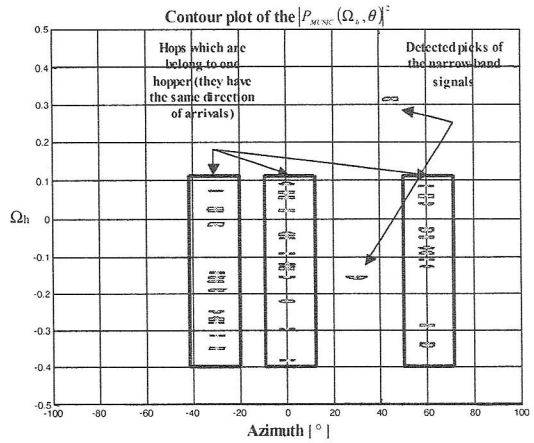
The segmentation procedure, defined in [1,5], is based on the direction of arrival (DOA) estimation using MUSIC algorithm applied in space-frequency domain. The segmentation procedure is based on the rule that all spectral components with same DOAs belong to the same information channel. It is supposed that the frequency hopper does not change the direction of arrival (DOA) during the given time observation interval ΔT. The procedure is based on the parameter estimation on the generalized spatial model of the superposition of radio signals defined in [1].

In this paper the results of segmentation are presented for the next signal scenario. Radio signal is received by the circular antenna array with characteristic (Nicquist) frequency $f_A = 80$ MHz. The frequency sub band $\Delta\omega_{BW} = 12.8$ MHz was supposed on the central frequency $f_A = 60$ MHz. Three frequency hopping signals arrive at the antenna array from the azimuths 60°, -30° and 0° respectively. The elevations of the arrivals are the same and they are 0°. The bandwidth of the elementary narrow band channel is 12.5 kHz, so $M_h = 1024$ are possible in selected frequency sub band. The number of time samples per hop is $n_h = 20000$ what is equivalent to the hop duration of 1.56 ms or to the hop rate of 625 hop/s. The total number of time samples is $N = 200000$ what is equivalent to the duration of time observation interval $\Delta T = 15.6$ ms.

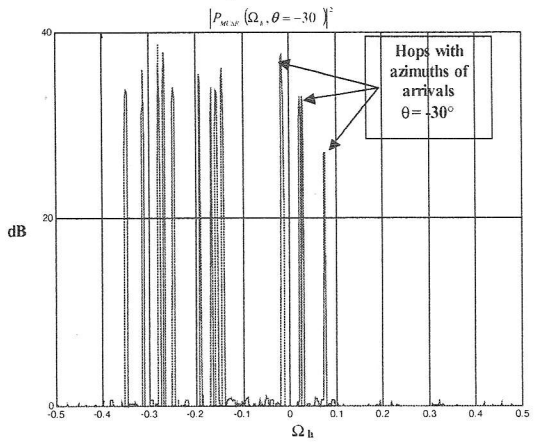
Two narrow-band signals (FSK-4 with symbol rate of 6400 symbols/s) with azimuths 45° and 30° ,and elevations 0° are also active in the given frequency sub band and observation interval. The signals of noise ratios are 15, 10 and 20 dB for the first, the second and third frequency hopping signals, 15 and 20 dB for the narrow band FSK signals. The FSK-2 modulation is used in frequency hopping signals. The biit rate is 6400 bit/s (it is slow frequency hopping since 10 simbols are transmitted per one hop)..

The results of parameter estimation of signals in space-frequency domain for the simulated scenario are presented on the figure 2. Contour plot of the MUSIC cost function $P_{MUSIC}(\Omega_h, \theta)$ is presented in the figure 2. By the grouping of the picks in $P_{MUSIC}(\Omega_h, \theta)$ by the criterion of the same direction of arrival, three frequency hopping signals as well as two narrow band signals can be clearly identified. The spectral range and space-frequency localization of the hopping signals can be also clearly identified.

The results of space/frequency localization of frequency hopping signals are presented in the fig.2. The contour plot of the function $P_{MUSIC}(\Omega_h, \theta)$ is plotted in the Fig 2a. It can be clearly seen from the fig.2 that three frequency hoppers and two narrow band emitters are active.



a)



b)

Fig.2. a) Contour plot of the $|P_{MUSIC}(\Omega_h,\theta)|^2$ *;b) Plot of the* $|P_{MUSIC}(\Omega_h,\theta=-30^\circ)|^2$.

14. ESTIMATION OF HOP DURATION

The problem of the separation or isolation of radio channels is one of the key problems in of the automatization of the monitoring of the radio-frequency spectrum. Detection and location of the frequency hoppers, separation of many different hoppers and identification of frequency hopping networks are the functions, which are required from the modern radio monitoring systems. In order to provide such functions, the parameter estimation of detected radio signals has to be performed in monitoring systems: Direction of Arrival, hop rate, hop range, channel bandwidth etc.

An algorithm for estimation of hop duration is proposed in this paper, Fig.3. It can be applied when many frequency hoppers from different frequency hopping networks are active in given frequency band. The proposed procedure is based on the segmentation procedure previously presented.

Estimation of unknown parameters is based on the *LxN* complex spatio-temporal samples of the IQ demodulated signals on antenna elements acquired in time observation interval ΔT and frequency sub band $\Delta\omega_{BW}$. It was supposed that the time observation interval ΔT is much larger then hop duration T_H ($\Delta T >> T_H$). By the calculation of the MUSIC cost function, DOA estimation $\{\theta_k\}, k=1,..,K$ of the superimposed signals is performed. Selection of the frequency hopping signal, which can be further analyzed, is based on the estimated direction of arrival.

MUSIC function $P_{MUSIC}(\Omega_h,\theta=\theta_k)$, Fig.2a, is further analysed. The number of picks in function $P_{MUSIC}(\Omega_h,\theta=\theta_k)$ is estimated for the selected azimuths. If many picks were estimated, the hopping signal would arrive from the selected azimuth with high probability. The rough estimation of the hop duration is performed $\hat{T}_H' = \Delta T / N_h$ where N_h is the estimated number of hops N_h and ΔT is duration of time observation interval ΔT.

In the next step coarse estimation of hop duration is performed using time samples on the new time observation interval $\Delta T_1 = 3\hat{T}_H'$. In this case the MUSIC cost function $P_{MUSIC}(\Omega_h,\theta=\theta_k)$ is calculated just for the selected azimuth. Using that function, the central frequencies Δf_{kv} of the each detected hops are estimated.

The spatial filtration of the selected frequency hopping signal is performed after that, and each hop is down converted to base-band using the information about its previously estimated central frequencies. The hop duration is estimated by the differentiation of the down converted signal of hops. The difference between the positive and the negative picks determines the hop duration. Averaging the results for all detected hops active in given time observation interval provides the average value of the hop duration ΔT.

15. RESULTS OF NUMERICAL MODELING

Performances of the proposed procedure for estimation of hop duration are illustrated in the two next examples. In the first example the antenna array is circular with 8 antenna elements in the array. Characteristic frequency of antenna array is $f_A = 80$ MHz. Nine frequency hopping signals are superposed in frequency sub band $\Delta\omega_{BW} = 6.4$, which is ??? from three independent frequency-hopping networks.

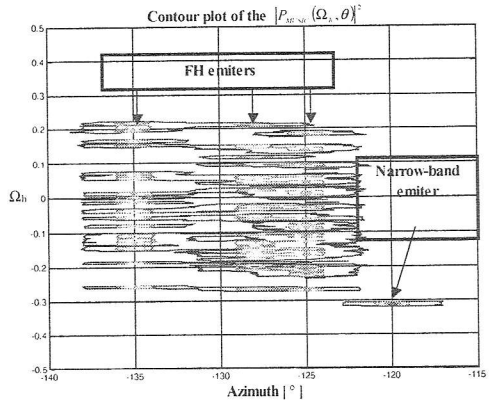
The azimuths and elevations of the hoppers are: 63°, 65° and 67° for the hoppers of the first network, 34°, 32° and 28° for the hoppers of the second network and 125°, -128° and 135° for the hoppers of the third network. The elevations are 0° for all hoppers. Frequency bandwidth of the elementary hop is 12.5 kHz for the hoppers of the first network, so the $M_{h1} = 512$ elementary hop channel is possible in given frequency sub band $\Delta\omega_{BW} = 6.4$ MHz. Frequency bandwidth of the elementary hop is 25 kHz for the hoppers of the second and third network, so the $M_{h2,3} = 256$ elementary hop channels is possible in given frequency sub band $\Delta\omega_{BW} = 6.4$ MHz. The number of time samples in one hop for the hoppers in first network is $n_{h1} = 11000$ what is equivalent to the hop duration 1.718 ms or the hop range 581.4 hops/s. The number of time samples in one hop for the hoppers in second network is $n_{h2} = 7500$ what is equivalent to the hop duration 1.171 ms or the hop range 853.4 hops/s.

The number of time samples in one hop for the hoppers in third network is $n_{h3} = 5600$ what is equivalent to the hop duration 0.875 ms or the hop range 1142.8 hops/s.

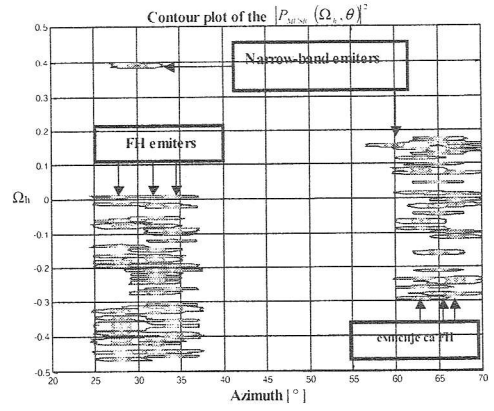
The number of time samples is $N = 100000$ what is equivalent to the time observation interval $\Delta T = 15.62$ ms. Three narrow-band signals with azimuths of arrival 60°, 30° and -120° and elevations 0° are also superposed in the same selected frequency band and observation interval

The signal of noise ratio for the frequency hopping signals are 15,10 and 15 dB for the hoppers of the first network, 20, 15 and 15 dB for the hoppers of the second network, 20, 15 и 15 dB for the hoppers of the second network and 20, 15 и 10 dB for the narrow-band emitters.

The results of estimation of hop duration base on proposed procedure, for the above simulated signal scenario, are presented on the table I. The error in hop duration estimation was less than 0.5% of the true hop duration in all cases.



a)



b)

Fig.4. a) Contour plot of the $P_{MUSIC}(\Omega_h,\theta)$ in spatial sector $\theta\in$[-140°, 115°], b) Contour plot of the $P_{MUSIC}(\Omega_h,\theta)$ in spatial sector $\theta\in$[20°,75°].

The results of segmentation for the simulated signal scenario are presented in the fig.4. Due to better visibility, the MUSIC cost function is calculated and presented for two spatial sectors: $\theta\in$[-140°, 115°], Fig. 4a and $\theta\in$[20°, 75°], Fig. 4b.

In the second example antenna array is circular with eight antenna elements in the array. Characteristic frequency of antenna array is $f_A = 80$ MHz. Nine frequency hopping signals is superposed in the selected frequency sub band $\Delta\omega_{BW} = 12.8$ MHz. on the central frequency $f_A = 60$ MHz. All frequency hopping signals arrive from the spatial sector of 30° and they are grouped in three frequency hopping networks, which are not spatially separated amongselves as in previous example. Azimuths of arrivals of frequency hopping signals are 24°, 37°, 18°, 16°, 33°, 22°, 42°, 27° and 30° respectively. The elevations are zero for all hoppers. The spectral bandwidth of the elementary hop channel is 25 kHz so the $M_{h1} = 512$ elementary channels are available in given frequency sub band.

The number of time samples in one hop for the hoppers in first network is $n_{h1} = 12525$ what is equivalent to the hop duration 0.97852 ms or the hop range 1022.5 hops/s. The number of time samples in one hop for the hoppers in second network is $n_{h2} = 8050$ what is equivalent to the hop duration 0.6289 ms or the hop range 1592.3 hops/s. The number of time samples in one hop for the hoppers in third network is $n_{h3} = 6800$ which is equivalent to the hop duration 0.53125 ms or the hop range 1882.4 hops/s.

The number of time samples is $N = 100000$ which is equivalent to the time observation interval $\Delta T = 7.81$ ms. The signal of noise ratio for the frequency hopping signals are 15, 10 and 20 dB for the hoppers of the first network, 15, 10 и 15 dB for the hoppers of the second network and 15, 20 and 10 dB for the hoppers of the third network.

Table I: Results of estimation of hop duration for the first example

Azimuth [°]	True value of T_H [ms]	Estimated value of T_H [ms]	Error in [μs] and [%]
63°	1.71875	1.71828	0.47 (0.027 %)
65°	1.71875	1.72250	3.75 (0.21 %)
67°	1.71875	1.71953	0.78 (0.045 %)
34°	1.171875	1.17281	0.93 (0.08 %)
32°	1.171875	1.17375	1.87 (0.16 %)
28°	1.171875	1.17250	0.62 (0.053 %)
-125°	0.875	0.87656	1.56 (0.17 %)
-128°	0.875	0.87718	2.18 (0.25 %)
-135°	0.875	0.87500	0 (0 %)

The results of estimation of hop duration for the second simulated signal scenario are presented in the Table II. Error in hop duration estimation is lower than 0.5 %. for eight hoppers. The error is much bigger for just one hopper.

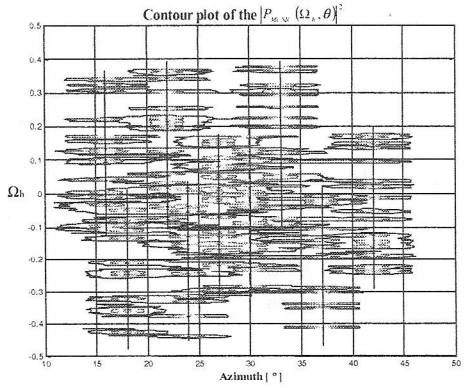


Fig. 5. Contour plot of the $P_{MUSIC}(\Omega_h,\theta)$ in spatial sector $\theta \in [10°, 50°]$.

The results of the segmentation for the given signal scenario are presented on the Fig.5.

Table II: Results of estimation of hop duration for the second example

Azimuth [°]	True value of T_H [Ms]	Estimated value of TH [ms]	Error in [μs] and [%]
42°	0.53125	0.53094	0.31 (0.058 %)
24°	0.97852	0.27590	950.9 (97 %)
16°	0.6289	0.62969	0.79 (0.124 %)
33°	0.6289	0.63195	3.05 (0.484 %)
37°	0.97852	0.97718	1.34 (0.135 %)
27°	0.53125	0.53203	0.78 (0.147 %)
30°	0.53125	0.5311	0.15 (0.029 %)
18°	0.97852	0.97875	0.23 (0.024 %)
22°	0.6289	0.62789	1 (0.161%)

16. CONCLUSION

Algorithm for estimation of hop duration in dense signal environment, when many frequency hopping and classical narrow-band emitters share the same frequency sub band is presented in this paper. The separation of frequency hoppers emitters and identification of frequency hopping networks based on the hop rate are possible. In the presented results of simulations the error of estimation of hop duration was lower than 0.5% of the true value of the hop duration. In the process of the hop duration estimation, the central frequencies and hop phase are also estimated. Those parameters can be further used for improvement of the separation of frequency hoppers and identification of frequency hopping networks.

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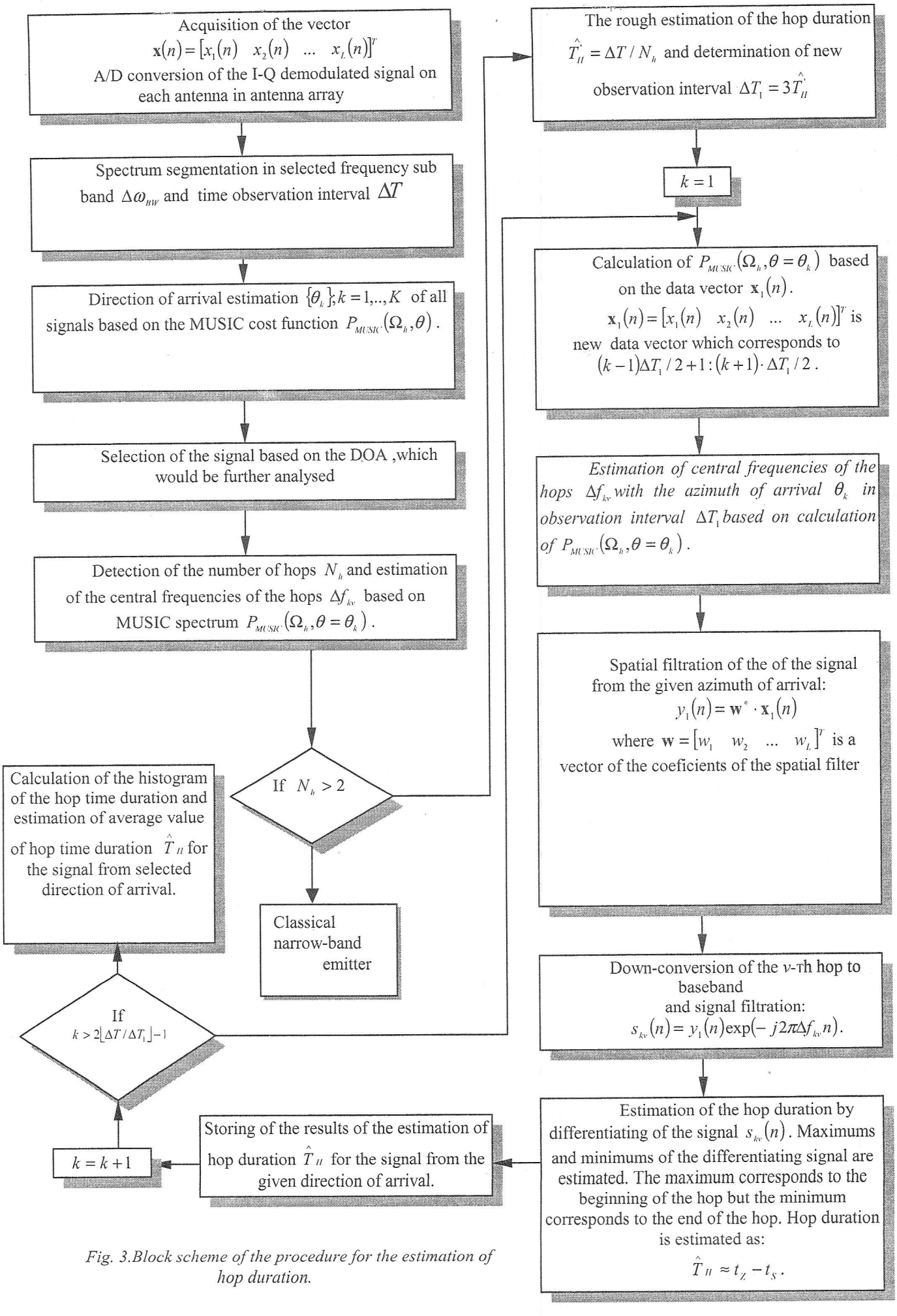

Fig. 3.Block scheme of the procedure for the estimation of hop duration.

ANALYSIS OF CHIRP-FREE OPTICAL PULSE PROPAGATION ALONG A NONLINEAR AND DISPERSIVE FIBER

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Petar Spalević, *Faculty of Technical Science, Kosovska Mitrovica*

Abstract- In system for transmission information on large distances with high velocity, we must consider combinated influence of nonlinear and dispersive effects on signal propagation along the fiber. This paper studies propagation of short pulses which width is going in limit from 10 fs to 10 ns and which is subjected common influence effects of GVD-group velocity dispersion and SPM-self phase modulation, along the fiber. Signal interference is frequent appearance in optical communication systems, and because of that in this paper is consider influence of signal interference on characteristics of optical pulse propagation along the nonlinear and dispersive fiber, too.

Keywords: *GVD-group velocity dispersion, SPM-self phase modulation, interference, Super-Gaussian pulses.*

1. INTRODUCTION

Today, optical communication IM-DD systems with large capacities for information transmission on large distance, are very applicable. Capacities of this systems are order of Gb/s, while the signals is transmited on distances order of thousand kilometers. At this transmission of informations, compensation of losses is doing by amplifiers, while the compensation of dispersion is doing by compensation fiber. The interference is frequent appearance in optical systems, and because of that in this paper is consider its influence on signal propagation when interference is at input of fiber. For solving of this problems is used nonlinear differential Schrödinger equation. As representative examples for signal propagation along the nonlinear and dispersive fiber we are considered Gaussian pulse and Super-Gaussian pulse (m=2 and m=3). Signal interference has the same shape as useful signal, and because of its presence at begining of optical fiber, conditions for solving of Schrödinger wave equation are changed [1,2,3].

2. NONLINEAR SCHRODINGER EQUATION

Signal propagation along the optical fiber under influence of nonlinear and dispersive effects can be descripted over equation of wave propagation:

$$\frac{\partial A}{\partial z}+\beta_1\frac{\partial A}{\partial t}+\frac{i}{2}\beta_2\frac{\partial^2 A}{\partial t^2}-\frac{1}{6}\beta_3\frac{\partial^3 A}{\partial t^3}=i\gamma|A|^2A \qquad (1)$$

where A(z,t) represents pulse envelope, $\beta_1=\frac{\partial\beta}{\partial\omega}=\frac{1}{v_g}, \beta_2=\frac{\partial^2\beta}{\partial\omega^2}, \beta_3=\frac{\partial^3\beta}{\partial\omega^3}$, β is the mode-propagation constant, v_g is group velocity. The nonlinearity coefficient γ is defined by:

$$\gamma=2\pi n_2/(\lambda A_{eff}) \qquad (2)$$

where n_2 is nonlinear-index coefficient, λ is wavelength and A_{eff} is known as the effective core area. Parameters β_2 and γ governs to effects GVD and SPM, respectively [1,5].

The equation (2) well descripts propagation of pulse, order of few picoseconds, along the fiber. In the cases when λ is very distant from zero-dispersive length, equation (2) can be simplifed because in that case β_3 become zero. We can do normalization on next way

$$\tau=\frac{T}{T_0}=\frac{t-\beta_1 z}{T_0},\quad U=\frac{A}{\sqrt{P_0}} \qquad (3)$$

where T_0 is pulse width, P_0 is peak power of the incident pulse, and L_D is the dispersion length which determined as:

$$L_D=\frac{T_0^2}{|\beta_2|} \qquad (4)$$

Parameter N represents nondimensional magnitude, which governs the relative importance of the SPM and GVD effects on pulse evolution along the fiber and it is determined:

$$N^2=\gamma P_0 L_D=\gamma P_0 T_0^2/|\beta_2|=L_D/L_{NL} \qquad (5)$$

where L_{NL} is nonlinear length, i.e.

$$L_{NL}=(\gamma P_0)^{-1} \qquad (6)$$

Now, equation (2) takes next form:

$$\frac{\partial U}{\partial z}=-i\frac{\mathrm{sgn}(\beta_2)}{2L_D}\frac{\partial^2 U}{\partial\tau^2}+\frac{i}{L_{NL}}|U|^2U \qquad (7)$$

In equation (7) $sgn(\beta_2)$ can take value +1 if optical fiber works in normal dispersion regime or -1 if it works in anomalous dispersion regime [1,4].

The equation (7) represents nonlinear partial differential equation and we can use great number of numerical methods for its solving. One of that methods is "*Split-step" Fourier methods* [1,3,5], which represents pseudospectral methods . In this paper, this method is used for solving nonlinear Schrödinger equation.

3. PROPAGATION OF SIGNAL ALONG THE NONLINEAR AND DISPERSIVE FIBER

Very often in optical systems, as useful signal is used signal which envelope has Super-Gaussian form:

$$U(0,\tau)=a\exp(-\tau^{2m}/2) \qquad (8)$$

and that's the reason for consideration this signal in this paper. In this paper are considered pulses can take values for m={1,2,3}. Super-Gaussian pulse for m=1 is known as Gaussian pulse. In equation (8), value of parameter *a* depend from that is it send "1" or "0". At transmission of signal along the optical fiber come to crosstalk from neighbouring channel, very often and it represents interference. Also, the signal interference have Gaussian form of envelope, which is time and phase shifted from useful signal. The useful signal at beginig of optical system can be descripted as:

$$s(0,\tau)=U(0,\tau)\cos\omega t \qquad (9)$$

Signal interference has next form:

$$s_i(z_i,\tau)=U_i(z_i,\tau)\cos(\omega t+\varphi),$$
$$U_i(z_i,\tau)=a_1\exp(-(\tau-b)^{2m}/2) \quad (10)$$

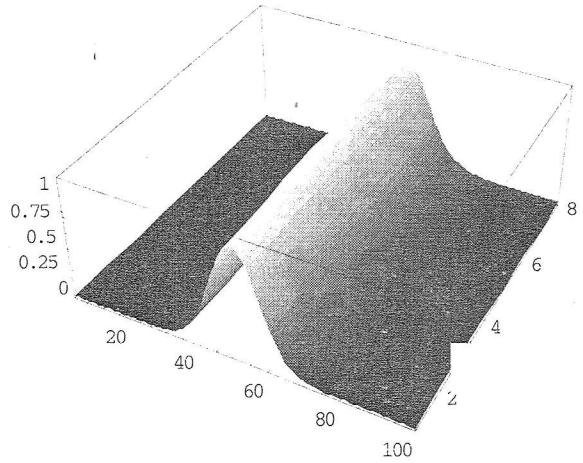
where value of parameter a_1 depends from the size of interference in optical system, z_i represents place of appearance of the signal interference, b and φ represent time and phase shift of signal interference, respectively. Envelope and phase of resulting signal in optical system are determined as [7]:

$$U_r(z_i,\tau)=\sqrt{U^2(z_i,\tau)+2U(z_i,\tau)U_i(z_i,\tau)\cos\varphi+U_i^2(z_i,\tau)} \quad (11)$$

$$\psi(z_i,\tau)=arctg\frac{U_i(z_i,\tau)\sin\varphi}{U(z_i,\tau)+U_i(z_i,\tau)\cos\varphi} \quad (12)$$

We can get signal shape along the optical fiber solving nonlinear Schrödinger equation (7) using *"Split-step" Fourier* method.

For all observed cases of propagation we have next parameters: λ=1550 nm, T_{FHWM}=1,665 ps i.e. T_0=1 ps, A_{eff}=80 μm^2, D=±1 ps/km·nm ($D\leq1$), n_2=2,24·10^{-20} m^2/W^2, P_0=0.89W, $\beta_2=-\lambda D^2/(2\pi c)$. This parameters lead that the influence of dispersive and nonlinear effects are equal.



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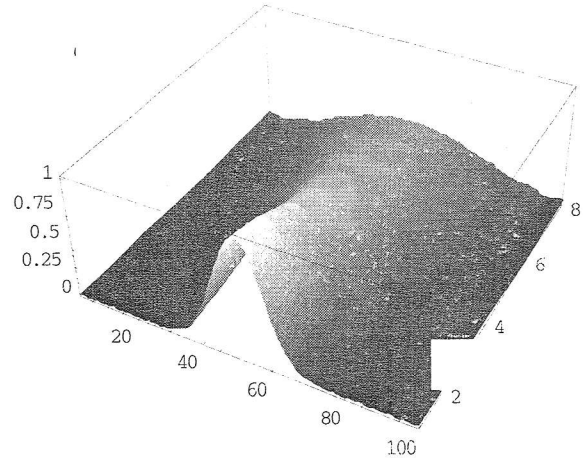
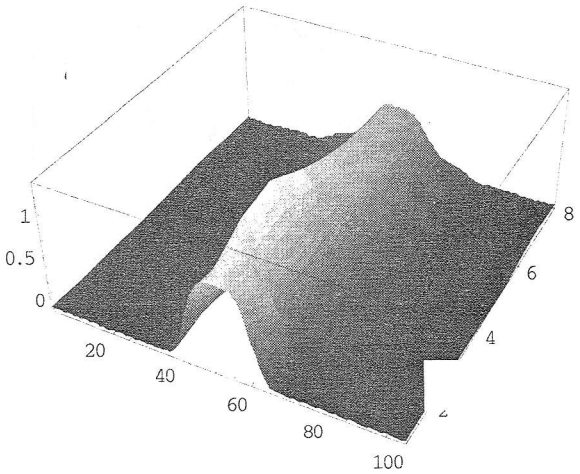


b)

Figure 1. *Propagation of Gaussian envelope form along the optical fiber a) $\beta_2<0$; б) $\beta_2>0$*

Figure 1. shows the propagation of optical pulse with Gaussian envelope along the nonlinear and dispersive fiber, in both dispersion regime. From figure 1, it can show that GVD and SPM cooperate with each other to maintain a chirp-free pulse. Also, we can see that performance of pulse propagation is much better in anomalous than in normal dispersion regime.



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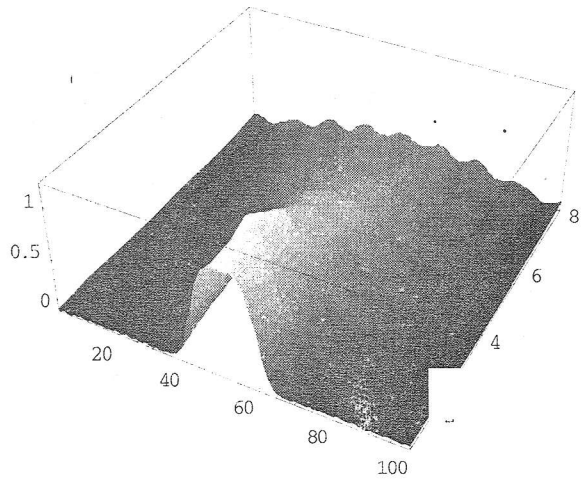

b)

Figure 2. *Propagation of signal with Super-Gaussian envelope form (m=2) along the nonlinear and dispersive fiber a) $\beta_2<0$; б) $\beta_2>0$*

Figure 2. and the figure 3. show propagation of optical pulse with Super-Gaussian form in cases m=2, i.e. m=3, respectively, in both dispersion regime. As in previous case, the pulse better saves form in anomalous dispersion regime. Also, it can see that the pulse width expansion and pulse distortion are larger if value of parameter m increases.

Figure 4. represents the evolution of Gaussian pulse shape along the nonlinear and dispersive fiber in both dispersion regime, in the presence of signal interference (SIR_{sr}=10dB) which appears at beginig of fiber. From that figure we can see that the cooperating work of GVD and

SPM creates less disturbance in anomalous than in normal dispersion regime, if signal interference is present.

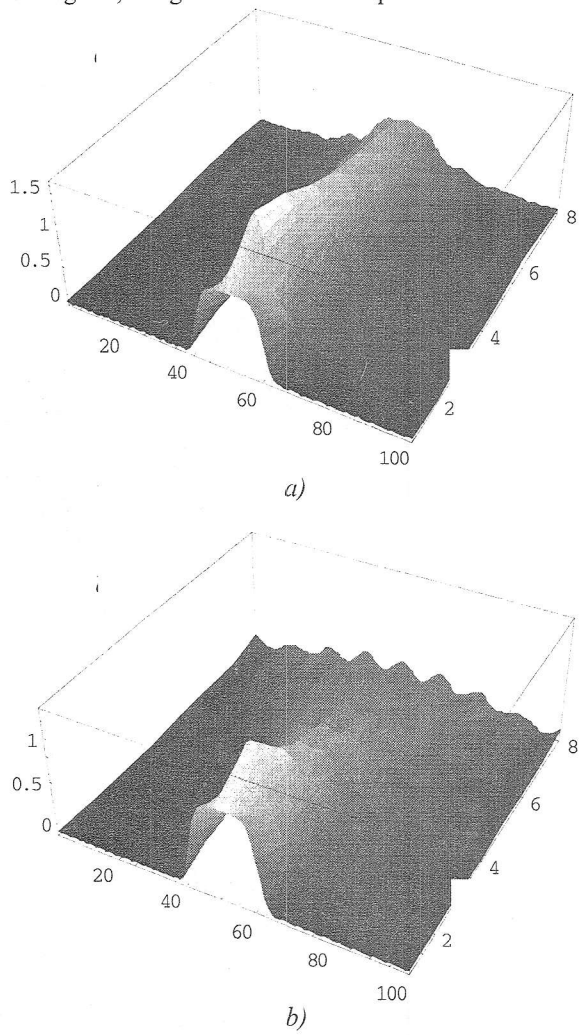

Figure 3. *Propagation of Super-Gaussian envelope form (m=3) along the optical fiber a) $\beta_2<0$; b) $\beta_2>0$*

Figure 5. and figure 6. represent the evolution of Super-Gaussian pulse shape in case m=2, i.e. m=3, in the both dispersion regime, in the presence of signal interference (SIR_{sr}=10dB) at begining of fiber. As in previous cases, anomalous dispersion regime better saves pulse shape than normal dispersion regime. The influence of signal interference is larger when the value of parameter m increases.

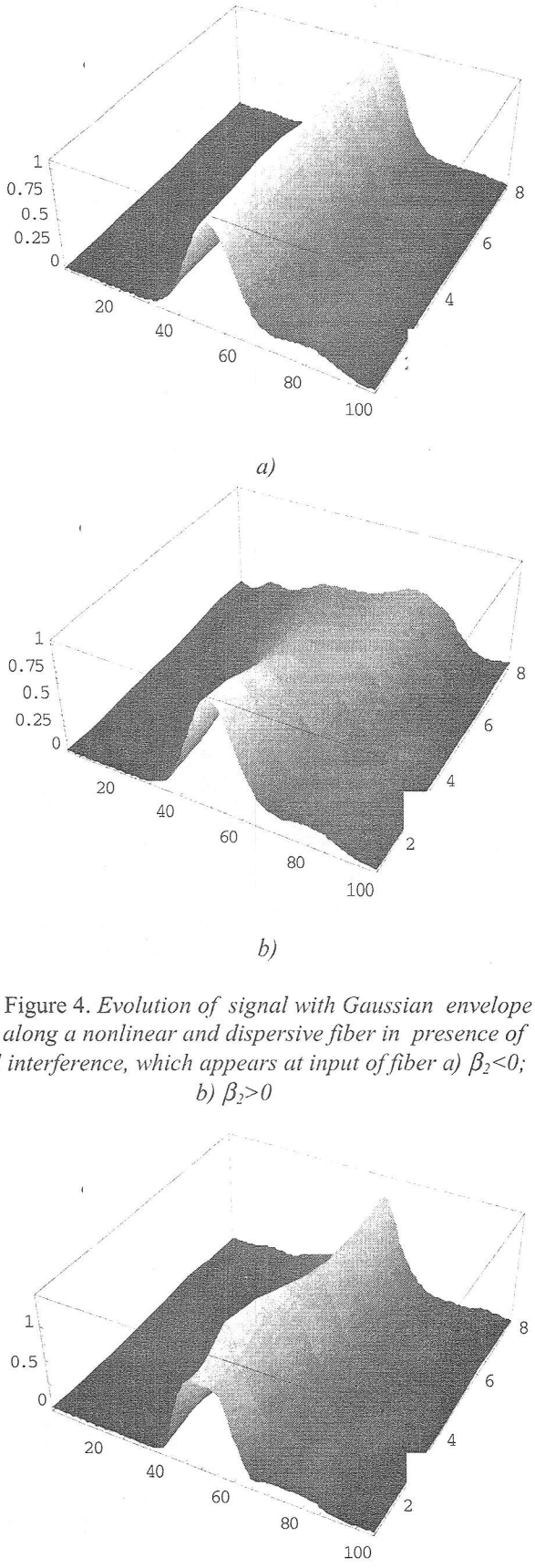

Figure 4. *Evolution of signal with Gaussian envelope form along a nonlinear and dispersive fiber in presence of signal interference, which appears at input of fiber a) $\beta_2<0$; b) $\beta_2>0$*

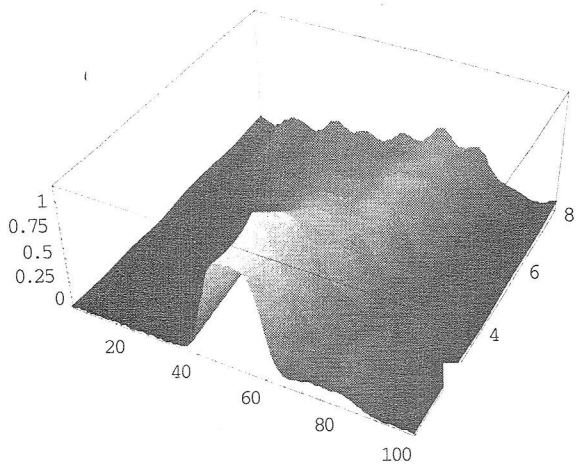

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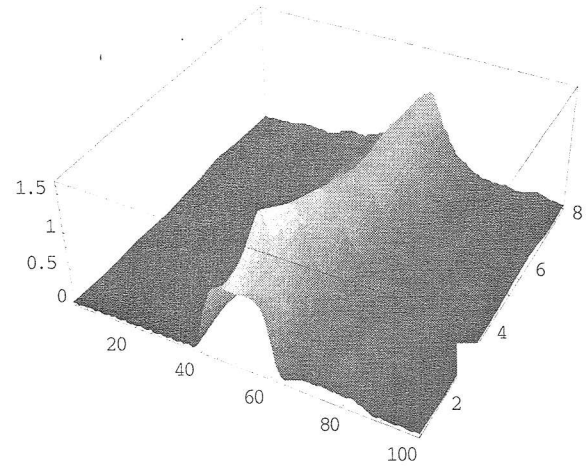
Figure 5. *Evolution of signal with Super-Gaussian envelope form (m=2) along the nonlinear and dispersive fiber in presence of signal interference, which appears at input of fiber a) $\beta_2<0$; b) $\beta_2>0$*



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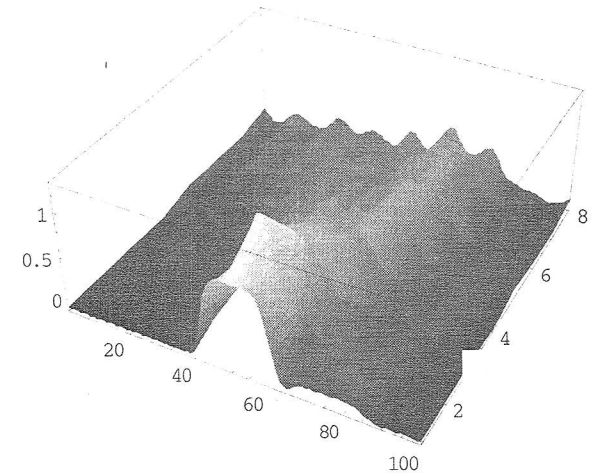

b)

Figure 6. *Evolution of signal with Super-Gaussian envelope form (m=3) along the nonlinear and dispersive fiber in presence of signal interference, which appears at input of fiber a) $\beta_2<0$; b) $\beta_2>0$*

4. CONCLUSION

Optical pulse with Gaussian envelope better keeps own pulse shape along the nonlinear and dispersive than Super-Gaussian forms. We could see that the increasing of parameter m leads to larger pulse disturbance along the fiber. The influence of signal interference at signal propagation is least for Gaussian form of envelope, and this influence increases if parameter m take biger value. Also, we can see that the propagation performance is better in anomalous than normal dispersion regime, in all cases, because cooperating work GVD and SPM.

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AN INTERACTIVE KNOWLEDGE BASED ANALOG DESIGN APPROACH

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Abstract – *Many CAD tools based on different methods are made to assist in analog design tasks. A lot of these methods use "global" analog design approach and can not really give insight into very complex interdependence of circuit and transistor level parameters. To really help the designer, a interactive analog design tool which can be used with the simulator is needed. In this paper, we present a standalone PC windows based tool for basic analog structures sizing that uses an interactive knowledge based analog design approach. A new chart-based approach is chosen to give the designer an intuitive understanding of the device behaviour. Transistor level calculator is capable to explore some complex relations and enables design of basic analog structures. Systematic operational amplifier design procedure is also implemented.*

1. INTRODUCTION

Every analog design task consists of one very common procedure – for given circuit specifications, the geometrical dimensions and bias current of each transistor of a circuit have to be determined. To accomplish this task analog designer usually uses the simulator as a unique tool that allows for the circuit parameter values to be changed, and to observe the effect. In this way, analog design procedure becomes very long-lasting, discovering of the interdependencies between circuit and transistor level parameters can be very difficult and large number of simulation runs is needed. On the other side, the simulator offers an accurate modelling, high precision calculations, but only global simulation approach.

In recent years, many CAD analog design tools are developed. The aim of these tools is to assist in analog design procedure. A lot of attempts are made to completely replace the designer and to automate analog design procedure. The role of designer is to supply the specifications and to "press one button". This automatic approach can give an optimal solution in very limited number of problems and for all other problems the designer goes back to the simulator, continuing very long and difficult procedure.

What the designer really needs is an interactive visualisation approach which can be used together with the simulator. In this way, he has an intuitive understanding of basic analog structure behaviour, all performances and dependencies displayed interactively, and minimal number of simulation runs. For this kind of a tool an automated design methodology for CMOS analog circuit blocks has to be used, which means cell level sizing approaches and even design oriented characterisation of CMOS transistor.

2. CAD TOOLS OVERVIEW

An overview of the most important previous CAD tools and methodologies is following.

- *Simulation tools*, such as Hspice, Psice, Eldo. This tools are easy to use, with very accurate modelling. But, on the other side global simulation approach which includes AC, DC, and transient analysis is very limitative for analog design procedure because of difficulty to discover tradeoffs. Nevertheless, every analog designer uses the simulator, and there is no replacement for this kind of tool.
- *CAD tools for design automation* that are based on top-down hierarchical design strategy and usually cover the full design path: topology selection, transistor sizing and layout generation. Some of them are made like software packages that for every design phase (topology selection, optimum sizing, layout generation, verification) have one special tool which is incorporated with all others according to precise design procedure. The representatives [1-8] are:
  - **ACACIA (OASYS, ANAGRAM)**, Carnegy Melon University, 1989.
  - **OPASYN**, University of California, Berkeley, 1990.
  - **ADAM (IDAC, ILAC, SYNAP)**, CSEM, 1990.
  - **ASAIC (HECTOR, OPTIMAN,AUTOLAC, ISAAC, DONALD)**, UKL, 1990.
  - **CHIPAIDE**, Imperial College, University of London, 1990.
  - **ASCOTA**, Electronic faculty, University of Nis, 1992.
  - **AMGIE**, UKL, 2001.

  These tools are made to automate almost every step and to give solution for specified problem. But, sometimes interactive action of the designer is very limited.
- *Automatic transistor sizing tools based on special mathematical methods and functions*, such as **GPCAD** tool [9], which uses convex optimization techniques and geometrical programming. These methods can solve large problems, with thousand of variables and constraints, and assure that global solution is always found.

Recent scientific research shows that there are more and more analog cell sizing approaches and even design oriented CMOS characterisations techniques [10-12]. These approaches are suitable to built in previous design experience and knowledge, to discover analog design tradeoffs very easy, to perform circuit partitioning and to accomplish procedural design. The designer has lot of freedom and can work in parallel with the simulator. What is missing to make this methodologies almost perfect for the analog design is the interactivity and visualization [13].

3. AN INTERACTIVE KNOWLEDGE BASED ANALOG DESIGN APPROACH

A new windows based tool for basic analog structures sizing has been developed. This is an interactive chart-based tool that allows to visually explore complex relations and parameter dependencies. This approach is chosen to give an

intuitive understanding of the device behaviour. Transistor level calculator uses complete set of equations based on EKV MOS model. It takes into account circuit topology as well as users defined specifications. The tool is knowledge and experience based capable to explore complex interdependencies and relations. Only basic design rules and principles are imposed, and the designer has a lot of degree of freedom. The tool can be very easily used in conjunction with the simulator, allowing design of very complicated circuits, as well as basic analog structures. The tool structure is presented in Figure 1. In the next a short description of the modules will be given.

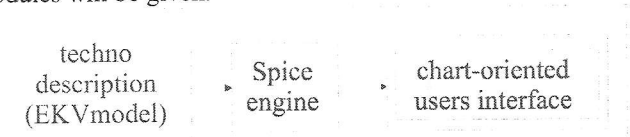

Figure1. The tool structure

- *The techno parameters and transistor model* – For the transistor modeling EKV MOS model [14, 15] is chosen. This model is very suitable for the circuit simulation because it links weak to strong inversion of the transistor operation in continuous way. A set of equations that is implemented can be inverted very easy. This is very important property, because it allows to find solution for different input parameter sets without using complex numerical methods. In addition, very large number of the transistor parameters important for the analog design procedure can be calculated. Those are: inversion factor, saturation voltage, Spice like threshold voltage, Early voltage, small signal parameters, parasitic capacitances, gm/ID ratio, transconductance efficiency factor etc.
- *The equations* – During analog design procedure, in order to discover the tradeoffs, the designer has to drive different sets of equations. The interdependencies between the parameters at the circuit level of description and the transistor level of description can be very complex. For some complicated circuits, sometimes it is very difficult to find exact expressions for some circuit parameters. So, the approach which is based on driving the equations for given specifications and finding an optimal solution becomes almost impossible.
- *Circuit partitioning and basic analog structures* - In the newly developed tool we implement an opposite point of view. Every analog circuit, even the most complicated one, can be divided into basic analog structures, from which we can form "analog library". The basic analog cells for the most common analog tasks are: current mirror, differential pair, cascode stage, cascode current mirror. If designer can analyze every of this basic structures, if he can determine easily the important properties and parameters, then he can easily size every block. All these analog basic structures are very well analyzed in the literature. This huge theoretical knowledge together with practical experience is implemented in our approach. A separate transistor is also considered as a basic analog structure, so the designer can analyze every transistor and its parameters in the environment imposed by the circuit, and easily to take some decisions for circuit design. In that way analog design becomes very simple, and the simulator becomes a tool for fine tuning.
- *The chart-oriented interface* – The visualization is the most important property of presented approach, because it allows transcription of set of mathematical relations into an appropriate graphical representation. The user-friendly graphic interface is made in the same manner for every block. The designer can enter different parameter sets, change basic parameters and observe in the same time values of all other parameters. Besides the general transistor parameters, for every analog structure the specific parameters are calculated. In this way, the designer doesn't have impression that he works with the set of equations. All the time he is concentrated to the analog structure and its important properties that are visualized. After some time of interaction, the designer gets an intuitive understanding of the structure's behavior. This is an excellent way to built on previous experience and knowledge. For an expert who designs on the analog structure level, this is excellent, very easy-used tool. For non expert, this can be very good didactical tool. An example of the users interface for the current mirror design is shown in Figure 2.

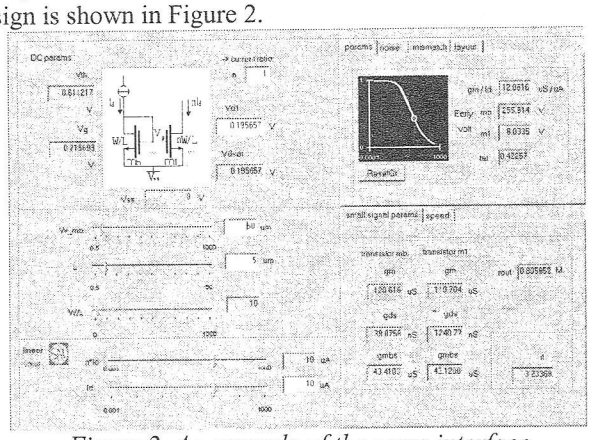

Figure 2. An example of the users interface

- *The design procedure* - The proposed design procedure is based on one transistor cell design, and the techniques that are very similar to [11, 12]. Every analog structure can be presented as a set of transistors, so it can be designed using the same way of reasoning. The key parameter is the g_m/I_D ratio. It is a measure of the translation of current into transconductance and in the same time gives indication of inversion level. The proposed design steps are following:
  - set the priority targets (speed, area, noise, …)
  - set the bias current
  - set the g_m/I_D ratio according to the circuit level specifications
  - change interactively the free variables, that are defined for every structure
  - watch in the same time all other parameters
- *The analog structures library* – A library of basic analog structures was created. We define a general behavior, related to the transistor, and a specific behavior, related to the structure. For every structure graphic interface consists of general parameters and specific parameters for that structure. The following basic analog structures are implemented:

- *NMOS transistor cell*
- *PMOS transistor cell*
- *N current mirror*
- *P current mirror*
- *N cascode current mirror*
- *P cascode current mirror*
- *N cascode stage*
- *P cascode stage*
- *N cascode pair*
- *P cascode pair*
- *N folded cascode stage*
- *P folded cascode stage*

- *The systematic design of operational amplifiers* – This tool offers possibility to perform the systematic design of operational amplifiers. In the present version three structures are implemented:
  - *OTA*
  - *Miller operational amplifier*
  - *Folded cascode operational amplifier*

For these structures the knowledge based design methodologies and procedures are implemented. First design step is to enter the design specifications. Then, every circuit is partitioned into basic analog structures, and previously described analog structure design procedure is implemented. All the time, it is possible to supervise the circuit specifications, but there are no imposed values. Simply, the designer can see the effect of his decisions on the circuit performances. After all blocks are designed, the circuit behaviour is summarised and the interaction with the simulator is proposed. The basic design procedure is illustrated in Figure 3.

This procedure can be repeated several times in the interaction with the simulator in order to perform fine tuning. In this way, the transistor sizing and circuit optimization can be achieved at the same time.

4. NEW APPROACH DISCUSSION

The new interactive knowledge based analog design approach has plenty of advantages. It is based on interactive, very easy to use procedure. The experience and knowledge are implemented and transferred in an intuitive way. Wide range of circuits can be designed – from the simplest to very complicated one, using this evolutive approach. On the other side, all simulation based methodologies limit the designer's interactive action, and the full mathematical methodologies limit implementation of "know-how" skills.

The disadvantage of this approach is that system design of cells is mandatory for transfer into procedural approach.

5. CONCLUSION

In this paper a new chart based approach and CAD tool are presented. The interactive knowledge based tool can be used together with the simulator. It is dedicated to help analog designer to make optimum design choices. For an expert this is very useful procedural design tool, for non expert this can be a didactical tool. Anyway, designer's time can be saved using transistor level calculator capable to explore the complex relations and the charts to display transistor level performances interactively.

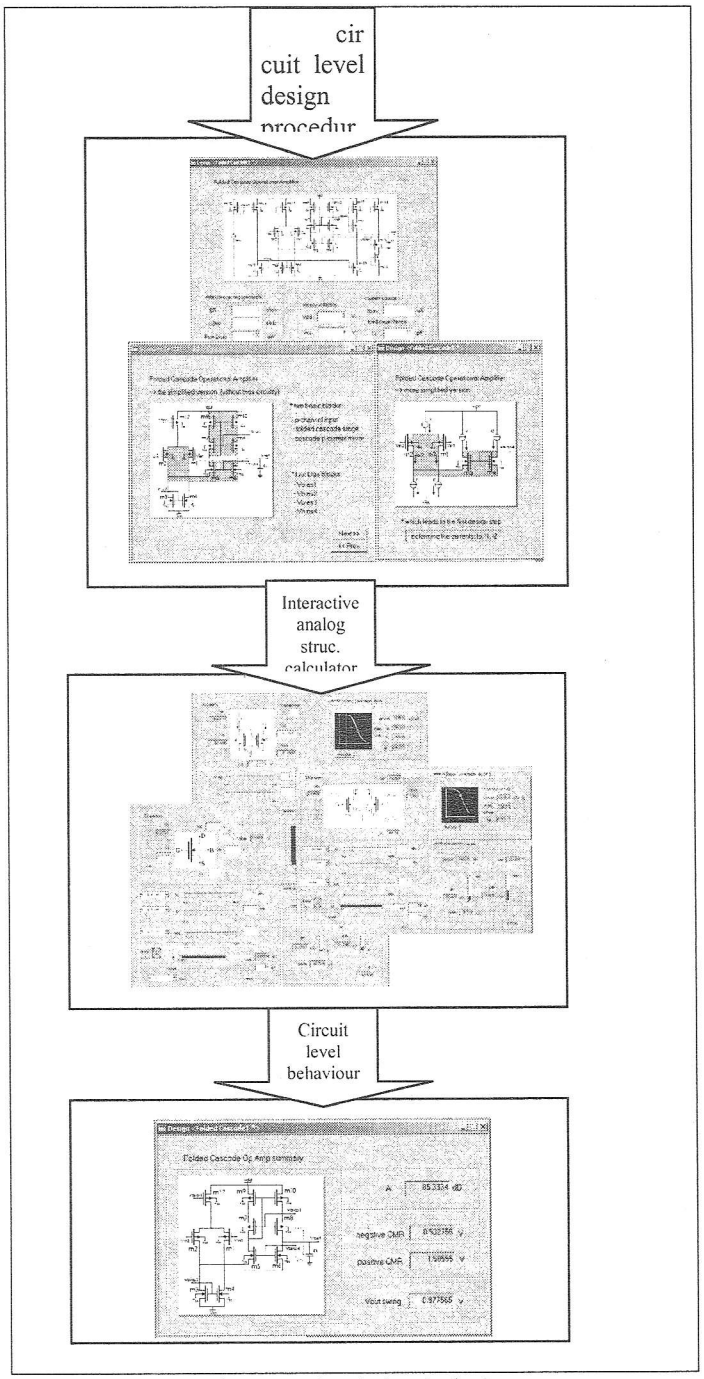

Figure 3. The procedural circuit design

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VEKTRA - A TEST BENCH FOR STUDENT EXERCISES AND DEVELOPMENTOF DIGITAL CONTROL ALGORITHMS FOR AC DRIVE CONTROL

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Abstract –*Laboratory Station for Vector Control of Induction Motor Drives, Vectra, is observed in this paper. This station is placed in the Laboratory for a Microprocessor Based Electrical Drive Control of Faculty of Electrical Engineering in Banja Luka. Basic parts of station as well as two implemented algorithms, Algorithm for Minimization Power Losses in Vector Controlled Induction Machine Drive and New Concept of Direct Torque Control of Induction Machine Drives are presented in this work.*

1. INTRODUCTION

Laboratory Station Vectra is purposed for development and testing different algorithms of induction machine drive control, scalar control, V/f control, vector control, direct torque control, efficiency improvement etc. Also, different methods for three-phase DC/AC converter control, like PWM modulation, space vector modulaton and harmonic elimination based technique can be implemented on Vectra. Vectra is primary purposed for the student education but, also, advanced algorithms for induction machine drive control are developed and verified. Hardware and Software of Vectra and two successfully implemented experiments are short presented in this paper.

Laboratory station is made following the model of samename station at the Faculty of Electrical Engineering in Belgrade. Comparing with the Vectra at the Faculty of Electrical Engineering in Belgrade station in Banja Luka is modernized especially on its acquisition and control elements using digital signal prosessor (DSP) based controller board . In this way we obtained better control characteristics. Also, modern software tools are available for programming and any changes in control software can be simple done.

Basic parts of the Laboratory Station Vectra are:

- induction motor
- incremental encoder connected with the motor shaft,
- three-phase drive converter (DC/AC converter and DC link),
- PC and dSPACE1102 controller board with TMS320C31 *floating point* processor and peripherals,
- interface between controller board and drive converter. Picture of Laboratory Station Vectra and its block diagram are shown in Fig.1. and Fig.2.

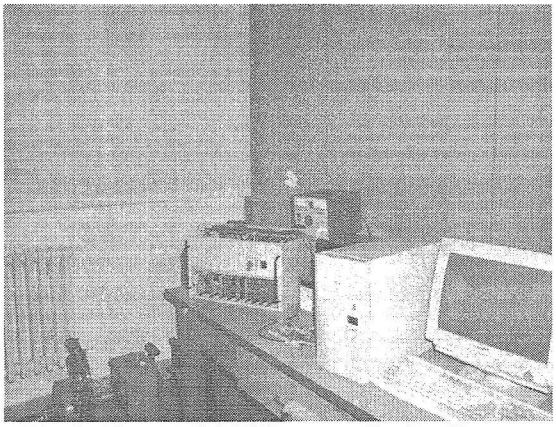

Fig. 1. Picture of the laboratory Station Vectra.

dSPACE DS1102 control board with digital signal processor is connected to PC via ISA slot. Control and acquisition function as well as signal processing are executed an this board, while PC provides comfortable interface toward user. Controller board DS1102 is purposed for digital signal processing and real time control. It consists of :

- TMS320C31 digital signal processor,
- TMS 320P14 microcontroller,
- 128×32 zero wait state static RAM,
- serial interface,
- 4 A/D converter (2 16-bit and 2 12-bit),
- 4 12-bit D/A converter,
- 2 incremental encoder interface,
- Host interface and
- digital I/O subsystem [4, 5].

DS 1102 control board block diagram is shown in Fig3.

TMS320C31 is a high performance floating point processor. It makes parallel multiply and aritmetic or logic operation on integers or real numbers presented in floating point format in only one singl instruction execution time. Single instruction execution time is 33.33ns. Processor supports a large address space $(16M \times 32)$ with various addressing modes allowing the use of high–level languages for application development [4-7].

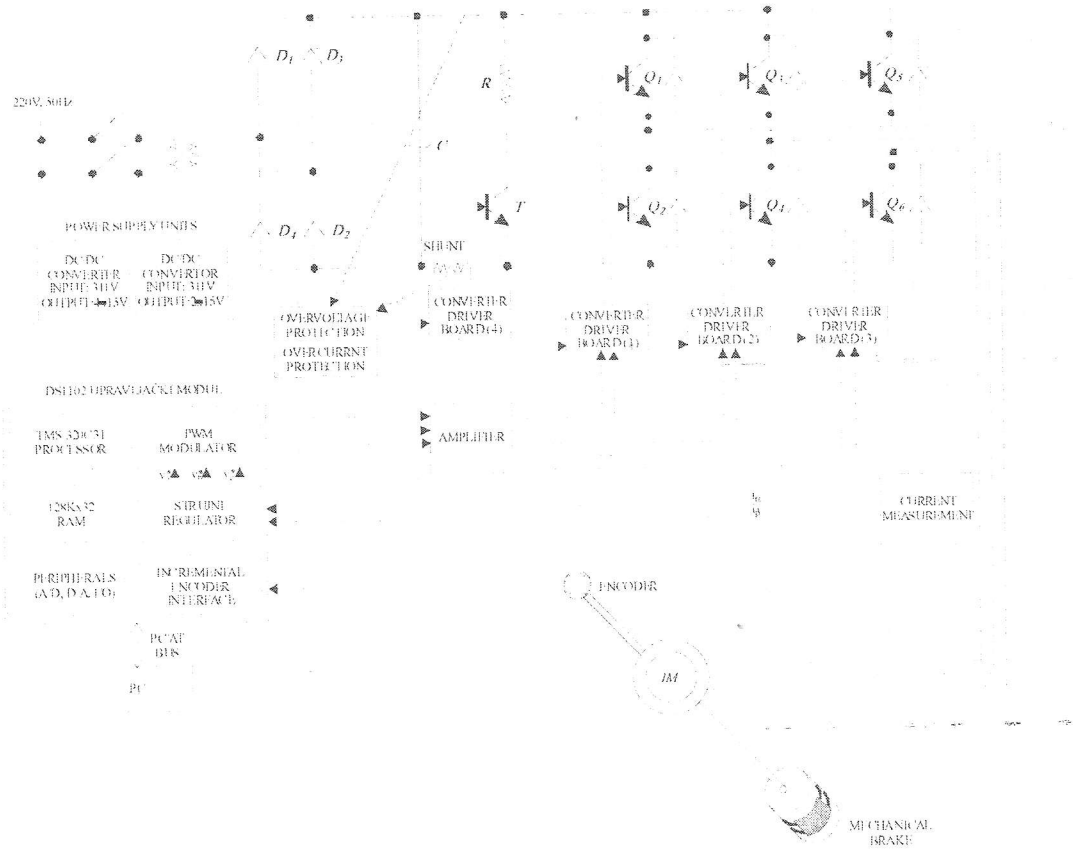

Fig 2. Block diagram of laboratory Station Vectra.

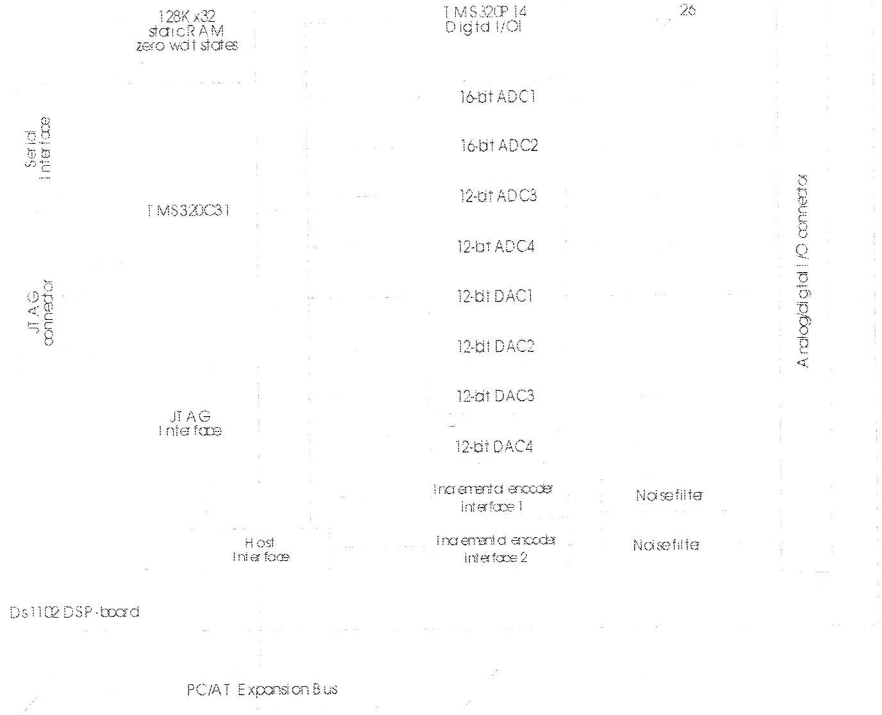

Fig. 3. Block diagram of DS1102 Controller Board.

Electrical motor in Vectra is squirrel cage 3-phase 4-pole induction machine. Motor parameters are given in the appendix of the paper.

Incremental encoder connected with motor shaft, gives 1000 pulses per cycle and it is used as speed and position sensor.

Drive converter is realized as 3-phase inverter bridge with 100A transistors and feedback diodes. Inverter is supplied from the standard distributive power source (220V, 50Hz), over 1-phase transformator, rectifier and DC link. Electrolyte capacitor 450V, 1000μF is built in DC link to reduce voltage ripple. There is one driver board for every inverter phase. Inverter drivers amplify control signals from the controller board and electrically isolate control stage from the power stage. Also, there is resistor built in inverter for power disipation during braking and generatory work of machine.

Analog and digital I/O subsystem of DS1102 controller board is adopted for real time applications. Some peripheral units are used in Vectra; PWM unit, incremantal encoder intarface and A/D converters.

Also, peripheral interface obtains power supply for incremental encoder and makes dead time control. Dead-time can be tuned from 0.1μs to 40μs.

Current sensor in Vectra is Hall's probe. Two Hall's probes are used and information of measured currents is hold by two A/D converters on the controller board. One Hall's probe measures a-phase current and second difference between b-phase and c-phase current. In this way we acquire information about stator currents in $\alpha-\beta$ system. Machine stator currents in $\alpha-\beta$ system are given by [1]:

$$i_\alpha = i_a, \tag{1}$$

$$i_\beta = \frac{1}{\sqrt{3}}(i_b - i_c). \tag{2}$$

Hall's probes convert measured currents into voltage signals and also electrically isolate controller board from the electrical machine. Voltage signal level is adapted to A/D converter input level by resistor divider. Each of the A/D converters contains a 16-bit successive converter, and a sample/hold circuit. The converter achieves a conversion time of 4μs. All A/D converters have single-ended bipolar inputs with ±10Vinput span.

Incremental encoder signals are hold by two incremantal encoder interfaces on the controller board. Each interface containes differential line-receivers for the input signals, a digital noise pulse filter, a quadrature decoder which converts the sensor's phase information to count-up and count-down pulses, a 24-bit counter which holds the current sensor position and a 24-bit output latch. Maximum count frequency is 8.3 MHz. [4,5].

PWM signals are generated in the compare unit in digital I/O subsystem on the DS1102 controller board. One of the feature of compare unit is the high precision PWM operating mode, and six PWM output lines is available. The compare unit consists of six compare registers and six action registers controlling the output pins. The compare registers continously compare their valuas with the counter registers of timer 1 or timer 2. If match is found corresponding output pin is set to 0 and high precision PWM signal is generated [4, 5].

2. SOFTWARE REALIZATION

dSPACE controller board with high performance TMS320C31 processor supports different programming techniques from the assembler to high-level languages. Two implemented algorithms described in this paper are software realized using Matlab – Simulink and dSPACE real-time interface for dSPACE hardware. dSPACE DS1102 Development Kit contains software for development real-time applications as Simulink models or C programs. This software is installed in Matlab ver. 5.1 or later and provides additional Simulink Toolbox for development real-time applications as Simulink models and their compiling, downloading and execution [6, 7].

dSPACE Development Kit contains:

- *MLIB/MTRACE* program library
- dSPACE Real-Time Library (*RTLib1102*)
- ControlDesk software which provides all the functions for controlling, monitoring and automating real-time experiments and makes the development of controllers more effective.
- Control Desk Hardware Management which offers the functions to handle a real-time applications assigned to the boards, such as download and start a real time application, stop real-time application, automatic loading of variable description files etc.

The Instrumentation Kits of ControlDesk which provides a set of powerful instruments. They are designed to monitor and/or control real-time variables interactively and to displey real-time captures.

Automate ControlDesk which offers automation the complete funcionality of ControlDesk by using the programming interface to the Pyton language.

Programming a real-time application in the dSPACE Development Kit is same as any other Simulink application. Interface with peripherials on the board is made by using corresponding blocks in the dSPACE Toolbox.

After Simulink model is finished and simulation parameters are specified a Build procedure can be started. During Build procedure Simulink blocks are automatic translated in the machine code and downloaded into program memory. Handling real-time applications can be done in Matlab or ControlDesk. ControlDesk graphic interface with the trace of measured variable on is shown in Fig. 4.

Sampling frequency depends from the application and in the applied experiments it was in the range from 2kHz to 3.5kHz.

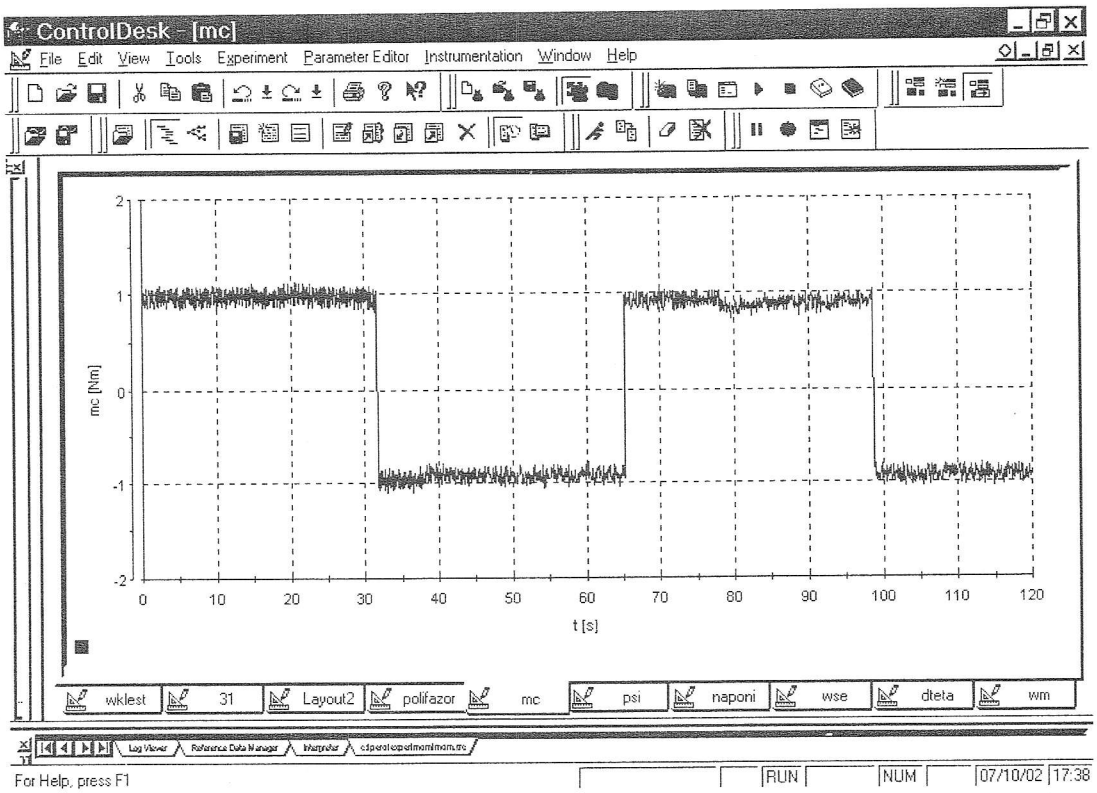

Fig. 4. ControlDesk graphic interface with the trace of measured variable on (machine torque).

3. EXPERIMENTAL VERIFICATION OF ALGORITHM FOR POWER LOSSES MINIMIZATION IN VECTOR CONTROLLED INDUCTION MACHINE DRIVE

A Fuzzy Based Algorithm for Minimization Power Losses in Vector Controlled Induction Machine Drives is observed in the paper [2}. Power losses as well as heating of machine can be reduced by this application. It holds qualitative characteristics of search based algorithms but also provides less torque ripple with flux changes, less sensitivety to load perturabations and better control characteristics. This algorithm is experimentally tested and verified on the Laboratory Station Vectra.

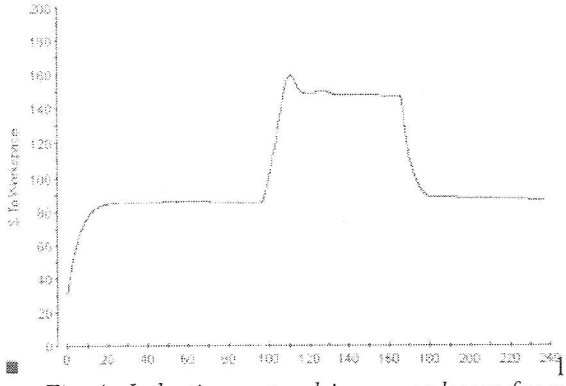

Fig. 4. Induction motor drive power losses for a step load torque and without algorithm for minimization losses.

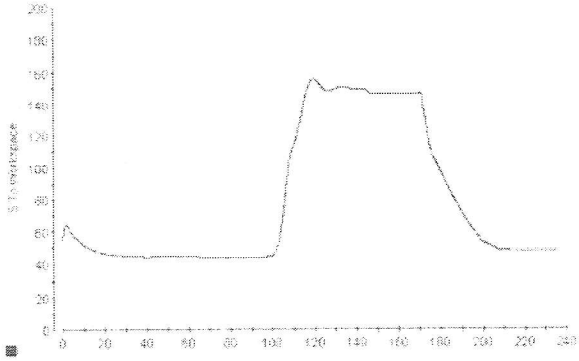

Fig. 5. Induction motor drive power losses for a step load torque and with algorithm for losses minimization.

Used electrical drive is indirect vector controlled, so Park's transformation is performed using information of motor speed. Speed sensor is existing incrementral encoder in Vectra. Stator current are measured by Hall's probes and hold by two A/D converter on the board. Inverter is driven by PWM signals generated in the capture unit on the controller board and amplified in the inverter drivers.

Power losses in the machine drive with and without appllied algorithm are shown in Fig. 4. and Fig. 5. respectively.

Applying this algorithm for power losses minimization next results are obtained:

Less torque ripple with flux changes;

Less drive sensitivity to load perturbations;

Electromagnetic torque margin is controlled so better control characteristics are obtained.

Total power losses are reduced especially when machine works with small loads.

4. EXPERIMENTAL VERIFICATION OF ALGORITHM OF DIRECT TORQUE CONTROL

Algorithm of Direct Torque Control is detailed observed in [3] and experimentally verified on the Laboratory Station Vectra. Software was written using Simulink and dSPACE Real-Time Library. Sampling frequency in this application is 3.5kHz. This algorithm doesn't use speed sensor information so only used peripherals are A/D converters and PWM unit.

Significiant problem in experiments was noise in the information of measured currents. This noise is filtered by low-pass hardware filter. According [3] experimental results are good and a case when torque and flux change are assigned in the same moment are shown in Fig 6. and 7.

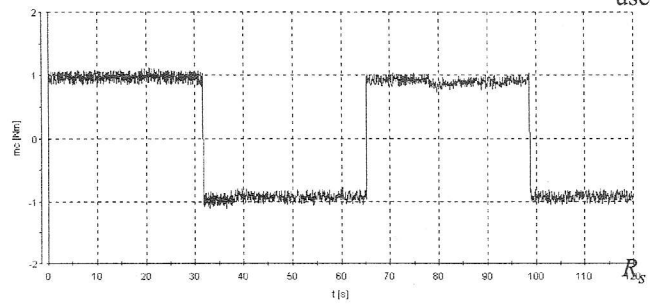

Fig. 6. Machine torque.

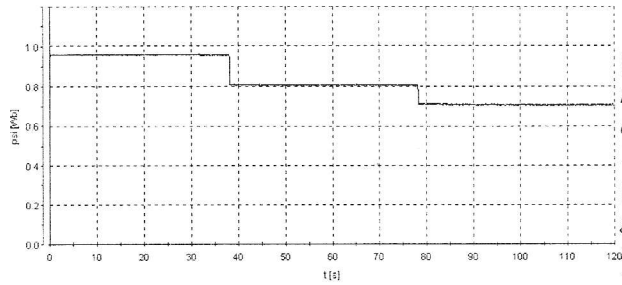

Fig.7. Machine flux.

Proposed Algorithm of Direct Torque Control in comparing to others is more simple and gives same or better torque and flux control [3]. Experimental tests show good characteristics of the algorithm.

5. NOTICED PROBLEMS

Laboratory Station Vectra, except dSPACE controller board is completely made by discrete components available on the domastic market. So, there is imperfects in Vectra in comparing with industrial drives. Noticed imperfects can be minimized:

- Dead–time effect is significant so dead-time compenstaion must be done by software;
- There is no possibility for automatic control AC power supply volatge and voltage in DC link, so constant inverter input voltage holds constant using regulated transformer.
- Significant vibrations appear on higher speeds (field-weaking region) and through motor shaft carry to encoder and cause speed mesurment error. Dinamic brake balance and more qualitative junction between motor shaft and encoder should be made.
- Noise in the information of mesured currents can be eliminated by well-designed low-pass hardware filter.

Besides above mentioned imperfects, by applying methods for negative effects elimination, Laboratory Station Vectra is successfully used.

Main advantage of Vectra in relation to industrial drives is in its programming and simple development of the applications.

6. CONCLUSIONS

Laboratory Station –Vectra and its posibilities in development and testing application of power converter and induction motor drive control are observed in this paper. Some practical experinces in works with Vectra and two implemented algorithm are presented. These results can be useful in development similar laboratory stations.

APPENDIX

Parmeters of the motor in Laboratory Station Vectra

3 MOT		$\Delta 220 / Y 380V$
$3,7 / 2,12A$		$0,75kW$
$\cos\varphi = 0,71$	$1410o / \min$	$50Hz$

$R_s = 10,4\Omega \quad R_r = 11,6\Omega \quad L_{\sigma s} = 22mH \quad L_{\sigma r} = 22mH$

$L_{mn} = 0,557H \quad J = 1,2kgm^2$.

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APPLICATION OF INTERNAL MODELS IN THE DESIGN OF DIGITALLY CONTROLLED ELECTRICAL DRIVES

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Abstract: *The design of a controlling structure with internal models for digitally controlled electrical drives is given. In the control portion of the structure, the nominal model of the plant and model of immeasurable external disturbances are included to improve the system robustness and to extract the expected class of disturbances. Particular attention is paid to the design of IMPACT (Internal Model Principle and Control Together) structure for digitally controlled drives and a suitable modification of the structure is proposed in order to improve the system performance and to facilitate system synthesis.*

Keywords: *Principle of absorption, Immeasurable external disturbance, IMPACT structure, Controlled electrical drives, Newton's predictor.*

1. INTRODUCTION

In many applications of controlled electrical drives the high dynamical performance and capability of the system to reject the influence of external disturbances on the steady-state value of the controlled variable are required. In the tracking regime, the tracking error is to be reduced to the level of sensor resolution, in the presence of the generalized disturbance that comprises the external disturbance and uncertainties of plant parameters. These requirements can be achieved by the design of IMPACT controlling structure [1-4] suited for the design of speed- and position-controlled electrical drives.

The IMPACT structure has the merits of both the structures based upon the IMP (Internal Model Principle) and IMC (Internal Model Control) [1,5]. As it is known, IMP means the inclusion of disturbance model into the controlling structure in order to compensate effects of expected class of external disturbances on the system output or the system controlled variable (angular speed or position of the motor shaft). The IMC structure is not suitable for disturbance rejection but it enables the achievement of the robust system stability and high dynamic performance.

In this paper, the conventional IMPACT structure is described and then its modification is proposed for application to the structural design of digitally controlled electrical drives. It will be shown that the application of predictive filters instead of disturbance observer, including the model of disturbance, gives the same or even better system performance. Unlike the structure with disturbance observer, the alternative control structure, proposed in this paper, is simpler and with a smaller number of tuning parameters within the internal models by which the robustness, filtering properties, and high dynamic performance of the system can be easily adjusted.

2. PRINCIPLE OF ABSORPTION

Suppose that kth sample of an external disturbance $f(t)$ may be determined by a finite number m_0 of previous samples. Then, the disturbance is regular and may be described by extrapolation equation [4]

$$f(kT) = D_f(z^{-1}) f((k-1)T) \qquad (1)$$

where $D_f(z^{-1})$ is the prediction polynomial of order m_0 -1. Relation (1) is called the equation of extrapolation or prediction [4] and it may be rewritten as

$$(1 - z^{-1} D_f(z^{-1})) f(z^{-1}) = 0 \qquad (2)$$

where $f(z^{-1})$ denotes the z-transform of disturbance. Relation (2) is called compensation equation and FIR filter having the pulse transfer function $1 - z^{-1} D_f(z^{-1})$ is the absorption filter or the compensation polynomial [4].

Absorption filter $\Phi_f(z^{-1}) = 1 - z^{-1} D_f(z^{-1})$ is designed for a known class of disturbances and its impulse response becomes identically equal to zero after n sampling instants, where $n \geq m_o$. Hence, the compensation equation (2) may be considered as the absorption condition of a given class of disturbances. The condition can be expressed as

$$\Phi_f(z^{-1}) f(z^{-1}) = 0, \text{ for } t = kT \geq (\deg \Phi_f) T. \qquad (3)$$

The extrapolation polynomial $D_f(z^{-1})$ is determined by an apriori information about disturbance $f(t)$ [4, 6], nevertheless, it is simply resolved as

$$\Phi_f(z^{-1}) = D_w(z^{-1}), \text{ from } f(z^{-1}) = \frac{N_w(z^{-1})}{D_w(z^{-1})}. \qquad (4)$$

In the case of a stochastic disturbance $s(t)$, absorption filter (4) should suppress as much as possible effects of disturbance on the system output. Thus, for a low frequency disturbance $s(t)$, which can be generated by double integration of the white noise, an appropriate choice of absorption filter is $\Phi_s(z^{-1}) = (1 - z^{-1})^2$ that corresponds to absorption of linear (ramp) disturbance [1, 7]. In majority of practical applications an appropriate choice might be $D(z^{-1}) = 2 - z^{-1}$. According to (4), prediction polynomial $D(z^{-1}) = 2 - z^{-1}$ rejects ramp disturbances; but, it enables also the extraction of slow varying disturbances and even suppression of the effects of low frequency stochastic disturbances.

3. IMPACT STRUCTURE

In the IMPACT structure shown in Fig.1, the controlling process is given by its pulse transfer function or by polynomials $P_u(z^{-1})$ and $Q(z^{-1})$, and the process dead-time given by integer k. Within the control portion of the

structure in Fig.1 (shaded part) two internal models are included: the two-input nominal plant model

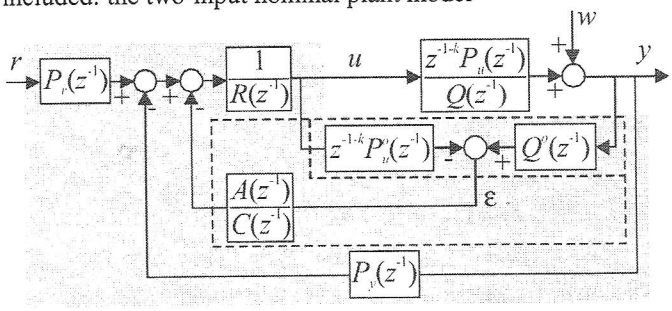

Fig.1. IMPACT controlling structure

$$W^0(z^{-1}) = \frac{z^{-1-k}P_u^0(z^{-1})}{Q^0(z^{-1})} \tag{5}$$

explicitly and the disturbance model embedded into the discrete filter $A(z^{-1})/C(z^{-1})$. Both the internal nominal plant model and disturbance model is treated as the disturbance estimator. The control portion has two control loops that can be designed independently. The minor local control loop is designed by the proper choice of polynomials $A(z^{-1})$ and $C(z^{-1})$, while polynomials $P_r(z^{-1})$ and $P_y(z^{-1})$ in the main control loop are determined to achieve the desired system set point response. For a minimal phase plant, the proper choice of polynomial $P_y(z^{-1})$ is $R(z^{-1}) = P_u^o(z^{-1})$ [1].

Under the nominal conditions $(P_u(z^{-1}) \equiv P_u^0(z^{-1}),\ Q(z^{-1}) \equiv Q^0(z^{-1}))$ and for $R(z^{-1}) = P_u^o(z^{-1})$, the closed-loop transfer functions $y(z^{-1})/r(z^{-1})$ and $y(z^{-1})/w(z^{-1})$ are easily derived from Fig.1 as

$$\frac{y(z^{-1})}{w(z^{-1})} = \frac{Q^0(z^{-1})\left[C(z^{-1}) - z^{-1-k}A(z^{-1})\right]}{C(z^{-1})\left[Q^0(z^{-1}) + z^{-1-k}P_y(z^{-1})\right]} \tag{6}$$

and

$$\frac{y(z^{-1})}{r(z^{-1})} = \frac{z^{-1-k}P_r(z^{-1})}{Q^0(z^{-1}) + z^{-1-k}P_y(z^{-1})}. \tag{7}$$

In virtue of (7), the system set-point response can be adjusted by determining appropriate polynomials $P_r(z^{-1})$ and $P_y(z^{-1})$ according to the desired system closed loop transfer function $y(z^{-1})/r(z^{-1}) = G_{de}(z^{-1})$. Then, the absorption of an external disturbance and the speed of disturbance transient response are adjusted by choosing the structure and parameters of the disturbance estimator.

3.1. Elimination of disturbance

From (6), the steady-state error in the presence of a known class of external disturbance $w(t)$ will become zero if

$$\lim_{z\to 1}(1-z^{-1})\frac{Q^0(z^{-1})\left[C(z^{-1}) - z^{-1-k}A(z^{-1})\right]}{C(z^{-1})\left[Q^0(z^{-1}) + z^{-1-k}P_y(z^{-1})\right]}w(z^{-1}) = 0 \tag{8}$$

In the case of stable polynomial $C(z^{-1})$ and the plant of nonminimal phase,

$$\lim_{z\to 1}\frac{Q^0(z^{-1})}{C(z^{-1})\left[Q^0(z^{-1}) + z^{-1-k}P_y(z^{-1})\right]} \neq 0 \tag{9}$$

and then the relation (8) is reduced to

$$\lim_{z\to 1}(1-z^{-1})\left[C(z^{-1}) - z^{-1-k}A(z^{-1})\right]w(z^{-1}) = 0. \tag{10}$$

As shown later, the stable polynomial $C(z^{-1})$ is to be chosen according to the desired speed of disturbance rejection and the required degree of system robustness and then polynomial $A(z^{-1})$ is determined to satisfy relation (10).

According to the principle of absorption, it is possible to design the observer estimator that rejects any kind of expected disturbances. To this end, consider the class of disturbances having the z-transform $w(z^{-1}) = N_w(z^{-1})/D_w(z^{-1})$. Then, relation (10) is satisfied if the following Diophantine equation holds

$$z^{-1-k}A(z^{-1}) + B_1(z^{-1})\Phi(z^{-1}) = C(z^{-1}) \tag{11}$$

where $\Phi(z^{-1})$ represents the absorption polynomial determined by $\Phi(z^{-1}) \equiv D_w(z^{-1})$. For example, to the polynomial and sinusoidal disturbances ($w(t) = \sum_{i=1}^{m} d_i t^{i-1}$ and $w(t) = \sin \omega t$) correspond respectively $\Phi(z^{-1}) = (1-z^{-1})^{m+1}$ and $\Phi(z^{-1}) = 1 - 2z^{-1}\cos\omega T_s + z^{-2}$, where T_s is the sampling period.

A unique solution of the Diophantine equation, which plays a crucial role in the design procedure of the observer estimator, proposed in this paper, does not exist [8]. Relation (11) is a linear equation in polynomials $A(z^{-1})$ and $B_1(z^{-1})$. Generally, the existence of the solution of Diophantine's equation is given in [9]. According to [9], there always exists the solution of (11) for $A(z^{-1})$ and $B_1(z^{-1})$ if the greatest common factor of polynomials z^{-1-k} and $\Phi(z^{-1})$ divides polynomial $C(z^{-1})$; then, the equation has many solutions. The particular solution of (11) is constrained by the fact that the control law must be causal, i.e., $\deg A(z^{-1}) \le \deg C(z^{-1})$. Hence, after choosing a stable polynomial $C(z^{-1})$ and degrees of polynomials $A(z^{-1})$ and $B_1(z^{-1})$, and inserting the absorption polynomial $\Phi(z^{-1})$ that corresponds to an expected external disturbance, polynomials $A(z^{-1})$ and $B_1(z^{-1})$ are calculated by equating coefficients of equal order from the left- and right-hand sides of equation (11). Polynomial $A(z^{-1})$ obtained by solving (11) guarantees the absorption of the expected class of disturbances, while the choice of $C(z^{-1})$ affects the speed of disturbance rejection, system robustness, and sensitivity with respect to measuring

noise. Good filtering properties and the system efficiency in disturbance rejection are the mutually conflicting requirements. Therefore, to reduce the noise contamination, the low-pass digital filter may be introduced to modify the internal model of the disturbance into

$$\frac{A(z^{-1})}{C(z^{-1})}=\frac{A_f(z^{-1})A_1(z^{-1})}{C(z^{-1})} \tag{12}$$

where $A_f(z^{-1})/C(z^{-1})$ represents the pulse transfer function of the low-pass filter and $A_1(z^{-1})$ is a polynomial that satisfies (11) and thus includes implicitly the internal model of disturbance. The lower bandwidth of the low-pass filter corresponds to a higher degree of system robustness and vice versa [10]. According to [10], complex disturbances require higher order of polynomial $A(z^{-1})$ and it will further reduce system robustness with respect to mismatches of plant parameters.

3.2. Parameter setting

The main control loop of the system of Fig. 1 is designed to achieve the desired set-point response determined by the system closed-loop transfer function

$$G_{de}(z^{-1})=\frac{z^{-1-k}H_{de}(z^{-1})}{K_{de}(z^{-1})}. \tag{13}$$

According to (7), the desired closed-loop transfer function is achieved if the following identity holds

$$\frac{z^{-1-k}P_r(z^{-1})}{Q^0(z^{-1})+z^{-1-k}P_y(z^{-1})}\equiv\frac{z^{-1-k}H_{de}(z^{-1})}{K_{de}(z^{-1})}. \tag{14}$$

To satisfy (14), it is first necessary to solve the Diophantine equation

$$Q^o(z^{-1})+z^{-1-k}P_y(z^{-1})=T(z^{-1})K_{de}(z^{-1}) \tag{15}$$

for polynomials $P_y(z^{-1})$ and $T(z^{-1})$ and then to determine the second polynomial of the main control loop of the system of Fig. 1 as

$$P_r(z^{-1})=T(z^{-1})H_{de}(z^{-1}). \tag{16}$$

where $T(z^{-1})$ in (15) is chosen as a stable polynomial. Recall that, for a minimal phase plant, $R(z^{-1})=P_u^o(z^{-1})$.

The characteristic polynomial $K_{de}(z^{-1})$ is read from (13) or it may be determined by the desired closed-loop system pole spectrum. To improve the system robustness with respect to uncertainties of plant parameters, polynomial $K_{de}(z^{-1})$ may be extended by factors

$$\prod_{i=1}^{n}(1-b_iz^{-1})^i,\quad 0\le b_i\le 0.9. \tag{17}$$

At the beginning, the values of b_i and integer n are to be chosen as small as possible and then they can be increased gradually until the required criterion of robust stability is satisfied. At the same time, polynomial $P_r(z^{-1})$ should be modified into

$$P_r(z^{-1})\frac{\prod_{i=1}^{n}(1-b_iz^{-1})^i}{\prod_{i=1}^{n}(1-b_i)^i} \tag{18}$$

to save the achieved set-point response and to keep unchanged the steady-state value of the system output.

4. MODIFIED IMPACT STRUCTURE

Fig. 2 shows the modified IMPACT structure for the control plants without transport lags, which may be applied for structural design of digitally controlled electrical drives [1,2]. Signal w_M modeled the influence of load torque on system output y (angular speed or position of the motor shaft).

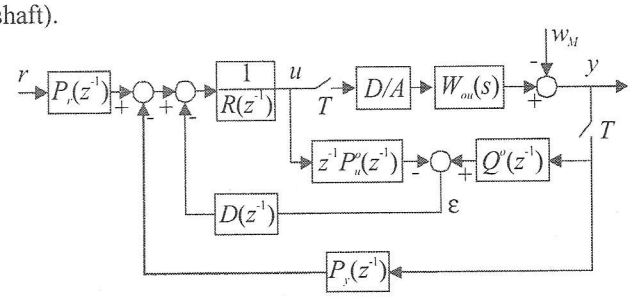

Fig. 2. Modified IMPACT controlling structure

The control plant of the structure in Fig. 2 is given by its nominal pulse transfer function

$$W^o(z^{-1})=\frac{z^{-1-k}P_u^o(z^{-1})}{Q^o(z^{-1})} \tag{19}$$

which is used as a two-input internal plant model within the control portion of the structure. Signal ε estimates the influence of generalized disturbance on the system output. Uncertainties of plant modeling may be adequately described by the multiplicative bound of uncertainties $\alpha(\omega)$ [11]

$$W(z^{-1})=W^o(z^{-1})(1+\delta W(z^{-1})) \tag{20a}$$

$$\left|\delta W(e^{-j\omega T})\right|\le\alpha(\omega),\ \omega\in[0,\pi/T]. \tag{20b}$$

Then, the system of Fig. 2 satisfies the condition of robust stability if the nominal plant is stable and if the following inequality holds

$$\alpha(\omega)<\left|\frac{Q^o(z^{-1})R^o(z^{-1})+z^{-1}P_u^o(z^{-1})P_y(z^{-1})}{z^{-1}P_u^o(z^{-1})(P_y(z^{-1})+Q^o(z^{-1})D(z^{-1}))}\right|_{z^{-1}=e^{-j\omega T}},$$
$$\omega\in[0,\pi/T] \tag{21}$$

The robust system performance is achieved by the operation of the local loop of the structure in Fig. 2. Namely, the role of local loop is to suppress as much is possible the effects of generalized disturbance on the system output. According to the principle of absorption, it is necessary to include, into the control part of the structure, the internal model of disturbance having the input ε. In the case of control plant without the transport lag, the internal model of

disturbance is reduced to the prediction polynomial $D(z^{-1})$. In Tsypkin's works, most frequently the prediction polynomial

$$D(z^{-1}) = 2 - z^{-1} \tag{22}$$

is proposed [3, 4]. This polynomial corresponds to linear disturbances but it effectively rejects different classes of slowly varying disturbances, too, especially in the case of small sampling period [1, 5]. According to the standard procedure of IMPACT structure design [5], in the case of minimum phase plants,

$$R(z^{-1}) = P_u^o(z^{-1}) \tag{23}$$

is to be adopted. The main control loop of the structure in Fig. 2 is designed to achieve the desired pulse transfer function $G_{dc}(z^{-1})$ of the closed-loop system. Namely, by equating identically the desired $G_{dc}(z^{-1})$ with

$$G_{dc}(z^{-1}) \equiv \frac{z^{-1}P_r(z^{-1})}{Q^o(z^{-1}) + z^{-1}P_y(z^{-1})} \tag{24}$$

one can easily determine the polynomials $P_y(z^{-1})$ and $P_r(z^{-1})$ and thus the structure design is completed.

In the structure of Fig. 2 the encoder detecting the angular speed or position is not indicated. When the rezolver to digital converter (R/D) of limited resolution is applied, the measuring signal is contaminated by quantization noise [2], which produces the fluctuation of control variable and losses in the motor. The predictive filter in the local loop increases the noise and that makes the system more sensitive to quantization of the speed and position. Therefore, the structure of Fig. 2 is modified by including the extended observer, as is shown in Fig. 3. The observer is extended by the model of disturbance to enable the estimation of angular speed in the case of the presence of a constant or slowlyy varying disturbance.

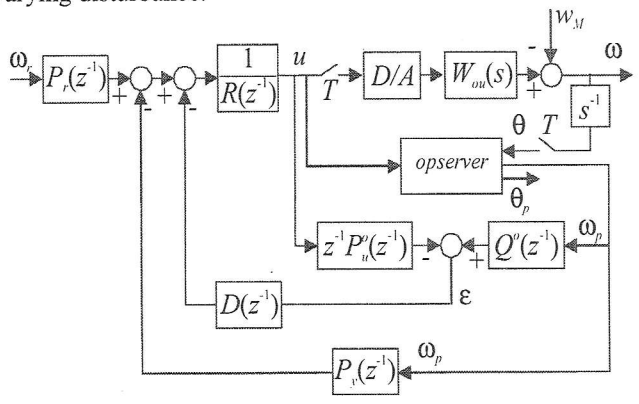

Fig. 3. Modified IMPACT structure of digitally controlled speed servomechanism

In this paper, for the extraction of disturbance, the simple polynomial predictor is applied in the local minor loop of the structure of Fig. 3, instead of internal model of disturbance used in the ordinary IMPACT structure of Fig. 2. Generally, the predictive filter is defined as an algorithm that estimates future values of the input signal and suppresses the noise contamination [12]. The relatively simple forms of digital predictive filters corresponding to polynomial disturbances are treated.

Suppose that signal $\varepsilon(k)$ may be modeled by polynomial

$$\varepsilon(k) = a_0 + a_1 k + \ldots + a_M k^M = \sum_{i=0}^{M} a_i k^i \tag{25}$$

where coefficients a_i are unknown real constants. For example, the pulse transfer function of Newton's predictor, which estimates signal (25) with prediction horizon of p samples (i.e. $\hat{\varepsilon}(k+p)$) has the form

$$H_M^p(z^{-1}) = \sum_{i=0}^{M} (1 - z^{-p})^i . \tag{26}$$

This filter estimates sample $\hat{\varepsilon}(k+p)$ by M+1 preceding samples $\varepsilon(k)$. In the particular case of M = 1 and p = 1, filter (26) becomes identical to prediction polynomial (22). Generally, when an electrical drive is under consideration (control plant has minimal transport lag) it is always p = 1. Filtering properties of the different Newton's filters are illustrated in Fig. 4. Frequency characteristics of Fig. 4 show that noise components in the signal are increased when the order of the filter becomes greater. Therefore a linear approximation of signal (M = 1) may be adopted as an adequate, from the standpoint of noise sensitivity.

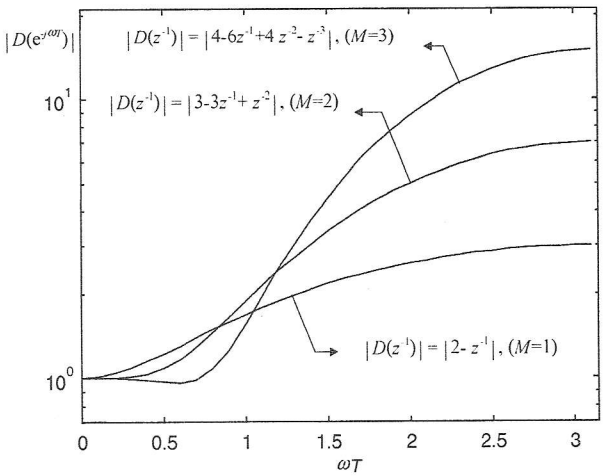

Fig. 4. Frequency characteristics of Newton's predictive filter for p = 1 and M = 1, 2 and 3

LSN (Linear Smoothed Newton) predictor [12], obtained by improving classical Newton's, passes *M*th difference of input signal through the low-pass digital filter $S(z^{-1})$. If the signal is adequately modeled by *n*th order polynomial, then the *M*th difference of signal is constant and the necessity of its filtering is evident. In a general case, LSN predictor is given by pulse transfer function

$$H_{M,LSN}^p(z^{-1}) = \sum_{i=0}^{M-1} (1 - z^{-p})^i + S(z^{-1})(1 - z^{-p})^M \tag{27}$$

For further simplification, the low-pass digital filter $S(z^{-1})$ may be adopted as a digital equivalent of the simplest low-pass analogue filter

$$S(z^{-1}) = \left.\frac{1}{T_f s + 1}\right|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}} = \frac{T(1+z^{-1})}{2T_f + T + (T - 2T_f)z^{-1}} \tag{28}$$

having only one tuning parameter T_f of a clear physical meaning. By increasing the value of T_f the better filtering

properties and higher system robustness are achieved, especially within the low frequency band. On the other hand, with greater T_f the speed of disturbance absorption is reduced and vice versa.

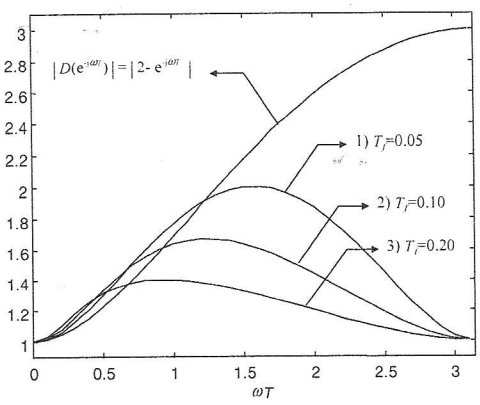

Fig. 5. Frequency characteristics of LSN predictor and prediction polynomial

For comparison, the frequency characteristics of the first order prediction polynomial and LSN predictor are illustrated in Fig. 5.

5. ILLUSTRATIVE EXAMPLE

The efficiency of LSN predictor with T_f = 0.2s, when compared with the application of prediction polynomial $D(z^{-1}) = 2 - z^{-1}$, in the case of IMPACT structure of positioning servomechanism is illustrated by Figs. 6 and 7. In the servomechanism, the 16-bits D/A converter and 12-bits R/D converter are applied. The results of simulation runs given in Fig. 6 (a) and (b) and Fig. 7 (a) and (b) are obtained by LSN predictor while the results in Fig. 6 (c) and (d) and Fig. 7 (c) and (d) are accomplished by the prediction polynomial. Notice that LSN filter suppresses the effects of quantization noise on the control variable and slightly slows down the speed of disturbance rejection. Sampling period T = 0.1s is assumed. The control plant is DC motor U12M4T having the electromagnetic gain factor K = 4.38 and mechanical time constant T_m = 0.32s. The desired close-loop system transfer function is specified by two conjugate complex poles with undamped natural frequency ω_n = 2.5 rad/s and relative damping coefficient $\zeta = 1$.

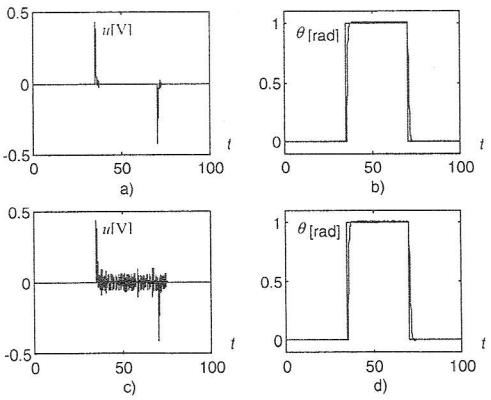

Fig. 6. Operation of IMPACT structure in the absence of torque disturbance

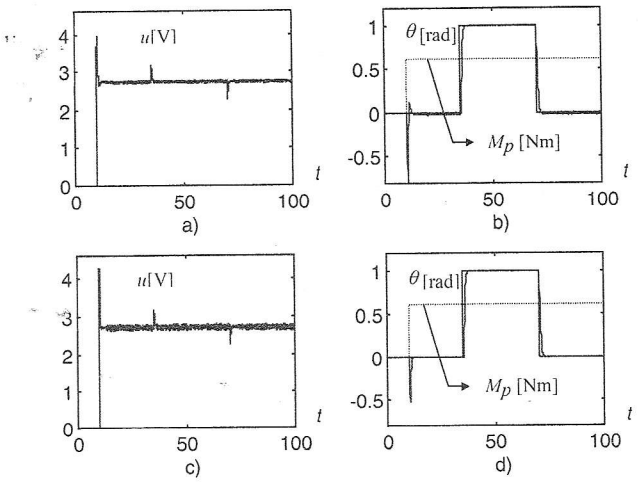

Fig. 7. Operation of IMPACT structure in the presence of torque disturbance

The efficiency of LSN predictor application as a prediction within the IMPACT structure of the speed-controlled electrical drive is illustrated in Figs. 8 and 9. The same DC motor U12M4T and T = 0.1s, as in the case of the positioning servomechanism, is applied. According to the proposed procedure, the desired closed-loop system transfer function

$$G_{dc}(z^{-1}) = \frac{0.312898z^{-1} - 0.259182z^{-2}}{1 - 1.687103z^{-1} + 0.740818z^{-2}} \qquad (29)$$

is specified and then the following polynomials of the control structure are calculated

$$z^{-1}P_u^o(z^{-1}) = 1.1765z^{-1},\ Q^o(z^{-1}) = 1 - 0.73146z^{-1},$$
$$R(z^{-1}) = 1.1765,\ P_y(z^{-1}) = -0.955642 + 0.740818z^{-1} \qquad (30)$$
and $P_r(z^{-1}) = 0.312898 - 0.259182z^{-1}$.

The system simulation is performed when 16-bits D/A and 12-bits R/D converters are applied (Fig. 8). The standard deviation of the difference between output signals generated with and without quantization noise, in the case of IMPACT structure with LSN predictor (Fig. 8), is 12% less than in the case of the observer based structure. By increasing time constant T_f, quantization noise is more suppressed but, at the same time, the speed of disturbance rejection is slowed down. Hence, the implementation of LSN predictor instead of prediction polynomial gave approximately the same results as in the case of observer implementation in IMPACT structure, but the structure with LSN predictor is significantly simpler. Furthermore, by tuning parameter T_f it is possible, in a simple way, to adjust system dynamic properties, suppression of quantization noise, and to improve robust stability of the system (Fig. 9).

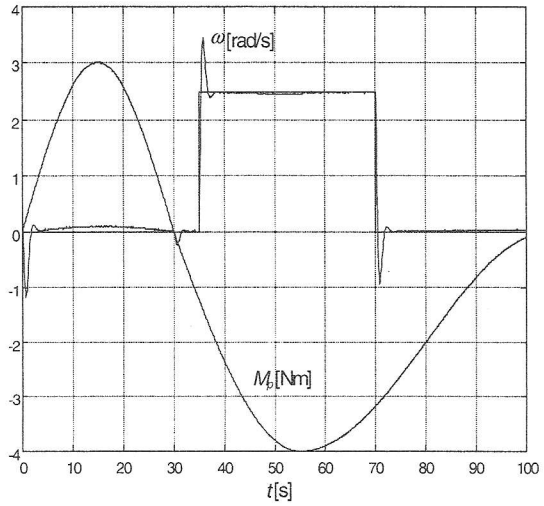

Fig. 8. Responses of IMPACT structure of speed-controlled servomechanism with LSN predictor (T_f = 0.2s)

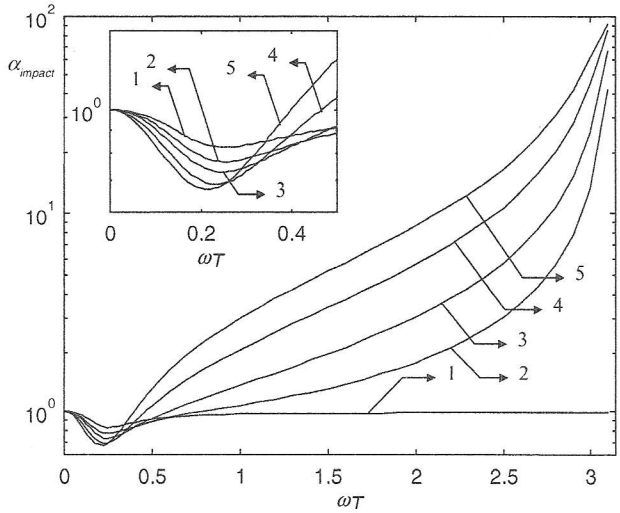

Fig. 9. Frequency characteristics of complementary sensitivity function of IMPACT structure with (1) prediction polynomial and (2) with LSN predictor having: (2) T_f = 0.05, (3) T_f = 0.1, (4) T_f = 0.2, and (5) T_f = 0.33.

6. CONCLUSION

The design procedure of IMPACT structure for digitally-controlled speed and position servomechanisms has been given. It was shown that the set-point response of the structure and speed of disturbance rejection could be adjusted independently. Instead of the design of disturbance estimator within the local loop of the structure, as in the case of basic IMPACT structure, different predictors are employed, for the purpose of disturbance extraction. This alternative approach has several advantages: the relatively easy setting of controller parameters, adjustable speed of disturbance rejection, and control of system robust stability.

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ON-LINE RESOLUTION SWITCHING OF THE RESOLVER TO DIGITAL CONVERTER WITHIN A POSITIONING SERVO DRIVE COMPRISING SIMULATED ENCODER

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Abstract: *The paper deals with the position and speed sensing in an environment of industrial servo drives equipped with resolver-type sensors. Problems of limited R/D converter resolution are outlined along with their influence on overall drive performance. Novice method for on-line R/D resolution change is proposed, and its software and hardware aspects are thoroughly examined. Primarily software based, proposed approach adapts the R/D resolution according to current shaft speed, so as to reduce the noise in feedback signals and optimize the drive performance. Experimentally verified, the method is proposed to potential users in the form of clear design guidelines..*

Keywords: *Resolver to digital converter, servo drive, simulated encoder*

1. INTRODUCTION:

Advanced servo drives with synchronous and induction motors demand high precision shaft sensors for the speed and the position measurement. Harsh industrial environment might include elevated temperatures, dust, oil vapors, noise and vibration that prevent the use of common optical transducers. When highly reliable operation in a severe environment is required, the shaft sensor commonly used is the robust electromagnetic resolver.

Resolver *sine* and *cosine* signals contain the information on the shaft position in an analog form. Ratiometric resolver to digital (R/D) converters are used for transforming the shaft position data in digital form, suitable for further processing. The resolution of conversion process might be preset from 10 to 16-bit with most of available R/D chips available on the market. High resolution gives the best precision of the position measurement and the lowest speed feedback ripple. Though, due to the finite topmost frequency of the VCOs and counters comprised within a R/D IC, the maximum shaft speed practicable in high resolution mode is limited. Hence, as the top speed of the drive increases, a lower R/D resolution must be preset, resulting in lower overall drive performance.

The drive performance might be significantly increased with variable resolution scheme, allowing the R/D converter's resolution to be adapted to the current shaft speed. In this paper, the method and application of novice, software implemented R/D resolution switching is proposed. Basic analytical consideration and design guidelines are accompanied with experimental results, illustrating clearly visible improvement of overall drive performance.

2. R/D CONVERTER OPERATION WITH FIXED RESOLUTION:

Resolver-to-digital converters obtain the digital word related to the shaft position from analog signals coming from the *SINE* and *COSINE* detection windings of the resolver. Conversion process is ratiometric [1], and involves closed loop position tracking. Assumed position is present in an UP/DOWN counter (Fig.1) in the form of a digital word with 10, 12 14 or 16 bits. Resolver is normally excited by a low power, high frequency signal [2], having the frequency at least an order of magnitude higher than required bandwidth of the R/D tracking loop. Resistive network in Fig. 1 switches in and out internal resistors according to the status of corresponding counter bits. At its analog input, resistive net is connected to the *sine* and the *cosine* signals, obtained from the resolver detection windings. The net is arranged in such a way that an AC-error signal appears at the output. The error signal is proportional to the difference between the actual shaft position and the estimation contained as a word within the counter.

High (excitation) frequency AC error is filtered demodulated, and processed through a PI (proportional - integral gain) block. Amplified error is used as the driving signal for a Bi-directional Voltage Controlled Oscillator; the BVCO generates the pulses at the "UP" output for positive values of VCO_IN signal (see Fig. 1); or, alternatively at the "DOWN" output in the cases whence the VCO_IN has a negative value. In both cases, the pulse frequency varies with the absolute value of the input signal. The BVCO is mostly [1] implemented as current controlled device.

The tracking loop is closed by feeding the BVCO output signals to the counter, providing for corrective action that forces the digital position estimate to track the actual shaft position. "UP" and "DOWN" pulses from the BVCO will increment or decrement the counter attempting to zero the error. The frequency of BVCO output is proportional to the rate of change of the shaft position, and hence, proportional to the shaft speed. The same way, the input to BVCO may be used as an analog representation of the shaft speed; the "tacho" signal.

Most of resolver-to-digital converters available [1] comprise a BVCO with the maximum pulse frequency below f_{max} = 1 MHz. Hence, the R/D converter will not be able to track the shaft position at a speed higher than ω_{max}[rps] = f_{max} [Hz] / 2^N; where N stands for the counter length in bits, and the ω_{max} designates the top speed in revolutions per second, assuming that resolver has one pair of poles. Generally, the top mechanical speed is obtained by dividing the value ω_{max} by the number of resolver pole pairs. The counter lenght N determines the resolution of the R/D converter, and might assume values of 10, 12, 14 or 16.

The best precision of the position measurement is obtained having N=16. In this case, full counter lenght is used (from b15=MSB to b0=LSB), the BVCO pulses affect the bits starting with b0, and the top speed ω_{max} is very small (example: with N=16, f_{max} = 1 Mhz and a 6-pole resolver, n_{max} = 305 [rpm]). In order to achieve higher speed, the R/D resolution has to be decreased to 14, 12 or 10, depending on the application requirements. For N=10, the resolution is at

the minimum and the top shaft speed is n_{max}= 19531 [rpm] for 6-pole resolvers, and 58593 [rpm] for 2-pole devices. The BVCO clocking pulses do not affect six least significant bits within the 16-bit counter (b5-b0). The effect of one pulse is addition/subtraction of one (1) to/from a 10-bit digital word consisting of the bits b15..b6.

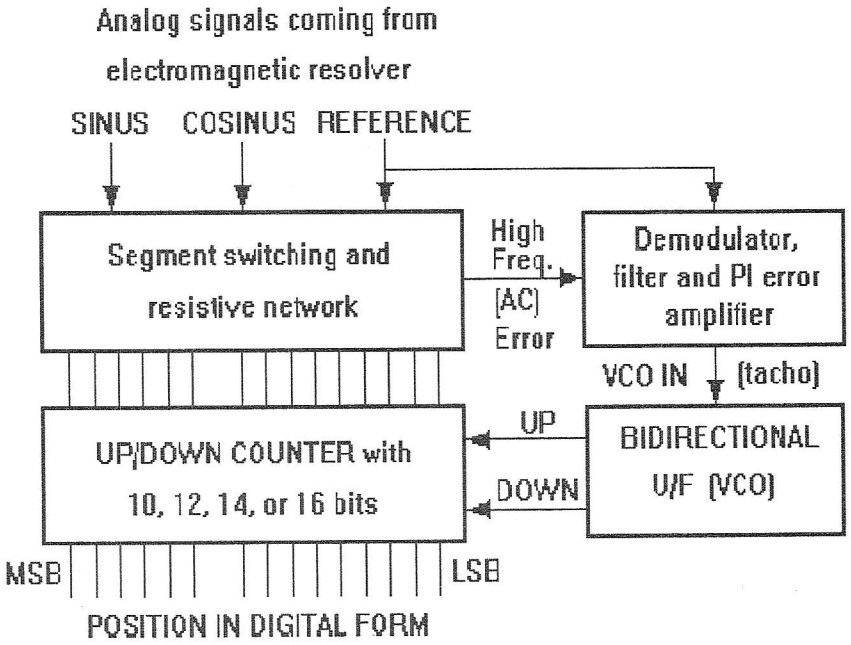

Fig. 1: Basic operation of the R/D converter with fixed resolution

Accuracy and response speed of the tracking loop depends upon the excitation frequency, resistive net accuracy, the PI error gains and the counter lenght (10 - 16 bits). Generally, tracking loop bandwidth of the order of one tenth the excitation frequency may easily be achieved. The counter length *N* is preset by the user; two dedicated pins of the R/D chip has to be connected to logical 0 or pulled up to logical 1. Four possible combination will set *N* to 10,12, 14 or 16. Along the drive operation, the resolution remains fixed.

The resolution of position measurement is directly determined by the counter length. Hence, it varies from $2^{-10} * 2\pi$ to $2^{-16} * 2\pi$. The speed signal is most frequently obtained from the position information by means of a speed observer. Due to the fact that the speed observers intrinsically bring in the differentiation and filtering of the position signal, the speed feedback noise will increase as the R/D resolution decreases. Consequently, lower R/D resolution will limit the speed loop bandwidth, since the gains of the loop must be reduced due to the noise contained in the feedback signal.

Plenty of servo drive applications require both high precision at a low speed and the possibility to reach very high speed with lower precision. Machine tools application frequently calls for a high speed, rough cutting mode; followed by final low speed, high precision cutting. Spindle drives with automatic tool exchange call for extremely high top speeds at which the precision is not essential, but need as well high precision position measurement in the tool exchange mode. If the resolver with the R/D converter is used as the shaft sensor, the overall drive performances will be bonded by the necessity to choose and keep fixed one resolution of the R/D converter. When the top drive speed is high, so has to be the value of ω_{max}, and the user must select a low R/D resolution. Consequently, low speed performances will worsen; the speed loop bandwidth, suppression of the torque disturbances and the precision of the positioning will be inferior with respect to the case of a higher *N;* that would have been applied if the high speed requirement were not imposed.

The method and the means for a software based on-line resolution adaptation are analyzed and proposed in this paper, with the aim to achieve better utilization of the resolver and the R/D converter; and allow simultaneously high precision low speed operation as well as high operational speeds with decreased accuracy of the position measurement. The method with both hardware and software aspects of proposed on-line resolution switching has been thoroughly tested and build into the digital multiaxes servoamplifier [3], showing excellent results field test results.

3. ON-LINE RESOLUTION SWITCHING: HARD-WARE ASPECTS

Drawbacks of the fixed resolution operation of R/D converter might be eliminated by selecting the resolution *N* lower at high shaft speeds, while switching to 14- or 16-bit resolution in low-speed high-precision mode of operation. The pins of the R/D (named SC1 and SC2 in the case of 2S82 part [1]) provided for hardware selection of R/D resolution might be software controlled, in which case their status, and hence, the R/D resolution might be changed on-line, during the drive operation.

On-line change of the R/D resolution basically means the change of the counter length; that is, a 10 => 12 resolution switching changes the counter format from [b15 ... b6] - 10 bit word, to 12 bit [b15...b4] word. Due to the fact that the shaft speed does not change significantly during the switching interval, and taking into account that the BVCO frequency is given f_{BVCO} [Hz] = 2^N ω[rps], the 10 => 12 resolution change must be followed by an increase of f_{BVCO} by four. The same way, reciprocal 12 => 10 resolution switching must be followed by a drop in the BVCO frequency by four.

The output frequency of the BVCO is controlled by the voltage level at the oscillators input (VCO IN signal in Fig. 1). This signal, in turn, is the output of an analog PI regulator, having the tracking error at the input. The VCO IN signal cannot change instantly, due to an inherently limited slope and response time of the PI block. Hence, inability to augment and diminish the VCO IN four times at the instant of the resolution switching will make impossible sudden changes in BVCO frequency. Therefore, a large tracking error will occur at the instant of SC1:SC2 switching, followed by the transient response of the tracking loop. In an environment of a servo drive with the speed loop, transient phenomena caused by the resolution change will provoke large torque spikes, speed errors, and the position error that is not acceptable. Severity of the problem might be observed better if the magnitude of the R/D internal speed error is considered: at each resolution change, the internal speed error is initially 400% - 100% = 300%.

It might be concluded from the above discussion that a means of step-changing the BVCO frequency by 4 must be found in order to obtain error-free, smooth resolution switching process; avoiding in such a way the interference with the speed and position loops. Solution to the problem is proposed hereafter, and applied on a 2S82 [1] R/D converter. Hardware details are given in Fig. 2.

The output of the PI block in Fig. 1 (the VCO IN signal) is labeled as the INTEGOP pin of 2S82 in Fig. 2. The BVCO within the 2S82 R/D converter is a current controlled device; that is, the frequency of the clock pulses varies with the current supplied into the VCOIP input pin. Under assumption that the INTEGOP output is at a constant value, the BVCO pulse frequency is determined by the resistance connected between the INTEGOP and the VCOIP pin. Step change in the BVCO frequency might be obtained by changing this resistance four times at the instants of the resolution change. For this purpose, resistors R_{sw1}, R_{sw2}, R_{sw3}, and R_{sw4} are introduced in Fig. 2, along with associated analog switches SW2, SW3, and SW4.

Analog switches SW2, SW3, and SW4 should be set ON and OFF in function of the current resolution of the R/D converter. To avoid transient response of the tracking loop and reduce the risk of a large tracking error, equivalent resistance should always change by the factor of 4. For 10-bit resolution, all the analog switches should be OFF, and the value of equivalent resistance between INTEGOP and VCOIP pins is $R_e = R_{sw1}$. Passing to 12-bit resolution, the switch SW2 must close at the same instant when the code signals SC1 and SC2 change to 12-bit status. Since R_e in this state must be exactly 1/4 of the previous R_{sw1}, the value of R_{sw2} might be found as R_{sw2} = 1/3 R_{sw1}. In such a way, equivalent resistance for the 12-bit resolution will be 1/4 R_{sw1}. Increasing further the resolution and passing from 12-bit to 14-bit resolution, the switch SW2 remains closed, while SW3 closes in exactly at the instant of the commutation on SC1-SC2 pins. In order to get R_e = 1/16 R_{sw1}, the value of R_{sw3} must be exactly 1/12 R_{sw1}. Going further to 16-bit, the analog switch SW4 must be turned on, and both SC1 and SC2 control signals must be driven to the logic 1 level at the same time. Since the equivalent resolution in such case must be 1/64 R_{sw1}, the value of R_{sw4} is calculated as 1/48 R_{sw1}.

The resolution change basically modifies the format of the UP/DOWN counter. Hence, the effect of one BVCO pulse expressed in terms of estimated position in [rad] changes from $2\pi/2^{10}$ for 10-bit resolution to $2\pi/2^{16}$ that we have for 16-bit resolution. Potentially, this might change the closed loop gain of the R/D tracking loop 64 times, and significantly affect the position measurement accuracy and dynamics. The tracking loop gain variation is avoided by inserting R_{sw1}..R_{sw4} and commutating the analog switches in the prescribed way. Along with the resolution change imposed by SC1-SC2 signals, the value of equivalent resistance between the INTEGOP and VCOIP pins is changed four times; causing the same INTEGOP level to provoke four times higher/lower BVCO frequency. In such a way, considering the signal flow from the INTEGOP pin to the counter, whatever the resolution the same level at the INTEGOP pin will produce always the same rate of change of the estimated position expressed in [rad/s]. Example: one BVCO pulse affects the estimated position 4 times less at 12-bit resolution that the same pulse when the resolution is 10-bit; but the INTEGOP - VCOIP equivalent resistance is 4 times smaller at 12 bit resolution, and the same INTEGOP voltage level makes BVCO count 4 times faster. As the consequence, the bandwidth and dynamics of the tracking loop does not change with the R/D resolution, the loop performs always in the same way.

At hardware design stage, care must be taken to the internal timing of the R/D device. Namely, after each BVCO clocking pulse, the data contained in the counter change, and the transition state may last 300-400 ns. During this interval, the counter outputs invalid data that should not be used. For this reason and due to internal R/D timing problems, the resolution must not be changed during the transition interval. Rather than that, the command for the resolution switching should be issued during the time interval when the counter data is stable. Even at the top (1MHz) BVCO frequency, there are 600-700 ns left to perform the resolution change.

The R/D converter marks the transition intervals by establishing high level at the BUSY pin (Fig. 2). In order to ensure that the R/D resolution changes are performed at the beginning of a "data stable" interval, flip-flops FF1 and FF2 are used. At their D inputs, the digital microcontroller outputs the code for SC1 and SC2 lines. The new status of SC1 and SC2 will determine the R/D resolution, as soon as FF1 and FF2 latch the data. For that to happen, the digital microcontroller must confirm the request by setting high the LOAD_NEW_SC line. Now, next falling edge of BUSY signal will provoke a rising edge at the FF's clock input, and new values for SC1 and SC2 will appear at Q outputs. These outputs will consequently set the status of SC1 and SC2 pins of the R/D, and determine the state of SW2, SW3, and SW4

analog switches. In the prescribed way, the resolution change will begin when the transition period ends, and adverse effects of switching during the transition will be avoided.

With the hardware prerequisites outlined above, the R/D tracking loop will suffer no error due to on-line resolution change, providing that components used in Fig. 2 are ideal ones. Some parasitic effects though, might provoke a small tracking error to occur at the switching instant, and these are listed in section 5. The next section deals with the software aspects of the resolution switching, and explains when and how the SC1, SC2 and LOAD_NEW_SC commands should be issued.

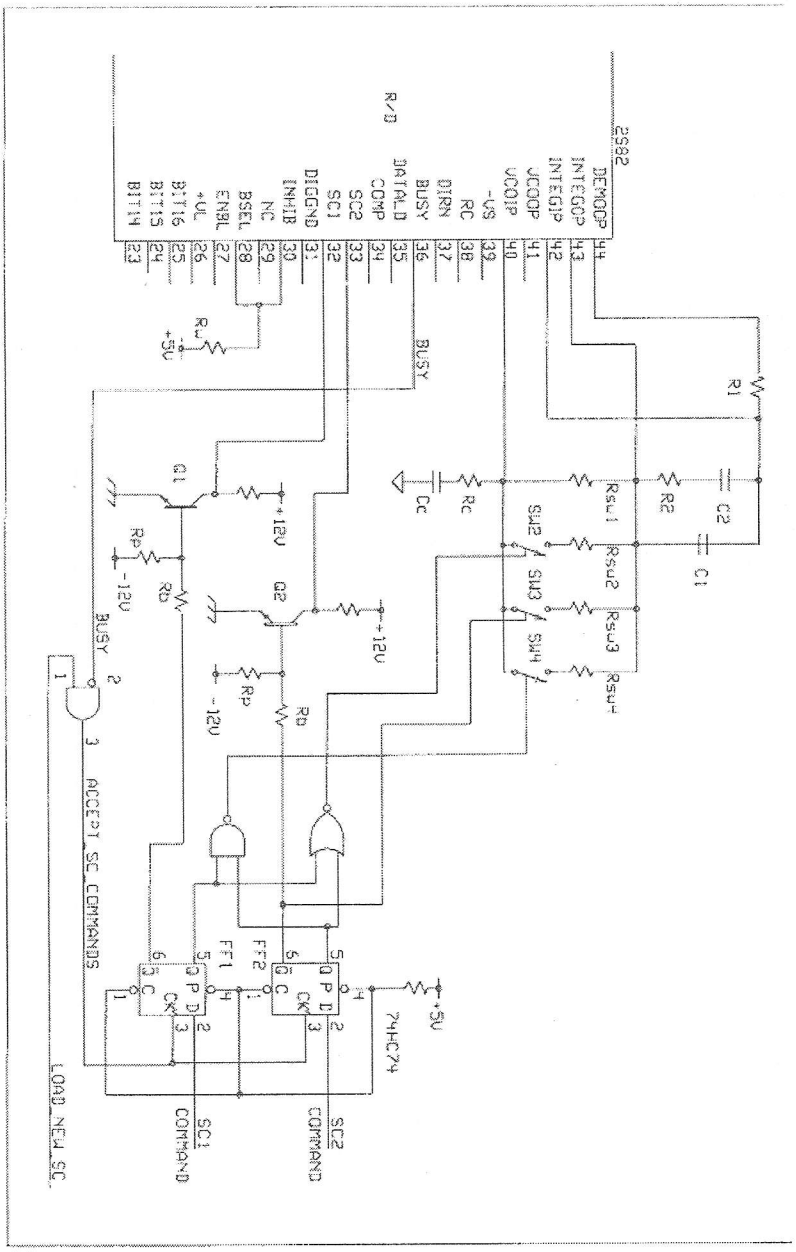

Figure 2. On-line R/D resolution switching: Hardware modification

4. SOFTWARE IMPLEMENTATION

The basic requirements with respect to the counter length N (that is, the resolution in terms of the number of bits) are to use the maximum possible resolution, while taking care not to exceed the BVCO maximum frequency. Basic rules might be inferred from the relation that connects the shaft speed and the BVCO frequency: $\omega_{max}[\text{rps}] = f_{max}$ [Hz] / 2^N. When the shaft speed is in a decline, the BVOC frequency will reduce as well. For values $f_{BVCO} < 0.25\ f_{max}$, the resolution might be increased. Setting the next higher resolution in such a situation, the BVCO frequency will increase by a factor of 4. Since the previous value was $f_{BVCO} < 0.25\ f_{max}$, the change will not pass over the BVCO top frequency, and the integrity of the position measuring system will be preserved.

During the acceleration phase of the drive, the shaft speed will increase along with the BVCO pulse frequency. When coming close to the top BVCO frequency, the R/D resolution must be decreased to the next lower value, in order

to allow for further shaft speed rise. The resolution drop will divide the f_{BVCO} by 4, making continued acceleration possible.

Decision on when and how to change the R/D resolution is made by the digital controller. Thresholds might be determined in terms of the shaft speed, or alternatively judged from the BVCO frequency. If the shaft speed were to determine the switching, a set of 6 thresholds would be necessary. For 12- and 14- bits both the upper and the lower limit would be necessary, while the minimum 10-bit and the maximum 16-bit resolutions will need only one threshold: lower (10-bit) and upper (16-bit).

Deriving the switching instants from the frequency of the BVCO pulses is natural choice, and much simpler to implement. It is sufficient to count the BVCO pulses, measuring in such a way the frequency. Only two limits have to be established: the minimum frequency (below which the resolution will be increased) and the maximum frequency (above which the resolution should be decreased).

The action of the digital controller consist in keeping the LOAD_NEW_SC signal in a passive state until the moment when the resolution change is required. At the instant of change, the lines SC1_COMMAND and SC2_COMMAND must be set first. Following that action, the LOAD signal should go into its active state, and remain active until at least on BUSY period passes; making sure in such a way that the flip flips latch the data.

5. PARASITIC PHENOMENA AND REMEDIES

Previous discussion assumed a linear relation between the BVCO input current and its output frequency. This linearity is essential for the proper operation of the proposed method. Namely, since each resolution change calls for a BVCO frequency change by a factor of 4, we designed the hardware in such a way that the change of the BVCO input current is ensured to be correct (that is, the BVCO input current will also change by a factor of 4). Now, if the BVCO input/output characteristics is linear, its output frequency will perform accordingly. Any error in the BVCO linearity will cause the pulse frequency to change at the instant of resolution switching by a factor higher or lower that 4. As a consequence, as explained above, the switching cause the tracking error and the transient response of the tracking loop. In order to avoid this problem, the switching thresholds (in terms of the BVCO pulse frequency) should be chosen in such a way that the corresponding points on the BVCO_IN / BVCO_OUT characteristics have the same ratio between the BVCO input current and the corresponding BVCO output frequency.

Special care should be taken in selecting the bipolar transistors Q1 and Q2 in Fig. 2, used for level-shifting the TTL signals up to the 12 V logic level; as well as their polarization resistors R_p, and R_b. Namely, the turn-on delay must be longer or equal to their turn-off delay; and that might be obtained by choosing the pull-up resistors, R_b and R_p. Having the turn-on delay longer, any transition on SC1 and SC2 pins of the R/D such as 10 => 01 will pass through the 11 state. Notice that the same transition will pass through the 00 state, providing that the turn-on is faster than turn-off. Due to the internal logic of the 2S82 R/D converter, it is essential to avoid passing through the 00 state. More specifically, 10 => 01 and 01 => 10 transitions correspond to the resolution change from 12 to 14 and vice versa. If transition passes shortly through the 00 state (that corresponds to the 10-bit resolution), the R/D converter will reset those counter bits that are not being used by the 10-bit resolution configuration. There are two bits that are being used by the 12- and 14-bit resolution, and not being used by 10-bit resolution. Hence, a short 00 interval will reset these bits and damage the data in the counter. In turn, the tracking loop will exhibit a transient response, attempting to correct the error. Having $\tau_{TURN\text{-}ON} < \tau_{TURN\_OFF}$ will completely eliminate the risk of generating the tracking error.

6. CONCLUSION

The paper proposes a software-based, simple to implement method of increasing the resolution of position feedback signal in an environment of the servo drive with electromagnetic resolver and the resolver-to-digital converter. The method requires minor hardware modifications that do not involve expensive parts and do not increase the hardware cost. Experimental verification shows and increase of the speed loop performance parameters by roughly 25%. The method is build into the series-produced DBM03 line of digital multiaxes servoamplifiers where it showed an excellent performance.

7. LITERATURE

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METHODS OF POWER DISTRIBUTION NETWORK HARMONICS REDUCTION

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Abstract: *Harmonics in distribution network present a serious threat to linear loads and especially to microprocessor-based ones, which are sensitive to voltage waveform distortion. In the paper, the methods for harmonics level reduction using standard solutions and the new ones are overviewed. The modern trend is application of more and more active electronics components, which leads to cost decrease and improvement of power conditioning devices characteristics.*

Keywords: *Harmonics, Distribution Network, and Filtering*

1. INTRODUCTION

Digital electronics devices, microprocessor based systems, PC computers, main frame computers, PLC controllers, process equipment in industry and other devices manufactured as a result of rapid development and spreading of microprocessors and digital electronics, have very strict demands toward power quality. Existing power supply systems and particularly power distribution network have been developed at a time when those loads had not existed and when certain deviation from nominal values could be much more easily tolerated, i.e. is a time when loads where designed to be immune to large number of disturbances. The result of this contrast is increase of complains on poor power supply over last decade and even court accusation and trials due to lost production and poor product quality. That is the reason why engineers in power supply companies turned with a great care to power quality issues - power quality of power supply as well as to power quality of supplied power. One of the most important power quality parameters is harmonics [1].

Higher or lower percentage of harmonics is constantly present in network voltage or current wave-shapes. However, in certain moment they may become a problem. It happens if harmonic source is too strong or if harmonic path is too long or if system response leads to harmonics amplification (resonance). To reduce harmonics several possible solution are known:

1. Reduction of harmonic currents effects – by conncting transformer windings in Δ/Y, increasing the rectifier's pulse number e.t.c.
2. Network reconfiguration – by increasing short circuit power (S_{sc}), separate supply line, connection at higher voltage level e.t.c.
3. Compensation unit reconstruction – changing the system resonant frequency,
4. Application of passive harmonic filters
5. Application of active harmonic filters

Apart from these methods, new solutions based on active electronic components are proposed in recent references. These solutions become attractive as costs of electronics devices have constant decreasing trend.

The paper presents an overview of certain number of methods for harmonics reduction, which are applicable primarily to large loads, industrial drives and similar.

2. REDUCTION OF HARMONIC CURRENTS EFFECTS

Reduction of harmonic currents usually means changing the working procedures of operation of the harmonic generated drives. Such approach is difficult to realize, as it can influence the whole production process, i.e. it possible only in the designing stage. However, some effects can be achieved by interventions in the circuit of non-linear load and rectifier transformer [2].

The simplest solution is changing of rectifier transformer windings connection. Connection of primary winding into delta, blocks of all harmonics multiple of 3, so the lowest dominant harmonics became the 5^{th} and the 7^{th}. But, it leads to increase of transformer losses, which should be taken into account during transformer design. Today, all rectifier transformers are Δ/Y connected.

Increasing the number of pulses of AC/DC converters, which are used in the controlled DC drives, the dominant harmonics can be moved toward higher orders. The effect of 12-pulse rectifier, where dominant harmonics are the 11^{th} and the 13^{th}, and where characteristic harmonics of the 6-pulse rectifier are eliminated (the 5^{th} and the 7^{th}), is obtained by connecting two 6-pulse AC/DC converters and additional transformer secondary winding. If one secondary winding connected into star supply the first 6-pulse rectifier and if the second secondary winding is connected into delta, supply the second 6-pulse rectifier, their series connection leads to the 12-pulse rectifier effect. Such AC/DC converter type is convenient for industrial drives, as it is much easier to realize than filter equipment installation. It is especially suitable for rectifier/inverter installation in high voltage DC (HVDC) power transmission. Fig. 1 represents input current waveform and its spectrum, where result of shifting dominant harmonics can be seen. However, voltage waveform, shown in Fig.2, has more commutation dips, which can influence the operation of control circuits.

3. NETWORK RECONFIGURATION

Non-linear load coupling to the higher power grid also reduces harmonics. Such grids have lower internal impedance, so voltage drop due to harmonics is lower. A connection to the higher voltage level or to the separate medium voltage line is also applicable.

These solutions are necessary for electric drives, which are known as large non-linear loads and sources of harmonics or other disturbances.

The well-known case is installation of the electric arc furnaces, which is supplied either from the separate medium voltage transformer grid (for example 35/10kV), or directly

from high voltage (110 kV). A detailed analysis is needed if one of these solutions is planned. Especially important factor is the rate between short circuit power of connection grid S_{ks} and short circuit power of furnace transformer S_T. If this rate is high enough, the negative effects are smaller and present no threat to the network and other loads. It is considered that in case of middle power furnaces (5-30MVA), such rate should be $S_{ks}/S_T > 60\text{-}100$. In other case, negative effects can be expected (flicker). If $S_{ks}/S_T < 30$ the flicker becomes intolerable, as well as harmonics [3].

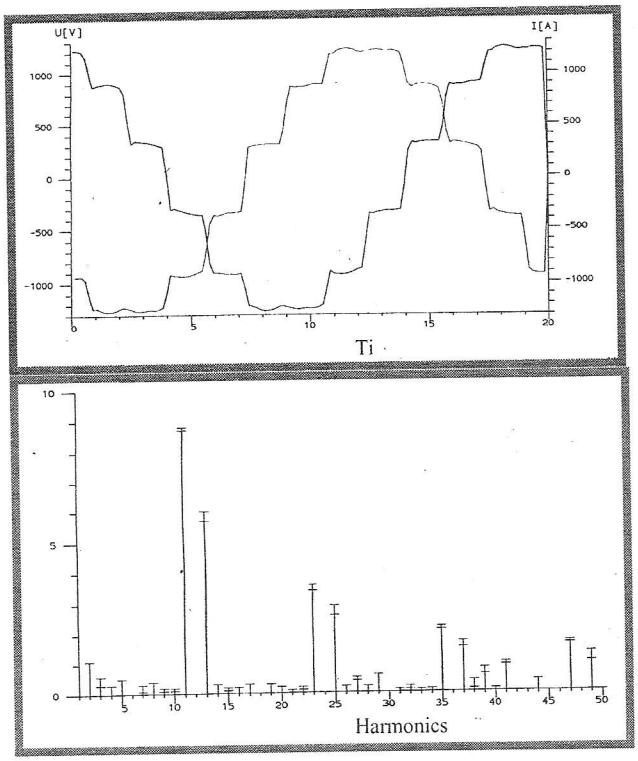

Fig. 1 – Network current of 12-pulse rectifier – phases L1 & L2 (up) and its spectrum (down).

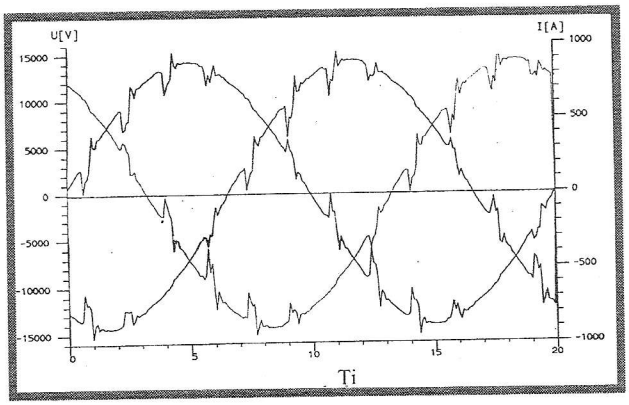

Fig. 2 – Voltage waveforms of 12-pulse rectifier.

Example 1: Foundry of »Cer« factory in Čačak is supplied from medium voltage transformer 35/10 kV, which is connected to the public network with separate cable. One electric-arc furnace of 1.5 t is situated in foundry, and it is over a furnace transformer 10/0.18 kV, S_T=1.2 MVA connected to the previously mentioned transformer. Measurement of current harmonics have shown extremely high harmonics levels at furnace transformer primary winding. Fig. 3 shows measurement results of current harmonics of phase »S« [4]. It can be seen that harmonics are above IEEE-519 limits for such a load class. However, simultaneous measurement of voltage harmonics at 10 kV PCC, have shown that there is no significant distortion. Fig. 4 presents measurement results of voltage harmonics. It can be seen that all harmonics values are below 2%, which is 4 times lower than maximum allowed value. Therefore, the medium voltage transformer is well designed, with short circuit power high enough, i.e. low enough internal impedance, so that high harmonic currents do not provoke significant voltage harmonics.

Example 2: Factory of cardboard wrapping »Lepenka« in Novi Kneževac has long continuous production line (about 120 m) for cardboard production, a special paper material used for cardboard boxes in transport wrapping. The production line is driven by several controlled electric drives, which generates significant current distortion into network. The 5th and other harmonic levels are significant, so that total harmonic distortion exceeds defined limits (Fig. 5) [5]. The designers of the plant, having known such problems, have connected the supply of the drive to 20 kV grid at medium voltage substation 110/20 kV. In that way they ensured that other loads are supplied from different grid and by way that protected from harmonics. Fig. 6 shows measurement results of voltage harmonics at the same grid. It can be seen that all THDU values are below 3%, which is 2.5 times lower than maximum allowed value (8%).

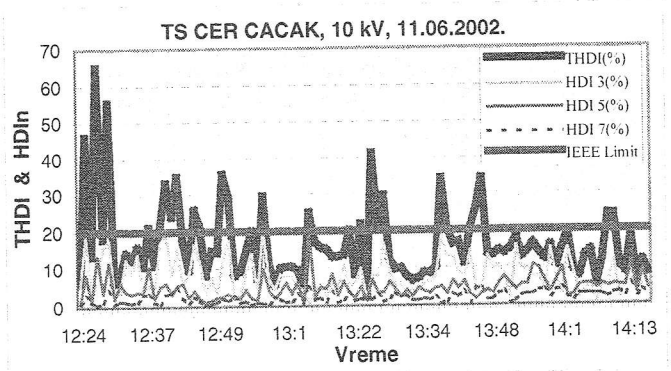

Fig. 3 – Current harmonics of electric-arc furnace - measurement results.

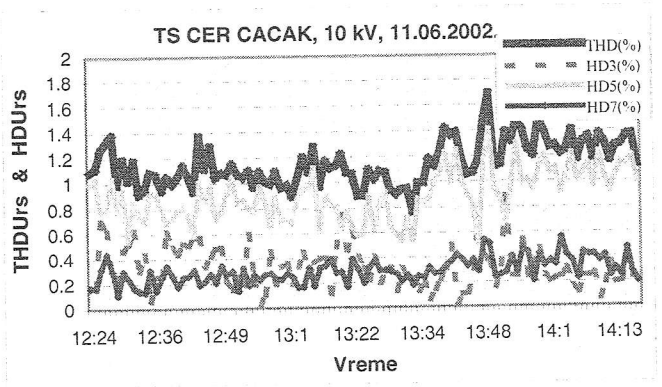

Fig. 4 – Voltage harmonics of electric-arc furnace - measurement results.

4. COMPENSATION UNIT RECONSTRUCTION

Change of resonant frequency of the network is necessary when in system or at load side exists a compensation units for reactive power compensation. The resonant frequency of network is often near frequency of characteristic harmonics, so negative effects can appear. Changing the size of capacitor banks, adding series impedance, connecting capacitors at another grid or simply abandon capacitors (but paying the price of reactive energy) are possible solutions to the problem.

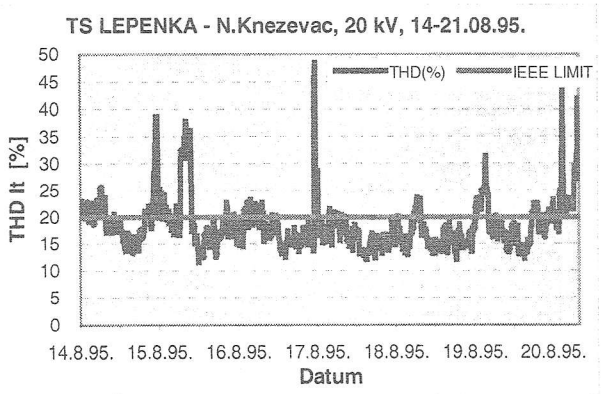

Fig. 5 – Complex electric drives THD current harmonics measurement results.

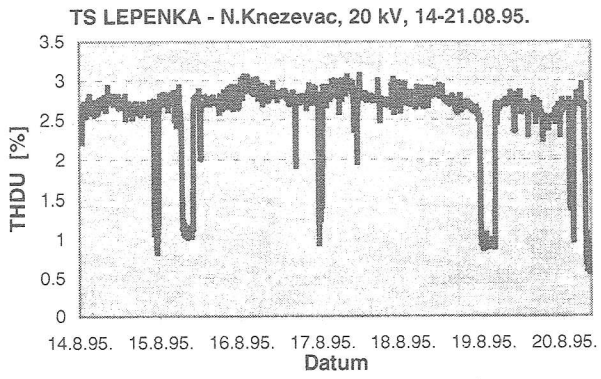

Fig. 6 – Complex electric drives THD voltage harmonics measurement results.

Example 3: In a mill there are two large AC/DC converter units – a 12-pulse (5184 kVA) and a 6-pulse (3700 kVA), several other loads and capacitor bank (3000 kVAr) connected at the same grid [6]. Several problems are notified in internal power network:

1) blowing the fuses of capacitor bank and damages of capacitor's frame
2) frequent motor failure
3) low accuracy of measurement instruments
4) communication problems (telecommand signals)

e.t.c.

Harmonic measurement has been performed at high-voltage side of 6-pulse rectifier transformer and at capacitor bank connection to investigate above problems. High values of the 7th harmonics of voltage have been recorded at transformer site - HDU_7=40%, THDU=107.7%, while high value of the 7th harmonic of current during capacitor site measurement - HDI_7=135%, THDI=170.7%. This provokes increase of capacitor current up to 36% of nominal. The engineers concluded that resonance conditions exists with capacitor bank and that resonant frequency is near the 7th harmonics. A temporary solution is found in decreasing the number of capacitors in the bank in order to shift resonance frequency away of 7th harmonic. The solution proved to be successful as the value of the current 7th harmonic decrease to HDI_7=15.5%, total harmonic distortion to THDI=114%, but on the other hand, the 9th harmonic increase from HDI_9=0.9% to HDI_9=19.6%, while the 11th increase from HDI_{11}=13.8% to HDI_{11}=45.4%.

Example 4: In tires factory "Tigar" from Pirot a production line is driven by large DC drive. During operation a failure at capacitor bank reactive power generation unit occurred. The failure was so heavy that the burning fire emerged, damaging not only the capacitors but several grids of transformer station TS "Tigar 1" too. Harmonics measurement were performed afterwards, with compensation unit disconnected. The results are presented in Fig. 7. A high value of the 5th and the 7th harmonics can be observed. So it is justified to assume that the cause of the failure was resonance of capacitor bank and DC drive harmonics. Based on measurement results, the engineers in the "Tigar" factory have built the filter-compensation unit. This solution is still in test stage and positive effects are to be reported.

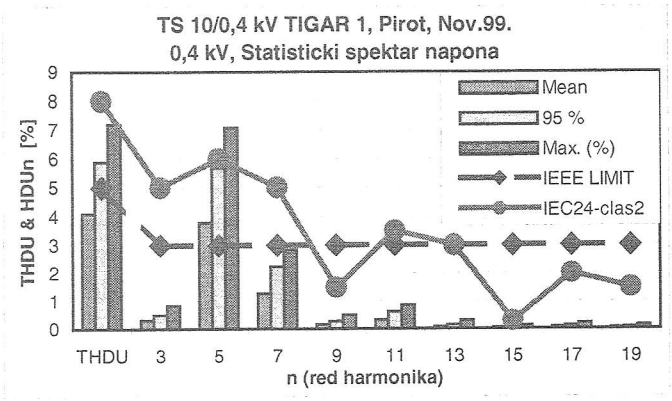

Fig. 7 – Statistical voltage spectrum at PCC of industrial transformer substation at "Tigar", Pirot industrial plant.

5. HARMONIC FILTERS

Nonlinear loads generate distorted current wave shapes, which can provoke significant negative effects on network and other loads. Therefore it is necessary to eliminate or diminish distortion level. Filters present the units where clensing of voltage and current wave shapes take place. The aim of filter application is to establish low impedance path for current harmonics and therefore prevent their spreading into network.

For that reason, filters are usually connected in parallel to the load - parallel filters. They consist of a capacitor with added inductance. The resonant frequency of the filter is always designed to be somewhat lower than the frequency of the lowest dominant harmonic. In such a way, it is provided that the filter operates correctly even in cases of oscillation of capacitor parameters due to temperature changes.

Another possibility is that filters are connected in series to the load - series filter. The aim is that they represent high impedance for harmonic currents and in that way block their flow into the network. A problem is that the filter components must withstand the full load current, including harmonics, which makes filter costly and of large size. In telecommunication application such problem is not so significant, as low power signals are in concern. In distribution network, economy concern is important, so application of series filters is rare.

Above-mentioned filters are called passive, while the new realization are called active. Active filters are in fact power electronic converters, which are designed in such a way to compensate harmonics. These filters enable "clean" sinusoidal current and unity power factor [7]. More complex configurations enable prevention of all power quality disturbances – Universal Power Quality Conditioning Systems [8].

In the paper only fundamentals of filters will be presented, as more detailed texts are already available – about passive filters in [9,10], and about active filters in [7,8,11].

5.1 Passive filters

Passive filters can be series or parallel. They consist of passive components, which are carefully selected to fulfill above-mentioned goals. As stated above, the series filters are rarely applied, as they have to carry full load current. Parallel filters are designed in different complexity depending to desired level of filtration:

1. single-tuned filters
2. double-tuned filters
3. damped filters

5.1.1 Single-tuned filters

Single-tuned filter is the simplest filter, which is used to eliminate single dominant harmonic (most frequently the 5th or the 7th). It consists of series connection of C, L and R (Fig. 8.a). Filter component are calculated in such a way that filter has sharp frequency characteristics concerning resonance frequency, i.e. maximum cutting of undesired harmonic order. The measure of filter quality is called Q factor. It is defined as rate of reactive to active component:

$$Q=\frac{X_0}{R} \quad , \quad X_0=\omega_n L=\frac{1}{\omega_n C}=\sqrt{\frac{L}{C}} \quad , \quad \omega_n=\frac{1}{\sqrt{LC}} \qquad (1)$$

where ω_n is resonant frequency of the filter and *R, L & C* are passive filter components from Fig.8.a. Quality factor is usually between 50 and 150.

The deviation of frequency from resonant one is defined as:

$$\delta=\frac{\omega-\omega_n}{\omega_n} \qquad (2)$$

Now, relations for filter components are:

$$C=\frac{1}{\omega_n X_0}=\frac{1}{\omega_n RQ} \quad , \quad L=\frac{X_0}{\omega_n}=\frac{RQ}{\omega_n} \qquad (3)$$

and equivalent impedance of filter is:

$$Z_f=R\cdot\left(1+jQ\delta\frac{2+\delta}{1+\delta}\right)\approx R\cdot(1+j2Q\delta) \qquad (4)$$

Fig.9 represent the frequency characteristic in case of filter application for eliminating the 5th harmonic (f_g=250Hz, R=4.2 Ω, C=1.96μF, L=210 mH).

5.1.2 Double-tuned filters

Three-phase bridge rectifier (6 pulse) generates harmonics in pairs (n=kp±1, k=1,2,..., p=6), so it is necessary to connect two single-tuned filter to eliminate the 5th and the 7th harmonics. However, more convenient solution can be application of the double-tuned filter.

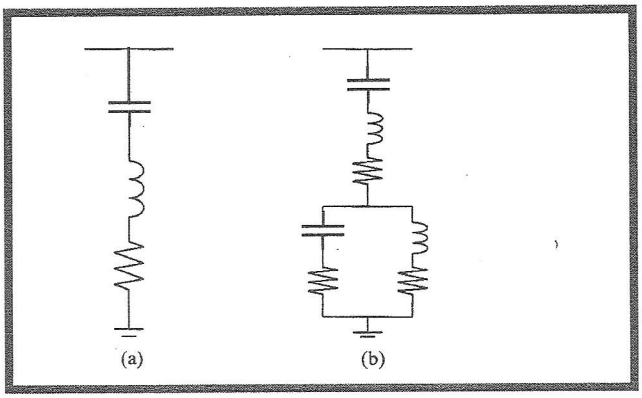

Fig. 8 – Single-tuned (a) and double-tuned (b) harmonic filters.

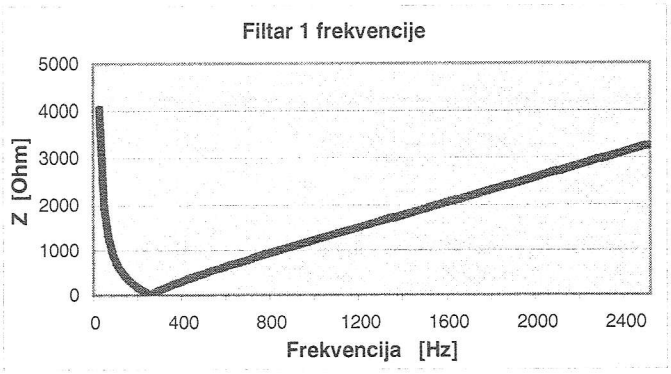

Fig. 9 – Single-tuned filter frequency response.

Double-tuned filter is a complex filter, which consists of 4 reactive components and has 2 resonant frequencies. It is combination of series and parallel connection of C, L and R passive components (Fig. 8.b). Its advantages are in lower losses and in lower voltage stresses of components. Such filter is applied for harmonics filtering in system for HVDC transmission between France and United Kingdom (Cross Channel Power Link) in the city of Echinghen [12]. Following components rates have been applied: R_1=4.2 Ω, R_2=1.656 Ω, R_3=2.11 Ω, C_1=1.51μF, C_3=12.08 μF, L_1=208 mH, L_2=24 mH.

Fig.10 presents frequency characteristic of filter impedance. The minimums at the 5th and the 7th harmonic order are clearly visible.

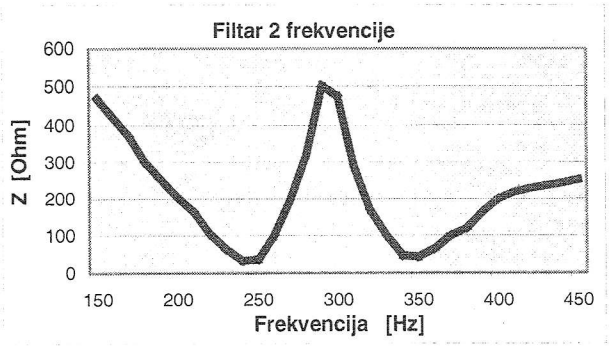

Fig. 10 – Double-tuned filter frequency response [12].

5.1.3 Damped filters

Damped-filters are used for eliminating harmonics of higher order (for example 11th and higher), usually in combination with single-tuned or double-tuned filters. Damped filters of the first, the second and the third order and c type filter are distinguished. Fig.11 presents all this filter schemes. It can be seen that they consists of one, two or three reactive components, which enables reduction of active losses and lower components ratings.

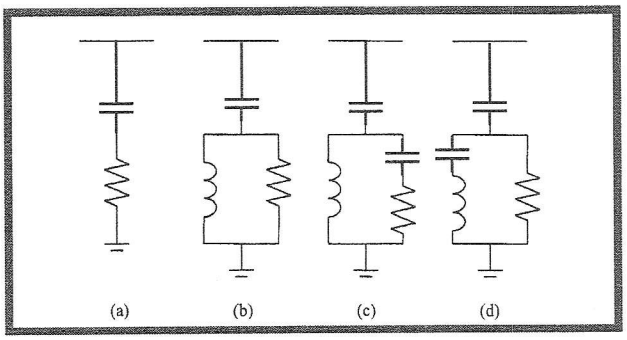

Fig. 11 – Damped filters: first (a), second (b) and third (c) order, and c type (d).

The simplest damped filter is filter of the first order, which consists of R and C component. However, it is rarely in use as it demands large capacitor and have losses at fundamental frequency. The best characteristic has the filter of the second order, although losses at fundamental frequency are greater than of the filter of the third order. Optimum solution is *C*-type filter, which has lower losses , but it is slightly more sensitive to changing of parameters.

Although passive filters are of simple construction, reliable and not so costly, they have significant drawbacks. In modern controlled electric drives and sophisticated non-linear loads, their application is not efficient. They often provoke parallel resonance or over-compensation on fundamental frequency. More, they are not flexible enough for modern dynamic compensation of different harmonics.

5.2 Active filters

Active filters present up-to-date solution for harmonics elimination. They do not have disadvantages of passive filters, and specific feature is quick adaptation to dynamics of operation of load and network, possibility to compensate several harmonics at the same time, and also to solve other power quality problems (flicker, voltage deviations e.t.c.).

The active filters are based on idea that distorted current wave shapes can be compensated by generating the similarly distorted wave shapes, but with opposite phase angle, so that original distortion is annulled. Active filters eliminate voltage distortion by adding or subtracting certain amount of voltage. Such task demands swift response and active operation of filter circuit, which is impossible to solve with passive components. For that reason active filters are developed with PWM converters, i.e. current and voltage PWM inverters. Current inverters are operated as source of non-sinusoidal current to be able to compensate current distortion generated by non-linear load. Voltage PWM inverter is more convenient solution, as it is lighter, cheaper and expandable to more functions. It is connected via inductance to network, and on DC side a capacitor ensures constant voltage.

Different classifications of active filters are possible. Most frequently they are divided to shunt, series and hybrid. Fig.12 shows block schemes of all three configurations.

6. SPECIAL CONTRACTS AND HARMONIC PRICING

Administrative or economical approach, as a special way of dealing with harmonics is developing in the last decade. Special contracts and harmonic pricing act unstimulating to excessive harmonic generation. For example in France a special type of contract has been developed. It is called "Emeraude" and offered to customers. It represents a collection of technical regulation rules and obligations of power supply company and consumer, all aiming to maintain certain power quality level. The results of contract application, which is published by the EDF, show that there was no violation of the contract at 99% of medium voltage level consumers. On the other hand a $150,000 worth compensation money is given, most frequently due to short interruptions. The new version of contract is published in 1995, by which a lower number of interruptions are stipulated and in 1998 revision is done, by which voltage sags are included into the contract.

The latest research are directed not only to detect existing situation, but to enable prediction and to give answer to the question – what are the costs of poor power quality (harmonic losses) and how to charge customers with large non-linear loads for polluting network with harmonics [13]. Methods of harmonic costs rating are of interest. Results of survey shows that 46% of power supply companies have intention to additionally charge for harmonics and flicker generation, 40% to charge for harmonics as additional apparent power (kVA), while others the duration (time) of pollution. Apart of this, the methods of measurement and methods of harmonic statement are not harmonized.

7. NEW SOLUTIONS

Growing demands for application of modern high performance electric drives, which means use of induction or synchronous motors, leads to development of complex control algorithms and use of power electronics converters in two stages. At the network side is AC/DC converter, while on the motor side is DC/AC converter. Such complex device is a non-linear load to the network and represents the source of current harmonics and poor power quality. IEC and IEEE harmonic standards put severe conditions for connection such loads to the public grid – use of filters or some of above-mentioned methods. However, such methods are costly and require action in the transmission network or distribution transformers. Therefore, research teams are looking for new solutions, which will maintain high operational performance and at the same time satisfy harsh harmonic standards. Constant dropping of electronic component prices and improving their characteristics, as well as much better performances of microprocessors and digital signal processors are leading the researches to implement more complex control algorithms and converters schemes. New solutions are looking in development electronics blocks and software, which is different from previous practice described above. Three directions can be distinguished:

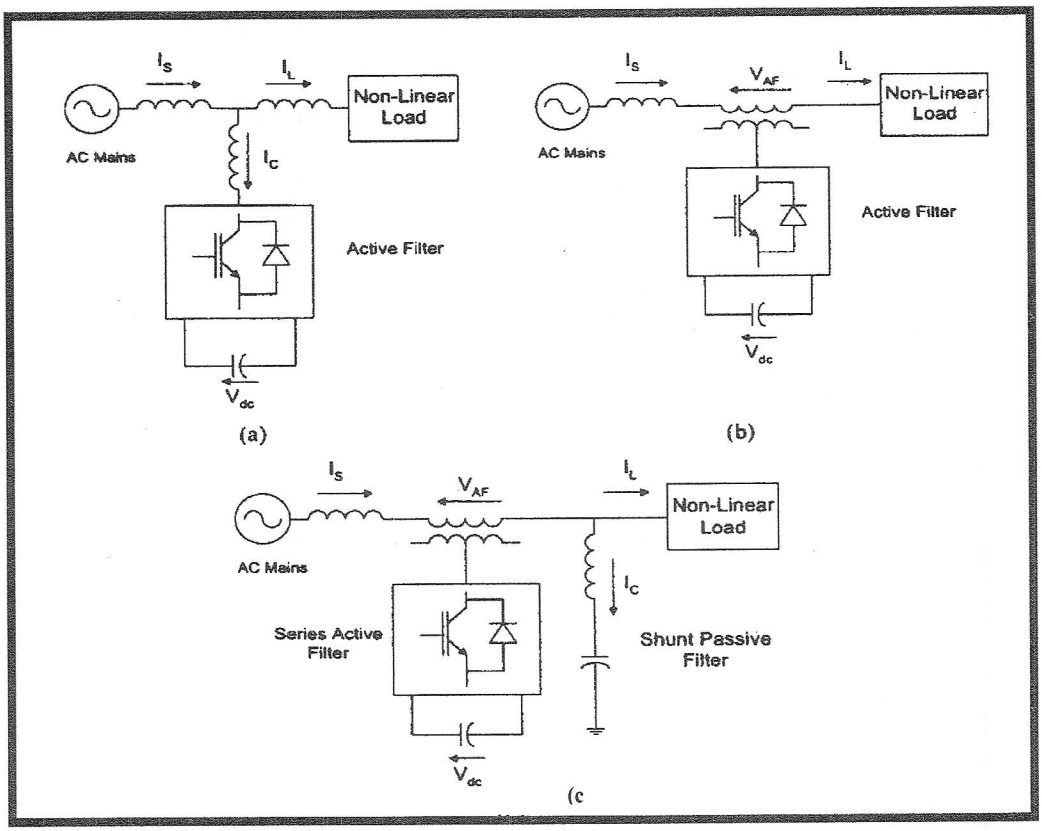

Fig. 12 – Active power filters topologies: a) Shunt, b) Series, c) Hybrid.

1. AC/DC converter transformation
2. Active filter application
3. Development of universal systems for power quality correction

The second point has been already explained above, while the solutions for the AC/DC converter transformation and universal systems for power quality correction have been researched in Serbia and will be shortly described next.

7.1 AC/DC converter transformation

AC/DC converter transformation means certain reconfiguration in converter scheme or method of control in order to decrease negative effects on network. Several solutions are possible:

1. Pulse number increase
2. Application of fast switching electronics components instead of thyristors (bipolar transistor, MOSFET or IGBT) controlled by a PWM techniques – PWM AC/DC converters
3. Application additional current injection circuits

Pulse number increase means more complex AC/DC converter and its control, but also more complex converter transformer too. In section 2 of this paper it is written about effects and advantages of this solution.

The PWM AC/DC converter applied on AC side of two stages frequency converter, enables unity power factor, reversible energy flow and simple filtering of harmonics. High switching frequency as well as proper PWM technique or control algorithm, enables shifting of spectrum components to higher orders, where there is no restriction (harmonic orders above the 100^{th}) or to orders where simple LC can be economically applied. In second case, low costs and size are enabled by already developed algorithm for filter components minimization in different operating conditions. The author has

devoted many papers to such solution, but limited length of this paper does not permit detailed explanation [1,14,15]. The solution is suitable for high power drives, where effect of energy returning to network is worthwhile, and where high performances are demanded.

Application of additional circuits for current injection in order to modify uncontrolled (diode) rectifiers, both single-phase and three-phase ones, has been developed to obtain unity power factor and the lowest possible harmonic distortion of input current. As very cheep, uncontrolled and with near unity power factor diode rectifiers are popular for input stage of low and medium power supplies. The basic idea of the method lies in intervention during period when input current is zero. These periods can be easily observed in the Fig.13, where current and voltage wave-shapes of single-phase rectifier are shown. During these periods a special circuits inject the current in that way to improve power factor and harmonic content [16]. The injection circuit consists of passive components (low power transformer and a LC circuit), and some active ones. Application of injection circuit is more convenient at three-phase rectifiers as results show that total harmonic distortion of input current can be decreased to THDI < 7%, and that power factor can be practically 1 (measured value was 0.993).

7.2 Universal power quality conditioning system

The latest research results are aiming not only to minimize the harmonics, but to decrease other voltage distortions too (flicker, unbalance, voltage sags and swells, short interruptions and so on) [8,11]. Such device is called Universal power quality conditioning system - UPQCS and represents a combination of parallel (shunt) active filter, series active filter and active AC/DC converter. The block scheme of the device is given in the Fig.14. AR stands for active AC/DC converter. It role is to enable and control the power transfer from and to common DC grid. Serial filter (SF) eliminate voltage harmonics, flicker, voltage sags and swells, unbalance and represent high impedance for current harmonics, which flow through parallel filter. Parallel filter (PF) minimize current harmonics, generated by non-linear load, and improve power factor.

At this moment such devices are not commercially applied, so results of their application can be observed only by simulation and laboratory experiments. Fig.15 represent an example of UPQCS operation in case of network voltage sag, obtained by measurement at laboratory prototype [8,11]. It can be seen that response to the network voltage sag (Fig.15-up) is swift and that the operation of load is not affected with the sag (Fig.15 – down).

Both new solutions feature more widely use of active electronics components. Such approach enables easy improvement of device characteristics, application of powerful control algorithms and at the same time use of constant electronic prices dropping privilege.

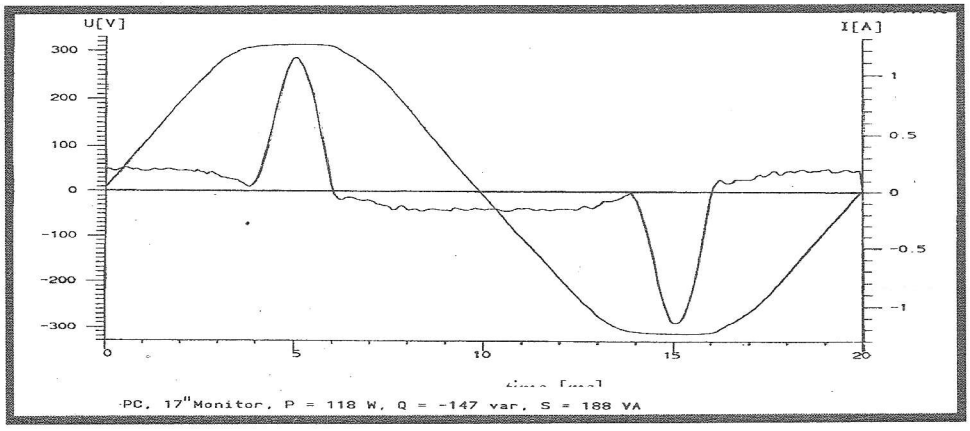

Fig. 13 – Network (input) voltage and current waveforms of single-phase rectifiers.

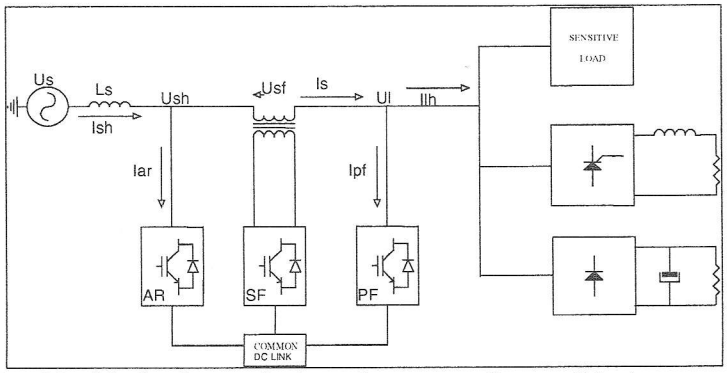

Fig. 14 – Block scheme of universal power quality conditioning system.

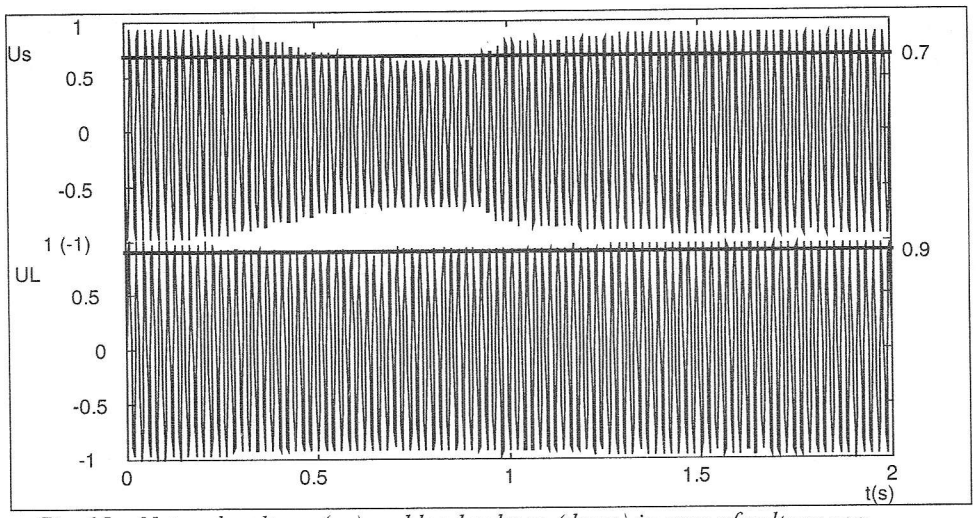

Fig. 15 – Network voltage (up) and load voltage (down) in case of voltage sag.

8. CONCLUSION

In the paper an overview of harmonic reduction methods is presented. Several standard methods are discussed (reduction of harmonic current effects, network reconfiguration, compensation units reconstruction, application of passive and active filters), which usually demands large and costly actions. Special recommendations, standards and contracts are also discussed, whose effects can be seen only after long and strict application. New trends are based on wider application of active electronic components, like special modifications of AC/DC converters, application of fast switching components, application of circuits for current injection and solution using Universal Power Quality Conditioning System. Such approach leads to performance improvements, applications of better control algorithms and constant decrease of device costs.

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THREE-PHASE HIGH POWER FACTOR RECTIFIER BASED ON THE THIRD HARMONIC CURRENT INJECTION WITH PASSIVE RESISTANCE EMULATION

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Abstract: *A novel high power factor rectifier that applies the third harmonic current injection and passive resistance emulation is presented. Conditions for the optimal third harmonic current injection are derived. Structure of the rectifier that applies passive resistance emulation enabling recovery of the power taken by the current injection network is presented. Resistance emulator consisting of a transformer, two diodes and a capacitor is proposed. Choice of the passive components is discussed. Dependence of the input current THD on the load level is presented. Analytically obtained results are verified on an 1.5 kW experimental rectifier.*

Keywords: *converters, harmonic distortion, power conversion harmonics, rectifiers*

1. INTRODUCTION

The third harmonic current injection is an approach to reduce input current harmonics of three-phase rectifiers. The method is suitable for high power applications, since it applies robust and reliable passive components, and the circuits of low complexity. In comparison to the multipulse rectifiers that dominate the application area, smooth waveforms of the input currents are obtained. The method is proposed in [1] and generalized in [2]. Interest in the method increased after simple rectifiers applying the method are proposed in [3] and [4]. In [5], the rectifiers proposed in [3,4] are analyzed, and it is shown that a part of the rectifier input power has to be taken by the current injection network in order to improve the input current total harmonic distortion (*THD*). This power is either dissipated on resistors, or processed by switching resistance emulators that enable recovery of the power at the rectifier output. Although this power is relatively low, 8.571 % of the input power in the case of the optimal third harmonic current injection [5], application of the resistors would reduce the rectifier efficiency. Furthermore, the resistors should have variable resistance to adjust to the load current variations, which will increase the rectifier complexity. Application of switching resistance emulators requires complex circuitry, increases the rectifier cost and reduces reliability.

To avoid mentioned drawbacks of the third harmonic current injection rectifiers, application of passive resistance emulation network is proposed in this paper. Concept of the rectifier connected in series with the load [6], coupled to the current injection path by a transformer, is applied as a resistance emulator. Injected current is filtered, resulting in low distortions of the input currents. Huge capacitors of [6] are avoided. Almost continuous waveforms of the input currents are achieved.

A method of the third harmonic current injection based on a magnetic current injection device is analyzed. The method is particularly suitable in the case a transformer is applied at the rectifier input, where the current injection can be performed at the transformer secondary neutral point [3], avoiding the need for the current injection device. In the case a magnetic current injection device is applied, its VA rating is 20.73 % of the input power [7].

2. THE CURRENT INJECTION

In a three-phase diode bridge, in each time point two diodes conduct, the diode connected to the highest of the phase voltages, and the diode connected to the lowest of the phase voltages. The phase whose voltage is neither minimal nor maximal at the considered time point remains unconnected. This results in discontinuities in the input currents. Patching of these discontinuities is the essence of the current injection method. The current injection method discussed in this paper applies simultaneous current injection in all three of the phases to patch the diode bridge input current gaps.

Let us assume that the rectifier of Fig. 1 is supplied by a three-phase voltage system

$$\begin{aligned} v_1 &= V_m \cos(\omega_0 t) \\ v_2 &= V_m \cos(\omega_0 t - 120°) \\ v_3 &= V_m \cos(\omega_0 t - 240°). \end{aligned} \tag{1}$$

In that case, if the optimal third harmonic current injection [5] is applied, waveform of the input current of the first phase is on $-180° < \omega_0 t < 180°$ period given by

$$i_1 = I_{OUT} \begin{cases} 1 + \frac{1}{4}\cos(3\omega_0 t), \text{ for } |\omega_0 t| < 60° \\ -\frac{1}{2}\cos(3\omega_0 t), \text{ for } 60° < |\omega_0 t| < 120° \\ -1 + \frac{1}{4}\cos(3\omega_0 t), \text{ for } 120° < |\omega_0 t| < 180°. \end{cases} \tag{2}$$

This waveform is characterized by

$$THD = \sqrt{\frac{32\pi^2}{315} - 1} = 5.125\% \tag{3}$$

with the displacement power factor equal to one [5]. Input current waveforms of the remaining two phases are displaced for 120° and 240°, being in phase with the corresponding phase voltages.

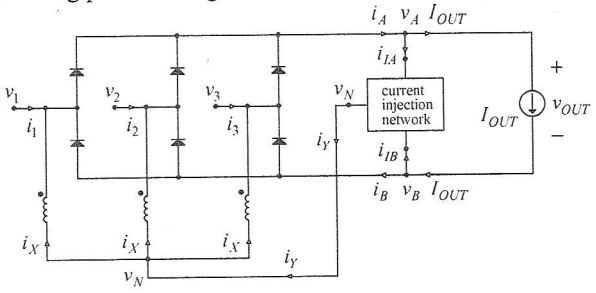

Fig. 1: *Structure of the rectifier*

In the case the diode bridge operates in the continuous conduction mode, the diode bridge output terminal voltages are given by their Fourier series expansions [5] as

$$v_A = \frac{3\sqrt{3}}{\pi} V_m \left(\frac{1}{2} + \sum_{n=1}^{+\infty} \frac{(-1)^{n+1}}{9n^2 - 1} \cos(3n\omega_0 t) \right) \quad (4)$$

and

$$v_B = \frac{3\sqrt{3}}{\pi} V_m \left(-\frac{1}{2} + \sum_{n=1}^{+\infty} \frac{1}{9n^2 - 1} \cos(3n\omega_0 t) \right). \quad (5)$$

This corresponds to the diode bridge output voltage waveform

$$v_{AB} = \frac{3\sqrt{3}}{\pi} V_m \left(1 - 2\sum_{k=1}^{+\infty} \frac{1}{36k^2 - 1} \cos(6k\omega_0 t) \right) \quad (6)$$

having the dc component

$$V_{AB} = \frac{3\sqrt{3}}{\pi} V_m . \quad (7)$$

Since the output current I_{OUT} is assumed to contain only dc component, the diode bridge output power equals

$$P_{AB} = \frac{3\sqrt{3}}{\pi} V_m I_{OUT} . \quad (8)$$

Analyzed method of current injection applied in the rectifier of Fig. 1 applies simultaneous current injection in all three of the rectifier phases, which is achieved applying a magnetic current injection device or injecting the third harmonic current at the input transformer secondary neutral point [3]. Output current of the current injection network, i_Y, is divided in three parts by the current injection device, and injected back at the rectifier input. The current injection device is characterized by

$$i_X = \frac{1}{3} i_Y \quad (9)$$

and

$$v_N = \frac{1}{3}(v_1 + v_2 + v_3) = 0 . \quad (10)$$

If the current injection device is realized as a special magnetic device, its VA rating is 20.73 % of the input power. To determine currents i_{IA}, i_{IB}, i_Y, and i_X that provide the optimal input current waveform specified by (2), let us analyze the circuit of Fig. 1. Assumption that currents i_{IA} and i_{IB} taken by the current injection network from the diode bridge output terminals are the same, containing only the spectral component at the triple of the line frequency, results in

$$i_{IA} = i_{IB} = \frac{1}{2} i_Y = \frac{3}{2} i_X . \quad (11)$$

To match the optimal input current waveform for the third harmonic current injection, current i_X injected in each phase of the rectifier should be

$$i_X = \frac{1}{2} I_{OUT} \cos(3\omega_0 t). \quad (12)$$

Since all the currents of the current injection network are assumed to contain only the spectral component at the triple of the line frequency, power taken by the current injection network is determined only by its currents and the fundamental harmonic component of v_A and v_B, which is also on the triple of the line frequency, with the amplitude

$$V_{A,1} = V_{B,1} = \frac{3\sqrt{3}}{8\pi} V_m . \quad (13)$$

The power taken by the current injection network to provide the optimal third-harmonic current injection is thus equal to

$$P_{INJ} = \frac{9\sqrt{3}}{32\pi} V_m I_{OUT} = \frac{3}{32} P_{AB} . \quad (14)$$

This power could be dissipated on resistors or restored applying a resistance emulation technique. In this paper, a resistance emulation technique that applies only diodes and passive elements is proposed.

3. STRUCTURE OF THE RECTIFIER

The rectifier that applies passive resistance emulation is presented in Fig. 2. In comparison to the general scheme of Fig. 1, structures of the current injection network and the resistance emulator are presented. Basic part of the current injection network consists of $C_S/2$ capacitors, 1:1 transformer, and L_S inductor. The capacitors and the inductor are applied to filter spectral components of v_A and v_B at the triple of the line frequency. The 1:1 transformer is applied to reject spectral components of i_{IA} and i_{IB} at even triples of the line frequency. This part of the current injection network is proposed in [8], but a resistor is applied to control the amplitude of the injected currents. Instead of the resistor applied in [8], a resistance emulator consisting of two diodes, a transformer, and a capacitor is applied in the rectifier of Fig. 2. The transformer is assumed to be with perfect coupling, thus it can be represented by a magnetizing inductance L_P, connected in parallel with C_P, and an ideal transformer. The capacitor C_P with the magnetizing inductance of the transformer forms a resonant circuit that forces the spectral component of i_Y at the triple of the line frequency to flow through the primary of the ideal transformer. The other spectral components are conducted through the resonant circuit formed of C_P and L_P. Voltage across the resonant circuit is reflected to the transformer secondary and rectified, increasing the output voltage dc component and transferring the power taken by the current injection network to the load.

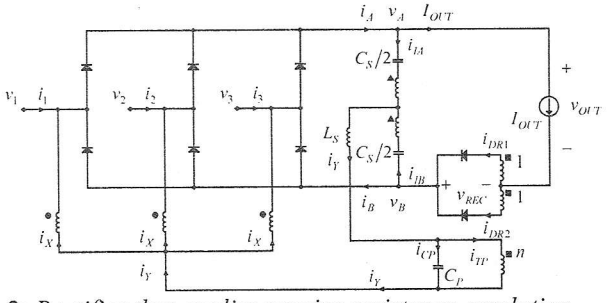

Fig. 2: *Rectifier that applies passive resistance emulation*

To analyze the current injection network, let us use the method of equivalent circuits proposed in [5]. The method is based on the fact that voltages v_A and v_B contain spectral components at triples of the line frequency, and that the components at odd triples of the line frequency have the same

equivalent circuit of the current injection network for these frequencies is an open circuit. On the other hand, at odd triples of the line frequency components of v_A and v_B are the same, and they produce the injected currents. Thus, the current injection network may be represented by a simplified equivalent circuit presented in Fig. 3. Voltage v_Y represents the voltage effectively applied across the current injection network, defined as

$$v_Y = \frac{v_A + v_B}{2} \tag{15}$$

which is

$$v_Y = \frac{3\sqrt{3}}{\pi} V_m \sum_{k=1}^{+\infty} \frac{1}{9(2k-1)^2 - 1} \cos(3(2k-1)\omega_0 t). \tag{16}$$

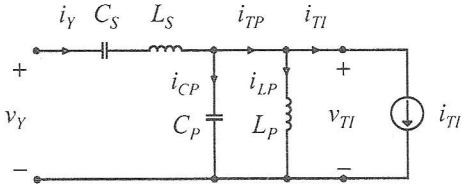

Fig. 3: *Equivalent circuit of the resistance emulator*

Primary current of the ideal transformer part of the n:1:1 transformer is represented by i_{TI}, which is given by

$$i_{TI} = \frac{1}{n} I_{OUT} \operatorname{sgn}(v_{TI}). \tag{17}$$

Reactive elements of the current injection network should satisfy resonance constraints for the triple of the line frequency

$$\omega_R = 3\omega_0 = \frac{1}{\sqrt{L_S C_S}} = \frac{1}{\sqrt{L_P C_P}}. \tag{18}$$

In the case the resonant constraints (18) are satisfied, equivalent circuit of the network of Fig. 3 for the triple of the line frequency reduces to the circuit of Fig. 4. From the circuit of Fig. 4 it can be concluded that the third harmonic component of i_Y equals to the third harmonic component of i_{TI}, while the third harmonic component of the voltage at the n:1:1 transformer primary equals to the third harmonic component of the voltage across the current injection network, v_Y.

The square waveform of i_{TI} is represented by the Fourier series expansion

$$i_{TI} = \frac{4}{\pi} \frac{I_{OUT}}{n} \sum_{k=1}^{+\infty} \frac{(-1)^{k+1}}{2k-1} \cos(3(2k-1)\omega_0 t) \tag{19}$$

with the amplitude of the spectral component at the triple of the line frequency of $\frac{4}{\pi}\frac{I_{OUT}}{n}$, which should be equal to the amplitude of the corresponding spectral component of i_Y. Thus, the n:1:1 transformer turns ratio should be

$$n = \frac{8}{3\pi}. \tag{20}$$

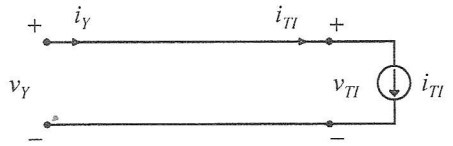

Fig. 4: *Equivalent circuit for the triple of the line frequency*

To simplify the analysis of the current injection network, let us introduce an approximation that the series resonant circuit formed of L_S and C_S is represented by an open circuit for frequencies other than the triple of the line frequency, and that the parallel resonant circuit formed of L_P and C_P is represented by a short circuit, as depicted in Fig. 5.

According to the equivalent circuit of Fig. 5, terminal currents of the current injection network will contain only the third harmonic component, while higher order spectral components of i_{TI} will close through the parallel resonant circuit. In practice, there will be some leakage of spectral components at higher order odd triples of the line frequency through the current injection network, which will slightly influence the input current *THD*.

Under the assumption made above, only the third harmonic component of v_Y is reflected at the n:1:1 transformer secondary. According to (20), the output voltage of the resistance emulator, v_{REC}, indicated in Fig. 2, equals

$$v_{REC} = \frac{9\sqrt{3}}{64} V_m \left|\cos(3\omega_0 t)\right| \tag{21}$$

resulting in the output voltage spectrum

$$v_{OUT} = v_{AB} + v_{REC} = \frac{3\sqrt{3}}{\pi} V_m \left(\frac{35}{32} - \sum_{k=1}^{+\infty} \left(\frac{2}{36k^2 - 1} + \frac{3}{16} \frac{(-1)^k}{4k^2 - 1} \right) \cos(6k\omega_0 t) \right) \tag{22}$$

The dc component of the output voltage is increased to

$$V_{OUT} = \frac{35}{32} \frac{3\sqrt{3}}{\pi} V_m \tag{23}$$

corresponding to the complete recovery of the power taken by the current injection network. On the other hand, amplitude of the output voltage ripple is reduced, especially its spectral components at odd multiples of the sixth multiple of the line frequency.

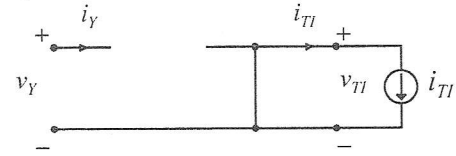

Fig. 5. *Idealized equivalent circuit for higher order harmonics*

Waveforms of the rectifier voltages and currents obtained applying the introduced approximation are presented in Fig. 6. The first diagram of Fig. 6 presents the diode bridge output terminal voltages, indicating that their spectral components at the triple of the line frequency are in phase, with the same amplitude. The second diagram presents voltage v_Y, effectively applied at the input of the equivalent circuit of Fig. 3. In the same diagram, spectral component of v_A and v_B at $3\omega_0$, $v_{A,1}$, is presented, illustrating that the third harmonic component dominates the voltage across the current injection network, v_Y. The third diagram presents the output voltage of the diode bridge v_{AB}, as well as the rectifier output voltage v_{OUT}. Analyzing the diagram, two conclusions can be made: first, that the rectifier output voltage dc component is increased in comparison to the diode bridge output voltage, which corresponds to the recovery of the power taken by the current injection network; second, that the rectifier output voltage ripple is lower than the output voltage ripple of the diode bridge. The forth diagram presents the injected current i_Y and the primary current of the ideal transformer part of the n:1:1 transformer, i_{TI}. In the fifth diagram, current flowing through the parallel resonant circuit of the equivalent circuit of Fig. 3 is presented, illustrating that higher order harmonics of i_{TI} are closed through the parallel resonant circuit.

4. CHOICE OF THE COMPONENTS

After the n:1:1 transformer turns ratio is determined by (20), choice of the reactive components of the current injection network and volt-ampere ratings of the magnetic components are analyzed in this section.

First, let us discuss components of the series resonant circuit, consisting of two capacitors of $C_S/2$ and the inductor L_S. Spectrum of the voltage applied across the circuit of Fig. 3 consists of the spectral components at odd triples of the line frequency. To pass the component at the triple of the line frequency, the resonant constraint (18) should be satisfied. On the other hand, to block the spectral components at higher order triples of the line frequency, inductor L_S should be as large as possible. Large L_S values result in expensive realizations and in high voltage stress on $C_S/2$ capacitors. In order to apply electrolytic capacitors for $C_S/2$, voltage across the capacitors should be unipolar. This constraint results in a limit for the value of L_S. Since the dc components of the voltages across the capacitors are equal to $\frac{3\sqrt{3}}{2\pi}V_m$, and the maximum ac components are $\frac{I_{OUT\max}}{2\omega_0 C_S}$, where $I_{OUT\max}$ is the maximum of the load current, minimal value of C_S that allows application of the electrolytic capacitors is

$$C_S = \frac{\pi}{3\sqrt{3}}\frac{1}{\omega_0 R_X} \qquad (24)$$

where

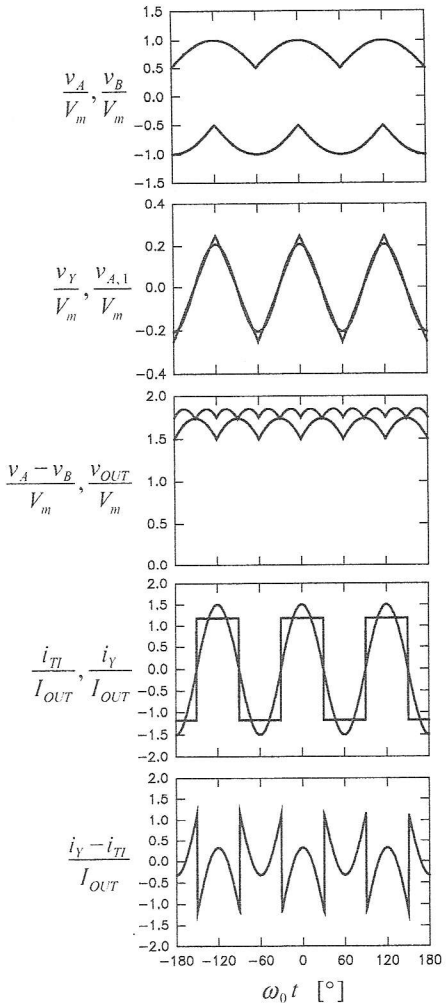

Fig. 6: *Waveforms of the current injection network voltages and currents*

$$R_X = \frac{V_m}{I_{OUT\max}}. \qquad (25)$$

This results in L_S value of

$$L_S = \frac{1}{\pi\sqrt{3}}\frac{R_X}{\omega_0}. \qquad (26)$$

This value of L_S is the largest value that allows application of electrolytic capacitors for $C_S/2$. Lower values of L_S result in reduced voltage stress on the capacitors, but also in higher leakage of higher order spectral components. Volt-ampere rating of the inductor specified by (26) is

$$S_L = \frac{\omega_0}{2\sqrt{2}} L i_{\max} I_{RMS} = \frac{2}{35} P_{OUT} = 5.71\%\, P_{OUT}. \qquad (27)$$

The parallel resonant circuit of Fig. 3 is applied to block spectral component of i_{TI} at the triple of the line frequency and to short the higher order spectral components of i_{TI}. To achieve this goal, capacitor C_P should be as large as possible. Dominant component of the voltage applied on the parallel resonant circuit is at the triple of the line frequency, with the amplitude specified by (13). Increasing the value of C_P, ringing current of the resonant circuit will

increase, resulting in increased losses and volt-ampere ratings of the components. On the other hand, ringing current of the parallel resonant circuit should be large enough to avoid discontinuous conduction mode of the resistance emulation rectifier. This discontinuous conduction mode is characterized by simultaneous conduction of both of the rectifier diodes. The discontinuous conduction mode is avoided if the amplitude of the current through L_P is higher than the amplitude of the secondary current of the ideal transformer,

$$\frac{1}{3\omega_0 L_P}\frac{3\sqrt{3}}{8\pi}V_m > \frac{I_{OUT\max}}{n}. \qquad (28)$$

Thus, minimal value of L_P that provides continuous conduction operating mode of the resistance emulation rectifier is

$$L_P = \frac{1}{\pi^2\sqrt{3}}\frac{R_X}{\omega_0}. \qquad (29)$$

Corresponding value of C_P is according to (18)

$$C_P = \frac{\pi^2}{3\sqrt{3}}\frac{1}{\omega_0 R_X}. \qquad (30)$$

Lower value of L_P and the corresponding value of C_P will contribute to the rejection of the higher order harmonics, but will increase volt-ampere rating of the components.

The parallel resonant circuit inductor L_P is realized as a magnetizing inductance of the n:1:1 transformer. This realization is simple and efficient, and it results only in somewhat increased volt-ampere rating of the transformer in comparison to the realization where separate inductor and transformer are applied. The volt-ampere rating of the resistance emulation transformer equals

$$S_T = \frac{\pi}{140\sqrt{2}}\left(1+\sqrt{\frac{3}{2}}\right)P_{OUT} = 3.53\%\ P_{OUT}. \qquad (31)$$

The 1:1 transformer, applied to reject spectral components at even triples of the line frequency, is characterized by low volt-ampere rating, computed applying a result for the flux-linkage presented in [8]. The volt-ampere rating is

$$S_T = \frac{2}{35}\left(\sqrt{\pi^2-9} - 3\arctan\frac{\sqrt{\pi^2-9}}{3}\right)P_{OUT} = \qquad (32)$$
$$= 0.1623\%\ P_{OUT}.$$

Obviously, volt-ampere rating of the 1:1 transformer is very small in comparison to the other magnetic devices.

5. EXPERIMENTAL RESULTS

To verify presented analyses, the rectifier presented in Fig. 2 is built. Rated power of the rectifier is 1.5 kW, and it operates at the input voltage rms value of 100 V, with the maximum output current of 6.5 A. For these specifications, near optimal values for the current injection network are chosen, $C_S/2 = 100\,\mu$F, $L_S = 5.63$ mH, $C_P = 275\,\mu$F, and $L_P = 4.09$ mH, corresponding to $R_X = 21\,\Omega$.

Waveforms of the input voltage and the input current at the maximum output power are presented in Fig. 7. The input current is slightly distorted, and the waveforms are in phase. Total harmonic distortions of the input currents and voltages in the full load case, as well as power factors for all three of the rectifier phases are presented in Table I. The results presented in Table I indicate that distortion of the input voltages of about 3 % negligibly affected the input current distortions that are about 4.7 %. Power factors at all three of the phases are above 0.99.

Waveforms of the output voltage v_{OUT} and the diode bridge output voltage v_{AB} are presented in Fig. 8. From the waveforms of Fig. 8, it can be concluded that the output voltage has higher dc component than the diode bridge output voltage, which is caused by the power recovered by the resistance emulator. Waveform of the output voltage has higher ripple than theoretically predicted and depicted in Fig. 6, which is caused by nonideal matching of the resonance constraint (18) and the resulting phase shift. Measured efficiency of the converter is almost constant from 5 % of the full load, with slight decrease near the full power. At full power, the efficiency of 96.7 % is measured.

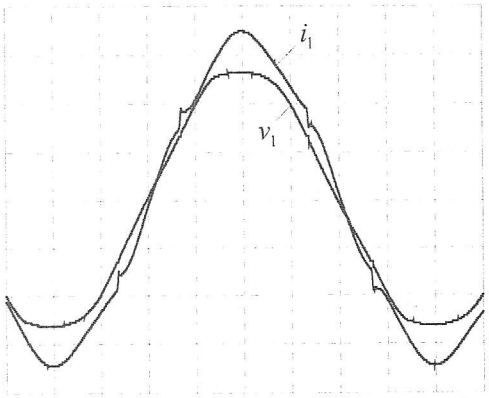

Fig. 7: *Waveforms of* v_1 *and* i_1*; voltage scale* 50 V/div, *current scale* 2 A/div, *time scale* 2.5 ms/div

Table 1. *Total harmonic distortions and power factors*

phase	1	2	3
$THD(i_{phase})$	4.60 %	4.73 %	4.73 %
$THD(v_{phase})$	3.10 %	2.99 %	3.12 %
PF_{phase}	0.9961	0.9963	0.9962

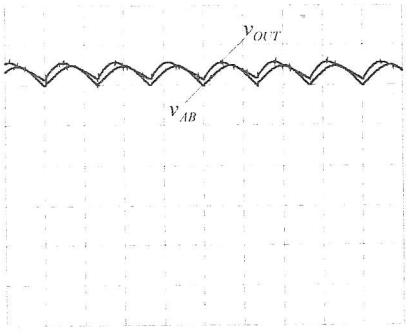

Fig. 8: Waveforms of v_{AB} *and* v_{OUT}*; voltage scale 100 V/div, time scale 2.5 ms/div*

To analyze dependence of the input current *THD* on the output current, a set of measurements is performed, and the results are presented in Fig. 9. In Fig. 9, three diagrams are presented: dependence of the input current *THD* on the load level computed numerically, analyzing only leakage of the resonant circuits at higher order triples of the line frequency ("theoretical"), numerically computed dependence including measured leakage of the parallel resonant circuit at $3\omega_0$ ("theoretical with leakage"), and the experimental curve. Discrepancy between the theoretical end experimental curve is obvious. Analyzing the rectifier, it is found that cause of the discrepancy is leakage of the parallel resonant circuit (C_P and L_P) at the triple of the line frequency, resulting in its finite impedance of 23Ω, with the phase shift of $-22.5°$. This phase shift caused the unexpectedly high ripple of the output voltage. Taking the leakage of the parallel resonant circuit at the triple of the line frequency into account in numerical computations, good agreement with the experimental results is obtained.

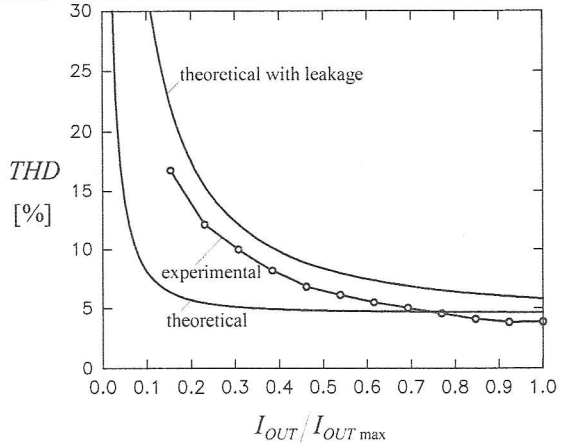

Fig. 9: *Dependence of the input current THD on the load level*

6. CONCLUSIONS

In this paper, a high power factor rectifier that applies the third harmonic current injection and passive resistance emulation is presented. Passive resistance emulation enables recovery of the power taken by the current injection network. Proposed resistance emulator consists only of a transformer, two diodes and a capacitor. Operation of the rectifier is analyzed applying idealized models of the resonant circuits in the current injection network. Choice of the passive components is discussed, and values that provide compromise between the third harmonic filtering, volt-ampere ratings of the components, application of electrolytic capacitors, and reduction of losses, are proposed. Volt-ampere ratings of the magnetic components are derived. To verify the analytical results, the current injection methods are tested on 1.5 kW experimental rectifiers. Dependence of the input current *THD* on the load level is analyzed. Experimental results are in excellent agreement with the theoretical predictions.

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TASK EXECUTION IN REAL-TIME SYSTEMS FOR INDUSTRIAL CONTROL AND MONITORING

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Abstract - *In this paper, the task execution in real-time systems for industrial control and monitoring is considered. The cigarette-packing control and monitoring system was described in order to illustrate some of the problems that have to be solved during system design and implementation. These problems are scheduling policy, real-time task implementation and the interface between different software parts. Development and debugging tools used in the system design are also considered.*

1. INTRODUCTION

The main feature of real-time systems is that regularity of their performance depends not only of the processing results accuracy, but also of the moment when the results are generated.

Automated industrial systems require precise performance, coordinated with numerous sensors and actuators. Therefore, real-time systems find particular appliance in industrial control and monitoring systems. Till recently, most of the hardware and software solutions for real-time systems were expensive. Nowadays, personal computers and open source software provide developers to build really powerful yet affordable systems.

In this paper, we will consider the problem of task execution in real-time systems for industrial control and monitoring. The problem will be considered through the example of one typical industrial control and monitoring system - the cigarette packing system in Tobacco Factory Nis. We will show how we solved the problems of scheduling policy, communication task implementation, interface between different software parts etc.

2. SYSTEM DESCRIPTION

Here, we will consider industrial control and monitoring system for the cigarette packing process. The whole system consists of four major parts: GD-X1 (forms cigarette packs), GD-A400 ("feeds" machine X1 with cigarettes), GD-CH (wraps packs with foil) and GD-GR ("group" machine that forms boxes, each containing 10 packs). The system was implemented as distributed hard real-time system with distributed process control functions and centralized monitoring function. Each machine is controlled by a hard real-time process-controller (PK). All process controllers concurrently realize following activities: control, sensor reading and tracking down relevant parameters, communication with process computer and self testing. Monitoring function is performed by central process computer, industrial PC (Intel 433 MHz, 256 MB RAM) with Touch Panel interface for the interaction between operator and the system. Communication between peripheral units and PC is realized via SUNIX 8134 ISA 16-bit 2 PORT RS-422/485 communication card. One channel is used for communication between PC and process controllers (four of them, each dedicated to one machine), and the other for communication between PC and 10 temperature controllers (TR). RS-485 half-duplex serial protocol is used. Graphical representation of the system is given in Figure 1.

Process computer performs the system monitoring task, archiving process parameters and events, generating reports and providing graphical interaction between operator and the whole system. Though the requirements for functionality were complex, choosing appropriate operating system immediately imposed itself as a problem that should be taken in serious consideration. We've chosen Linux operating system, mainly for its robustness, stability and having all other good features of UNIX-like operating systems. Since particular application also requires satisfying the timing constraints in task response, we've chosen Linux with its extension for real-time processing, i.e. Real-Time Linux (RT Linux) [1]. In that manner we came to the system that provides real multitasking and multithreaded processing, satisfying, in the same time, timing constraints, as well as the requirements concerning system reliability.

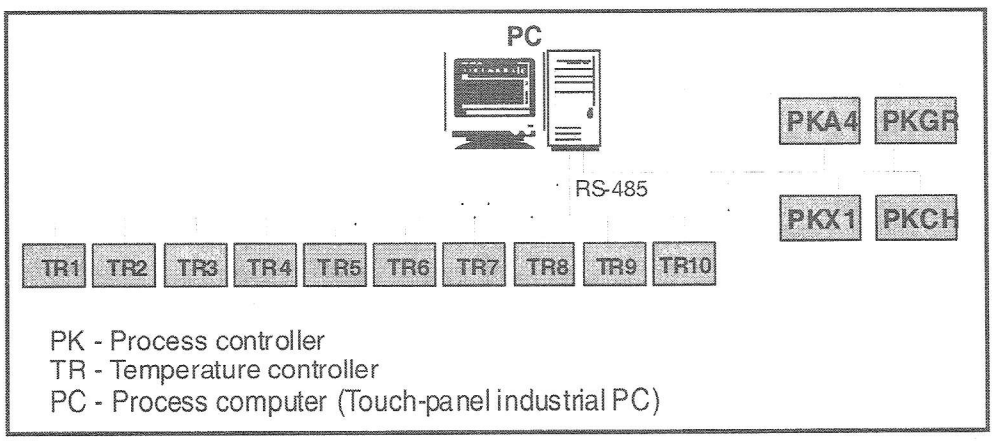

Figure 1. Control and monitoring system graphical representation

However, hardware platform and appropriate operating system are not merely enough for complete implementation of a real-time system for control and monitoring. We could say that it's just the basis, and that the real problem is how to develop efficient application, that would utilize the maximum of the chosen platform and, in the same time, fulfill all of the, often strict, functional requirements. The implementation phase especially brings numerous questions, such as: How to provide data to be available to the algorithm in exact moment? What will happen if the result is not available at that moment? What is the most appropriate scheduling algorithm for the tasks? How will time-critical tasks affect the non critical? In the next section we will try to give some answers on those questions.

3. APPLICATION SOFTWARE ARCHITECTURE

Since, this is a distributed system, the first question that comes to mind is where should each task be executed, or, more precise, what functions should be implemented in process controllers, and what in process computer. Furthermore, concerning process computer, there is a problem of allocating time-critical and non-critical code.

If we have a look at the whole system on Figure 1, it is natural for the time-most-critical tasks of packing process control, to be executed in process controllers. On the other side, in process computer, the situation is a bit complicated. The whole application contains both time-critical tasks and tasks that don't have strict timing constraints. In the first group certainly belong the tasks for communication with process controllers and temperature controllers. System parameter archiving, event archiving (writing the hard disk), as well as the human-system interaction (in which we can tolerate certain latency, but it mustn't be too large in order not to break the concentration of an operator) belong to the other group of non real-time tasks.

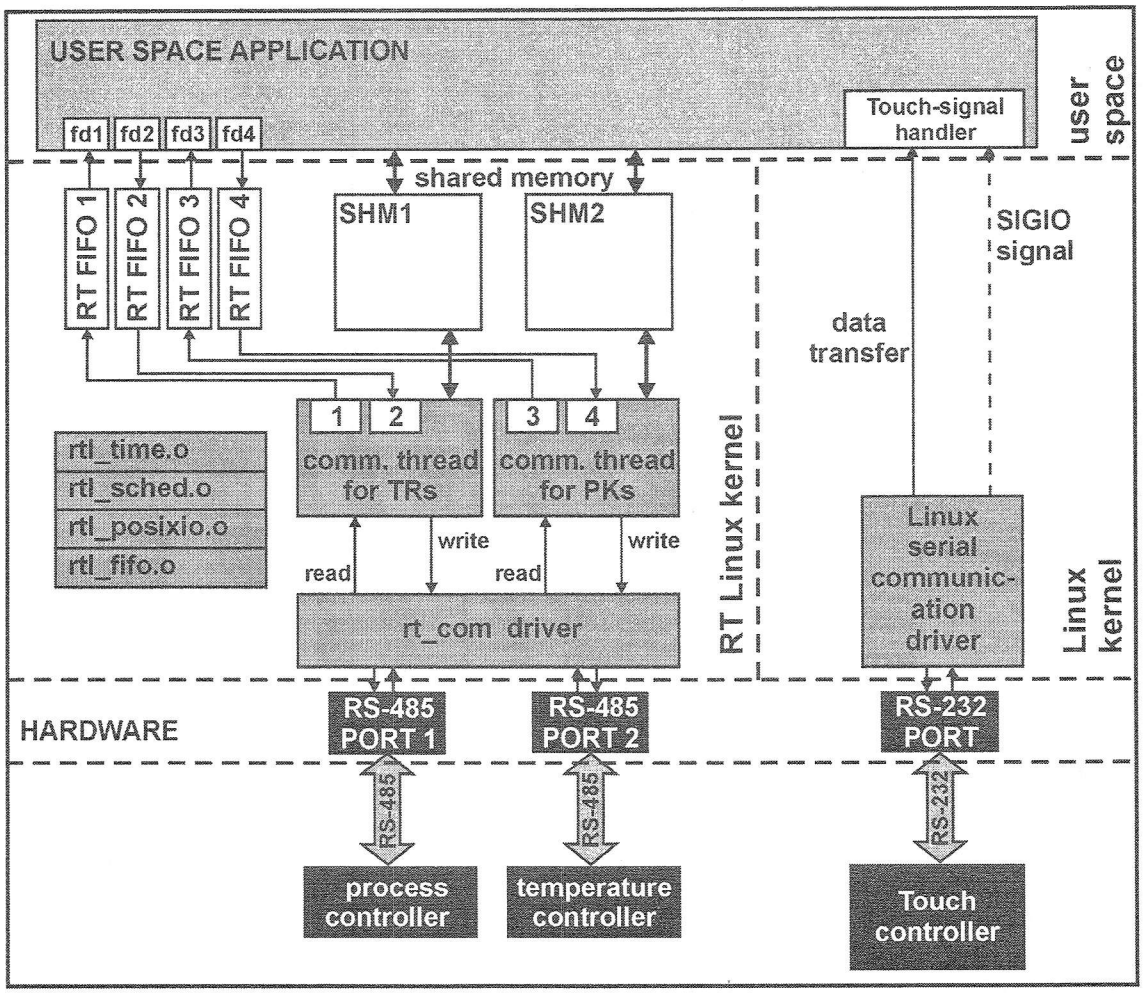

Figure 2. Application software architecture

Concerning task allocation in process computer, the solution for the mentioned problem is to physically separate time-critical and non-critical tasks. During the development of Real-Time Linux, the designers experimented, allocating different address spaces to real-time tasks. They found out that the best performance is achieved when all the real-time tasks are executed in the same address space, to be exact, the kernel address space [2].

3.1. Software in hard real-time process controllers

The following tasks are concurrently executed in the process controllers:

- interrupt driven communication with central process computer;
- urgent asynchronous events handling - setting the system to the secure state with system stop (for

example "UNCONDITIONAL STOP" etc.);
- execution of the control algorithm synchronously with the machine phase angle with the resolution of 1 degree (≈1/1800 sec);
- machine test and function execution in specified time interval;
- process computer command processing, starting the response preparing task and starting the response sending task;
- sequential test of all the conditions for regular performance;
- sensor testing;
- actuator testing;
- monitoring and registering product parameters (number of regular packs, number of rejected packs);
- short-term event archive generation;
- perpetual check whether time deadlines are missed;

Process controller software is not executed under RT Linux, but under process controllers' small embedded operating system, which has its own scheduler and interrupt dispatcher.

3.2. Kernel drivers in the process computer

Here, we will talk about achieving real-time performance in Linux. In order to merely use real-time kernel, it's needed that four kernel modules, modules providing hard real-time performance, are loaded and linked with Linux kernel. These modules are:

- `rtl_time`;
- `rtl_sched`;
- `rtl_posixio`;
- `rtl_fifo`;

The first module provides RT Linux to have complete control over system clock interrupts. When system clock issues an interrupt, this module catches it and passes it to the real-time scheduler (`rtl_sched`), which will start the execution of the first real-time task waiting to be scheduled. If no real-time tasks wait for execution, it will execute "normal" Linux, as the real-time task with the lowest priority. That's in short the whole "philosophy" of RT Linux, where we can see that it is not an autonomous operating system. It's actually the system with two coexisting kernels, where "standard" Linux kernel is a real-time task with the lowest priority. In that way real-time tasks are enabled to preempt Linux processes, providing minimum real-time processing latency [2].

On the other side, one of the process computer's main tasks is the communication with PKs and TRs. As already mentioned, ISA 16-bit 2 PORT RS-422/485 communication card is used. Since it's a distributed system with multiple-point structure, RS-485 serial protocol with half-duplex mode was chosen. Concerning the communication card is unintelligent one, accessing its ports is identical to accessing serial ports on the computer main board. That's why it wasn't necessary to write a driver for this card, therefore we used already existing RT Linux serial communication driver, written by Jochen Kuepper. That driver has real-time features concerning interrupt handling and data protection, and it guarantees that data we want to send will be sent to the communication line in specified moment, without the possibility of the process to be interrupted with some other system request [3]. Since the driver was originally written for the RS-232 port it couldn't be used without changes. However, the only change we had to make was setting the RTS (*Request To Send*) and CTS (*Clear To Send*) signals properly in the interrupt handler routine, in order to switch direction of data flow over the communication line.

3.3. Real-time tasks

In Real-Time Linux, a real-time task is actually a kernel thread, organized as a kernel module and allocated in the kernel address space. The advantages of this solution are numerous. This solution provides optimal system performance concerning minimum memory paging latency and system call execution latency. Above that, the feature of loadable kernel modules (modules that can be dynamically loaded and linked with kernel) eases the development, since, during the real-time system design, even a small bug may cause the whole system to be wiped out [4].

Real-time thread looks like the subroutine and can have parameters. The main difference, comparing to the standard subroutines, is the calling mechanism. The task can be called as a result either of a timeout within the scheduler or of an interrupt. The first case is used for periodic tasks, when scheduler starts the execution of the thread at the beginning of each previously defined time interval, i.e. real-time task period. The latter case is when a task is event driven.

In our system, there are two real-time tasks in process computer, both referring to the communication. One real-time thread is responsible for the communication with temperature controllers, and the other for communication with process controllers. A typical master-slave communication model was applied, where process computer addresses one by one TR (10 of them), and one by one PK (4 of them). The purpose is to read the states of the peripheral units, and to set some of their parameters at the request of the operator. Both threads are periodical.

Generally, a real-time thread for serial communication has four basic functions:

- `thread_function` - the function which does the job;
- `fifo_handler` - RT FIFO buffer handler;
- `init_module` - standard routine for kernel module initialization;
- `cleanup_module` - standard routine that removes kernel module from the memory and reallocates resources taken by thread;

Thread function is actually the function performed by the real-time task. In this case its job is to communicate with the slave, i.e. to periodically read the parameters of the peripheral unit. The parameters read are passed to the user space process by means of shared memory. The main demands during real-time task design is that the code should be sequential, as short as it can be (because of the speed) and we should strictly take care of not getting into "dead loop". The period is given in nanoseconds, and its 100ms for each thread. TRs are read one time each in a second, and PKs two times each in a second. Since it's not necessary to dig deep into the thread code, we should say only that after every reception we check if an error occurred during the transfer, and if there's no error, after some processing the results are passed to the user space process.

Shared memory is the most efficient mechanism for inter-process communication, when we need to exchange large amounts of data between user space process and real-

time threads and when built-in synchronization is not required. Sharing the same memory space provides tasks to exchange data similarly to the use of global variables, and yet to have their own protected address spaces.

Function `fifo_handler` is a kernel routine that provides asynchronous interaction between user space process and real-time thread. RT FIFOs are memory buffers used for communication between kernel space real-time threads and user space Linux processes. A RT FIFO provides data transfer only in one direction, therefore for bidirectional data transfer we need to open two of them, one for each direction. One RT FIFO is always used to start and stop the real-time thread, as well as to change same parameter used in it `thread_function`. RT FIFO handler monitors that RT FIFO and, when data in the FIFO is available, momentarily reads data, if necessary does some processing, and then performs the command needed (start, stop or parameter modification). The communication protocol for user process - thread data transfer, i.e. commands used to communicate and actions on each command are user defined.

The `init_module` routine provides a real-time thread to be dynamically loaded into the kernel address space and linked with the kernel code. In particular case it is also used to create and allocate the resources needed by thread (serial port, RT FIFOs, fifo handler and shared memory). The state diagram for real-time threads is given in Figure 3. When thread is created, it is in the READY state. After the start command from the user space process is sent through the RT FIFO, fifo handler creates the thread to be periodic, and real-time thread starts its execution. At the beginning of each previously defined time period, the thread function is executed (RUN state), and then thread goes to the SUSP state, i.e. suspends its execution until the beginning of the next period. At the time of the thread creation, the thread priority is also defined. It is necessary because of the priority-based real-time scheduler. RT Linux conforms to the POSIX standard, which implies assigning priorities up to 10000000. Under POSIX the higher the priority number the higher the priority. Communication tasks are very important to any real-time system, therefore we could assume that they would certainly have a high priority, if not the highest.

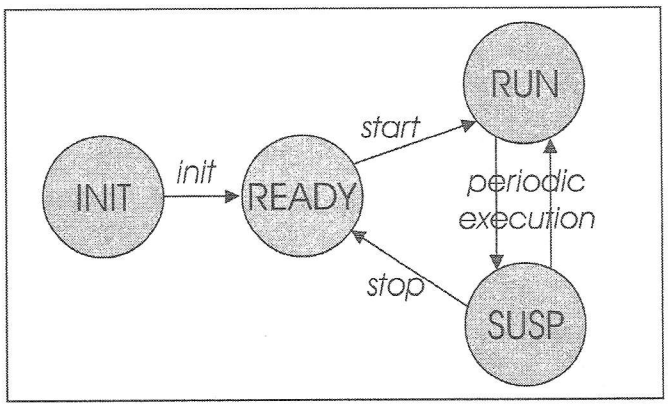

Figure 3. Thread state diagram

Similarly to the `init_module` routine, there is a `cleanup_module` routine, which, when it's called, frees the system resources taken by thread. Both functions are executed after proper shell commands are performed.

4. SCHEDULING

Scheduling in real-time systems concerns the determination of a temporal ordering of tasks allocated to a set of processors within the constraints of some specified timing, precedence and resource requirements.

As far as the process computer is concerned, we used existing priority-based real-time scheduler that comes with the RT Linux. That was the solution that gave more than satisfying results in scheduling the two real-time tasks for communication. We should say only that real-time scheduler is fully preemptive, which provides the ready-to-execute higher priority task to preempt any lower priority task from execution. If there are several tasks ready to execute, the task with the highest priority will be executed.

Much more interesting is the scheduler implemented in process controllers. It is based on modified ADM (adaptive deadline-monotonic) scheduling algorithm, which is the combination of DMS (deadline-monotonic scheduling) algorithm and VBS (value-based scheduling) algorithm. It is modified for the case of having a task with the topmost priority needing to be executed at once.

DMS algorithm is time-based algorithm and under non-overload conditions DMS algorithm schedules all tasks in a timely manner while sustaining optimal processor throughput. During transient overloads, VBS algorithm orders task execution on the basis of the task's value to the system. ADM scheduling algorithm is combination of DMS and VBS algorithm. ADM scheduling algorithm [5],[6] enacting a scheduling-mode change from DMS to VBS algorithm, when active algorithm doesn't give good result.

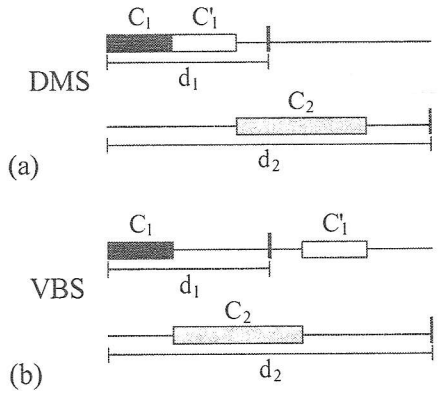

Figure 4. Transient surge not resulting in an overload (a) DMS active algorithm (b) VBS active algorithm

In Figure 4 a transient surge occurs without resulting in system overload. DMS algorithm (a) schedules all tasks in a timely manner. Initiating a mode change (b) to VBS causes degrading performance. We evaluate system performance as the sum of the task performances. If the task completes on time, we add its value to the task's performance, otherwise we subtract it. Therefore, in the first case we have both tasks complete on time, but in the latter case, the first task missed its deadline, which causes the performance degradation.

In Figure 5 a transient surge does cause the system to overload. DMS algorithm (a) causes a high value task to fail while the less valuable task completes on time. VBS algorithm (b) schedules the high value task on time while the less valuable task is delayed.

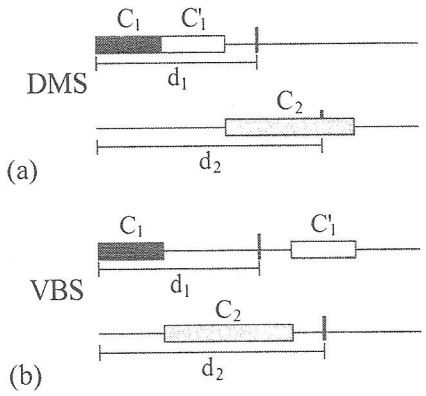

Figure 5: Transient fault resulting in an overload (a) DMS active algorithm (b) VBS active algorithm

If the ADM algorithm detects a transient fault which causes system overload, it has to enact a scheduling-mode change from DMS to VBS algorithm. If the ADM algorithm detects a transient fault which doesn't cause system overload, then DMA algorithm will stay active.

We modify ADM algorithm for the case when a task with the topmost priority, which has the priority to interrupt any other task, appears (Figure 6) [7]. Now, we have one more task, with the highest priority and the shortest time of execution. In Figure 6 the worst case of the highest priority task interrupting the task with the closer deadline is shown. This situation implies ADM algorithm to regard the possibility of the occurrence of such a task, in calculating sliding-window edges and deciding whether the mode should be changed or not.

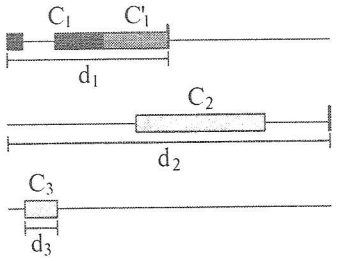

Figure 6. Task with the topmost priority interrupts the task with the closer deadline

Generally, if τ_i is the task its sliding-window size is being computed, and τ_j is the task with the topmost priority, able to preempt any other task from execution. The following algorithm may be used for determining sliding-window edges:

Extent_determination
if (τ_i **or** *fault*$_i$) **and not** τ_j **then**
  if $(t_k - t_{j.n-1}) \leq t_{jmin}$ **then** $LWE = t_{current}$
  else $LWE = t_{current} + C_j$
  endif
else $LWE = t_{current}$
endif
if $(UWE - LWE) < 0$ **then** *mode_change*
endif

First, ADM algorithm determines the upper and lower edge of the sliding-window for τ_i. Then, it is checked whether task τ_i has finished execution or an execution error occurred (fault$_i$), as well as whether the task τ_j was executed or not. If that's true, *LWE* gets the value of $t_{current}$, and then the sliding-window size is computed. Whether the mode should be changed or not is determined upon that size. If the task τ_j was not executed, the time interval between the moment of its last occurrence ($t_{j.n-1}$) and the moment when the time interval of our interest (t_k) ends, is checked (in our case, with two tasks, that's the interval between the moment when the request for execution for both tasks occurs and the d_2 task deadline, which is greater in our case). If this time interval is less then the interval between the two occurrences of the task τ_j (t_{jmin}), then the task τ_j surely won't request execution and *LWE* gets the value of the current time $t_{trenutno}$ and no further correction is made. If this interval is greater then t_{jmin} then the adjustment of the sliding-window edge has to be made by adding the value of C_j (the worst case execution time of the task τ_j). After the determination of the sliding-window edges, sliding-window size is computed, and, upon that value, the decision whether the mode should be changed or not is made.

With this modification, ADM algorithm is adapted for the case of a single asynchronous task, with known worst case execution time, validity for the system, as well as the minimal time interval between its consequent requests for execution.

5. DEVELOPMENT AND DEBUGGING

As mentioned before, there are two major parts of the mentioned cigarette-packing real-time system software: one part resides in PKs, and the other in the process computer.

As far as process computer is concerned development and debugging problems are the main problem of using open source software, like Linux. The constraints imposed on by the particularity of the described application (considerable processing and boot up speed, as well as the fact that the process computer is located in the factory hall and is served by the factory worker) prevented us of using the X Window system and existent integrated development environments (IDE). That's why we used only gcc compiler for development, and gdb line debugger for digging dipper into the core-dump files. However the most common way of debugging was inserting print-statements at certain critical points in the code. That was especially useful for debugging real-time threads, because, there's actually no other way to really debug a real-time task, and not to decrease system performance. The same policy was used for the PK software, therewith their performance was monitored with laptop computer.

The biggest constraint in real-time system debugging is the fact that whatever debugging tool we use to monitor our program, it will inflict the severe system performance decrease. Yet, the performance is actually our basic interest. Therefore, beside the software that analysis timing features of the developed system, a good way of determining whether our real-time task properly performs its functions is the use of print-statements, as mentioned above. In that manner there's no severe performance decrease, and, after all, we have the information accurate enough about the duration of one print-statement.

6. CONCLUSION

In this paper we described some problems concerning task execution that need to be solved, through development and implementation of one typical industrial control and monitoring system,.

For the process computer software environment we have chosen Linux with its real-time extension RT Linux. This choice was imposed by the good features of RT Linux in a sense of minimum interrupt handling and context switch latency, as well as shorter system call execution time. We've shown how allocating real-time and non real-time tasks in different address spaces, provides slow processes not to affect real-time processing. Successful and reliable implementation of the system was provided by widely available Linux and RT Linux documentation.

Scheduling policies were also considered in this paper. For the hierarchically topmost level, the process computer, we use priority based real-time scheduler. That scheduler has also the feature of scheduling periodic tasks. At lower level (the PKs), the modified ADM scheduling algorithm is used. We described the main benefits of ADM scheduling, and also the modification we made in the algorithm. Our modification implies ADM algorithm to regard the possibility of the occurrence of a task with the highest priority, in calculating timing deadlines and deciding whether the mode should be changed or not, and permitting the highest priority task to preempt lower priority task that has the control over processor at that moment. In that manner, the algorithm is enhanced in order to be used for hard real-time control.

At this point we can be sure that open source solutions for embedded and real-time systems will have more and more extensive use in the future. This conclusion is implied by the described features of RT Linux, as well as its lowest possible price - it's free. All this provides development of the applications that are affordable and efficient in the same time. RT Linux is more and more frequently used in industrial appliances, but also in the other fields, like flight simulators, medical instrumentation, embedded communication software, etc.

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MODERN 32-BIT MICROCONTROLLER CHARACTERISTICS AND AUTOMOTIVE APPLICATIONS

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Abstract: *Modern 32-bit microcontrollers get an ever-increasing popularity. In this paper, an overview of currently available microcontrollers is presented. A comparison among architectures and electrical characteristics is made that shows the state-of-the-art solutions and makes easier the selection of the most appropriate microcontroller for the specific application. A case study is given with the guidelines and performance analysis from the point of view of the automotive applications.*

1. INTRODUCTION

The main goal of the microcontroller manufacturers today is to develop a device with high performance, low cost and broad range of possible applications. Latest achievements in multimedia, telecommunications, networking and automotive area emphasised the need for microcontrollers and increased their role in the overall technological progress. Hence, the 32-bit microconrollers have won important and stable position [1, 2]. At the same time, from the user's point of view, the choice of appropriate 32-bit microcontroller has become the question of crucial importance. Wrong choice is usually paid with a lot of time and money. This paper is trying to make this choice easier by providing an application-oriented analysis of the characteristics of available microcontrollers. Section 2 presents the architecture solutions, main features and electrical characteristics of the leading-edge 32-bit microcontrollers, defining the most decisive factors in selecting a microcontroller for the specific application. Some additional microcontroller selection criteria are considered in section 3. Finally, section 4 gives a case study considering the selection of the most appropriate 32-bit microcontroller for a group of automotive applications.

2. ARCHITECTURES END ELECTRICAL CHARACTERISTICS OF 32-BIT MICROCONTROLLERS

Microcontroller's internal structure considers processor core, memory system and connection with the peripheral units [3, 4, 5]. Especially interesting in modern 32-bit microcontroller unit (MCU) design is the peripheral connection. Two basic solutions are possible.

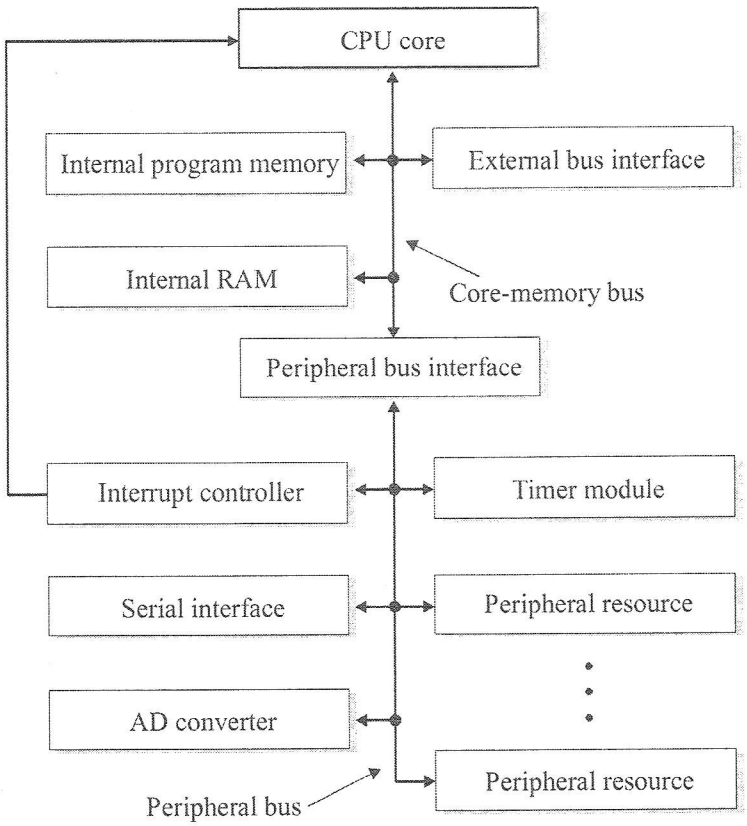

Figure 1: MCU architecture – classical approach

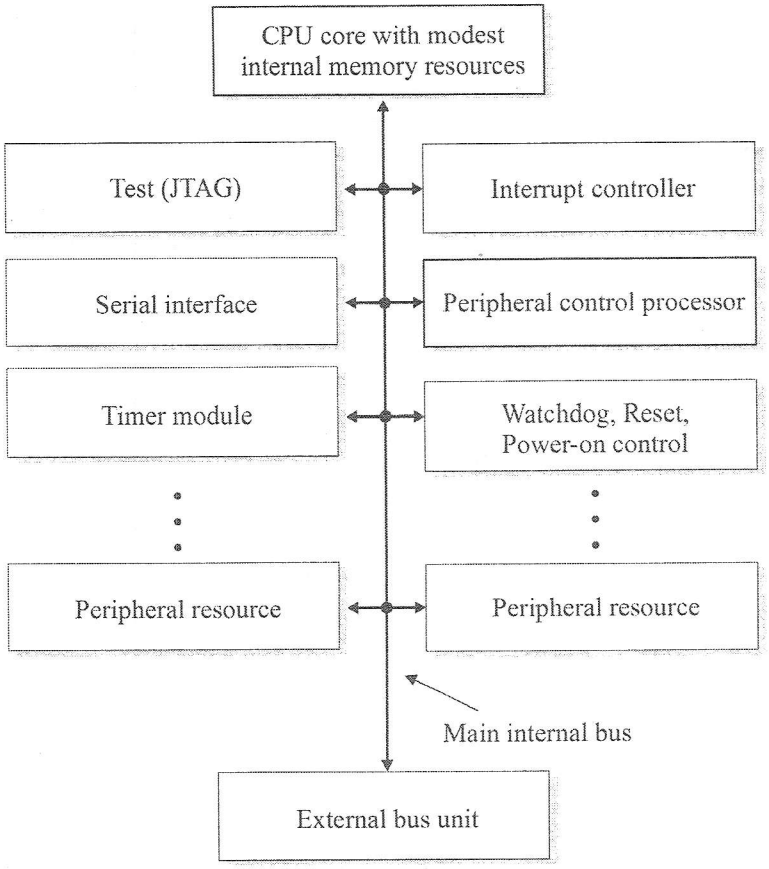

Figure 2: MCU architecture – two-processor solution

The classical approach, presented in Figure 1, is to directly couple the core and the peripherals through internal bus system for the data transfer. These architecture solutions usually include significant internal memory resources, targeting stand-alone applications and resulting in hierarchical bus organisation. Special bus is dedicated to the CPU core and memory system, while the peripheral bus is accessed a through special interface. Exceptionally, the interrupt controller must be able to send the information directly to the CPU. Standard peripheral modules in 32-bit MCUs with classical configuration are: analogue-to-digital (AD) converter, serial interface and timer module. Since the number of peripherals and internal operating frequency are constantly increasing, the main problem of this architecture is configuring of the peripheral bus system in such a way that the bus never gets overloaded.

Another solution is to implement an additional processor to support the peripherals (peripheral control processor). This results in two-processor system shown in Figure 2. Current two-processor solutions do not insist on internal memory capacity but relay on efficient external bus and external memory resources. The main goal is to achieve the highest possible processing speed, so the bus structure is simplified to only one main bus.

While the first solution is straightforward and simple to use, two-processor system is targeting problem of very "busy" I/O modules. Modern applications, especially in networking area, are asking for "intelligent" peripherals, capable of processing more and more data, having more operational power. Implementing hardware solutions is not flexible and cost effective thus leading to the second processor unit. Of course, two-processor system programming can be extremely complex and tricky.

Presented MCU architectures and bus hierarchies must also be reconsidered in the light of their electrical characteristics. The main electrical characteristics from the user's point of view are: available clock frequencies, power supply voltage, power consumption and power saving modes.

In the system clock area, most of the modern solutions go for two oscillators. The main one generates high operating frequency. The other one is much slower and it is used for real-time clock and special low frequency modes. Main oscillator frequency does not have to be very high as it can be multiplied internally by PLL module. In this way, high internal operating frequency is provided without using an expensive oscillator. Usually a number of multiplying modes is offered, making the choice of the desired frequency flexible and power consumption adjusted to real application needs.

Power supply voltage is usually between 3V and 5V. Usually a 5V supply is used for I/O ports, to be compatible with system environment, but supply voltage is internally reduced to 3V for the core and the rest of internal functions.

Power consumption is proportional to the system operating frequency, power supply voltage and to the MCU complexity [6]. As the MCU complexity and operating frequency increase, the question of power saving becomes more important. A number of power saving techniques is commonly used that can be grouped into dynamic and static [7, 8]. In this paper only the techniques concerning the power down modes of the MCU will be discussed since they are under direct user's control. Most of the available MCUs offer two main power-down modes. The first one (power down mode 1 - PD1) disables some chip functions, such as the CPU or some peripherals, while others remain active. It is possible to quickly return from PD1 to normal operation mode (RUN mode). The necessary time interval for this transition is usually denoted as T_{PD1_RUN}. In the second power saving mode (power down mode 2 - PD2) most of the device functions are stopped, which results in efficient power saving. Consequently, the time needed to return to RUN mode (denoted as T_{PD2_RUN}) is much longer. Time periods needed to switch from normal operation to power down modes (denoted as T_{RUN_PD1} and T_{RUN_PD2}) are usually relatively short. The mode change can occur under different conditions, such as: software instructions, interrupts and reset.

In the following an overview of CPU manufacturer offers will be given. For each CPU family the characteristics will be summarised using three tables. In the first table the following electrical characteristics will be given: external oscillator frequency, PLL multiplication modes, power supply voltage and power consumption in normal operation (denoted as P_{RUN}). In the second table the overview of power saving modes will be presented together with the transition times and power consumption in PD1 and PD2. In the third table the advantages and the disadvantages of the MCU family will be listed. The MCU platforms, to be presented, are selected as the top offers of the leading 32-bit MCU manufacturers in 2001 and beginning 2002. Application aspect in popular and fast growing areas of automotive, networking, multimedia and telecommunications is also used as an important selection criteria, i. e. MCU platforms not competitive in these application areas are not considered. Moreover, the attention is concentrated to microcontrollers, microprocessors (leading manufacturer Intel) and DSPs (Digital Signal Processors – leading manufacturer Texas Instruments) are not included in the scope of this paper.

A. Epson's E0C33000

Epson's MCU family E0C33000 has classical architecture with separate address and data bus. Also, special bus lines are dedicated to interrupt request controller. The I/O ports are either bidirectional or unidirectional inputs, but always multifunctional (TTL, CMOS level, eight inputs provide external analogue signals for 8-channel AD conversion), imposing careful initialisation during programming. Most of the peripherals, such as direct memory access (DMA) module, analogue-to-digital converter (ADC), serial interface, timers and real-time clock unit, can generate interrupts with associated routines. Serial communication can be configured as synchronous or asynchronous. Processor clock generator with programmable 8-bit timer can set various communication rates (maximum 3.75MHz in synchronous and 468.75kHz in asynchronous mode). The timer configuration is very flexible. Four different timers are available: watchdog, real-time clock, 8-bit and 16-bit general purpose timer. DMA functionality is divided into two levels: 1) 'high speed DMA' for external source data transfer and 2) 'intelligent DMA' in charge of internal transfers (AD conversion results etc.). A 10-bit ADC and an 8-bit digital-to-analogue converter (DAC) are also standard peripherals in E0C3000 MCU family.

Electrical characteristics of this MCU family are summarised in Table I. Two oscillator option is offered with very high main oscillator frequency of 33MHz, imposing the need for expensive external oscillator if the MCU is supposed to operate at full speed. Some devices are equipped with PLL x2 feature, reaching internal operating frequency of respectable 66MHz. Power supply voltage range and power saving modes are flexible, as shown in Table II. Power consumption values in different operation modes correspond to the MCU complexity.

Table I: Electrical characteristics of the E0C3000 MCU family

Device	Frequency I	Frequency II	PLL	Power Supply Voltage	P_{RUN}
E0C33A104	33MHz	32.768kHz	-	3.3±0.3V; 5±0.5V	400mW(5V,33MHz) 100mW(3V,20MHz)
E0C33208/20 4/202	33MHz	32.768kHz	x2	1.8-3.6V (internal); 1.8-5.5V (I/O)	215mW (3.3V, 50MHz)

An overview of the most interesting features of this MCU family is given in Table III. E0C3000 offers efficient standard peripheral functionalities, without special modules dedicated to modern application areas such as networking and automotive. This approach narrows its application spectrum, but provides high operation speed, very competitive price and simplicity of use. Input ports, equipped with flexible options, make this MCU family especially attractive for so called "keyboard matrix" applications.

Table II: Power saving modes in E0C3000

E0C33A104, E0C33208/204/202	
Condition RUN→PD1	Software instruction
T_{RUN_PD1}	Few cycles
Condition PD1→RUN	Interrupt
T_{PD1_RUN}	Few cycles
P_{PD1}	200mW(5V,33MHz) 40mW(3V, 20MHz)
Condition RUN→PD2	Software instruction
T_{RUN_PD2}	Few cycles
Condition PD2→RUN	Interrupt, real-time clock timer
T_{PD2_RUN}	
P_{PD2}	5μW(5V), 4μW(3V)

Table III: E0C3000 Feature Highlights

Advantages	Disadvantages
• Additional DMA dedicated to ADC • Flexible ports • Standard resources present • High internal operating frequency	• Lack of special resources (CAN, …) • Need for expensive main oscillator

B. Fujitsu's MB91360

Fujitsu's MB91360 [9] is also one-processor family, but with wide module spectrum, forcing the need for very careful structuring and more hierarchy levels. The first functional level contains processor core area that provides for direct connection among CPU, clock control unit, instruction cache, watchdog timer and user RAM. A 32-bit bus converter connects the second functional level. This level includes fast internal RAM, 5-channel DMA and so-called external bus interface. External bus interface provides the connection to external memory blocks and also to on-chip flash memory and controller area network (CAN) bus. The third functional level is connected through a bus adapter and 16-bit resource bus, containing external interrupt controller, units for serial communication standards (synchronous, asynchronous, I^2C-Inter Integrated Circuit bus), 10-bit ADC, 10-bit DAC, pulse programmable generator, sound generator, variety of timers (real-time clock, 16-bit free-run timer with input capture and output compare functions), step motor controller and clock modulator.

The electrical characteristics of the MB91360 MCU family are shown in Table IV. Very high PLL frequency multiplying factor if available, but maximal internal operating clock frequency of 12x4=48MHz does not recommend this MCU family for very high speed applications. P_{RUN} is high as a result of the MCU complexity. Power-down modes are offered, as shown in Table V, with the option to have PD1 mode with active sub-clock (32.768kHz) and thus low P_{PD1}.

Table V: Power saving modes in MB91360

MB91V360/MB91F361	
Condition RUN→PD1	Software instruction
T_{RUN_PD1}	Few cycles
Condition PD1→RUN	Interrupt
T_{PD1_RUN}	Few cycles
P_{PD1}	2.5mW (32.768kHz)
Condition RUN→PD2	Software instruction
T_{RUN_PD2}	Few μs
Condition PD2→RUN	External interrupt, reset
T_{PD2_RUN}	Few ms
P_{PD2}	1mW

Table VI summarises the main features of the MB91360 MCU family. It is very complex MCU family targeting wide range of applications. Its implementation strategy aims at function quantity while the quality level is still satisfying. MB91360 is best suited for automotive and industrial applications.

Table IV: Electrical characteristics of the MB91360 MCU family

Device	Frequency I	Frequency II	PLL	Power Supply Voltage	P_{RUN}
MB91V360/MB 91F361	4MHz	32.768kHz	x12	5+0.25/-0.75V	1250mW(5V,48MHz)

Table VI: MB91360 Feature Highlights

Advantages	Disadvantages
• High memory capacity • Low frequency external oscillator with PLL x12 option • Standard resources present • Special resources offered (CAN, step motor controller, flash memory, clock modulator)	• Power consumption is high • Internal operating frequency is modest

C. Hitachi's SHx

Main characteristic of Hitachi's SHx family [10] is very complex architecture enabling as much as possible parallel processing in an one-processor environment. To make the load on particular buses lower and to avoid timing problems due to unfortunate device floorplan, a multiple bus system is used. With a skilful programming these buses can be used in parallel for different processing tasks. Especially interesting is the bus directly connecting some peripherals (ADC, DAC, serial communication modules) with the DMA unit. Using this bus the data transfer can be performed without involving the CPU. To provide this kind of MCU organisation the processor core is directly connected only with the cache controller and memory management unit. Therefore, the processor accesses the rest of the functional modules only through these two modules.

Table VII: Electrical characteristics of the SHx MCU family

Device	Frequency I	Frequency II	PLL	Max. Internal freq.	Power Supply Voltage	P_{RUN}
SH7040	4-10MHz	-	x1...x4	33MHz	3.3±0.3V; 5±0.25V	900mW(5V,33MHz) 264mW(3.3V,16.7MHz)
SH7709A	20-66.7MHz 20-66MHz	32.768kHz	x1...x6 x1...x4	133MHz (Core)	3.3±0.3V (I/O); 1.8±0.25V(Core till 100MHz); 1.9±0.15V(Core till 133MHz)	270mW (100MHz), 400mW(133MHz) for Core; 66mW for I/O system with bus clock 33MHz
SH7750	9-66MHz	32.768kHz	x1...x6	200MHz (Core)	3.3±0.3V (I/O); 1.5-1.95V (for 128-200MHz)	2500mW (200MHz)

The advantages of the sophisticated architecture are carefully exploited in the domain of electrical characteristics of the SH7709A and SH7750 devices (see Table VII). Three main clock nets control the MCUs: core, peripheral and bus-operation clock, that are in case of SH7709A generated by two external oscillators and two PLL modules. In this way, core frequency can be increased up to 200MHz (SH7750), providing for extremely high data processing power. In order to decrease power consumption, power supply voltage is lowered for the core. Power saving modes are also offered in every device of the family, as shown in Table VIII.

To conclude, Hitachi offers an efficient environment for the users ready to cope with complex programming challenges. SHx MCU family, skilfully implemented, targets applications with extensive use of peripherals and high data processing power, especially in telecommunication area.

Table VIII: Power saving modes in SHx devices

	SH7040	SH7709A	SH7750
Condition RUN→PD1	Software instruction	Software instruction	Software instruction
T_{RUN_PD1}	Few cycles	Few cycles	Few cycles
Condition PD1→RUN	Interrupt, DMA error	Interrupt, DMA error	Interrupt, DMA error
T_{PD1_RUN}	Few cycles	Few cycles	Few cycles
P_{PD1}	800mW(5V,33MHz) 230mW(3.3V,16.7MHz)	445mW(1.9V,133MHz)	450mW(1.95V,200MHz)
Condition RUN→PD2	Software instruction	Software instruction	Software instruction
T_{RUN_PD2}	Few cycles	Few cycles	Few cycles
Condition PD2→RUN	Special interrupt, reset	Special interrupt, reset	Special interrupt, reset
T_{PD2_RUN}	Few ms	Few ms	Few ms
P_{PD2}	100μW maximum	300μW maximum	12μW maximum

Table IX: SHx Feature Highlights

Advantages	Disadvantages
• Sophisticated architecture • Very high internal operating frequency • Standard resources present	• Lack of special resources (CAN, flash memory, ...)

D. Infineon's TriCore

Infineon's TriCore MCU has two-processor architecture. Besides the main processor (CPU), a peripheral control processor (PCP) is included. PCP is activated through interrupt requests and can execute small programs in parallel. In this way I/O operations are not restricted to DMA transfer and are not CPU-dependent, but fast and equipped with data processing power. A drawback is that PCP must always be handled through interrupt request system that takes care of the interrupt prioritisation. Hence, the real efficiency is highly dependent on complex programming techniques. Bus structure is simple to make programming a bit easier. Standard peripherals are also included, such as serial and parallel communication modules and flexible timer configuration.

The electrical characteristics of the TriCore MCU family are presented in Table X. Two external high frequency oscillators are needed in order to have flexible clocking scheme and maximally exploit two-processor architecture advantages. Frequency I can be multiplied by PLL, while frequency II is input of the clock divider. The family also offers power-down modes with low power consumption values, as shown in Table XI.

TriCore MCU architecture is usually the best choice for complex and yet extremely fast networking applications, due to processing parallelism supported by powerful operating frequency scheme. The advantages and disadvantages of this MCU family are summarized in Table XII.

Table X: Electrical characteristics of the TriCore MCU family

Device	Frequency I	Frequency II	PLL	Max. Internal freq.	Power Supply Voltage	P_{RUN}
TC10GP	10-25MHz	max. 40MHz	x8...x15	66MHz	3.3±0.3V(I/O); 2.5±0.25V(Core)	750mW (66MHz)

Table XI: Power saving modes in TriCore

TC10GP	
Condition RUN→PD1	Software instruction
T_{RUN_PD1}	Few cycles
Condition PD1→RUN	Interrupt, watchdog
T_{PD1_RUN}	Few cycles
P_{PD1}	380mW (66MHz)
Condition RUN→PD2	Software instruction
T_{RUN_PD2}	Few cycles
Condition PD2→RUN	Special interrupt, reset
T_{PD2_RUN}	Few ms
P_{PD2}	42μW

Table XII: TriCore Feature Highlights

Advantages	Disadvantages
• Two-processor architecture • Flexible frequency scheme to support parallel processing • Standard resources present	• Lack of special resources (CAN, ...) • Complex programming

E. Mitsubishi's M32R

The main advantage of Mitsubishi's M32R family is large on-chip memory. On-board high capacity flash memory is available. Internal RAM integrates real-time debugging interface. The bus concept has two levels. First level is connecting memory system with MCU core through a 32-bit bus, while the rest of the peripherals (second level) are coupled with 16-bit bus. Peripheral units target a wide range of applications. The modules included are: 10-channel DMA controller, two 10-bit AD converters, six serial communication channels, interrupt request controller, CAN module, flexible timer configuration.

Electrical characteristics shown in Table XIII are modest except for low P_{RUN}. There are no power saving modes. Still, CAN module and high capacity flash memory favour M32R MCU for robust automotive applications without strict speed constraints, since peripheral operating frequency is limited to as low as 20MHz. The advantages and disadvantages of this MCU family are summarized in Table XIV.

Table XIII: Electrical characteristics of the M32R MCU family

Device	Frequency I	Frequency II	PLL	Max. Internal freq.	Power Supply Voltage	P_{RUN}
M32170	5-10MHz	-	x4	40MHz(Core); 20MHz(Peripherals)	5±0.5V(I/O); 3.3±0.3V(internal)	250mW (40MHz)

Table XIV: M32R Feature Highlights

Advantages	Disadvantages
• High memory capacity • Standard resources present • Special resources offered (CAN, flash memory) • Low P_{RUN}	• Low operating frequency • No power saving modes

F. Motorola's M-Core

Motorola's M-Core MCU is another two level bus system controlled by one processor. This configuration is very popular because it enables simple data access and processing with acceptable speed (bus load is not critical). Core bus connects the CPU, internal flash memory, RAM and external bus interface, while the peripheral bus supports serial communication protocols, ADC, thoroughly developed timer configuration and interrupt controller. A special characteristic of M-Core is extremely flexible interrupt handling. The interrupt controller processes 40 potential interrupt sources with as much as 32 priority levels. From that point of view, M-Core is highly user-oriented. However, some application specific peripherals, like CAN module, are missing.

The electrical characteristics are given in Table XV. Available power saving modes are shown in Table XVI. Pros and cons are summarized in Table XVII. Low speed, low power consumption and powerful user-oriented programming environment make M-Core MCU family one of the most popular in consumer electronic applications.

Table XV: Electrical characteristics of the M-Core MCU family

Device	Frequency I	Frequency II	PLL	Max. Internal freq.	Power Supply Voltage	P_{RUN}
MMC2107	2-10MHz	-	x1...x9	33MHz	2.7-3.6V	max. 660mW

Table XVI: Power saving modes in M-Core

MMC2107	
Condition RUN→PD1	Software instruction
T_{RUN_PD1}	Few cycles
Condition PD1→RUN	Interrupt, reset
T_{PD1_RUN}	Few cycles
P_{PD1}	250mW (33MHz)
Condition RUN→PD2	Software instruction
T_{RUN_PD2}	Few cycles
Condition PD2→RUN	Interrupt, reset
T_{PD2_RUN}	Few ms
P_{PD2}	330μW

Table XVII: M-Core Feature Highlights

Advantages	Disadvantages
• User-oriented programming style • Low P_{RUN} • Standard resources present • Flexible interrupt handling	• Lack of special resources (CAN, flash memory, ...) • Low operating speed

G. NEC's V850

An interesting feature of the NEC's V850 MCU family is that a lot of modules are coupled over one main bus. V850 offers as much as 123 digital I/O ports, 8 analogue inputs for 10-bit ADC, DMA, serial communication protocols, timers, RAM, on-chip flash or mask ROM and very flexible interrupt controller for 25 external interrupt sources. This is an easily programmable, user-friendly MCU family. However, the price for one-bus architecture is paid in speed. Some modern peripherals such as CAN and Pulse

Width Modulation (PWM) modules are also available in specific devices of V850 family, targeting low-speed automotive and industrial applications.

Table XVIII: Electrical characteristics of the V850 MCU family

Device	Frequency I	Frequency II	PLL	Power Supply Voltage	P_{RUN}
V850/SA1	1-20MHz	32.768kHz	-	3.3±0.3V (2.7V till 17MHz)	66mW(3.3V,20MHz)
V850/SB1	2-20MHz	32.768kHz	-	4.75±0.75V	125mW (5V,20MHz), 166mW(with Flash memory)
V853	3.3-6.6MHz	32.768kHz	x1...x5	5±0.5V	365mW (5V,33MHz)

Table XIX: Power saving modes in V850 devices

	V850/SA1	V853
Condition RUN→PD1	Software instruction	Software instruction
T_{RUN_PD1}	Few cycles	Few cycles
Condition PD1→RUN	Interrupt, reset	Interrupt, reset
T_{PD1_RUN}	Few cycles	Few cycles
P_{PD1}	30mW (20MHz)	250mW (33MHz)
Condition RUN→PD2	Software instruction	Software instruction
T_{RUN_PD2}	Few cycles	Few cycles
Condition PD2→RUN	Interrupt, reset	Interrupt
T_{PD2_RUN}	Few ms	Few ms
P_{PD2}	25μW; 3.3μW without sub-clock	10μW

The electrical characteristics shown in Table XVIII are very modest due to the architecture simplicity. Power saving mode options are described in Table XIX. The pros and cons are summarized in Table XX. This family is an ideal choice if the functionality spectrum is more important then speed.

Table XX: V850 Feature Highlights

Advantages	Disadvantages
• Easy programmable • Wide resource spectrum (CAN, flash memory, ...) and high resource capacity	• Low speed, constrained by simple architecture

H. Toshiba's TX39

Toshiba's TX39 MCU family uses three level bus concept. The first level consists of the processor core, exception coprocessor and cache memory that are tightly connected together over the local bus. The second level bus, known as G-bus, is in charge of interrupt request controller and DMA unit, while other peripherals are coupled on third bus level. TX39 provides synchronous dynamic RAM. Besides standard peripheral modules, some interesting application oriented modules are offered: liquid crystal display (LCD) support and infrared module. This is a general-purpose MCU architecture equipped with some additional and unusual functions.

Table XXI: Electrical characteristics of the TX39 MCU family

Device	Frequency I	Frequency II	PLL	Max. Internal freq.	Power Supply Voltage	P_{RUN}
TMPR3911	9.216MHz	32.768kHz	x4	36.8MHz	3.3±0.3V	165mW(9.216MHz)
TMPR3912	11.52MHz	32.768kHz	x8	92.16MHz	3.3±0.3V	900mW (10MHz)
TMPR3927	8.33MHz 66.67MHz	-	x16 x2	133MHz 133MHz	3.3±0.3V(I/O); 2.5±0.2V(inter.)	1050mW (133MHz)

TX39 is highly competitive MCU family in high speed networking application area due to its extremely good electrical characteristics (Table XXI), but it should also be seriously taken into consideration for specific industrial applications requiring LCD driver or infrared modules. Power saving modes are also available, as shown in Table XXII. Advantages and disadvantages are summarized in Table XXIII. The column with disadvantages is left empty, since TX39 family represents a good balance between quantity and quality.

Table XXII: Power saving modes in TX39

TMPR3911/3912	
Condition RUN→PD1	Software instruction
T_{RUN_PD1}	Few cycles
Condition PD1→RUN	Interrupt
T_{PD1_RUN}	Few cycles
P_{PD1}	130mW (10MHz)
Condition RUN→PD2	Hardware, signal
T_{RUN_PD2}	Few ms
Condition PD2→RUN	Switch, real-time clock timer
T_{PD2_RUN}	Few ms
P_{PD2}	66μW

Table XXIII: TX39 Feature Highlights

Advantages	Disadvantages
• Good electrical characteristics • Some specific resources (LCD, infrared module) • Standard resources present	

H. ARM and Samsung's S3C2400X

ARM (Advanced RISC Machine) is the name frequently found in the MCU world. The company behind this name does not produce microcontrollers, but sales the know-how to design the stable and efficient MCU core. ARM offers following: synthesised MCU core in certain technologies, MCU core ready for synthesis (VHDL/Verilog codes), macrocells (microprocessor, Memory Management Unit (MMU), cache) and some peripheral modules. ARM MCU core includes efficient RISC CPU supported by two separate cache modules, one for data and other for instructions, both controlled by MMU. If needed, floating-point co-processor can be implemented to increase additionally CPU performance. Furtheron, ETM (Embedded Trace Macrocell interface) is supported, providing simple and efficient debugging environment. Internal bus interface is adjusted to Harvard architecture, i.e. address and data buses are separated. As peripheral resource spectrum, ARM offers RTL (Register Transfer Level) codes and appropriate documentation of following modules: UART, synchronous serial interface, general purpose I/O, real-time clock, keyboard and mouse interface.

Table XXIV: Electrical characteristics of the S3C2400X

Device	Frequency I	Frequency II	PLL	Max. Internal freq.	Power Supply Voltage	P_{RUN}
S3C2400X	10-20MHz	32.768kHz	x8	150MHz	1.8±0.15V (internal) 3.3±0.3V (I/O)	-

There are many ARM partners producing MCUs based on ARM core. Even though the core is extremely efficient and fast (200MHz operation frequency in 0.18μm technology), the real application value can be estimated only by analysing complete MCU.

The best example of ARM based MCU is Samsung's S3C2400X. Table XXIV shows electrical characteristics, but the data for power consumption are missing (not officially published by Samsung). Power saving modes are well structured (Table XXV), besides normal operation mode with active PLL (RUN), there is, so called, SLOW mode (PLL is off and machine clock is directly generated from the external clock).

ARM based S3C2400X is targeting high speed and data processing demanding applications, like high speed networking and telecommunications.

Table XXV: Power saving modes in S3C2400X

TMPR3911/3912	
Condition RUN→SLOW	Software instruction
Condition SLOW→RUN	Software instruction
Condition RUN/SLOW→PD1	Software instruction
T_{RUN_PD1}	Few cycles
Condition PD1→RUN	Interrupt, real-time clock

T_{PD1_RUN}	Few cycles
P_{PD1}	-
Condition RUN→PD2	Software instruction
T_{RUN_PD2}	Few ms
Condition PD2→RUN	Interrupt, real-time clock
T_{PD2_RUN}	Few ms
P_{PD2}	5μW

Table XXVI: S3C2400X Feature Highlights

Advantages	Disadvantages
• High speed • Efficient CPU core • Standard resources present	• No special resources

3. OTHER MCU SELECTION CRITERIA

Besides already mentioned MCU features, some other criteria must be considered before a suitable MCU for a specific application is selected. For example, the price of the MCU is very important factor. Selecting complex, fast, flexible and expensive MCU is not a good choice if only 50% of its resources will actually be used. Also, insisting on cheap MCU even though the needs are complex can be very time consuming and still result in an inefficient final solution.

Following issues should be analysed as well: implemented memory system and memory capacity, available interrupt sources and interrupt managing, stack configuration. Modern MCU solutions are very powerful in these areas. Therefore the user's task actually is to check the device offers within a specific family.

Eventually, it must not be forgotten that the MCU should be programmed and efficiently employed in an electronic system. The user has to consider the programming and development tools supporting the MCU family and the implemented CPU command set. In general, a programmable system is only as good as its development environment. The absolute minimum is an assembler, but without a C-compiler the environment cannot be considered as serious [11]. Most of the mentioned MCU manufacturers offer the C++ support. Recently, Java gets more and more popularity in the world of embedded systems programming [12]. Among the MCU families described in section 2, NEC, Infineon, ARM and Mitsubishi support Java programming environment.

Besides high level programming language support, debugging tools should also be seriously considered. Since the debugging in modern multi-tasking systems is extremely complex, almost an art, the user must be well equipped. In the best case, debugging tools are organized in an integrated environment with debugger, simulator, performance analyser, emulator, logic analyser and evaluation board.

An overview of supported tools for the MCU platforms presented in section 2 is given in table XXVII.

Implemented command set and CPU efficiency are also very important from the application aspect. One application is usually designed in high-level programming language, like C. C-compiler translates the design into machine code, thus determining directly the final program efficiency. Depending on compiler quality, available CPU command set and addressing flexibility, the same C-program can result in significantly different number of machine instructions. Even though the modern 32-bit CPUs are all fast RISC machines, the average CPI (Clocks Per Instruction) can also differ. To conclude, the real MCU speed, often referred to as MIPS (Million Instructions Per Second) number, is result of three factors: operating frequency, average CPI and adjustment between supported compiler and CPU command set. While the operating frequency is defined, other two factors can not be determined accurately and they are often estimated through the execution of different testbench programs. Still, there are no generally accepted testbenches, mostly because the manufacturers optimise CPU core and command set having in mind the primary target application area. Thus, the same MCU can show extremely high efficiency in one testbench class and low performance executing a testbench in other application area. That is why some manufacturers do not officially provide MIPS numbers for their products. However, here are some manufacturer's estimations:

- Toshiba TX39 - 97MIPS @ 92MHz;
- Fujitsu MB91360 - 25MIPS @ 33MHz without cache;
- NEC V853 - 60MIPS @ 33MHz.

Table XXVII: Tools supported by presented MCU platforms

	Compilers	Development and debugging	Logic analysers	Evaluation boards	Emulators	Operating systems
Epson	C	Disassembler, Debug Monitor, Make		Epson	Epson	ROS33 (Epson)
Fujitsu	C	Fujitsu Simulator/Debugger Softune Workbench		Fujitsu (MB91101, MB91361)	Fujitsu MB2197	OSEK (Fujitsu), REALOS, Euros
Hitachi	C	Debugger: GNU, Hitachi Simulator: Hitachi Embedded Workshop, Green Hills		Hitachi EVB and EVX	Hitachi E6000	Nucleus+, Microsoft Windows CE, Linux, QNX, OS-9, PSOS
Infineon	C, C++, Java	Debugger: Wind River, Green Hills, High Tec, Ashling, Tasking, Hitex Simulator: I-Logic, Green Hills, Lauterbach	dli	SK-TC10GP, STK10GP, STK1775	Ashling, Hitex, Lauterbach, Signum Systems	EUROSplus, OSEKWorks, Nucleus+, ERCOSEK, Rubus OS
Mitsubishi	C, C++, Java	Debugger: PD32R, KD32, PD32RSIM Simulator: PD32RSIM		MSA2114	M32x100T-SDI-E	Mitsubishi MR32R, ERCOSEK, OSEKWorks, osCAN
Motorola	C, C++	Debugger: Wind River, Green Hills, Tasking, iSystem, Lauterbach Simulator: Wind River, Green Hills, Tasking, Metrowerks Performance Analyser: Wind River, Green Hills	dli, Agilent, Tektronix	Motorola, Axiom, emWare	Lauterbach	Nucleus+, AMX, Integrity
NEC	C, C++, Java	Debugger: ATI, DIAB-SDS, Green Hills, IAR System, Lauterbach Simulator: Green Hills	dli, Tektronix	NEC StartWare	NEC N-Wire, Lauterbach, Ashling, Corelis	Nucleus+, Enea OSE, Wind River, ETAS, Integrated Systems, Segger, Vector
Toshiba	C, C++	Debugger: Green Hills, GNU Simulator: Green Hills		Pallas, Juno	Agilent	Microsoft Windows CE, Linux, Wind River, Enea OS, Integrated Systems
ARM	C, C++, Java	Debugger: Lauterbach, Wind River Simulator: Wind River	Agilent, Tektronix	ARM Developer Kit	ARM Multi-ICE, Lauterbach	Microsoft Windows CE, EPOC32, EUROS, OSE RTOS

4. A CASE STUDY: AUTOMOTIVE APPLICATIONS

Last decade set the automotive applications as one of the most challenging and advancing MCU application areas [13]. Steady growth in number of MCUs in a car, presented in Figure 3, is driven by consumer demands for enhanced safety features, entertainment systems and additional convenience functions. It is estimated, for instance, that a better middle range car has sixty to seventy independent microcontrollers working in it. The situation is even more drastic in some top models. Furthermore, systems that are first introduced on luxury car-models eventually migrate down to lower priced cars, as their costs are reduced.

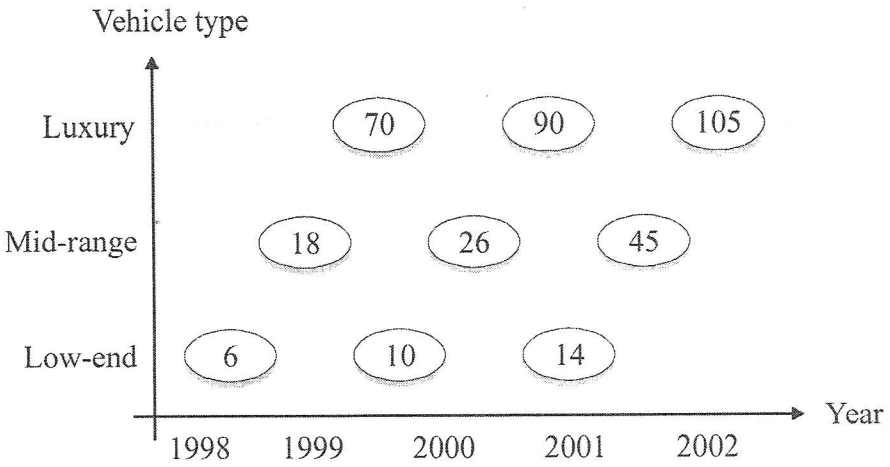

Figure 3: Average number of MCU controlled electronic systems inside a car during the latest years

Not only that the number of automotive MCU applications grows, but also most of the current electronic systems are being enhanced and expanded. Let us consider airbag systems. It is common today that every low-end car has two frontal airbags, but in more expansive cars there are several sidebags, rear passenger airbags, further frontal airbags for knees etc. Similarly, braking, steering, suspension and other body control functions are further improoved and developed to increase the safety. The most popular newly introduced electronic systems are GPS (Global Positioning System) – based navigation systems, stability management systems, 'by-wire' braking and steering, collision warning and avoidance, voice recognition, internet access, night vision enhancement.

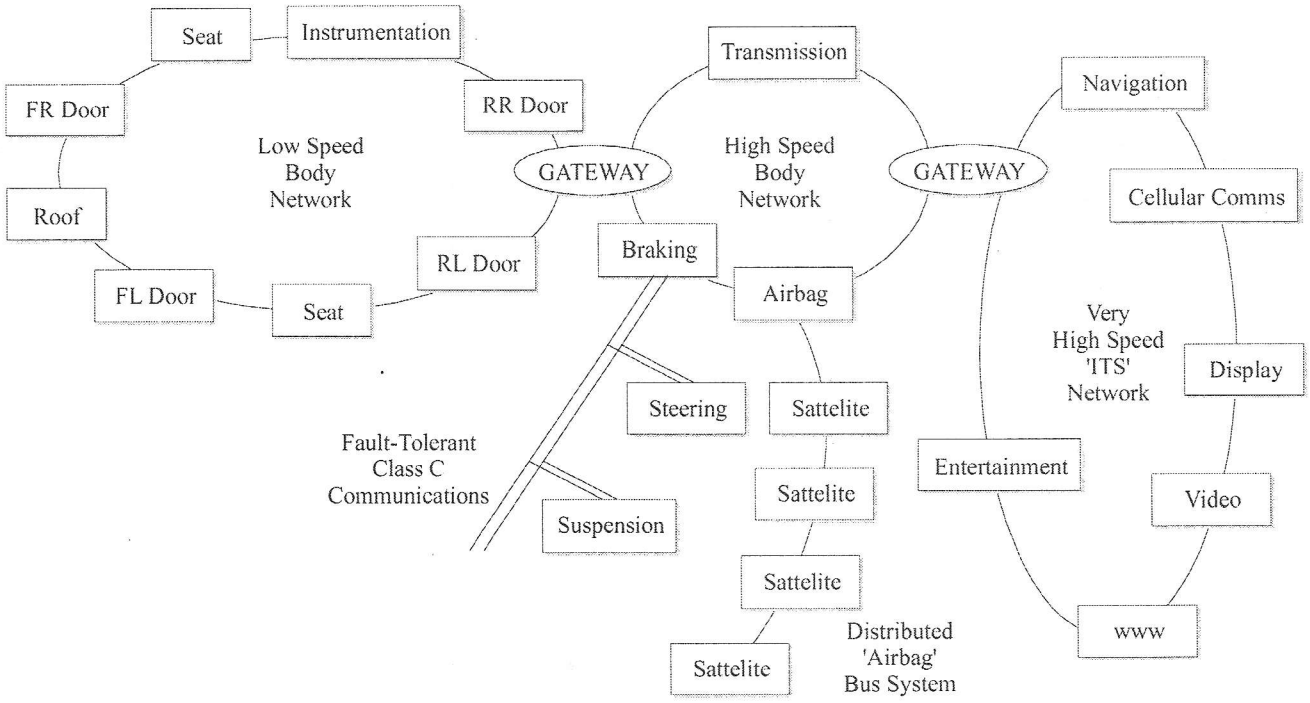

Figure 4: MCU automotive applications

Figure 4 summarises the automotive application area. Its main characteristic is networking of electronic systems. The sub-systems must share data in real-time manner and thus perform control in a more intelligent way. The best example for networking benefit is the coordination of the data generated by the braking, steering and suspension systems. Also, the technique of 'second guessing' becomes possible. It is a practice to use data from one system as a back-up for the other system under certain conditions. Thus, the wheel speed and vehicle direction information, already used in a stability management system, could be used to back-up the navigation system, especially if the GPS signal is lost.

Five distinct main communication systems are usually implemented, as shown in Figure 4. Very high speed network is in charge of processing of the external signals and requires high processing power. Body electronics is distributed in two networks according to speed requirements. Critical safety control functions (braking, steering, suspension) are grouped on a redundant network in order to meet fault tolerance criteria. Thus, only safety critical information is allowed on

these buses. Due to becoming more and more robust, the airbag system is usually implemented as an independent network. Between the networks there are 'gateways' to share information across the boundaries when necessary.

In order to cope with mentioned trends and requirements in automotive area, a MCU must be scanned through several criteria. These criteria are discussed in the following.

A. Data Processing Speed

The increasing complexity of automotive electronic systems imposed the need to process the inputs from many sensors and communication systems and to perform real-time control of many actuators. It is roughly estimated comparing last three generations of automotive MCUs that data processing power for corresponding applications has increased 100 times.

The low speed body network is still a 16-bit MCU application area. The reasons for this are obvious. The applications are not safety critical, they require relatively simple algorithms, communication within the network is not very intense, while the difference between the prices of a 16-bit and a 32-bit MCU is still significant.

Other four application networks in Figure 4 require 32-bit MCUs with RISC processors. RISC CPU is desired due to higher performance then in CISC units. Instead of using microcode to decode instructions, RISC instructions are hardwired and thus faster.

Efficient CPU is not enough for very high speed automotive network. Navigation systems with fast map search capability and video distribution systems impose the need for high operating frequency. The best candidates for these applications are Hitachi's SH7709A (core is operating on 133MHz, see Table VII) and SH7750 (200MHz, see Table VII) and Toshiba's TMPR3912 (92.16MHz, see Table XXI) and TMPR3927 (133MHz, see Table XXI). Other presented MCU families are simply too slow.

B. Memory Requirements and Trends

As the algorithm complexity grows, the program memory capacity drastically increases. Comparing corresponding applications in high speed body network over last three MCU generations, program memory is today 40 times bigger. It should be added that most of the automotive applications are "compact". Usually a stand-alone MCU is needed without use of external memory resources.

The memory capacity is not the only important factor. As flash ROM becomes ever more cost effective and is offering the possibility of on-board reprogramming, this memory type is becoming a must. The automobile manufacturers often need to revise the software in the field. Removing and replacing a sealed MCU is time consuming, expensive and very inconvenient for the car owner. Moreover, the software upgrades are very practical and popular today. Some attractive features can be easily implemented in software, for example adjusting side view mirrors to point to the rear wheels when the vehicle is placed in reverse gear.

High capacity flash ROM is offered in Fujitsu's MB91360, Mitsubishi's M32R and NEC's V850 MCU families (see Tables VI, XIV, XX). Fujitsu's flash ROMs seem to be the most advanced, providing fast 32-bit data transfer, simultaneous read, write and erase functions (of course, different memory sectors must be addressed) and minimum 10000 times reliable reprogramming.

C. Efficient Communication

As already mentioned, communication among the MCU systems is a growing trend. Real-time data sharing directly results in reducing interconnections, costs and complexity. That is why modern automotive MCU must dedicate respectable silicon area to communication protocol modules. The most important is CAN bus interface [14] that is specially developed and designed to efficiently join the electronics control with the vehicle mechanics. CAN bus protocol is almost a standard for the body network applications. Other standard synchronous and asynchronous communication protocols are also highly desirable.

While the standard communication protocols are implemented in all presented MCU families, CAN is offered only in Fujitsu's MB91360, Mitsubishi's M32R and NEC's V850 MCU families (see Tables VI, XIV, XX).

D. Power Consumption

Until recently, low power consumption was not automotive primary requirement. This is changing as the number of systems required to operate when the ignition is off grows. Battery-life of these systems would be very short, unless special care is taken of power consumption.

The door modules are good example. The MCU must permanently be in a 'ready' mode in order to recognize a signal from a remote controller. To solve this kind of situation power saving modes are introduced as described in chapter 2 [6, 7, 8, 15]. Power saving modes are implemented in all presented MCU families (see Tables II, V, VIII, XI, XVII, XX and XII), except in Mitsubishi's M32R (see Table XIV). M32R relies on low P_{RUN} (see Table XIII), but lack of power-down modes still excludes this family from some automotive applications like door modules.

Also, the airbag MCU needs to function in a crash situation, even if the electrical power supply for the MCU is disconnected. For this feature, a large capacitor is usually connected to dedicated MCU pin (output of internal voltage regulator). This capacitor stores enough energy to fire the airbag system. This feature is offered in all MCU families targeting automotive body applications, such as Fujitsu's MB91360, Mitsubishi's M32R and NEC's V850.

E. Electromagnetic Emission

Electromagnetic interference (EMI) becomes a major problem, ever more important with the increasing number of in-car electronic systems, since the probability that the systems will interfere with each other grows. The leading car manufacturers are nowadays setting extremely stringent EMI standards on the equipment they install, in the form of electromagnetic emission thresholds that must not be

exceeded. Today, this problem cannot be left just to the automotive electronic system manufacturers, but must be shared by their silicon supplier [16].

That is the reason why Fujitsu's MB91360 MCU family offers clock modulator module (see Table VI). It is based on randomly varying the clock frequency of the microcontroller for a small amount. A random number generator defines a new clock frequency at every clock cycle. The result is smoothing out of the electromagnetic emission generated by the MCU, through spreading the energy more evenly across the spectrum. This eliminates electromagnetic emission peaks that are above the critical thresholds. Described task is very challenging considering that CPU systems usually require stable clock frequency, since many blocks are designed assuming stable input clock.

F. Safety Critical Operation

Special communication network is dedicated to safety critical control functions (braking, steering, suspension), as shown in Figure 4. Safety critical systems must be fault-tolerant. They need not only recognize that an electrical fault has occurred, but must continue to operate safely in the presence of the fault. Usually the CPU, as the main supervisor, validates other system components by continual testing, but the CPU must be controlled too. A commonly used solution is the second, redundant CPU that checks the operation of the main CPU. The redundant CPU can be another standalone MCU, which is expensive, or carefully programmed second CPU on the same MCU (feature implemented in Infineon TriCore family, as mentioned in Table XII).

G. MCU Selection

Having this all in mind, the most suited 32-bit MCU families for different automotive applications can be proposed as follows.

- Low speed body network applications

This is a 16-bit MCU application area, which is out of the scope of this paper.

- High speed body network, distributed airbag bus system and safety critical network

Fujitsu's MB91360, Mitsubishi's M32R and NEC's V850 MCU families offer CAN interface coupled with high on-chip memory capacity and flash ROM, imposing themselves as the most serious candidates. Fujitsu offers the highest quality flash ROM.

Regarding data processing speed and power management, the competition among the three candidates is more interesting. Fujitsu's MB91360 provides the highest operating frequency. Internal frequency of 48MHz is obtained with a cheep 4MHz external oscillator (see Table IV). Flexible power saving modes are also available, but P_{RUN} value is relatively high.

Mitsubishi's M32R can also operate on high internal speed (40MHz), but it requires more expensive 10MHz external oscillator (see Table XIII). Also, its peripheral modules can operate on frequencies of up to 20MHz only. There are no power saving modes offered, which excludes this MCU from low-power applications. However, P_{RUN} value of 250mW at 40MHz is very low, recommending the M32R for the applications that need MCU constantly working in normal operation mode (stability management systems).

NEC's V850/SA1 offers the most efficient power management (see Table XIX), but the internal operating frequency is too low (20MHz, see Table XVIII).

In the field of EMI characteristics Fujitsu's MB91360 is dominant due to clock modulation feature.

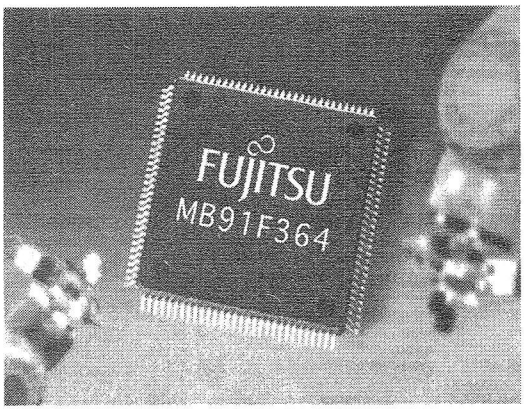

Figure 5: MB91F364 is the most popular device of Fujitsu MB91360 MCU family

Taking into account everything mentioned, Fujitsu's MB91360 MCU family (the most popular member is shown on Figure 5) is the top candidate for most of the high speed body network automotive applications. Additionally, Infineon's TriCore MCUs should be considered for fault tolerant applications.

- Very high speed network

This application area is nowadays clearly dominated by Hitachi's SH7709A (core is operating on 133MHz, see Table VII) and SH7750 (200MHz, see Table VII), Toshiba's TMPR3912 (92.16MHz, see Table XXI) and TMPR3927 (133MHz, see Table XXI) and ARM core MCUs (150MHz, see Table XXIV) due to their high data processing power.

5. CONCLUSION

Available top quality 32-bit MCUs are analysed and great variety of their features is systematized. The analysis was user-oriented (without going too much into technical details) and intended to simplify the selection of the best microcontroller for the specific application. The more powerful microcontroller characteristics are, the more important it is to implement them efficiently. There are many factors influencing the selection: the MCU's internal organisation, available peripheral modules, electrical features, memory organisation and capacity, embedded system development environment, the price etc. All these factors must be seen 'through the eye' of specific application needs. The modern application areas, such as networking, multimedia, telecommunications and automotive area, are

constantly demanding for more performance, providing more and more popularity to 32-bit MCUs and moving 16-bit MCUs to consumer electronics application area. At the same time, technology scale-down is working in favour of 32-bit MCUs, decreasing the price gap between 16-bit and 32-bit MCUs. Also, the trend of integration continues, since the MCU systems are ever more complex, demanding for more and more resources on-chip.

An analysis of current status in automotive application area is presented and the best MCUs for specific applications are recommended. Future prospects in this area anticipate integration of microelectromechanical sensors (MEMs) and microcontrollers on the single silicon chip. Emerging applications like brake-by-wire and steer-by-wire [17] are demanding timing-triggered communication protocols and the new MCUs implementing these protocols are already announced by some manufacturers.

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APPLICATION OF SIGNAL FLOW GRAPH THEORY FOR OBTAINING THE STATE SPACE MODEL FROM NON-LINEAR BOND GRAPH MODEL

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Abstract. *In this paper a new approach, for state space equations obtaining from the causal bond graph with non-linear elements and only the integral causality, is put forward. By following "the paths of traveling" of two general bond graph variables (effort e and flow f) through causal non-linear bond graph, the equivalent signal flow graph is obtained. On the basis of the signal flow graph, the equation system is formed and arranged in order to obtain the state space model.*

1. INTRODUCTION

Systematic procedures for obtaining the state space model from the bond graphs are very important because of the strong connection between bond graph models and all the analysis and design methods based on the state space model. This topic has been considered by *Breedveld* [1], *Cornet* and *Lorenz* [2] and others [3-10]. In 1988, *Breedveld* proposed the procedure for obtaining the relations between effort and flow for every bond graph element considering causality stroke position. A desired equation system can be determined by ordering initial equation system [1]. In 1989, *Cornet* and *Lorenz* proposed the procedure based on two additional equation systems [2]. The first one, the "head queue", is organized as FIFO (first input first output), and the second one, the "tail stack", is organized as LIFO (last input first output). The desired (ordered) equation system is determined by calculating "forward" variables of the first list and "reverse" of the second one, while following causality propagation in linear bond graph [2]. However, a special approach to this problem, based on using signal graph theory as an indirect tool, is put forward in [7, 8, 10]. The systematic procedure for obtaining the state space model based on the linear bond graph model and the corresponding signal graph, presented in [7, 10] is limited to the specific case where the linear bond graph contains only integral causality. The state space model may be obtained directly from the signal graph without any transformation of the equations. However, the presence of derivative causality on any C or I element points out the existence of dynamical dependence among the state space variables so that it requires the additional transformations of the equations obtained from the signal graph which is equivalent to initial linear bond graph [8, 10]. The other methods for obtaining the state space model from the lienar bond graph model are reduced to the writing of the equations for each element and connection in the bond graph, and their additional arranging [1, 2]. The number of necessary transformations of initial equations is increased with the bond graph complexity increasing. Then, the application of these methods become rather complicated.

In this paper the systematic procedure for obtaining the state space model of non-linear system from corresponding non-linear bond graph model and the corresponding signal flow graph is put forward. The efficiency of this procedure is shown on the example of the three coupled tanks.

2. SYSTEMATIC PROCEDURE FOR OBTAINING EQUIVALENT SIGNAL FLOW GRAPH BASED ON BOND GRAPH

Taking the bond graph model as a starting point, the corresponding signal flow graph is obtained by applying the following systematic procedure [7]:

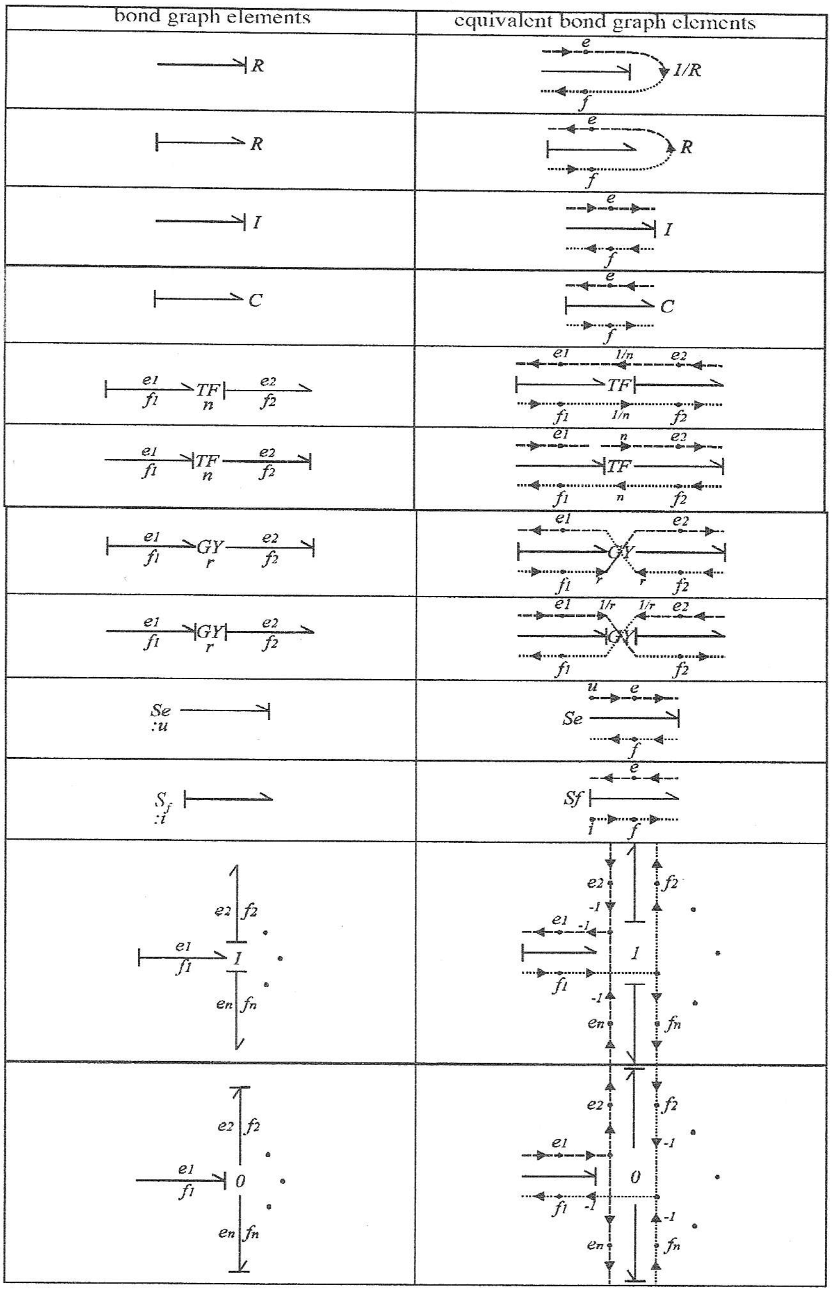
1. Marking the causal orientation of bonds in bond graph model (adding causality strokes to bond graph model), as described in [1], [2] and [3].
2. The equivalent signal flow graph obtaining,

- each R bond graph element is replaced by the equivalent R element from Table 1,
- each C bond graph element is replaced by the equivalent C element from Table 1,
- each I bond graph element is replaced by the equivalent I element from Table 1,
- each TF and GY are replaced by the equivalent TF and GY from Table 1,
- every *"1"* and *"0"* junctions of the bond graph model are replaced by the equivalent *"1"* and *"0"* junctions from Table 1,
- S_e and S_f sources are replaced by the equivalent elements (u and i - nodes) from Table 1,
- The signal flow graph is derived where nodes are sources, effort and flow of a bond graph.

All this should be linked to produce wholeness, i. e. the signal flow graph whose nodes, sources, efforts and flows are in the bond graph.

Direct examples which explain the application of this procedure in detail may be found in [7, 8].

Table 1



3. THE SYSTEMATIC PROCEDURE FOR OBTAINING THE STATE SPACE MODEL FROM NON-LINEAR BOND GRAPH MODEL

The non-linearity of bond graph is conditioned by the presence of nonlinear *R*-element, which may be often seen in the bond graph models of hydraulic and thermal systems.

The state space model can be derived based on non-linear bond graph model using following procedure:

1. Drawing the bond graph model of the considered system and determining the positions of causal strokes
2. Drawing the equivalent signal flow graph on the basis of the procedure obtained in part 2
3. Selecting the flows through *I* elements and the efforts on C elements: e_{Ci}, f_{Ij}, for the state variables
4. Expressing these sink nodes as a function of all the source nodes
5. Expressing the state variables derivatives as a function of the input variables and the state variables

In order to ilustrate the efficiency of the proposed procedure let us consider a hydraulic system as shown on Figure 1.

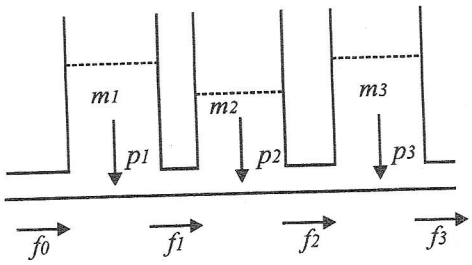


Fig. 1 Three coupled tanks

The system shown in Figure 1 consists of three uniform tanks of incompressible liquid connected by pipes [3]. Neglecting inertia effects, the pipes are modeled as pure, but nonlinear, resistance

$$f_i = k_i \sqrt{\Delta p_i} \tag{1}$$

where: k_i is a constant of *i*-th pipe (related to the size of orifice opening, pipe diameter and density of the material in the pipe), f_i is the mass flow in *i*-th pipe and Δp_i is the corresponding pressure drop. The tanks are modeled as pure capacities:

$$\frac{dm_i}{dt} = f_{i-1} - fi$$
$$p_i = \frac{g}{a_i} m_i \tag{2}$$

where: a_i is cross-section of *i*-th tank, m_i is the liquid mass in the *i*-th tank and p_i is corresponding pressure. Its bond graph is shown in Figure 2.

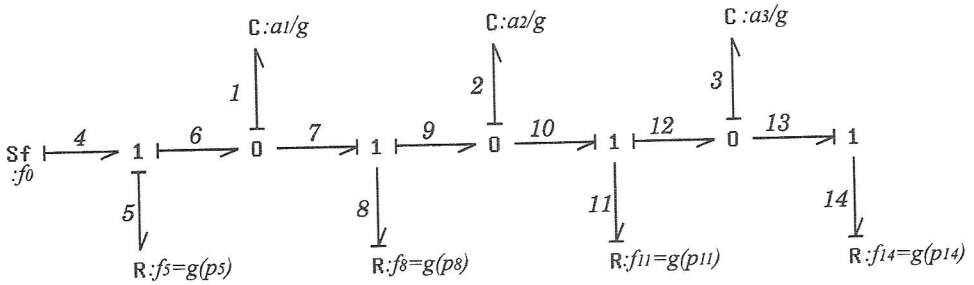


Fig. 2. Three coupled tanks - bond graph

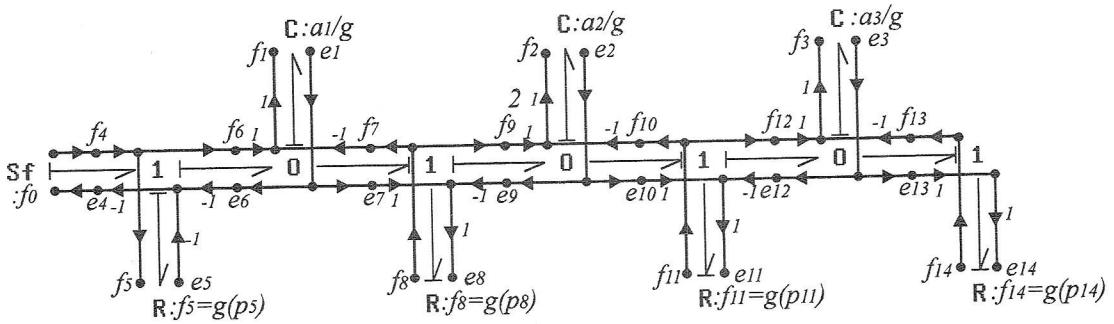


Fig. 3. Three coupled tanks - signal flow graph

Using the procedure described in part 2 the equivalent signal flow graph shown in Figure 3 can be obtained. Nodes e_1, e_2, e_3 are implemented as relevant, so the state vector

$$\mathbf{x} = \left[e_1\ e_2\ e_3\right]^T = \left[p_1\ p_2\ p_3\right]^T$$

and the input vector $\mathbf{u} = \left[f_0\right]$. It may be seen that the nodes $e_1, e_2, e_3, f_0, e_5, f_8, f_{11}$ and f_{14} are completely source nodes while the nodes $f_1, f_2, f_3, f_5, e_8, e_{11}$ and e_{14} are completely sink nodes. By finding the ways (from Figure 3) between each source node and the considered sink node (for each of them), the following system of equations is obtained.

$$\begin{aligned} f_1 &= -f_0 - f_8 \\ f_2 &= f_8 - f_{11} \\ f_3 &= f_{11} - f_{14} \\ f_5 &= f_0 \\ e_8 &= e_1 - e_2 \\ e_{11} &= e_2 - e_3 \\ e_{14} &= e_3 \end{aligned} \qquad (3)$$

Regarding that

$$\dot{e}_1 = \frac{g}{a_1} f_1;\ \dot{e}_2 = \frac{g}{a_2} f_2;\ \dot{e}_3 = \frac{g}{a_3} f_3 \qquad (4)$$

from the system of equations (3), the state space model is obtained

$$\begin{aligned} \dot{e}_1 &= \frac{g}{a_1}\left(-f_0 - k_1\sqrt{e_1 - e_2}\right) \\ \dot{e}_2 &= \frac{g}{a_2}\left(k_1\sqrt{e_1 - e_2} - k_2\sqrt{e_2 - e_3}\right) \\ \dot{e}_3 &= \frac{g}{a_3}\left(k_2\sqrt{e_2 - e_3} - k_3\sqrt{e_3}\right) \end{aligned} \qquad (5)$$

4. CONCLUSION

The systematic procedure, put forward in this work, may be equally efficiently applied to the nonlinear bond graphs which beside the integral have the derivative causality as well. In that way, their nonlinearity is caused by the presence of non-linear *R* element. In the case when the linearity of a bond graph is caused by the presence of modulated *TF* and *GY* elements and source, the application of the theory of the signal flow graphs on determining the state space model is also possible but is considerably more complex.

5. REFERENCES

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INSTRUCTION FOR AUTHORS

Name of the author/s, Affiliation/s

Abstract: *Short instruction for authors is presented in this paper. Works that are to be printed in the review "Electronics" should be typed according to this instruction.*
Keywords: *Review Electronics, Faculty of Electrical Engineering in Banjaluka, Instruction for authors.*

1. INTRODUCTION

In the review "Electronics", we publish the scientific and professional works from different fields of electronics in the broadest sense like: automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. In addition to the scientific and professional works, we present new products, new books, B. Sc., M. Sc. and Ph.D. theses.

In order to enable the unification of the technical arrangement of the works, to simplify the printing of the review "ELECTRONICS", we are giving this instruction for the authors of the works to be published in this professional paper.

2. TECHNICAL DETAILS

2.1. Submitting the papers

The works are to be delivered to the editor of the review by the E-mail (elektronika@etfbl.net) or on floppy (or CD) by post mail to the address of the Faculty of Electrical Engineering (Elektrotehnicki fakultet, Patre 5, 78000 Banja Luka, Republic of Srpska, Bosnia and Herzegovina).

2.2. Typing details

The work has to be typed on the paper A4 format, 8.27" width and 11.69" height (21.0x29.7 cm), upper margin of 1" (2.54 cm) and lower margin of 0,59" (1,5 cm), left and right margins of 1,57" (2 cm) and 0,39" (1cm) (mirrored margins). The header and footer are 0,5" (1.27cm) and 57" (2 cm). The work has to be written in English language. Our suggestion to the authors is to make their works on a PC using the word processor MS WORD 97/2000, and for the figures to use the graphic program CorelDraw, if the graphs are not going from the original programs, i.e., from the programs received (like MATLAB).

The title of the work shall be written on the first page, in bold and 12 pt. size. Also, on the first page, moved for one line spacing from title, the author's name together with the name of his institution shall be printed in the letter size (10pt, *Italic)*. The remaining parts of the manuscript shall be done in two columns with 0.5cm distance. The work shall be typed with line spacing 1 (Single) and size not less than 10 pt (like as this instruction). After the title of the work and the name of the author/s, a short content in English language follows, written in italics. The subtitles in the text shall be written in bold, capital letters of the size as in the text (not less than 10 pt.). Each work shall, at the beginning, comprise a subtitle INTRODUCTION, and, at the end, the subtitles CONCLUSION and BIBLIOGRAPHY / REFERENCES.

The operators and size marks that do not use numerical values, shall be written in common letters. The size marks that can use numerical values shall be written in italics. The equations shall be written in one column with right edge numeration. If the breaking of equations or figures is desired, those may be placed over both columns.

Illustrations (tables, figures, graphs etc.) may be wider than one column if necessary. Above a table there shall be a title, for instance: Table 2. *The experimental measuring results.* The same applies to figures and graphs but the accompanying text comes underneath the figure of graphs, for instance: Fig.3: *Equivalent circuit diagram...*

The work should not be finished at the beginning of a page. If the last manuscript page is not full, the columns on that page should be made even. Number of pages should not go over 6.

3. CONCLUSION

This short instruction is presented in order to enable the unification of technical arrangement of the works.

4. REFERENCES

At the end of work, the used literature shall be listed in order as used in the text. The literature in the text, shall be enclosed in square brackets, for instance: ...in [2] is shown ...

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