ELEKTRONIKA

ELECTRONICS

PREFACE

This special issue of the International journal "Electronics", published by University of Banja Luka, is devoted to the 6th IEEE International Conference on Telecommunications in Modern Satellite, Cable, and Broadcast Services - TELSIKS 2003. The editor of the journal, Prof. Dr. Branko Dokić, has invited us, as guest-editors, to present the most interesting papers from the conference.

TELSIKS 2003, was held from 1 to 3 October 2003, in Niš, Serbia & Montenegro. It was organized by the Faculty of Electronic Engineering - Niš under IEEE MTT-Society, communications Society, AP-Society and IEEE Region 8 technical co-sponsorships, and in co-operation with Yugoslavia IEEE Section, national IEEE MTT Chapter and national IEEE Communications Chapter. In addition, the conference was supported by Serbian Academy of Science and Art, Engineering Academy of Serbian & Montenegro and many domestic societies.

Conference topics were: Mobile communications, Classical cable and optical communications, Multimedia communications, Antennas and propagation, RF and microwave technique, Electromagnetic compatibility, Digital signal processing, Broadband wireless access, Telecommunication networks, Modulation and coding, Internet technologies, etc. 150 regular papers were accepted for oral or poster presentation. In addition, a number of experts were called to present their invited papers. At this year's conference an invited plenary talk (Prof. Ke Wu from Ecole Polytechnique, Montreal, Canada), 18 invited keynote talks and 9 invited papers dedicated to the 70th birthday of Prof. Aleksandar Marincic, member of SANU, were given The authors were from 31 countries and from all 5 continents.

All accepted papers were published before the conference. The Conference Proceedings have been distributed as an IEEE publication (*Book Broker Post-conference Distribution Program*) and included in the well-known IEE INSPEC database as well.
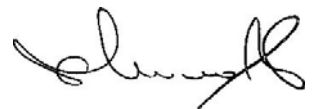
In addition, the technical program included an exhibition, two workshops and two round tables.

It is important to note that TELSIKS conferences have been evaluated by IEEE officers as a leading scientific conferences in the field of modern telecommunication technologies in Central and Southeastern Europe.

The selection of the papers presented in this issue is based on the suggestions of the reviewers and session chairmen. We would like to thank to the authors of these papers.

We would also like to invite all readers of the »Electronics« journal to submit the papers for the next TELSIKS 2005 conference and participate in this significant scientific event.

Guest Editors:

Prof. Dr. Bratislav Milovanović
TELSIKS Conference Chairman

Prof. Dr. Vera Marković,
TELSIKS Conference Program Committee, Member

BIOGRAPHIES OF GUEST EDITORS

Prof. Dr. **Bratislav D. Milovanović** was born in 1948 in Rosica, Serbia. He received his B.Sc. (as the best student of his generation), M.Sc. and Ph.D. degrees from the Faculty of Electronic Engineering, University of Niš in 1972, 1975 and 1979, respectively. From 1972 onwards he was promoted to all academic positions to full Professor (1990). From 1981 till 1984 he was head of the Chair for Theoretical Electrical Engineering and since 1994 he is head of the Chair for Telecommunications Department. Also, he was the Vice-dean in the period from 1989-1991, and the Dean from 1994-1998. Since 1996, he is the President of the Administrative Committee of Ei-Holding Co., Niš.

Prof. Milovanović is the author of three student textbooks and he has also founded two microwave laboratories: one for student's practical exercise and a research one. He has supervised six Ph.D theses, over ten M.Sc., and more than one hundred diploma works.

In addition to his graduate and postgraduate teaching activities, he was head of over 20 R&D projects. Professor Milovanović is one of the most successful researchers in the field of electronic engineering and information communication technologies. His scientific interests are in field of telecommunication, and specially in field of microwave technique. As the author or co-author, he has published over 340 scientific papers (33 in the world-known scientific journals and over a hundred papers in Proceedings of international conferences). Also, he is a reviewer of several world-leading scientific journals and conferences, and a member of the Editorial Boards of several scientific journals. In addition, he has been a guest-editor of special issues of several international scientific journals.

Prof. Milovanović is the general Chairman of series of the International IEEE TELSIKS conferences. He was the Vice-chairman of International ICEST conferences and the member of Program Committees of more other ones.

He is an IEEE member, member of Serbian Scientific Society and full member of Yugoslav Academy of Engineering. Also, he is the President of national MTT Society and Vice-chairman of YU MTT Chapter, Vice-president of ETRAN Program Committees and the President of Commission of ETRAN Sections for microwave and sub-millimeter technique.

Prof. **Vera Marković** was born in Niš, Yugoslavia. She graduated at the Faculty of Electronic Engineering, University of Niš, in 1980 and after that she joined the same faculty. She received the M.S. and Ph.D. degrees in electrical engineering from the University of Niš, in 1985 and 1992, respectively. She became Assistant Professor in 1992, Associate Professor in 1997, and Full Professor in 2002, at the Department for Telecommunications of the Faculty of Electronic Engineering in Niš. She was teaching in many courses as for instance: *Microwave Electronics, Microwave Technique, Satellite Communications, Microwave Systems, Mobile Communications, Telecommunication Software, Microwave and Optical Electronics*, etc.

Professor Vera Markovic has published a monograph, a textbook and more than 170 papers in international and national journals and conference proceedings. She managed or participated in many research projects. Current research interests of Dr. Markovic include the modeling of low-noise microwave active devices, application of neural networks in the microwave technique, the biological effects of microwaves and, generally, the analysis and design of microwave circuits and systems.

She has been a member of program and organizing committees of the IEEE international conference TELSIKS. In addition, she was a member of program committee of international conferences PES and ICEST and various national boards, expert groups and commissions. She was guest-editor of several journals. Currently, she is editor of national journal "*Microwave Review*". She was a reviewer of leading international journals "*IEE Proceedings on Circuits, Devices and Systems*" and "*Microelectronics Reliability*". She is for years a member of IEEE. She is also a member of YU IEEE MTT Chapter, MTT Society, Society for Telecommunications, etc.

Control of Charging in High Aspect Ratio Plasma Etching of Integrated Circuits

Zoran Lj. Petrović[1,2], Toshiaki Makabe[2]

Abstract - **In this paper we discuss some recent studies on control of charging during plasma etching of silicon dioxide in integrated circuits. These are required to reduce the damage on the devices and allow further increase in speed and capacity of integrated circuits. Such possibilities have a bearing in development of telecommunications. In particular we discuss how properties of incoming ions, geometry of the nano-structure, aspect ratio and plasma properties affect the kinetics of charging.[1]**

Keywords - **integrated circuits, plasma etching, charging, ion energy distribution**

I. INTRODUCTION

Further advances in increasing the capacity and speed of integrated circuits depend very much on two main technologies photo-litography and plasma etching. Both technologies have reached certain limitations in making progress towards sub 100 nm resolutions. This paper deals with the research that has been carried out to optimize plasma etching and make it compatible with further miniaturization.

Perhaps the critical problem in further optimization of plasma etching is control of charging of high aspect ratio (height divided by width ratio) during plasma etching [1-4]. Deposited charge at the bottom of narrow contact holes or nano trenches produces potential which blocks further ions from reaching the bottom of the etched structures. Thus various problems may be associated with different forms of charging including micro loading, aspect ratio dependent etching, micro trenching, etch stop in case of SiO_2 and notching due to electron shading in case of poly Si etching [5]. Etching of SiO_2 is the most frequent operation in plasma etching and critical in achieving contact between different layers and the devices.

Only few studies have been performed for etching of oxides. It would be wrong to assume that the high energy ions that are normally used in oxide etching [6] are less likely to be affected by the fields due to charging since the accumulated charge density on an insulating oxide may be high enough to produce local potentials of the order of hundred volts and more. In addition to problems for the process of etching itself the charging may also damage the devices that are being processed. The thickness of oxide layers in FET is so small that even several of elementary charges deposited at the bottom of a contact hole may induce voltages that exceed breakdown potential of the oxide material.

Several approaches were proposed to reduce charging which include:

1. application of pulsed capacitively coupled plasmas (CCP) [7] and inductively coupled plasmas (ICP) [8];

2. etching by fast neutral beams [9,10];

3. application of fast electron beams to neutralize the surface [11];

4. application of pulsing technique and two frequency plasma production and biasing that would allow negative ions to enter the nano structures and neutralize the positive ions accumulated in the trench;

5 adjustment of plasma and surface chemistry by addition of oxygen.

Positive effects were demonstrated with most of these techniques. However, full understanding and optimization of these techniques requires understanding of the process of charging, of ion energies and trajectories as a function of plasma properties, of the dynamics of charges on the surface and potentials within the structures that are being manufactured. This paper will review some of the results obtained in this direction.

For improvement of telecommunications it is important to establish the limitations of integrated circuits. Optical communications were made possible not only by advances in lasers and optical fibers but also by large processing power that became available with improvement of integrated circuits. Further improvements in mobile telephones will more and more rely on increased processing power especially with the transfer of images and development of reconfigurable systems. For that purpose not only the power but also the speed and facilities to amplify high frequencies in domain of MHz and even THz are required.

II. TRANSPORT AND DEPOSITION OF IONS IN TRENCHES

The simulation technique that was applied most frequently to study processes of charging is Monte Carlo simulations [12]. On the other hand direct numerical solution of Boltzmann equation may be more efficient and easier to integrate into large models of plasma. Thus comparisons between the two techniques is required to validate the simpler, approximate numerical technique.

In this paper we study the charging in a fixed structure. The geometry of the system is shown in Fig. 1. We assume that the oxide layer is 200 nm thick and that the trench is 100 nm wide with the thickness of the oxide at the bottom of only 50 nm. The trench structure is symmetric with respect to x-axis, i.e. only one half is shown here and modeled under periodic boundary conditions. The trench as defined in our study does not have a very high aspect ratio.

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Fig. 1 Geometry of the system of nano trenches that was used in modeling of ion and electron redistribution.

Fig. 2 Trajectories of ions inside a nano-trench defined in Fug. 1 case 2 for initial energies of 60 eV [13].

In the first instance we assume that we have positive charge at the center of the bottom ρ_{s1}=1.3 10^{-5} C cm^{-2} (case 1). We also studied [13] a situation when we have both ρ_{s1} and a negative charge at the top of the side wall ρ_{s2}=3.25 10^{-6} C cm^{-2} (case 2). The assumed charge densities are realistic and lead to a potential of 73 V (case 2), so we will regard voltage higher than this value as high. However, since the charge is not spread uniformly throughout the bottom, the potential has a maximum at the center (x=0) and it gradually drops down towards the corner.

In MCS we typically release 1-3 10^6 electrons and ions to obtain relatively smooth distributions. We varied ion energy from 20 eV to 120 eV. Typical set of trajectories for case 2 and initial energy of 60 eV is shown in Fig. 2. Specific characteristic of this initial condition is that the ions will have enough energy to reach some parts of the bottom but not all. Close to center (small x) the ions are bent and travel almost parallel to the bottom. As soon as they come near the position with the potential lower than their initial energy they reach the bottom wall. As a result the corner and a part of sidewall are reached by two groups of ions, one that traveled directly and the other that was diverted by the electric field.

The distributions of ion fluxes inside the trench are shown in Fig. 3 for z (downward) direction. The data in that figure were obtained for the second case by Monte Carlo simulations (MCS). There is no flux to the bottom up to x=35 nm and the distribution of the flux starts with a peak, peaking again in the corner. Along the sidewall there is a flux of ions in z direction in the corner but not towards the top and the profile of downward flux ends with a peak. This is due to the maximum of potential at the corner of the trench caused by negative charges at the top of the sidewall.

It appears that, due to poor resolution direct numerical solution to the Boltzmann equation differs from MCS in such a way that the peaks are averaged out. However in general agreement between the two techniques is quite good. If we allow ions to be initialized with a small range of angles (5-10°) final results begin to appear more similar to those obtained from the Boltzmann equation.

The main difference between cases 1 and 2 is due to the large field at the top corner of the trench which causes a more pronounced drop in the downward flux and a more pronounced sideways flux near the top of the side-wall.

As mentioned in discussion of the trajectories, most points along the walls may be reached by two groups of ions. The first is the downward moving ions i.e. those starting close to the side-wall to hit the side-wall or close to the same x coordinate to hit the bottom (group a). The second group, (the group b) consists of ions that were reflected of or diverted significantly by the high potential of positive surface charges at the bottom of the trench and consequently start at a quite different x value as compared to the point where they reach the walls. The group (b) ions originate from the initial x values that at the bottom correspond to the potential greater than the initial energy and when they reach the bottom of the trench they move mainly sideways or upwards. As a result two groups will hit the surface at two different angles and with different energies.

Fig. 3 Downwards flux of ions obtained by MCS in case 2 for initial energy of ions of 60 eV [13].

III. DEPENDENCE OF CHARGING POTENTIAL AS A FUNCTION OF ASPECT RATIO

In this section we will summarize the results [14] obtained by Monte Carlo simulation and application of Poisson's equation to obtain the growth of potential during the development of nano-trench profile in dielectric SiO_2. The models is developed to represent the contact hole which has to go through the highest aspect ratio in development of the profile and yet at the same time the bottom is in electrical contact with the transistor. This is done in order to determine the physical and electrical mechanisms of the etch-stop processes. The idea is also to optimize removal of charging by determining the required timing for pulsed plasmas.

We model a series of nano-trenches and ridges 100 nm in width each and with variable depth corresponding to aspect ratios in the range from 1.5 to 10. The trench is inside the SiO_2, and conductive poly-Si is arranged below the oxide layer at the grounded potential. The geometry of the system that is being modeled is similar to that in the previous section and is shown in Fig. 4. It is assumed that the walls are saturated by active radicals so the ion-assisted etching is proportional to the flux of ions. The flux, in our case is assumed to be equal to that of ions and is equal to 10^{16} cm^{-2}s^{-1}, which is a realistic value [14].
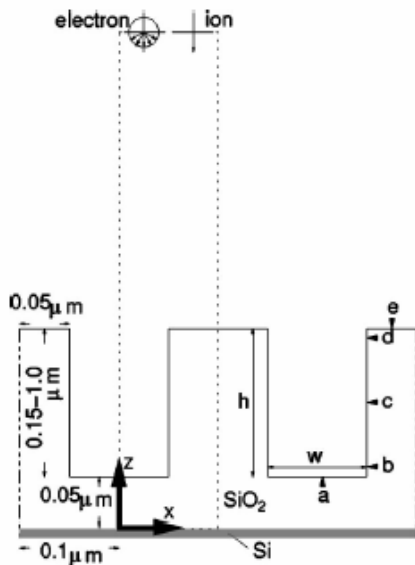
Fig. 4 Geometry of the model system. The trench dimensions are shown. The points where potential will be recorded are denoted by the letters a–e.

The electrons have isotropic velocity distribution with energies of 3 eV, while ions are orthogonal to the surface with an initial energy of 300 eV.

Ion and electron trajectories are followed from a point within the sheath towards the surface. Neutralization of opposite charges are allowed based on fluxes to the surface and the remaining charge is allowed to stick to the surface. Space and time resolved calculations were performed. Time dependence was obtained from using realistic etch rate of 500 nm/min [ref] and fluxes of charged particles. Evolution of trench and potentials were followed.
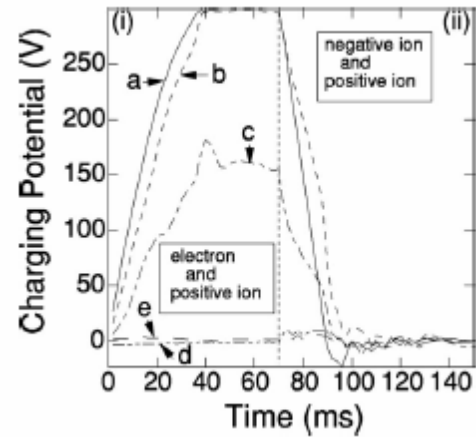
Fig. 5 The time development of potentials at five points inside the trench at the aspect ratio of 10 for pulsed plasma: (i) plasma on phase 0-70 ms, (ii) plasma off phase 70- 140 ms [14].

The time required to reach the final, stationary value, t_{charge} , was the critical result for optimization of pulsed plasma technique. It was typically few tens of ms. The time development of potentials at different points (defined in Fig. 1) is shown in Fig. 5. In this calculation in the plasma period both electrons and ions are released. However, in the afterglow period ambipolar field has collapsed and both negative ions and positive ions are reaching the surface. Thus efficient neutralization of the charge is achieved. The figure indicates how much should the on and off periods of pulsed plasma last in order to avoid buildup of high potential at the bottom of the trench that leads to etch stop [14].
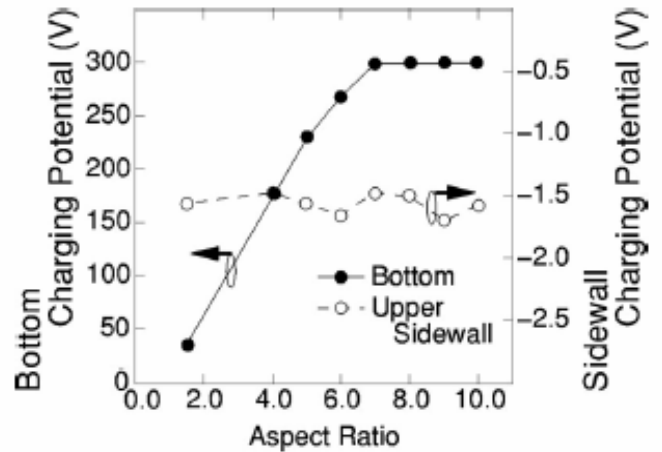

Fig. 6 Potential at the bottom of the trench and at the top of the sidewall as a function of aspect ratio [14].

Another critical result may be obtained if we observe the saturated potentials at the bottom and at the top of the sidewall as a function of aspect ratio (Fig. 6). While the potential at the top of the sidewall is independent on aspect ratio the potential at the bottom is quite strongly dependent. For aspect ratios greater than 6 the potential reaches the value of the initial energy of ions and therefore etch stop develops. It occurs when the potential at the bottom approaches the maximum ion energy. The ions are either reflected to the sidewall, causing notching, or back to the plasma. This is consistent with some experimental observations [15].

The simulations show that most of the positive charge is deposited at the bottom of the trench and negative at the top of the sidewalls. The major difference between ions and electrons is in the fact that electrons have isotropic velocity distribution and are slowed down by the sheath field. Thus they have very little chance to reach the bottom of the trench and effectively they are deposited at the top of the sidewalls of the trench. This affects transport of electrons in the trench even further. The potential at the sidewall is thus determined by electron energy. For moderate aspect ratios, the shading of electrons produces predominant deposition of electrons on the sidewalls, while ions predominantly reach the bottom of the trench.

At very high aspect ratios, the positive field at the bottom is sufficiently high to prevent all the ions from reaching the bottom wall, while the electrons are diverted by the potential at the top of the trench. Thus, the total particle flux to a set of trench/ridge system is zero,

For realistic particle fluxes the etch rate is 500 nm min^{-1} a monolayer of SiO_2 is stripped at intervals of hundreds of ms. Therefore charging potential is developed in time shorter than that and therefore will affect plasma etching very much and lead to complete etch stop. As mentioned above pulsed operation allows removal of accumulated charges and continuation of etching [6]. In addition it was shown that double layers that occur during the afterglow may facilitate transport of negative ions to the bottom of the trench and lead to very efficient neutralization of deposited charges. Ions are less affected by the field at the top of the trench and at the same time in electronegative plasmas density of negative ions is typically large.

IV. MODELING OF TRANSPORT OF IONS THROUGH THE PLASMA SHEATH AND ITS INFLUENCE ON CHARGING
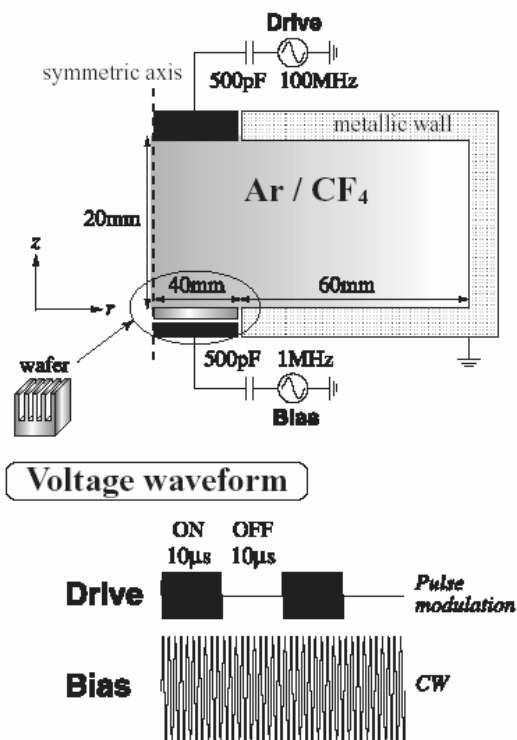
Fig. 7 Schematics of experimental CCP system with 2 frequencies and pulsed plasma sustaining voltage .

Plasma etching of poly Si is usually carried out by using ICP with relatively small biasing voltages as high energy of ions is not required to achieve etching. However, for etching of SiO_2 the polymer layer of SiF_n (where n<4) should be bombarded by ions with energies in excess of 200- 300 eV and up to 1000 eV [6]. For this purpose a CCP is best suited (Fig. 7) though it may be possible [6,7] to develop even ICP [8] with high-biasing voltage, low-frequency power supply. So far we have considered monoenergetic beams of ions but it is of course necessary to establish temporal dependence of ion energy distributions (IED) at the surface of biased electrode for realistic conditions. Because of its importance IEDs have been measured [16-23] or calculated [24-27] in different gases and systems on a number of occasions. The other aspect of this calculation, the structure and other properties of the sheath have also been investigated [28-33]. Time resolved IEDs are difficult to measure [34] but it is relatively straightforward to simulate once a complete and well tested plasma model is available [35].
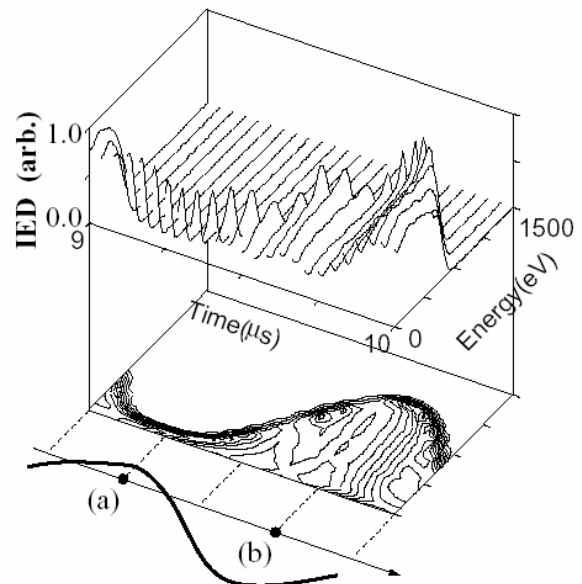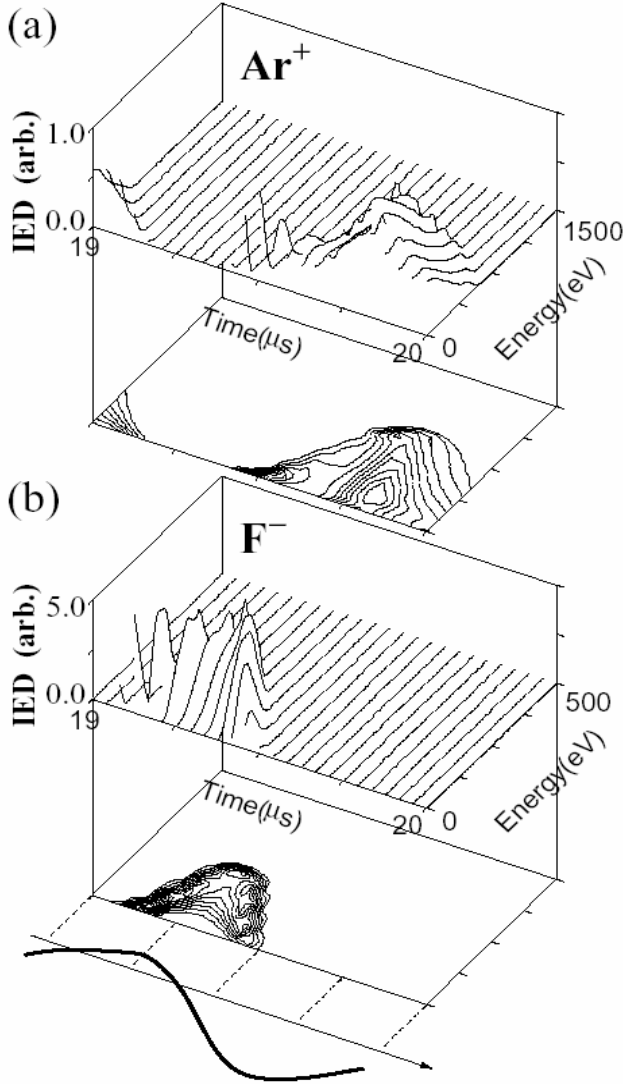

Fig. 8 Time-dependent IED of Ar+ incident on a wafer during one cycle of the LF bias in the *on* period of the VHF source. The external conditions are 50 mTorr in gas pressure, 1 MHz in bias frequency, and 700 V in bias amplitude for the plasma source of 100 MHz and 300 V [36].

A. Details of the model

In this paper we discuss some of the results presented by Yagisawa and Makabe [Yagisava MakabeIEEE2003] of Ar$^+$ CF$_3^+$ and F$^-$ ions in CF$_4$(5%)/Ar CCP. Pulsed two frequency operation is assumed that corresponds well to practical conditions in SiO_2 etching. Optimum conditions are achieved for 100 MHz very high frequency (VHF) plasma-sustaining source and with 1 MHz low frequency (LF) biasing source [ref]. VHF source had typically 300 V (200 V – 1000 V) in amplitude with an on/off cycles of 10μs/10μs. In Fig. 7 we show the system that is subject to modeling.

It is important to point out that both experimental [24] and [23] theoretical evidence have been produced for this plasma that show injection of negative ions due to double layer formation during the afterglow. Charging was shown to

be significantly reduced or even removed under those circumstances. 2D-t plasma characteristics, potential $V(r, z, t)$, and positive and negative ion number density $n_p(r, z, t)$ and $n_n(r, z, t)$, are self-consistently obtained. The other module is the estimation of the temporal characteristics of the two-dimensional velocity distribution $g(v_r, v_z, t)$ under the 2D-t plasma structure given by the first step. Ions are traced by using the Monte Carlo test particle method in the calculated sheath region in front of the wafer biased at LF.

Fig. 9 Time-dependent IED of Ar+ (a) and F- (b) incident on a wafer during one cycle of the LF bias in the *on* period of the VHF source. The external conditions are the same as those in Fig. 7 [36].

B. Temporal behavior of ion velocity distribution

Time dependence of IED of Ar+ incident on a wafer during the one period of the VHF source (and last LF period) is shown in Fig. 8. The external conditions are 50 mTorr in pressure, 1 MHz in bias frequency, and 700 V in bias amplitude. Only the positive ions reach the wafer during the *on* phase, because of the positive ion sheath accelerating positive ions to the wafer. When the transit time of ions through the sheath is less than half of the period of bias frequency, almost all ions are swept away by the sheath field. Therefore the incident energy shows a strong time modulation with a delay due to collisions.

The IED is swept by the electric field in the sheath which is generated by the potential between plasma and the biased electrode. The potential oscillates between two values and the time averaged IED will thus have two peaks. One expects stronger time modulation of IED for lower pressures as plasma approaches collisionless conditions.

While in the *on* period only positive ions reach the surface of the biased electrode, in the off period both negative ions and positive ions reach the surface (Fig. 9). Negative ions have three time lower energy but a five times larger flux allowing neutralization at the bottom. Special design of pulsing and two frequency operation was discussed by Makabe and coworkers [35-37]. The plasma in the afterglow (*off*) phase is ion-ion plasma and it is designed to facilitate the negative ion injection into the nano-trenches.

C. Time averaged IEDs

The time-averaged IED of positive ion Ar+ over one cycle of the LF bias during the *on* period of VHF plasma sustaining supply, is shown in Fig. 10. Two peaked structure is observable at the lowest pressure covered here. It is still present to a smaller degree at the intermediate pressure and the high energy peak disappears at 50 mTorr where the sheath is collision dominated. In that case angular distribution is much broader.
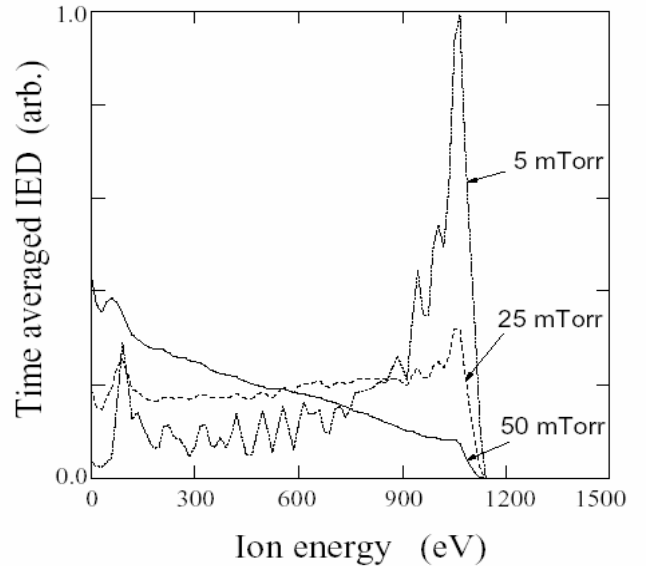

Fig. 10 Time averaged IED of Ar+ over one cycle of the LF bias during the *on* period of the VHF source as a function of gas pressure. External and internal conditions are the same as those in Fig. 8 except in regard to pressure [36].

The low energy component of the IED may help reduce the negative charges at the top of the trench provided that angular distribution is broad. [26]. This is in particular important if we want the negative ions to cross that barrier and reach the bottom of the trench. Negative ions in the *off* period have a lower energy (as mentioned above) than positive ions.

The dependence of maximum and minimum ion energies on the bias voltage is shown in Fig. 11. (for 50 mTorr). The maximum energy increases linearly while the lowest energy is independent on the bias voltage. The increase is somewhat greater for Ar+ ion than for the CF_3^+ ion.

These partial results are only a confirmation that our representation of plasma is almost complete and that it may

be employed to predict exact mechanisms of charging and model techniques for removing charging and the associated damage.
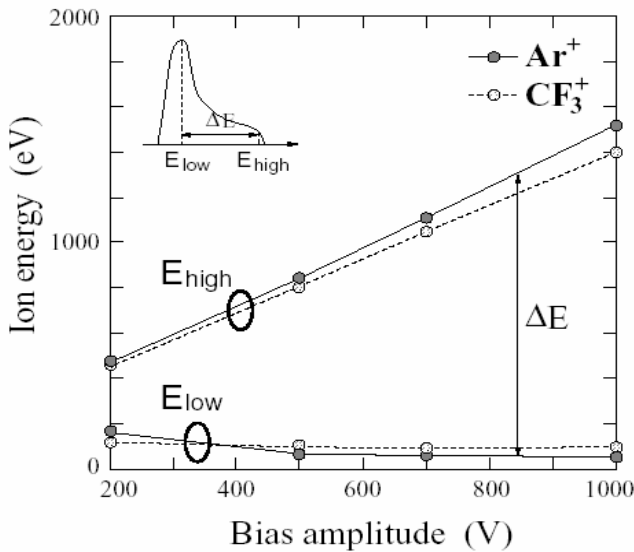

Fig. 11 Maximum and minimum energies of the time averaged IED of Ar^+ and CF^+_3 as a function of the LF bias amplitude. External conditions are the same as those in Fig. 5 except in regard to the bias amplitude.

V. DAMAGE CURRENT IN REALISTIC SYSTEMS

We should finally consider a realistic system where a high aspect ratio contact hole should be made to connect to the FET at the bottom of several layers of SiO_2 and metal or poly Si. Such a system may be modeled very accurately for the conditions of actual plasma etching. In Fig. 12 we show a system that is modeled.
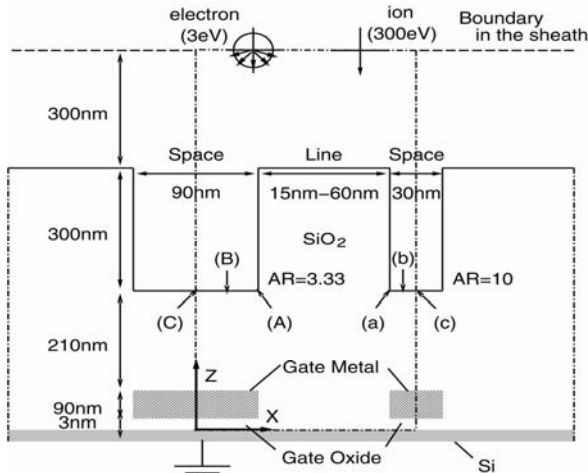
Fig. 12 Typical setup for etching a contact hole to the Gate of a FET [ref].

If realistic plasma surface model is applied [Makabe ref] one may determine the damage current that flows as a result of avalanches inside the gate oxide and inside the insulators. In Fig. 13 the damage current is shown as a function of time for different and as a function of distance between two trenches. In the simulation we use 300 eV ions typical for etching of SiO_2.

A higher current flows through the bottom resistor and these semiconductor breakdowns are the main cause of damage of Integrated circuits. Recently realistic plasma

models were developed as computer design and control tools, and it became possible to model the damage to ICs during production. It also became possible to prove and optimize reduction of charging related damage by application of some of the recently proposed techniques such as pulsed plasmas.
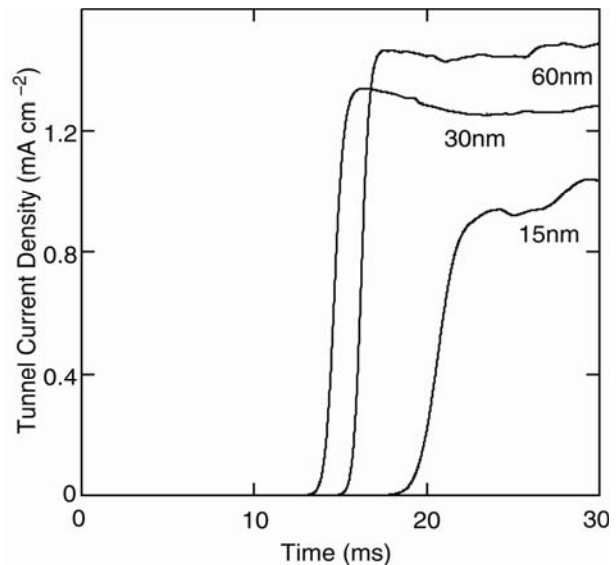
Fig. 13 Damage current flow through the gate oxide for three different distances between trenches.

VI. CONCLUSION

In this paper we present some of the results obtained in studies of the dynamics of the charge deposited at the bottom of high aspect ratio nano-structures which may lead to damage of ICs. Mainly Monte Carlo simulation was applied together with plasma models. Some conclusions were discussed especially optimization of pulsing and two frequency techniques to reduce the charging and the corresponding damage. Details of discussion may be found in the specific technical publications. In general we hoped to indicate how charging problems can be dealt with both from the microscopic point of view (dynamics of ions), from the point of view of integrated plasma models such as Vicaddress [ref] and from the point of view of device production. The control of the damage due to charging may be the limiting factor in development of faster and more powerful ICs and may determine the dynamics of development of telecommunication devices that rely heavily on processing power.

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Optimization of Test Signals for Analog Circuits

V. Guliashki[1], B. Burdiek[2], W. Mathis[2]

Abstract – **In this paper the optimization of test signals for integrated analog circuits by means of a genetic algorithm is considered. The test signal generation problem is formulated as an optimization problem, where through minimization of specific objective function a fault detection criterion for the tested circuit is maximized. The simulation results show that the use of optimized test signals leads to considerable increasing of the detected faults number.**[*]

I. INTRODUCTION

The necessary conditions for optimality of the test signals for integrated analog circuits are proven in [1] by means of Pontrjagin's Maximum principle. It is shown there that for a general analog circuit only binary signals, one for each circuit input, can maximize a given fault detection criterion of arbitrary structure. Therefore the input signals used for our experiments consist of rectangular pulses (see Fig.1a). Here α is the amplitude of the input signal. Although such test signals satisfy the necessary conditions for optimality, they don't possess a concrete optimal form, which could guarantee the detection of maximum number faults during the tests. The qualitative form of the test signals is already known – rectangular pulses, but the width of these pulses in the optimal signal may be different. This means that the positions, where the test signal jumps from $-\alpha$ to $+\alpha$ and vice versa, have to be fixed through an optimization procedure. A program, performing circuit's simulation is used for optimization of the test signals. Circuits with one or two input signals have been tested. For each circuit a test fault set F_f was created, $F_f = \{f_1, \dots, f_n\}$, where $f_1, \dots, f_n$ are hard to detect parametric faults, for which the output signal curve for circuit having such faults deviates very little from that one of the good circuit without faults.

For our consideration the test interval Δt is divided in k subintervals Δt_j, $j = 1,\dots,k$; and Δt_j is the minimal existence time of one pulse. $\Delta t = t_f - t_0$, where t_f and t_0 are correspondingly the final and the initial point of the test time interval Δt. During the optimization, the pulse form of the input signal $x(\Delta t)$ is expressed by means of binary variables (see Fig. 1b), so that one k-dimensional binary vector $x_b(\Delta t)$ corresponds to each concrete signal $x(\Delta t)$. If $x(\Delta t_j)=\alpha$, the corresponding component $x_b(\Delta t_j)=1$, and if $x(\Delta t_j)=-\alpha$, then $x_b(\Delta t_j)=0$. In case a pulse is m subintervals wide, the corresponding part of the binary vector consists of m consecutive zeros (or m consecutive units respectively).
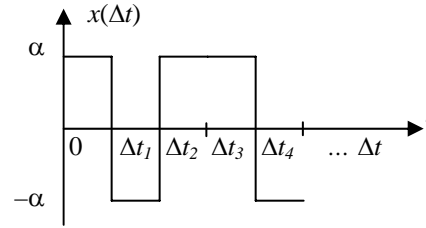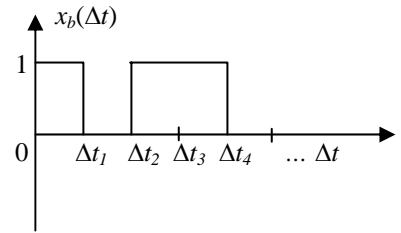

Figure 1a: The test signal $x(\Delta t)$.

Figure 1b: The binary vector $x_b(\Delta t)$.

The functional J (1), proposed in [1] is used as a fault detection criterion and the optimization problem is presented in the following form:

$$\textbf{Min } J(\boldsymbol{x}(\Delta t)) = \sum_{i=1}^{n} w_{fi}\Phi_{fi}(V_g, V_{fi}) \qquad (1)$$

$$\Phi_{fi} = \int_{t0}^{tf} |V_g(t) - V_{fi}(t)|\, dt \qquad (2)$$

$$\boldsymbol{\Delta t} = t_f - t_0 = \boldsymbol{kt'} \qquad (3)$$

where V_g and V_{fi} are the output signals correspondingly for a good device without faults and for a device having a fault from the set F_f. The weighting factors w_{fi} are negative numbers, used to distinguish faults in J (1) and are determined from an initial fault simulation. Generally the functional J (1) is nonlinear. Its minimal value corresponds to input signal, for which the difference between $V_g(t)$ and $V_{fi}(t)$ curves is maximal. The signals $x(\Delta t)$ correspond to the vectors $x_b(\Delta t)$:

$$\boldsymbol{x_b}(\Delta t) \in \boldsymbol{B^k}, \qquad (4)$$

where $\boldsymbol{B^k}$ is the set of k-dimensional binary vectors.

The test interval Δt is restricted final time interval. Hence the number of subintervals k is finite integer number. The test signal $x(\Delta t)$ may be converted into a k-dimensional binary vector $x_b(\Delta t)$ by means of simple assigning 0 or 1 to the i-th x_b-component according the value of $x(\Delta t)$ for the i-th subinterval. This is a polynomial (more precisely - linear on k) procedure, as well as the back converting $x_b(\Delta t)$ to $x(\Delta t)$.

Statement: The problem (1)-(3) belongs to the class of NP-hard problems.

Proof: The nonlinear binary programming problem is NP-hard programming problem (see [4], [8]). It may be converted to the problem (1)-(3) by means of linear in k procedure for converting $x_b(\Delta t)$ to $x(\Delta t)$, where k is finite integer number, and choice of (1) as a nonlinear objective function. Hence the

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problem (1)-(3) belongs also to the class of NP-hard problems.

There does not exist an exact algorithm, which can solve such kind of problems in time depending polynomially on the problem input data length or on the problem size. The way for overcoming this disadvantage is the creation of efficient approximate algorithms. A class such algorithms are the genetic algorithms (GAs). Their main characteristic is the very good balance between efficiency and efficacy for a broad spectrum of problems (including nonsmooth, multimodal and nonconvex problems). GAs were proposed by Holland [6] as a model that applies the evolution mechanism of systems in the nature and simulates the evolution of organisms. In the eighties the theory of GAs was refined [3]. In contrast to the existing exact algorithms GAs do not need highly domain-specific knowledge (only the objective (fitness) function needs to be evaluated during the search process). As a heuristic technique GAs cannot guarantee the obtaining of an optimal solution. This disadvantage could be compensated to a great degree by means of some modifications in the trivial scheme of GAs. One good idea is for example the adjunction of some form of local search to the genetic approach as considered by Pirlot [9]. Another possible modification, giving to genetic algorithms the form resembling scatter search, is proposed by Glover [2]. On this ground we propose here a modified genetic algorithm for solving the problem (1)-(3).

II. GENETIC ALGORITHM GAITET

The proposed algorithm is called GAITET and can solve the optimization problem (1)-(3) for integrated analog circuits having one or two input signals. It is written in JAVA language and uses a population of 100 individuals, where each individual is represented by one or two input signals $x(\Delta t)$, according the necessary input for the concrete analog circuit. The input signals are expressed (see (4)) as binary vectors $x_b(\Delta t)$, having 100 binary variables, i.e. $k = 100$. The algorithm GAITET runs under UNIX and starts by means of Runtime.getRuntime().exec() method the program TORAD (**T**est Genera**tor** for **A**nalog **D**evices), written in C++ language, which is used to generate the output signals V_g and V_{fi}, and to evaluate the objective functional J (1). The last program writes the value of J in an output file. The main program, realizing the GAITET algorithm reads this output file every time, takes the value of J and continues its performance. The genetic algorithm includes two selection strategies and three kinds of crossover, giving in this way possibility the user to apply different strategies. Additionally, a phase of local search in the neighborhood of the best individual may be performed at every k' generations (iterations). This may lead to an improvement of the best-found solution.

2.1 Selection strategies

The sequential genetic algorithm GAITET uses the "Elite selection" strategy. $E\%$ of the best individuals is selected among the P individuals of the current population (in GAITET E=10%). These individuals mate each with all others. After the crossover the obtained offspring individuals replace the worst individuals (with high fitness value) in the old population. This selection may be confronted with optimization problems, where plateau(s) of individuals with equal fitness values are available in the feasible domain and the crossover is unable to generate individuals outside the plateau. The second selection strategy in GAITET is based on the trivial "Roulette wheel selection", but the individuals selected for reproduction are ordered in a decreasing order of their fitness values and are mated not randomly, but in the following manner: the first with the last (in the order), the second with next to the last and so on. This kind of mating is used with the aim parent's pairs to be composed of strong differing from one another individuals.

2.2 Crossover

Let $x, y \in B^k$ be vectors constituting a parents pair and $\Omega = \{ \{x,y\}, x, y \in B^k\}$ is the set of such pairs: $x = [x_1,...x_k]^T$, $y = [y_1,...,y_k]^T$. GAITET can perform the usual two-point and three-point crossover, but its advantage is the use of a "diversification" crossover. The parent's pair generates five children in this crossover (which could be often meet in the nature), making an attempt to diversify the available genetic material. The best two children (according their fitness values) among them take part at the creation of the new population, replacing individuals with lower fitness value in the old population. The five children of pair $x, y \in B^k$ are generated as follows:

$x'_i = \{0$ when $x_i = y_i = 0$; 1 in all other cases;$\}$;
$x'' = x*y$; $x''' = |x-y|$;
$x''''_i = \{0$ when $x_i = y_i = 1$; 1 in all other cases;$\}$;
$x'''''_i = \{0$ when $x_i=0$; $y_i=1$; 1 in all other cases;$\}$;

2.3 Local search

Let i and $i+1$ be the consecutive indices of two different components in the k-dimensional 0-1 vector x, i.e. $x_i \neq x_{i+1}$, and let L be defined as a set of all such component pairs. Then let s' be a k-dimensional 0-1 vector, such that $x+s' = x'$, where $x'_i = x'_{i+1} = 0$; and let s'' be a 0-1 vector, such that $x+s'' = x''$, where $x''_i = x''_{i+1} = 1$. The set S is defined as a set of all vector pairs (s', s''), corresponding to the component pairs in L: $S=\{(s'_j, s''_j)/ j \in L\}$. The neighborhood $N(x)$ of each solution x is defined by $N(x) = \{(x'_j, x''_j)/ x'_j = x'_j +s'_j; x''_j = x''_j +s''_j; (s'_j, s''_j) \in S; j \in L\}$. The solutions in the neighborhood $N(x*)$ are enumerated for each $x*$ solution having greatest fitness value at every k' generations. The combination of local search technique with the genetic algorithm ensures higher solutions quality without great additional computational efforts.

2.4 Termination criteria

Two termination criteria are used: a) limit of generations; and b) limit of consecutive generations without improving the best-obtained solution;

2.5 "Pseudo-code" form of algorithm GAITET

Algorithm GAITET (with "Roulette wheel" selection)
Generate an initial population P_0 of 100 individuals; Set $i :=$ 0; (iteration counter);
Evaluate the individuals in P_i;

While no stopping criteria is met **do**
    Set $i := i+1$;
    For j=1,50; **do**
        Select two individuals I_1 and I_2 in P_{i-1};

        Apply the *crossover* operator to I_1 and I_2
    for creating offspring O_1 and O_2;
        Decide whether or not O_1 and O_2 should
    enter P_i for replacing older solutions;
    EndFor
    Create the population P_i from P_{i-1}, replacing
    the worst individuals in P_{i-1} with the best
    generated children individuals**;**
    If i is multiple of a given integer k', perform a local
    search in the neighborhood $N(x^*)$ of the best individual
    x^*;
EndWhile

The mutation is not used in GAITET, because it can change a solution, but contrarily to improvement procedures, the change has unexpected results on the value of the objective function, in sense that it does necessarily improve it (see [5]) and is inefficient. Seeking global convergence the user has possibility to use "diversification" crossover, which can extrapolate beyond the region spanned by the individuals in the population.

III. TEST RESULTS

Useful circuits for test experiments can be found in [7]. In this study five relative small and simple analog circuits are used. They are generated at the Institute of Electromagnetic Theory and Microwave Technique (IETMT), Hannover, Germany. The circuit Opamp (see Table 1, Table 2) has two input signals and the other four circuits have one input signal. One of them – the "Biquad"-filter circuit is presented on Fig. 2 for illustration.
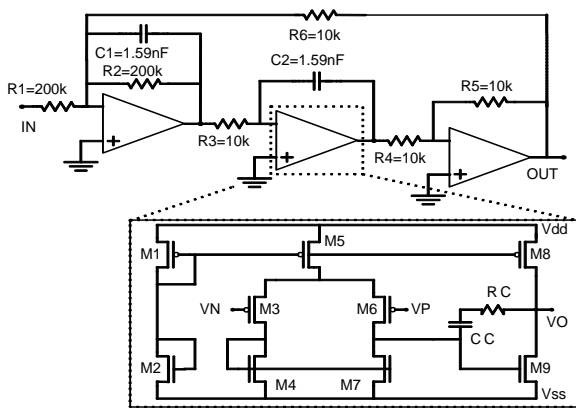
Figure 2: "Biquad"-filter circuit

A Pentium III, 450 MHz, computer is used for the experiments. The obtained results depend strongly on the initial choice of faults, included in the set F_f. The maximal number of faults used in the test experiments was 96. When the "Elite selection" strategy is used the computational time decreases about five times in comparison with the "Roulette wheel selection" strategy, but the quality of the obtained solutions also decreases.

Two different search approaches are used for the experiments with GAITET algorithm. The first one uses a local search phase around the best-found solution $x_b(\Delta t)$ at the end of each generation (iteration). In the second one the local search phase is omitted. The obtained differences between $J(x_b(\Delta t))$-values obtained by means of local search phase and without the local search phase are less than 3% for each of the used circuits, with exception of "Ctvs" circuit, for which the obtained difference is equal to 26.63%. In the most of the cases, the better signals obtained after local search phase do not lead to great increasing of the detected faults number. Hence the local search technique does not exert essential influence on the improvement of the test signals. When local search is used, the total computational time t_{ls} increases in comparison to t (the total time, when no local search is used) about 40% (see Table 1). Nevertheless the local search could be very useful in the cases when for some reason only a small number of genetic iterations have been performed.

In Table 1 and Table 2 are presented the test results after 3 generations (iterations) of GAITET program using "Roulette wheel selection" strategy, two-point crossover and local search phase. The experiments with GAITET on simple problems, when the program TORAD is not used, show that the computational time for performance of 10 iterations may be less than two seconds on a Pentium III computer. For this reason the use of JAVA language does not delay considerably the performance of the program. The evaluation of $J(x(\Delta t))$ functional (1) is the most time-consuming operation, taking almost 100% of the total computational time. This evaluation is performed by TORAD subroutine, written in C++ language.

TABLE 1.
COMPUTATIONAL TIMES OF GAITET

Circuit's name	t [sec]	t_{ls} [sec]	T / t_{ls} [%]
Opamp	3034.002	6043.872	50.200
Biquad	1121.794	1809.647	62.010
Ctvs	2344.092	3410.148	68.739
Bessel3rd	1145.934	1306.887	87.684
Leapfrog	5937.051	7222.918	82.197

Let by x_{bst} be denoted the best-found signal corresponding to the lowest J-value, and by x_s – the standard symmetric signal (The mean deviation of the standard symmetric signal from the worst signal having the highest J-value is 7.143%.). The percent of detected faults from the set F_f for the best and for the standard symmetric signal, denoted by $DF(x_{bst})$ and $DF(x_s)$ correspondingly, is presented in Table 2. The obtained improvement after the optimization of the test signals is denoted by $\Delta DF = DF(x_{bst})–DF(x_s)$.

TABLE 2.
J-VALUES AND FAULTS DETECTION OF GAITET

Circuit's name	$J(x_b)$	$J(x_s)$	$DF(x_{bst})$ [%]	$DF(x_s)$ [%]	ΔDF [%]
Opamp	-0.29602	-0.08801	90	79	11
Biquad	-0.04717	-0.00423	97	92	5
Ctvs	-2.29610	-0.27979	91	83	8
Bessel3rd	-13.5853	-4.18144	96	87	9
Leapfrog	-3.68204	-1.09183	97	90	7

IV. Conclusions

The test experiments with the genetic optimization algorithm GAITET were realized on realistic circuits. The obtained results show that the test signal optimization leads to improvement of fault detection capability. Although the signal quality has been improved in all experimental cases, the mean computational time for the five used circuits is about 1 hour for 3 GAITET iterations. Taking into account that the used circuits are simple and have relative small number of elements, the experiments with more complex circuits and with larger faults set F_f could require more powerful computers. Another way for overcoming the slow performance is the flexible use of GAITET algorithm (for example applying the "Elite selection" strategy, if the obtained improvement of the test signals is sufficient).

The third way for speeding up the GAITET performance is to realize this algorithm in a parallel version. A step in this direction is already made through the creation of a coarse grained parallel genetic algorithm PGAITET, designed to run in a computer network. The advantages of JAVA language for creation of parallel algorithms, which can run under different operating systems, are very important. The parallel version of GAITET is already realized in JAVA by means of JAVA sockets.

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A Robust Approach for the Direct Extraction of HEMT Circuit Elements vs. Bias and Temperature

Alina Caddemi, Nicola Donato and Giovanni Crupi[1]

Abstract **We here present the results of our most recent activity in the implementation of robust and easy-to-perform techniques for the extraction of reliable equivalent circuits for microwave transistors. Our effort also led to the development of a compact software tool written in Agilent VEE language for totally automated measurement and direct model extraction. Its effectiveness has been tested at several bias and temperature points and the modeling results have been compared with those obtained by application of other procedures. This procedure can be adopted for both Schottky-gate devices (MESFET's, HEMT's) and insulated gate devices (RF MOSFET's, CMOS) since no direct polarization of the gate is requested.**

Keywords – **HEMT, MESFET, TEMPERATURE, DIRECT EXTRACTION MODELING .**

I. INTRODUCTION

Modeling and simulation of solid-state active devices are basic aspects of modern advanced electronics and a key point is a rapid and accurate determination of electrical models for CAD of microwave circuits. The target of interest to microwave engineers is the implementation of robust and easy-to-perform techniques for the extraction of reliable equivalent circuits of the devices under test, valid over over a wide range of operating conditions. We here present the results of our most recent activity in this field leading to the development of a compact software tool written in HP VEE language for microwave device measurement and direct model extraction. Its effectiveness has been tested at several bias and temperature points and the modeling results have been compared with those obtained by application of other procedures. The structure of the model network is shown in Fig.1. For the direct extraction of the circuit elements, we first derive the extrinsic ones by measuring the scattering parameters in "off" (V_{GS}=0, V_{DS}=0) and "pinched" (V_{GS}<V_{PO}, V_{DS}=0) bias conditions [1]. Then, the scattering parameters are measured at each desired bias point and the relevant data are employed to calculate the intrinsic elements [2]. This procedure can be adopted for both Schottky-gate devices (MESFET's, HEMT's) and insulated gate devices (RF MOSFET's, CMOS) since no direct polarization of the gate is requested such as proposed in [3]. The consistency of the procedure has been tested upon a set of on wafer pseudomorphic HEMT's having fixed gate length (0.25 μm) and scaled gate widths (300, 600, 900 μm) characterized in the following conditions: 0≤ V_{DS}≤6 V, -1≤ V_{GS}≤0 V, 290≤ T_{DEV}≤340 K. The on wafer thermal measurement system has been totally designed and realized in our lab. It allows a 130 K temperature span (220 to 350 K) with an accuracy of ±0.2 K obtained by means of a Peltier cell controlled with a PID loop [4]. The value trends of each circuit elements graphed vs. bias, temperature and gate width exhibit a highly consistent behaviour enhancing the robustness of the procedure. As a cross-check, the circuit models have been implemented in a commercial microwave package (*Microwave Office 2001, by Applied Wave Research*) and the scattering parameters generated by the models have been compared with the measured data.

II. EXTRACTION PROCEDURE

Several direct extraction procedures have been developed to determine the small signal equivalent circuital model of FET's by means of scattering ([S]) parameter measurements. These techniques allow to extract the extrinsic circuit elements from [S] parameter measurements at fixed bias conditions and the intrinsic circuit elements from [S] measurements at the operating bias point. By the procedure described in [1], it is possible to extract the circuit model shown in Fig. 1 with no direct polarization of the gate Schottky junction, thus preserving device performances from an excessive drain current. The developed software allows to control every single variable concerning the characterization and modeling processes. It is fast and easy to use without complex operations required from the user. The parasitic elements are extracted from [S] parameter measurements at OFF (i.e., with the three electrodes at the same potential) and STRONG PINCH-OFF (i.e., at V_{DS} = 0 and V_{GS} < V_{PO}) bias conditions. At both bias points (pinched and off), V_{DS} is equal to zero in order to achieve a symmetric circuital configuration and to simplify the associated equivalent circuit model. The OFF [S] parameter set is converted into a set of [Z] parameters to compute the parasitic inductances and resistances.
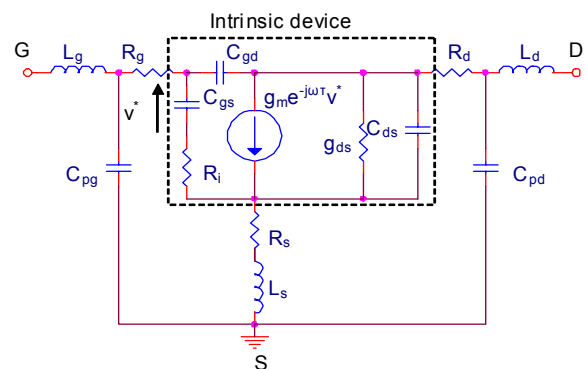

Fig. 1 FET equivalent circuit model .

We can write the [Z] parameters of the OFF device as reported in the following equations:

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$$Z_{11} = R_s + R_g + 0.5R_{ch} + j\left[\omega\left(L_s + L_g\right) - \frac{1}{\omega C_g}\right] \quad (1)$$

$$Z_{12} = Z_{21} = R_s + 0.5R_{ch} + j\omega L_s \quad (2)$$

$$Z_{22} = R_d + R_s + R_{ch} + j\omega\left(L_s + L_d\right) \quad (3)$$

The parasitic inductances L_s and L_d can be extracted from imaginary part of (2) and (3). Once L_s is computed, we can extract L_g by considering the imaginary part of (1) at two different frequency values and assuming L_g and C_g constant. The parasitic resistances can be computed by means of the real part of eqs.(1), (2), (3) and the real part of Z_{11} at the pinch-off condition:

$$\text{Re}[Z_{11}] = R_s + R_g \quad (4)$$

For the extraction of parasitic capacitances, we need again the [S] parameters at pinch-off conditions and convert them in [Z] parameters. As a first step, we subtract the resistances and inductances previously computed:

$$Z_{11} - R_s - R_g - j\omega\left(L_s + L_g\right) \quad (5)$$

$$Z_{12} - R_s - j\omega L_s = Z_{21} - R_s - j\omega L_s \quad (6)$$

$$Z_{22} - R_d - R_s - j\omega\left(L_s + L_d\right) \quad (7)$$

and then transform the results into [Y] parameters:

$$Y_{11} = j\omega\left(2C_b + C_{pg}\right) \quad (8)$$

$$Y_{12} = Y_{21} = j\omega C_b \quad (9)$$

$$Y_{22} = j\omega\left(C_b + C_{pd} + C_{ds}\right) \quad (10)$$

By means of eqs. (8) and (9), we extract the values of C_b ($C_b = C_{gs} = C_{gd}$) and C_{pg}. From eq. (10), we can compute C_{pd} by assuming $C_{pd} = C_{ds}/4$ [1]:

$$C_{pd} = \frac{1}{5}\left(\frac{Y_{22}}{\omega} - C_b\right) \quad (11)$$

Finally, we determine the intrinsic elements from HOT [S] parameters by applying a deembedding procedure of the extracted parasitic elements. By transforming [S] in [Z] parameters, we subtract the gate and drain parasitic series inductances:

$$Z_{11} - j\omega L_g \quad (12)$$

$$Z_{22} - j\omega L_d \quad (13)$$

With a conversion to [Y] parameters, we eliminate the effects of the two parasitic parallel capacitances:

$$Y_{11} - j\omega C_{pg} \quad (14)$$

$$Y_{22} - j\omega C_{pd} \quad (15)$$

A successive transformation into [Z] parameters allows us to subtract the three resistances and the source inductance, all of them as series elements:

$$Z_{11} - R_s - R_g - j\omega L_s \quad (16)$$

$$Z_{12} - R_s - j\omega L_s = Z_{21} - R_s - j\omega L_s \quad (17)$$

$$Z_{22} - R_d - R_s - j\omega L_s \quad (18)$$

Finally, with the last [Y] conversion and using eqs.(19)-(25) we determine the intrinsic elements [4]:

$$C_{gd} = -\frac{\text{Im}(Y_{12})}{\omega} \quad (19)$$

$$C_{gs} = \frac{\left[\text{Im}(Y_{11}) - \omega C_{gd}\right]}{\omega}\left[1 + \frac{\text{Re}^2(Y_{11})}{\left[\text{Im}(Y_{11}) - \omega C_{gd}\right]^2}\right] \quad (20)$$

$$g_{ds} = \text{Re}(Y_{22}) \quad (21)$$

$$C_{ds} = \frac{\text{Im}(Y_{22}) - \omega C_{gd}}{\omega} \quad (22)$$

$$R_i = \frac{\text{Re}(Y_{11})}{\text{Re}^2(Y_{11}) + \left[\text{Im}(Y_{11}) - \omega C_{gd}\right]^2} \quad (23)$$

$$\tau = \frac{1}{\omega}arcsen\left[\frac{-\text{Im}(Y_{21}) - \omega C_{gd} - \omega C_{gs}R_i\,\text{Re}(Y_{21})}{g_m}\right] \quad (24)$$

$$g_m = \left[\left[\text{Im}(Y_{21}) + \omega C_{gd}\right]^2 + \text{Re}^2(Y_{21})\right]^{\frac{1}{2}}\left(1 + \omega^2 R^2{}_i C_{gs}{}^2\right)^{\frac{1}{2}} \quad (25)$$

III. RESULTS

By means of the procedure here described, several pHEMT's from TRIQUINT foundry (USA) have been modelled. These devices have 250 μm pitch, 0.25 μm gate length and $300 - 600 - 900$ μm of gate widths. The on wafer [S] parameter measurements were performed in the 350 MHz - 6 GHz frequency range with a step of 297.5 MHz. In Figs. 2-4, the eight parasitic elements of a 900 μm device vs. frequency are reported. It can be seen that the element values reach a constant level as the frequency increases.
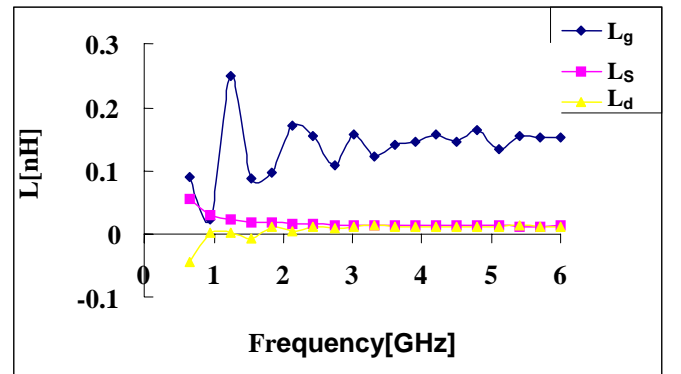

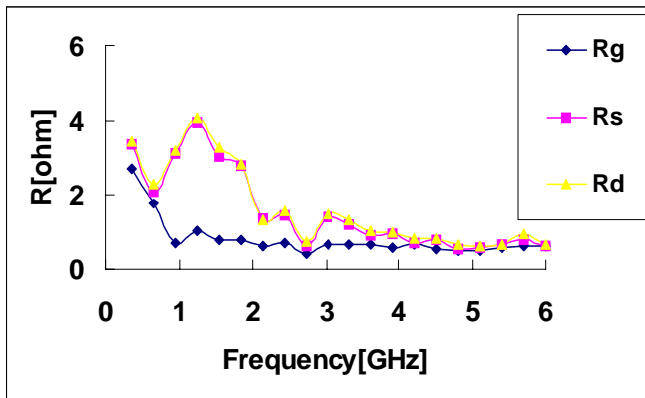**Fig.2** Frequency dependence of the parasitic inductances

Fig.3 Frequency dependence of parasitic resistances

The intrinsic elements of the small signal equivalent model have been extracted at several bias conditions. The behavior of the tranconductance g_m at 56 bias points is reported in Fig. 5 for a 900μm gate width device.
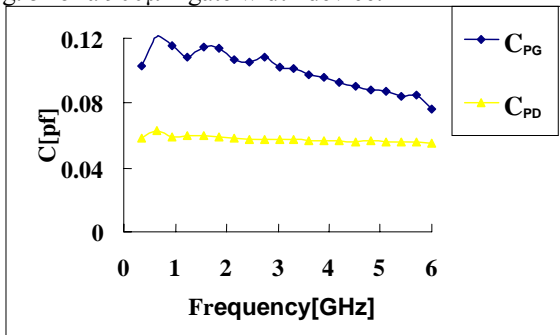

Fig.4 Frequency dependence of parasitic capacitances

The consistency of the extracted elements values has been evaluated as a function of either the bias conditions and the device dimensions. Both extrinsic ed intrinsic elements depend on the gate width. As an example, in Fig 6 the behavior of the transconductance is reported and clear scaling effects can be seen.

Fig.5 Bias conditions dependence of the transconductance g_m
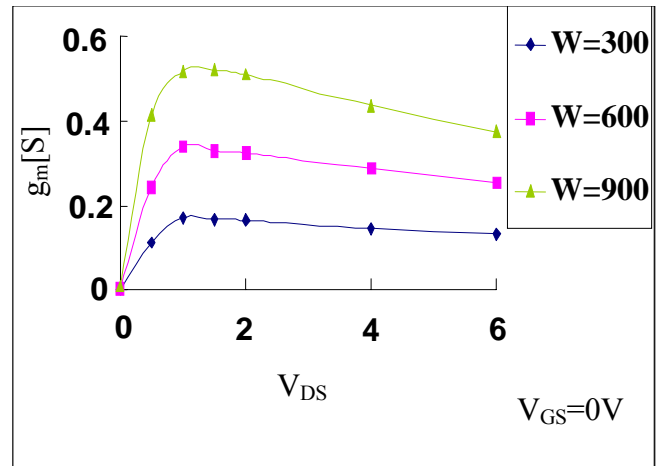
Fig.6 Behavior of g_m vs. V_{ds} for devices of scaled gate widths

We report in Figs. 7-10 the comparison between the measured and simulated [S] parameters sets, as outputs of the AWR software, for a 900 μm device. This test thus gives a demonstration of the fitting performance of the extracted model.
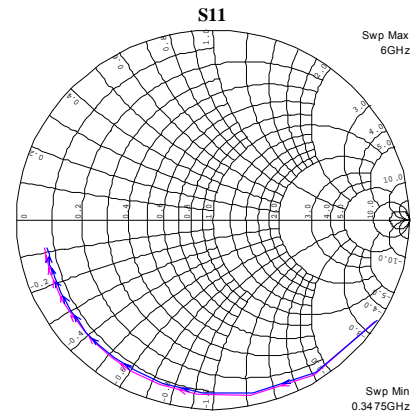
Fig. 7 S_{11} parameter measured and modeled
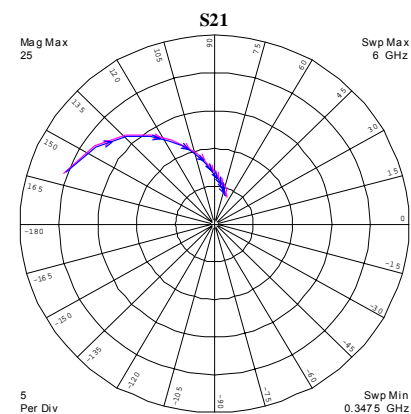
Fig. 8 S_{21} parameter measured and modeled

S12

Fig. 9 S_{12} parameter measured and modeled

S22
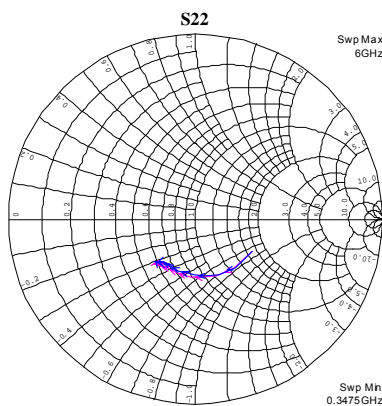
Fig. 10 S_{22} parameter measured and modeled

at several bias and temperature conditions with minimum handling required. The software facilities guide the user during all the characterization and modeling procedures, with interactive messages and suggestions.

CONCLUSIONS

We here present the results of our most recent activity concerning the implementation of robust and easy-to-perform techniques for the extraction of reliable equivalent circuits of microwave transistors. The work also led us to the development of a compact software tool written in Agilent VEE language for device measurement and direct model extraction. Its effectiveness has been tested at several bias and temperature points and the modeling results have been compared with those obtained by application of other procedures. This procedure can be adopted for both Schottky-gate devices (MESFET's, HEMT's) and insulated gate devices (RF MOSFET's, CMOS) since no direct polarization of the gate is requested. The high level of automation lets the user make a large number of measurements and relevant model extraction with high accuracy and great time saving.

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The characterization and modelling processes of the devices was completely automated by means of a home-made software developed with Agilent VEE6 tools. By means of this software is possible to extract a large number of models

Microwave Transistor Noise Models Including Temperature Dependence

Zlatica Marinković, Vera Marković, Alina Caddemi[1], Bratislav Milovanović

Abstract- **This paper presents results of transistor noise parameters' modeling including their temperature dependence. Transistor noise models based on multilayer perceptron neural networks are proposed. Using transistor noise data for certain number of temperatures, appropriate neural networks were trained. Once trained the developed model can be used for efficient prediction of transistor noise parameters for any operating temperature, avoiding additional measurements.**

Keywords - **Neural networks, microwave transistors, noise parameters, temperature.**

I INTRODUCTION

Low noise microwave transistors are very important part of active circuits in modern communication systems, especially in mobile, wireless and satellite systems. For the circuit design purposes it is necessary to know transistor behavior for different operating conditions in a wide frequency range. Since many of these circuits have to work at different temperature condition, it is necessary to know how transistor will operate and what its noise performance will be when the temperature is changed. In order to avoid complex and time consuming measurements for acquiring transistor noise data necessary for design purposes, many transistor noise models are developed, e.g. [1], [2]. But, these models, based on transistor equivalent circuit, are developed for specified operating conditions and nominal temperature. Therefore, for any new bias conditions or for a new ambient temperature, a new set of experimental data has to be gathered and new recalculating of model elements has to be done.

Here, a neural network approach to the transistor noise modeling is suggested. As it is very-well known, artificial neural networks have ability to learn from the presented data. Therefore, they have been applied in a wide area of problems. Especially, they are interesting for problems not fully mathematically described. They can learn highly non-linear input-output dependences and once trained they can predict response with quite a good accuracy without changes in their structure and without additional knowledge. Neural models are simpler than physically based ones, but retain the similar accuracy. They require less time for response providing; therefore, using of neural models can make simulation and optimization processes less time-consuming, shifting much computation from on-line optimization to off-line training.

Neural networks have been successfully applied in the microwave area for the passive and active component modeling, [3]. There are several neural models referring to the microwave transistors. For instance, scattering parameters, [4], [5], dc current –voltage characteristics, [6], and elements of small-signal intrinsic circuit, [7], have been modeled. In the previous work, the authors of this paper have developed some noise models based on neural networks trained to predict transistor noise parameters dependence on bias conditions and frequency, [8]-[10].

However, several research results show that noise parameters of microwave transistors are dependent on temperature. For instance, temperature-dependent noise characterization of transistors has been extensively performed by the research group at the University of Messina, [11], [12], using a specially developed automated measurement system. It was shown that noise parameters are generally affected by thermal variations. Therefore, if one intends to develop transistor noise models valid over the wide range of operating conditions, it is necessary to include temperature dependence in transistor noise models.

In the authors' most recent work, neural models for transistor noise parameters that include the dependence on both frequency and temperature have been developed. The details of this modeling procedure and the obtained results will be presented in the further text of this paper.

II MULTILAYER PERCEPTRON NEURAL NETWORK

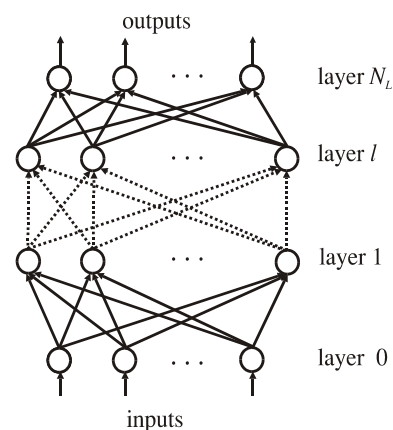A standard multilayer perceptron (MLP) neural network is shown in Fig.1. [3].

Fig.1. *MLP neural network*

This network consists of an input layer (layer 0), an output layer (layer N_L) as well as several hidden layers.

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Input vectors are presented to the input layer and fed through the network that then yields the output vector. The l-th layer output is:

$$\mathbf{Y}_l = F(\mathbf{W}_l \mathbf{Y}_{l-1} + \mathbf{B}_l) \qquad (1)$$

where $\mathbf{Y}_l$ and $\mathbf{Y}_{l-1}$ are outputs of l-th and (l-1)-th layer, respectively, $\mathbf{W}_l$ is weight matrix between (l-1)-th and l-th layer and $\mathbf{B}_l$ is bias matrix between (l-1)-th and l-th layer. Function F is an activation function of each neuron. Here, a linear activation function for input and output layer and for hidden layers a sigmoid function in the form

$$F(u) = \frac{1}{1 + e^{-u}} \qquad (2)$$

has been chosen.

The neural network learns relationships among sets of input-output data (training sets) during a training process. First, input vectors are presented to the input neurons and output vectors are computed. The output values are compared with desired values and the errors are computed. Error derivatives are then calculated and summed up for each weight and bias until whole training set has been presented to the network. These error derivatives are then used to update the weights and biases for neurons in the model. The training process proceeds until errors are lower than the prescribed values or until the maximum number of epochs (epoch - the whole training set processing) is reached. Once trained, the network provides fast response for different input vectors, even for those not included in the training set, without additional computational effort.

III Transistor Noise Modeling

Any noisy two-port component can be characterized by the *noise figure F,* which is a measure of the degradation of signal-to-noise ratio between input and output of the component due to component-generated noise, [13]. The noise figure depends on the generator reflection coefficient at the device input. A commonly used relationship that describes this dependence has the following form:

$$F = F_{\min} + \frac{4R_n}{Z_0} \frac{\left| \Gamma_g - \Gamma_{opt} \right|^2}{\left(1 - \left| \Gamma_g \right|^2\right)\left|1 + \Gamma_{opt}\right|^2}. \qquad (3)$$

In this expression, $F_{\min}$ (minimum noise figure) R_n (equivalent noise resistance) and Γ_{opt} (optimum reflection coefficient) are the noise parameters of the device. The noise parameters describe inherent noise behavior of the transistor and are independent of a connected circuit. Z_0 is normalizing impedance, usually 50 Ω.

For noise parameter modeling including the temperature dependence, use of MLP neural networks has been proposed, as it is presented in Fig. 2 in the form of a block diagram. These networks have two neurons in the input layer corresponding to:

- Temperature, T and
- Frequency, f.

The output layer consists of four neurons corresponding to:

- Minimum noise figure ($F_{\min}$ (dB)),
- Magnitude of optimum reflection coefficient,
- Angle of optimum reflection coefficient and
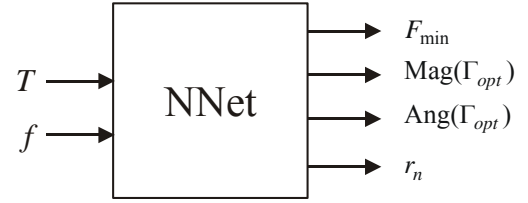- Equivalent noise resistance

Fig. 2. *Neural model for noise parameters dependence on bias conditions and frequency*

For this purpose MLP neural networks with one or two hidden layers could be used. Number of hidden layers depends on the training data size and the data behavior.

In addition, with the aim to obtain as best modeling as possible, the neural networks with different number of neurons in the hidden layer(s) have been trained. In order to quantify models' accuracy, average test error (ATE [%]), worst-case error (WCE [%]), and the Pearson Product-Moment correlation coefficient r between the referent and the modeled data were calculated, [1]. The coefficient r is defined by:

$$r = \frac{\sum (x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\sum (x_i - \bar{x})^2 \sum (y_i - \bar{y})^2}} \qquad (4)$$

where x_i is referent value, y_i is the neural network computed value, $\bar{x}$ is the referent sample mean, and $\bar{y}$ is the neural network sample mean. The correlation coefficient indicates how well the modeled values match the referent values. A correlation coefficient near one indicates an excellent predictive ability, while a coefficient near zero indicates little predictive ability.

IV Modeling Example

In this section, a modeling example referring to the NEC20283A transistor series (5 devices) will be presented.

The training data used in modeling procedure is obtained from direct noise measurements, performed by the research group with the University of Messina.

Transistor's noise parameters were measured for different ambient temperatures in (233-333) K range, using an automated measurement system. The data refers to the frequency range (6-18) GHz. The devices were in packaged form and the characterization was performed by using a metallic air-coaxial test fixture enclosed within a thermostatic chamber. The experimental data were processed by extracting a weighted average value at each frequency over the measured samples. Therefore, the noise parameters determined represente the performances of the typical device from a statistical point of view.

The neural network architecture with one hidden layer was chosen. Networks with different number of hidden neurons were trained using the same training set. On the base of above-mentioned criteria, the developed neural models are compared. An additional test is performed as well. Namely, in some cases network over learning could be happen. It is happen sometimes when the network is too much forced to learn training data. In this case, the network prediction for the input values that were used for the training can be excellent (meaning very small ATE and WCE and correlation coefficient very close to one), but for some other inputs the network can give very bad and unexpected results. Therefore, for each trained network its responses for continuous changes of temperature and frequency (small step of change) are generated and plotted, and visually check is performed.

In the case of the mentioned transistor, a model with 10 neurons has got the best prediction from all considered neural models. In Table 1, prediction statistics for training data is given. It could be seen that ATE is less than 0.5%, WCE less than 3% and correlation coefficient greater than 0.9995. Those results are very good and acceptable.

Table 1. *Neural model prediction - statistics*

	ATE[%]	WCE[%]	*r*
F_{min}	0.2711	1.1381	0.99987
$\left|\Gamma_{opt}\right|$	0.4467	1.8063	0.999807
$Ang(\Gamma_{opt})$	0.3223	1.78356	0.999901
r_n	0.4516	2.8782	0.999583

(a)

(b)

(c)

(d)
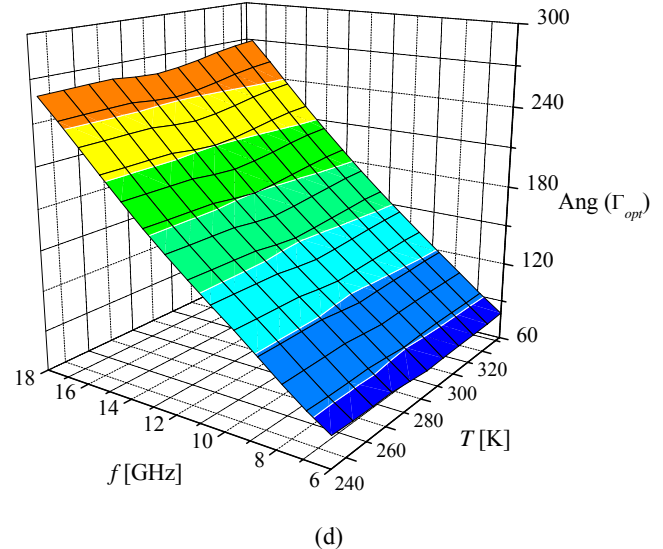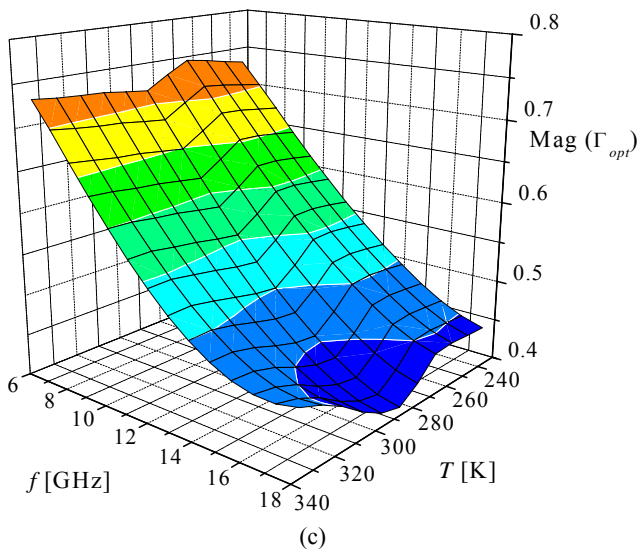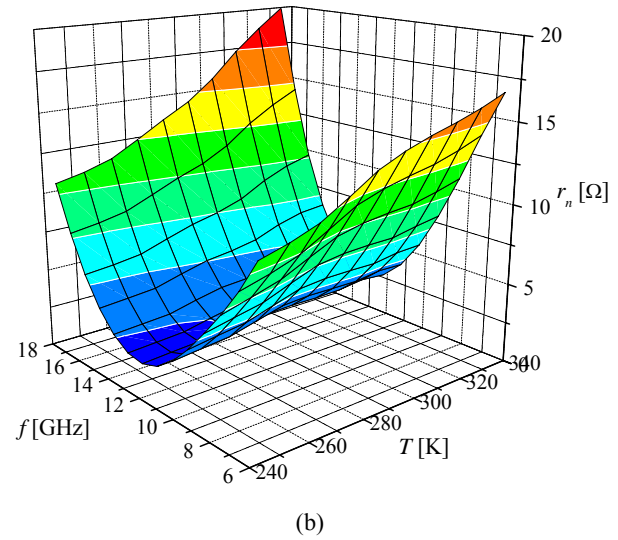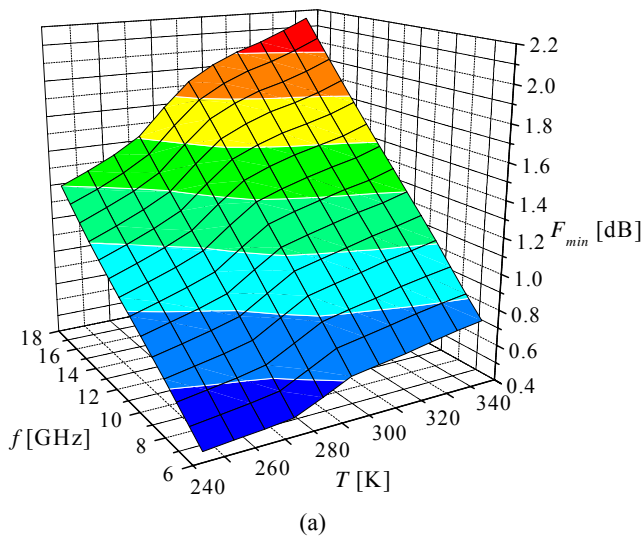
Fig. 3. *Prediction of transistor noise parameters using neural model*
(a) Minimum noise figure; (b) Equivalent noise resistance;
(c) Magnitude of optimum reflection coefficient; (d)Angle of optimum reflection coefficient

Further, in Fig 3, three-dimensional plots of all four noise parameters vs. temperature and frequency, obtained using this neural model, are given.

It is clear that the prediction of transistor noise parameters for any other temperature or frequency different from the ones used for the training purposes does not require any

additional measurements of transistor noise parameters or changes in the model. Simply, neural model responses for desired combinations of temperature and frequency should be calculated.

V Conclusion

For fast and efficient design of low-noise microwave circuits, microwave transistor models that can reliably predict noise parameters in a wide range of frequencies and operating conditions are needed. Since many active microwave circuits have to work in an environment whose temperature can be changed, it is important to know how transistor noise performances vary with the temperature.

Here, one possible approach to the noise parameters modeling including temperature dependence using neural networks has been proposed. Multilayer perceptron neural networks are trained with the aim to learn noise parameters dependence on temperatures and frequency.

It is necessary to measure transistor noise parameters at different temperatures for training data acquiring only. Once trained neural models do not require additional measurements or additional change in the model for any combination frequency - ambient temperature from the considered range but different from ones used for the training purposes. Process of optimization of model elements is shifted from microwave simulators to training of neural networks. After training of neural models, transistor noise prediction is very efficient, fast, simple and highly accurate.

Since this approach belongs to black-box approaches, it is independent of mechanism of transistor noise generated, and therefore, it can be applied to other types of microwave transistors.

Additionally, it is possible to develop transistor neural models for prediction of transistor noise parameters not only for different temperatures and frequencies but also for different bias conditions. This could be done by introduction of new input neurons corresponding to bias conditions. In this case, the training process requires gathering of transistor noise data for different bias and temperature conditions in operating frequency range.

Acknowledgements

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RF MOSFETs Noise Modeling - the Wave Approach

Olivera R. Pronić, Vera V. Marković

Abstract — **This paper presents a new procedure for noise modeling of microwave MOSFETs based on the wave approach. The procedure is based on circuit theory concepts and on similar kind of analysis we proposed earlier for MESFETs / HEMTs noise modeling. Noise wave parameters are derived in terms of three equivalent noise temperatures. Noise parameter characteristics obtained by proposed modeling procedure are compared with the measured ones for a typical RF MOSFET.**

Keywords – **RF MOSFET, noise temperatures, noise wave parameters**

I INTRODUCTION

CMOS (Complementary – Metal – Oxide - Semiconductor) technology has now reached a state of evolution, in terms of both frequency and noise, where it is becoming a serious contender for wireless applications in the GHz range, [1]-[3]. Today ultradeep-submicrometer technologies have surpassed the transit frequencies achieved by bipolar transistors and enable operating frequencies which cover the frequency range of many popular wireless products today, such as cell phones, WAP, GPS, Home RF, Bluetooth, etc.

The main advantages of RF CMOS technology over the traditionally used GaAs or heterojuction technology lie in low production cost and the ability for high-level integration and combining digital, analog and RF circuits on the same chip. These properties together with low power consumption, small dimensions and weight and high reliability make this technology very promising for multi-mode, multi-band third generation mobile terminals.

Advances in the fabrication of ultradeep-submicrometer RF MOSFETs and intentions to apply them for microwave wireless products have induced many efforts during the last years in order to develop the appropriate device models. Small-signal and noise modeling are of the special interests. For RF applications, noise performance plays a very important role. The thermal noise of sub-micrometer MOS transistors does not satisfy well-known long-channel approximation. The increase of noise in the short channels was found by experimental investigations and could be explained by some effects caused by velocity saturation and/or hot carriers [4]. But the exact physical mechanisms of noise generating in RF MOSFETs are not yet known.

There are some physically-based compact MOSFET models commercially available, for instance BSIM4, [5], specially offered for RF applications. However, it is often too complex to implement such a compact model with many input physical parameters for circuit simulation purposes.

Having in mind that many effects inside the short-channel MOSFETs are very complex and not yet completely explained, a circuit-oriented modeling approach can be very convenient for CAD purposes. Several methodologies were developed for extracting parameters related to MOSFET equivalent circuit, including the noise sources, from measurements.

On the other hand, during the last two decades, much more work has been done for developing small-signal and noise models of the traditionally used microwave transistors, like MESFETs. Small-signal equivalent circuits of MESFETs and MOSFETs are very similar. Consequently, having a great experience in noise modeling of MESFETs, our basic idea was to apply the similar kind of analysis to RF MOSFET's noise modeling.

There are several different representations of a noisy two-port circuit, [6]. Each representation is characterised by the existence of a noiseless two-port network and two additional correlated noise sources. Noise is typically characterised using combinations of equivalent voltage and current sources.

A significant contribution to MESFET noise modeling was made by Pospieszalski, [7]. The noise model he presented is based on *H* representation of MESFET intrinsic circuit with two uncorrelated noise sources. For noise parameters calculation, it is necessary to know equivalent circuit elements and two frequency independent temperatures called equivalent gate and drain temperature.

For high frequency circuit applications, however, a wave interpretation of noise seems more appropriate. It is shown, [8], that the wave approach could be useful for both noise modeling and measurement of microwave FETs. Combining the wave approach with Pospieszalski's concept, simple expressions for MESFET and HEMT noise wave parameters were derived, [8].

In this paper we applied a similar procedure for RF MOSFET's noise parameters determination. For the reason of better accuracy, the noise model with two uncorrelated noise sources is extended by introducing the correlation between them. Therefore, the noise wave parameters are obtained in terms of three equivalent temperatures: gate, drain and correlation temperature, as well as, *S* parameters. The standard noise parameters are derived as the function of the scattering parameters and the wave parameters calculated in the described way. The noise model where the correlation is ignored, [8], is also considered and the comparative analysis is done. It is shown that our model has better accuracy than the existing one.

The complete microwave MOSFETs' noise modeling procedure proposed in this paper is based on circuit theory concepts and therefore is very convenient for implementation in the commercial high-frequency circuit simulators.

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II RF MOSFET NOISE MODEL

Circuit-oriented noise modeling of microwave transistors is based mostly on the well-known fact that any linear noisy two-port may be represented by a noiseless two-port and two external correlated noise sources, [6].

We considered a commonly used MOSFET's small-signal equivalent circuit, as shown in Fig. 1 ($y_m = g_m e^{-j\omega\tau}$). The intrinsic circuit with the noise sources included is denoted by the dashed line. H representation of the intrinsic circuit with two correlated noise sources is applied.

Extending the Pospieszalski's concept, [7], three equivalent noise temperatures are assigned to the transistor intrinsic equivalent circuit, as it is shown in Fig. 1.
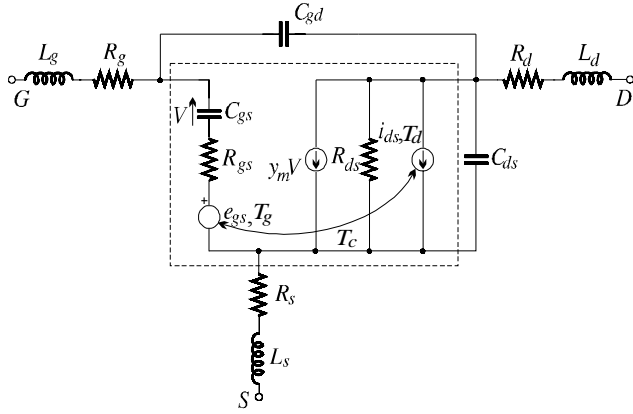
Fig.1. MOSFET small-signal equivalent circuit including noise sources

The equivalent gate and drain temperature, T_g and T_d, are assigned to the resistance R_{gs} and conductance $G_{ds}=1/R_{ds}$, respectively, so that

$$\langle |e_{gs}|^2 \rangle = 4kT_g R_{gs} \Delta f , \qquad (1)$$

$$\langle |i_{ds}|^2 \rangle = 4kT_d G_{ds} \Delta f , \qquad (2)$$

where the brackets < > indicate the time average, k is Boltzmann's constant and Δf is noise bandwidth (it is assumed that $\Delta f = 1$Hz).

The third equivalent temperature, the correlation temperature, is introduced here with the aim to express the correlation between the noise sources. This parameter has a complex value, $T_c = |T_c| e^{j\omega\tau_c}$, and it is defined in the following way:

$$\langle e_{gs} i_{ds}^* \rangle = \rho_c \sqrt{\langle |e_{gs}|^2 \rangle \langle |i_{ds}|^2 \rangle} = 4kT_c \Delta f , \qquad (3)$$

where ρ_c is the correlation coefficient.

The remaining parasitic resistances generate thermal noise according to their absolute temperature.

With the aim to determine the noise wave parameters of a MOSFET intrinsic circuit, we considered an S representation of a noisy two-port, as shown in Fig. 2. The linear matrix equation describing this noisy two-port is

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} + \begin{bmatrix} b_{n1} \\ b_{n2} \end{bmatrix} , \qquad (4)$$

where a_i and b_i are the incident and output waves at the i-th port (i=1, 2), respectively, and the noise wave sources b_{n1} and b_{n2} represent noise generated in a noisy two-port.

Generally, the elements of noise source vector are correlated and characterized by a correlation matrix C_S given by

$$C_s = \begin{bmatrix} \langle |b_{n1}|^2 \rangle & \langle b_{n1} b_{n2}^* \rangle \\ \langle b_{n2} b_{n1}^* \rangle & \langle |b_{n2}|^2 \rangle \end{bmatrix} , \qquad (5)$$

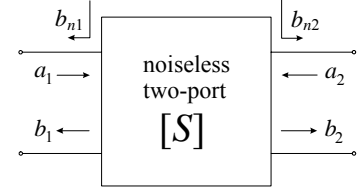where * indicates complex conjugation.

Fig. 2. S representation of a noisy two-port

The formulas for noise wave sources b_{n1} and b_{n2} in terms of voltage and current noise sources, e_{gs} and i_{ds}, respectively, are derived in the following form, [9]:

$$b_{n1} = \frac{e_{gs}(1 - S_{11})}{2\sqrt{Z_0}} , \qquad (6)$$

$$b_{n2} = -\frac{\sqrt{Z_0}}{2}(1 + S_{22})i_{ds} - \frac{S_{21}}{2\sqrt{Z_0}} e_{gs} , \qquad (7)$$

and

$$\langle b_{n1} b_{n2}^* \rangle = -\frac{(1-S_{11})S_{21}^* \langle |e_{gs}|^2 \rangle}{4Z_0} - \frac{(1-S_{11})(1+S_{22}^*)\langle e_{gs} i_{ds}^* \rangle}{4} . \qquad (8)$$

By applying these expressions and the proposed noise model (equations (1)–(3)), the noise wave parameters for the transistor intrinsic circuit are obtained as:

$$\langle |b_{n1}|^2 \rangle = kT_g \left(1 - |S_{11}|^2\right) , \qquad (9)$$

$$\langle |b_{n2}|^2 \rangle = kT_d \left(1 - |S_{22}|^2\right) + \frac{|S_{21}|^2}{|1-S_{11}|^2} \langle |b_{n1}|^2 \rangle + \\ + 2\operatorname{Re}\{kT_c S_{21}(1+S_{22}^*)\} , \qquad (10)$$

$$\langle b_{n1} b_{n2}^* \rangle = \frac{S_{21}^*}{S_{11}^* - 1} \langle |b_{n1}|^2 \rangle - kT_c(1-S_{11})(1+S_{22}^*) . \qquad (11)$$

Ignoring the correlation between noise sources in transistor noise model, ($\langle e_{gs} i_{ds}^* \rangle = 0$), expressions (9) - (11) are reduced to those presented in [8].

The complete expressions for the noise wave parameters in terms of the intrinsic circuit elements and three equivalent noise temperatures are:

$$\langle |b_{n1}|^2 \rangle = \frac{4kT_g R_{gs} Z_0 \omega^2 C_{gs}^2}{1 + \omega^2 C_{gs}^2 (R_{gs} + Z_0)^2} , \qquad (12)$$

$$\langle |b_{n2}|^2 \rangle = \frac{4kT_g R_{gs} Z_0 g_m^2 R_{ds}^2}{(Z_0 + R_{ds})^2 [1 + \omega^2 C_{gs}^2 (R_{gs} + Z_0)^2]} + \frac{4kT_d R_{ds} Z_0}{(R_{ds} + Z_0)^2} - \\ - 8\operatorname{Re}\left\{ \frac{kT_c y_m}{1 + j\omega C_{gs}(R_{gs} + Z_0)} \right\} \frac{R_{ds}^2 Z_0}{(R_{ds} + Z_0)^2} \qquad (13)$$

$$\langle b_{n1}b_{n2}^*\rangle = \frac{j4kT_gR_{gs}R_{ds}Z_0\omega C_{gs}y_m^*}{(R_{ds}+Z_0)\left[1+\omega^2C_{gs}^2(R_{gs}+Z_0)^2\right]} -$$
$$- j\frac{4kT_cR_{ds}Z_0\omega C_{gs}}{(R_{ds}+Z_0)\left[1+j\omega C_{gs}(R_{gs}+Z_0)\right]} \quad . \tag{14}$$

III NUMERICAL RESULTS

The numerical results presented here are related to the modeling of RF MOSFETs fabricated by 0.35 μm technology, [10]. All simulations are performed within the microwave circuit simulator Libra, [11].

At the beginning, the equivalent circuit element values are extracted from the scattering parameter data. With the aim to obtain as accurate small-signal model as possible an extended set of optimization goals (S parameters, input and output reflection coefficients, stability factor and maximum available gain) is used, [12]. The following element values are extracted: R_g=5.68Ω, L_g=2.83pH, R_d=4.11Ω, L_d=6.86pH, R_s=0.05Ω, L_s=0.1pH, g_m=8.73mS, τ=3.12ps, C_{gd}=14.72fF, R_{gs}=0.6Ω, C_{gs}=157.1fF, R_{ds}=1368.9Ω and C_{ds}=140.2fF.

For the noise wave parameters calculation, in addition to the equivalent circuit element values, it is also necessary to know the equivalent noise temperatures. These temperatures are obtained by using the optimization capabilities of Libra, in the following way: Noise parameters of intrinsic circuit may be expressed in terms of noise wave parameters and scattering parameters by finding the inverse relations to the following ones, [8],

$$\langle|b_{n1}|^2\rangle = kT_0\left(F_{min}-1\right)\left(|S_{11}|^2-1\right)+\frac{4kT_0R_n}{Z_0}\frac{|1-S_{11}\Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2}, \tag{15}$$

$$\langle|b_{n2}|^2\rangle = |S_{21}|^2kT_0\left(F_{min}-1+\frac{4R_n}{Z_0}\frac{|\Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2}\right), \tag{16}$$

$$\langle b_{n1}b_{n2}^*\rangle = -\frac{S_{21}^*\Gamma_{opt}^*}{|1+\Gamma_{opt}|^2}\frac{4kT_0R_n}{Z_0}+\frac{S_{11}}{S_{21}}\langle|b_{n2}|^2\rangle . \tag{17}$$

After that, the remaining parasitic elements should be connected and the topology of entire transistor is described. Finally, the noise temperatures are optimized with the aim that the complete model fits the measured S parameters and noise parameters. The extracted noise temperatures are T_g=5525 K, T_d=7987 K, and the magnitude and angle of the correlation temperature are $|T_c|$=30.4 K and τ_c=94.8 ps, respectively. It can be observed that the noise temperatures obtained for RF MOSFET are much higher than those typically obtained for microwave MESFET's, [13].
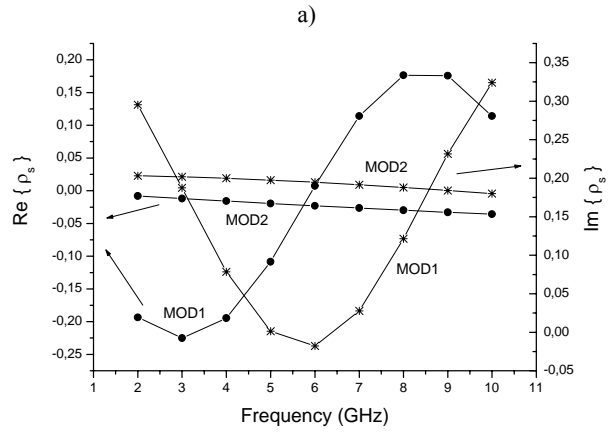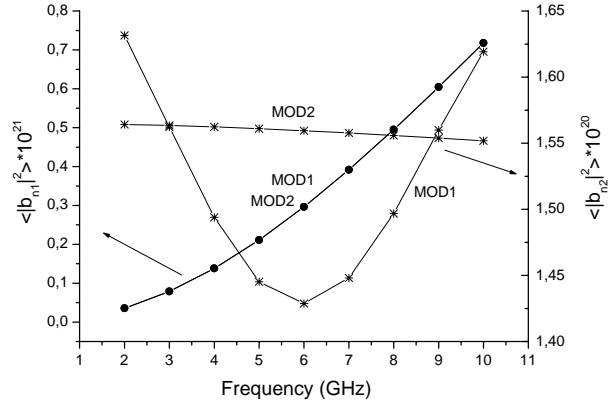

a)

b)

Fig. 3. a) The frequency dependence of the strength of noise wave sources; b) The frequency dependence of the real and imaginary part of correlation coefficient

The frequency dependences of the noise wave parameters are shown in Fig. 3. The correlation coefficient ρ_S is defined as $\rho_S = \dfrac{\langle b_{n1}b_{n2}^*\rangle}{\sqrt{\langle|b_{n1}|^2\rangle\langle|b_{n2}|^2\rangle}}$. Noise wave parameters of RF MOSFET are modeled in two different ways. The frequency dependences of noise wave parameters obtained by using the derived expressions ((12) - (14)), as well as, the ones where the correlation in transistor noise model is ignored ($\langle e_{gs}i_{ds}^*\rangle=0$), [8], are shown. The corresponding characteristics are denoted by MOD1 and MOD2, respectively. It is obvious that the same strength of noise wave sources is obtained only for the noise source at the input. The other noise wave parameters deviate because of the influence of the terms containing correlation temperature.

With the aim to perform a comparison with the available experimental data, [10], the noise wave parameters are converted to standard noise parameters. The characteristics for the minimum noise figure, the optimum source reflection coefficient and the normalized noise resistance for the complete transistor are shown in Figures 4 - 7, respectively. The curves obtained by using the proposed model (denoted by MOD1) are compared with the measured data (denoted by REF). Besides the numerical results for MOSFET noise modeling based on presented approach, the characteristics obtained when the correlation between noise sources is ignored, [8], are also shown and denoted by MOD2.

It is obvious that the MOSFET noise parameters are very well simulated in both cases, but a little better agreement with referent data (especially for minimum noise figure and noise resistance) is achieved when the correlation between the noise sources in transistor noise model is included.

IV CONCLUSION

The wave approach to RF MOSFETs' noise modeling is presented in this paper. The modeling procedure is based on some approaches proposed earlier for the other technology microwave transistors. The noise wave parameters are calculated in terms of equivalent circuit elements and three equivalent noise temperatures and shown graphically as a function of frequency. The standard noise parameters are also calculated and good agreement with measured noise parameters is observed. The presented procedure is very convenient for CAD applications, enabling simple and reliable prediction of noise parameters over a wide frequency range.

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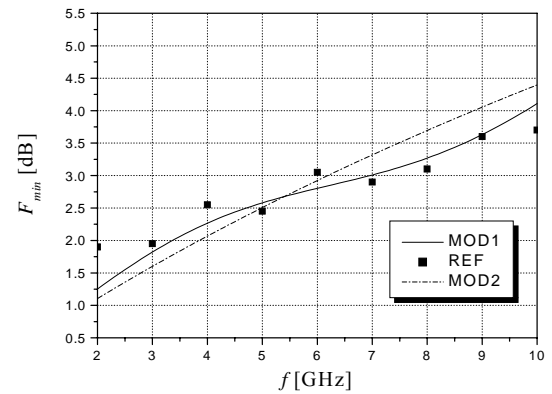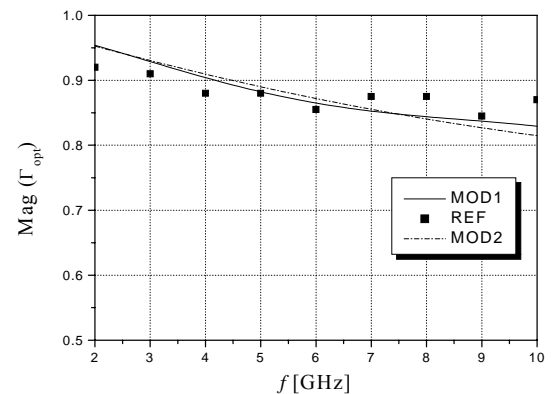
Fig. 4. Minimum noise figure

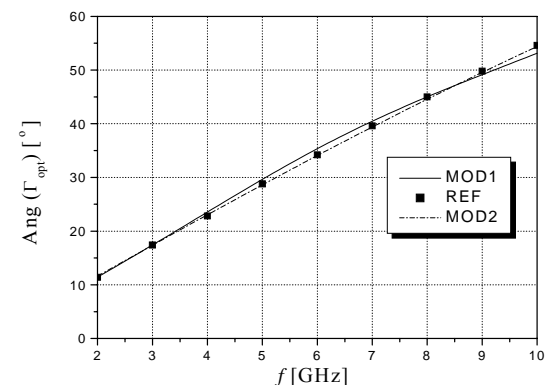Fig. 5. Magnitude of optimum reflection coefficient
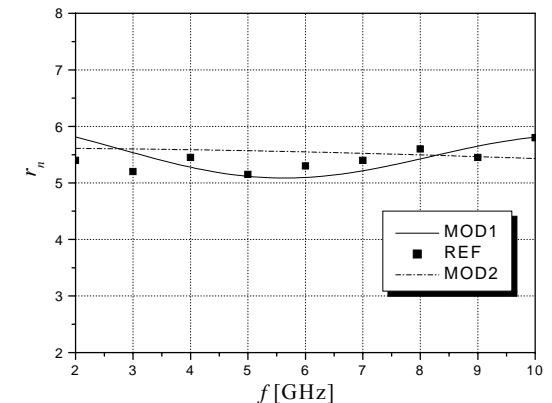

Fig. 6. Angle of optimum reflection coefficient

Fig. 7. Noise resistance

Self-Heating Effects in Virtual Substrate SiGe HBTs

Nebojsa D. Jankovic[1], Aulton B. Horsfall[2]

Abstract - **In this paper we investigated the self-heating effects in SiGe heterojunction bipolar transistors (HBTs) fabricated on SiGe alloy virtual substrate. Using a two-dimensional process and device numerical simulation, we have found that self-heating effects and local temperature increase due to the internal power dissipation are substantially more pronounced in virtual substrate HBTs in comparison with identical HBT devices on silicon substrate.**

Keywords - **HBT, virtual, substrate, self-heating**

I INTRODUCTION

Modern Silicon Heterojunction Bipolar Transistors (Si HBTs) with strained-SiGe base are very promising devices for high-frequency circuit applications [1]. The ECL microwave circuits in SiGe HBT/CMOS technology has already achieved f_{max}>180-GHz [2]. Recently, a new type of so-called "virtual substrate" technology [3] is emerging that allows a fabrication of both the high-performance heterojunction MOS FETs (HFETs) and SiGe HBTs on the same chip. The virtual substrate (VS) consists of thick (1um) fully relaxed SiGe buffer layer epitaxially grown on silicon substrate. The ability to synthesize on-chip HFETs, inductors and microstrip structures together with HBTs on VS makes SiGe HBTs ideal for microwave and RF applications [4]. There is no fundamental difference in the operation between Si HBTs and virtual substrate HBTs (VS HBTs) [5]. However, the thermal conductivity of the SiGe alloy forming the virtual substrate layer is much lower (approximately 15x lower at 20% Ge composition(then that of silicon [6].

Thus, during the DC operation of the device, VS HBT experiences considerably more self-heating than conventional Si HBT. Lattice self-heating results from the high dissipated power density in the device. Even in low-power-applications, the scaled sub-micron VS HBTs operating at high collector current densities for maximum speed experience a non-negligible self-heating effects. A local increase of device temperature degrades VS HBT performance by reducing its cutoff frequencies f_t and f_{max} and increasing internal leakage currents . Self-heating of HBTs can also significantly affects the behaviour of precision analog circuits, such as current sources and current mirrors, by changing their output admittances and introducing errors due to the increased device mismatching [7,8].

In this paper, we will evaluate the self-heating effects in VS HBTs by using a commercial numerical technology and device simulation software (TCAD) from SILVACO [9]. For accurate prediction of the self-heating in sub-micron devices, it is necessary to employ a full energy balance and thermionic emission models thath are connected with appropriate thermal models in simulations. It is achieved using SILVACO (GIGA) software package [9], which solves self-consistently the electro-thermal coupled transport equations. A comparison between self-heating effects occurring in Si HBT and VS HBT at the similar DC power dissipation will be performed with respect to the VS HBT's output impedance, and current gain.

II 2D DEVICE STRUCTURE AND NUMERICAL MODELLING

The two-dimensional (2D) cross-section and 1D doping profile of the vertical npn VS HBT structure investigated in this paper is shown in Fig.1. It is generated by a simulation of the hypothetical SiGe HBT process flow using process simulator (ATHENA) from SILVACO [9]. A single poly-silicon VS HBT device structure was aassumed for simulation study, having a box-like Ge-profile in the highly doped p-type base and a N^+/N^- structure for both emitter and collector. A 1μm thick virtual substrate layer (collector) with 15% Ge mole fraction is adopted for VS HBT, while the zero Ge substrate (monocristal Si) is taken in case of Si HBT. The SiGe strained base layer has 25% more Ge persantage then the collector in both Si HBT and VS HBT cases. Consequently, the Ge mole fractions in the bases of Si HBT and VS HBT were 40% and 25 % respectively. A resulting base peak doping concentration and total base width after process
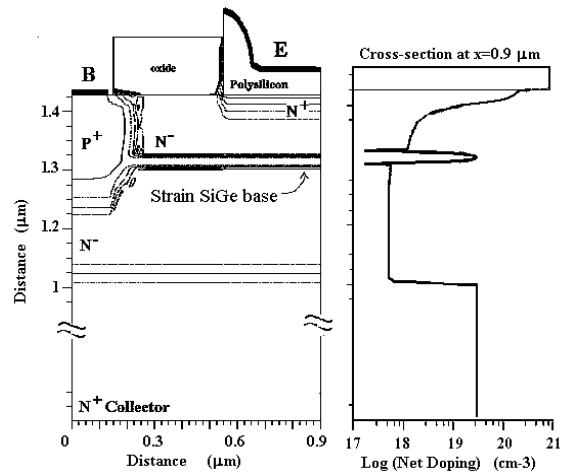

Fig.1. 2D cross-section of the simulated VS HBT device structure and 1D net impurity doping profile.

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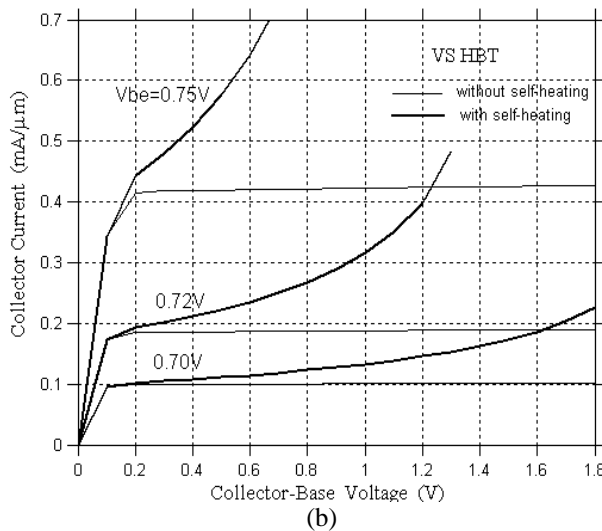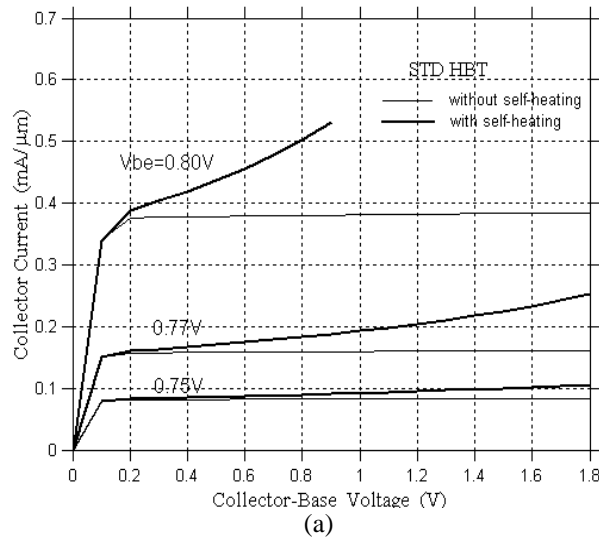
Fig.2. Comparison of the standard Si substrate HBT and the VS HBT output characteristics simulated without and with lattice heating.

equations. In simulation, the heat capacity of SiGe alloys was taken to be the same as for Si, since the specific heat of pure Si and Ge differ by less than 5% for T > 300 K [10]. As for the thermal conductivity of SiGe layers, we have adopted an average value of 72 mW/cmK at 300 K. The temperature dependence of thermal conductivity was adjusted in the simulator so that the numerical model approximately fits the available experimental data for SiGe alloys [6]. Collector and emitter contacts were modelled as internal thermal contacts with externally attached thermal conductivities of 2000 W/cmK and 3000 W/cmK, respectively. Note that with the external thermal conductivities accounting for the HBT's extrinsic regions and packaging, a more realistic temperature distribution within the simulated device is obtained as suggested by Grasser et al [11]. All other temperature variations in physical and transport parameters were taken to be the same as for Si in the simulations.

III RESULTS AND DISCUSSION

Fig. 2 shows simulated output characteristics of standard Si HBT (x=0.25, y=0) and a VS HBT (x=0.40, y=0.15) simulated with and without lattice heating. A substantial more degradation of the Early voltage and output impedance for similar levels of power dissipation can be observed for the VS HBT. The simulated 2D temperature distributions of the same Si substrate and VS HBTs used in Fig.2 are shown in Fig.3.
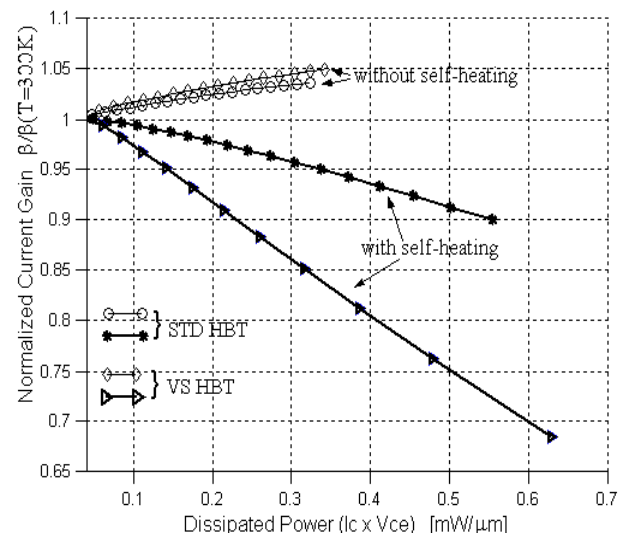

Fig.4. Normalized current gain $\beta(T)/\beta(300K)$ versus power dissipation $I_c \times V_{ce}$ of the standard Si HBT(Vbe=0.75V) and the VS HBT (Vbe=0.7V).

simulation were $2 \times 10^{19} cm^{-3}$ and 27nm, respectively, yielding a base pinch resistance of $85\Omega/\square$ at Vcb=1V. Simulation results of the HBT structure in Fig.1 also revealed that it exhibit reasonable values of breakdown voltage BV_{CE0} and Early voltage (3.5V and 13V, respectively). These values were extracted using non-local impact ionisation carrier models in device simulation.

For a valid comparison between electrical characteristics of Si HBT and VS HBT, the physical models in device simulator (ATLAS) [9] were calibrated with SiGe material parameters as described in [5]. In order to analyse quantitatively the self-heating effects in VS HBTs, we have performed 2D numerical device simulation using (GIGA) [9], which solves self-consistently the electro-thermal coupled
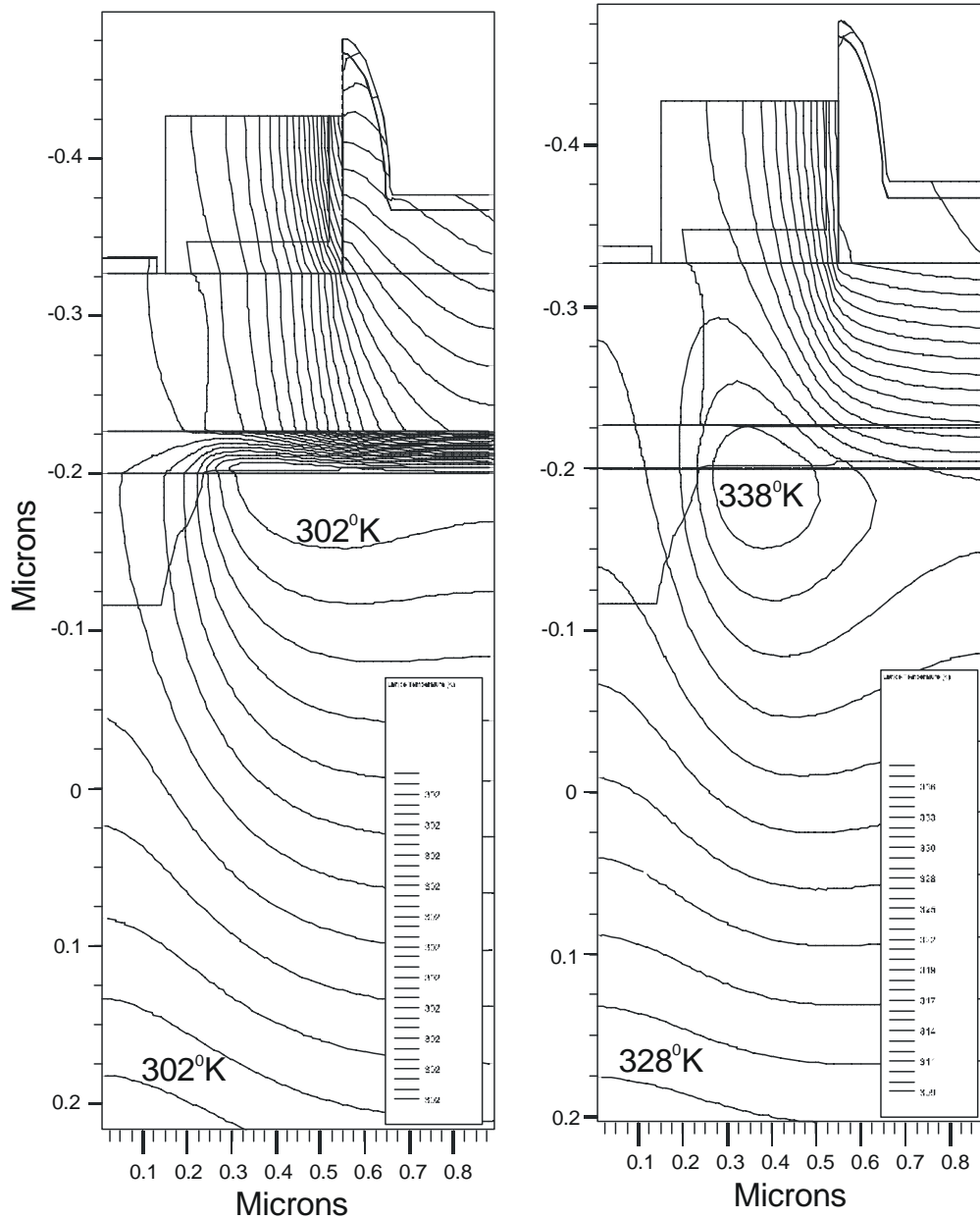
Fig.3. Simulated 2D temperature distribution in (a) the Si HBT
and (b) the VS HBT for $V_{be} = 0.72$ V and $V_{ce} = 2$ V

Although 2-D lattice-heating simulation tend to overestimate actual device internal temperature [11], the simulation results in Fig.3 reveal a peak temperature difference of 26 ^{0}K appearing in Si substrate and VS HBTs for the same power dissipation. It is interesting to note that a premature hot-spot formation is clearly seen in the VS HBT device due of Fig.3.b to the emitter injection current crowding, causing local heating at the emitter edge with potential thermal run-away problems. However, owing to the good thermal conductivity of the silicon emitter and collector (substrate) layers, a hot-spot does not appear in standard Si HBT for a similar level of power dissipation. Fig.4 shows a normalized current gain $\beta(T)/\beta(300K)$ versus power dissipation extracted from the self-heating simulation of standard Si HBT and VS HBT at Vbe of 0.75V and 0.70, respectively. In both devices, self-heating induces a decrease of current gain β with increasing internal temperature due to the band-gap difference between the base and the emitter region [4]. However, the rate of β decrease is much higher in VS HBT compared to Si HBT due to the more pronounced self-heating

effects. The local increase of device temperature is known to degrade f_t and f_{max} [12]. Consequently, we may conlude from our simulation results that VS HBTs will experience a severe degradation of f_t and f_{max} at high collector currents and collector voltages in comparison with Si HBTs. It requires a need for special attention when dealing with the self-heating effects in future RF and microwave integrated circuits that combine HFETs and VS HBTs using a virtual substrate technology.

IV CONCLUSIONS

A study has been made of the self-heating effects in virtual substrate SiGe HBTs using a calibrated numerical process and device simulator. It is found that self-heating in sub-micron base VS HBTs substantially degrades the Early voltage (output admitance) and the DC current gain even at moderate Vbe, owning to low thermal conductivity of SiGe alloys.

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Extraction Photodiodes with Auger Suppression for All-Weather Free-Space Optical Communication

Zoran Jakšić[1], Zoran Djurić[2]

Abstract – **We analyze the use of nonequilibrium, minority carrier extraction photodiodes with Auger generation-recombination suppression as receivers for second-generation wireless optical communications in the long wavelength infrared range. We chose mercury cadmium telluride as the detector material. We numerically simulated the device figures of merit utilizing a generalized form of van Rosbroeck-Shockley model, taking into account the band nonparabolicity of mercury cadmium telluride. Our analysis shows that extraction photodiodes could satisfy the posed requirements.**

Keywords – **wireless communication, infrared receivers, extraction photodiodes, Auger suppression, nonequilibrium detectors**

I. INTRODUCTION

Free-space optics (FSO) communication systems for the last mile solutions operating in the long wavelength infrared (LWIR) range were recently proposed as the 'all-weather systems' [1], [2]. They offer an alternative to both the microwave links and 0.7-1.55 μm infrared wireless systems for the last mile access, private networks and mobile infrastructure applications. The LWIR FSO are expected to operate in the range of 8-14 μm, or more specifically at 10.6 μm. Based on previous experience with night vision, surveillance and targeting in the same range, it is expected that these systems could allow wireless communications under harsh meteorological conditions while showing at least a 10-20 times lower sensitivity to fog, rain, smog and other atmospheric disturbances than the first generation wireless optical communication systems. Although their superior behavior is disputed by some [3], the performance of infrared systems in the LWIR range is confirmed by decades of the army experience. Recent measurements strictly dedicated to wireless communication applications seem to confirm the usefulness of the LWIR range for the FSO [4].

Among the arguments in favor of the use of the night vision infrared wavelengths for the FSO is that this range offers low start-up and operation costs, since this range does not require expensive licensed spectrum, i.e. it may be utilized anywhere without restrictions. The other important issue is laser eye
safety, since the LWIR FSO systems are to be used in densely populated areas. The night vision spectrum allows at least 50 times higher laser powers with an even diminished danger to the eye [5] as compared to the currently utilized

Currently a number of groups are performing experiments with LWIR FSO systems or developing emitters and receivers for that range [1], [5], [6].

Nonequilibrium devices with Auger suppression [7], [9] were also first proposed for military night-vision systems. They were intended for uncooled or slightly cooled operation with a performance equivalent to that of cryogenically cooled detectors. However, the subsequent research showed them to have an excess level of flicker (1/f) noise [8]. That noise component disappears at higher frequencies (of the order of MHz and above) which makes nonequilibrium devices worth considering to be used for high-speed free-space optical communications. These devices could offer the required performances at a fraction of the cost of the cryogenically cooled ones.

The use of nonequilibrium detectors for all-weather FSO was proposed in [10]. The first proposed generic type of devices for LWIR wireless were exclusion photoconductors. Magnetoconcentration devices for the FSO were considered in [11]. The issues of the response speed of nonequilibrium detectors were dealt with in [12].

This paper analyzes the applicability of the third generic type of nonequilibrium LWIR photodetectors for LWIR FSO, the extraction-based diodes. Their main figures of merit are calculated and the achievable performance considered.

II. EXTRACTION DIODES FOR FSO

The basic structure of an extraction diode we considered is shown in Fig. 1. This is a device fabricated in narrow-bandgap semiconductor. The typically used material for the LWIR range is mercury cadmium telluride ($Hg_{1-x}Cd_xTe$).
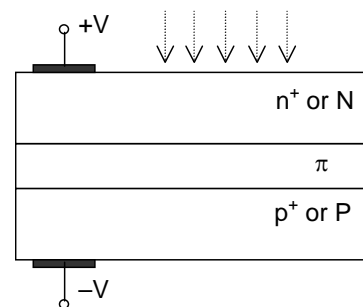

Fig. 1. Three-layered, two-contact extraction diode structure of $p^+\pi n^+$ or $P\pi N$ type

The detector is either a structure with heavily doped p and n region or a heterostructure with wider-bandgap P and N regions. Between these two regions there is a near-intrinsic p-doped material region (denoted as π) with a thickness smaller than the diffusion length. Such devices are typically prepared by epitaxy (for instance, molecular beam epitaxy – MBE).

The exclusion effect prevents carriers from entering the π region from the p^+ (or P) side, while the minority carrier extraction is responsible for carriers being removed from the π region into the n^+ (or N). Thus at a large enough bias to cause nonequilibrium between the carriers and the semicon-

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0.7-1.55 μm range.

ductor crystal lattice the majority carrier concentration approaches the intrinsic value. The minority carrier concentration, in order to retain neutrality, decreases several orders of magnitude more. Auger generation-recombination (g-r) processes are proportional to carrier concentration and thus become strongly suppressed. Since the prevailing noise mechanism in narrow-bandgap semiconductors is g-r noise, its level proportionally drops and the detector effectively behaves as cryogenically cooled.

Fig. 2 shows one of the possible approaches to obtain larger-area extraction devices, an alternative to that being the use of a matrix of separate but interconnected devices, possibly oriented in different directions in space.
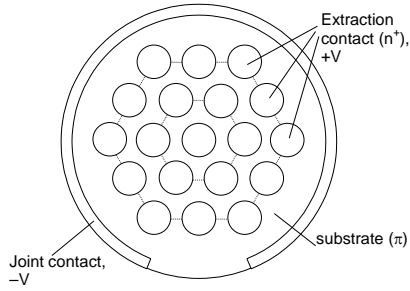
Fig. 2. "Pixelated" form for improvement of total dimensions of extraction photodetectors: matrix of extraction diode elements of $n^+\pi$ type on a joint substrate.

Such systems may be used together with light concentrators to further enhance their performance. The paper [11] considers the use of compound parabolic concentrators to that purpose. The following investigation, however, is dedicated to the performance of extraction diode-based systems without light concentration.

III. SIMULATION RESULTS

One of the key parameters in assessing the applicability of a receiver is its specific detectivity. We used numerical modeling to determine the parameters of our extraction photodiodes. We applied modified van Rosbroeck-Shockley model to that purpose, generalized to take into account nonparabolicity of bands and other particularities of direct narrow-bandgap semiconductors to which mercury cadmium telluride belongs [13]. To determine its value, first we used our finite-difference based simulation model to calculate their generation-recombination (g-r) rates. We chose a realistic temperature of 250 K, readily achievable with single-stage thermoelectric coolers.

Fig. 3 shows the Auger recombination rate, this being the dominant g-r mechanism. It can be seen that already at small bias voltages the level of Auger recombination rate drops several orders of magnitude. Thus the detectors begin to behave as cryogenically cooled.
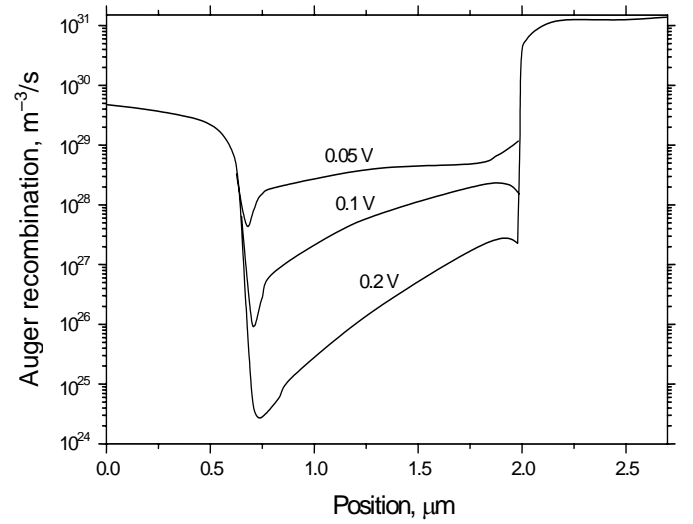

Fig. 3. Auger recombination rate in a reverse biased extraction $Hg_{1-x}Cd_xTe$ photodiode for different values of bias, x=0.187, T=250 K, λ_{co}=8.35 μm, w=2.7 μm, y_{p+}=0.65, y_{n+}=0.5 μm, N_D^{n+}=10^{18} cm^{-3}, N_A^{p+}=10^{18} cm^{-3}, N_A^{π}=10^{14} cm^{-3}
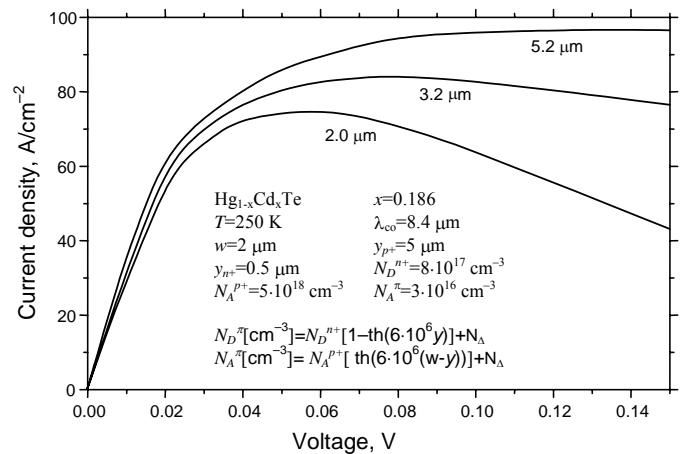

Fig. 4. Current-voltage characteristics of a homojunction HgCdTe extraction $n^+\pi p^+$ diode for various widths of the extraction zone

Further we calculated current-voltage characteristics of our devices. Fig. 4 shows this dependence for different values of the active area thickness. The right part of Fig. 4 shows the zone with negative dynamic resistance, which is characteristic for all nonequilibrium detectors with Auger process suppression.

It is visible that the diode characteristics become improved as the active area thickness decreases. This is a favorable property, since this at the same time improves the extraction diode response speed.

The calculated noise is shown in Fig. 5. As expected, it decreases more strongly for larger values of bias. Already at a bias of 0.3 V a noise generation density improvement is observed of more than an order of magnitude.
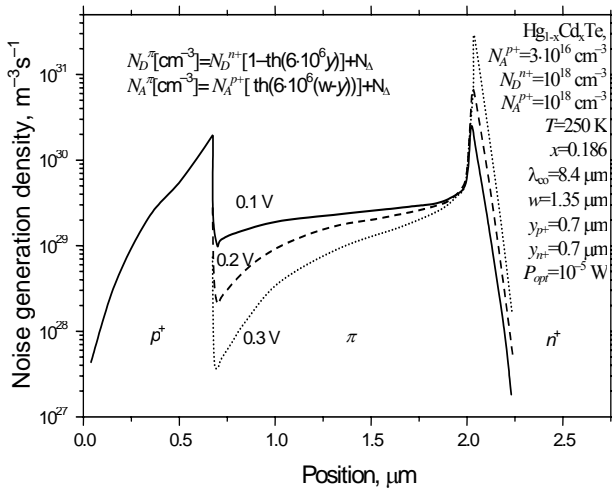
Fig. 5. Spatial distribution of noise generation density in an extraction-type diode for various values of bias.

Finally, the resulting specific detectivity is shown in Fig. 6. Values close to 10^9 cmHz$^{1/2}$/W are obtained. It is expected that alternative detector geometries and optimized material parameters could furnish the values in excess of 10^{10} cmHz$^{1/2}$/W [9].
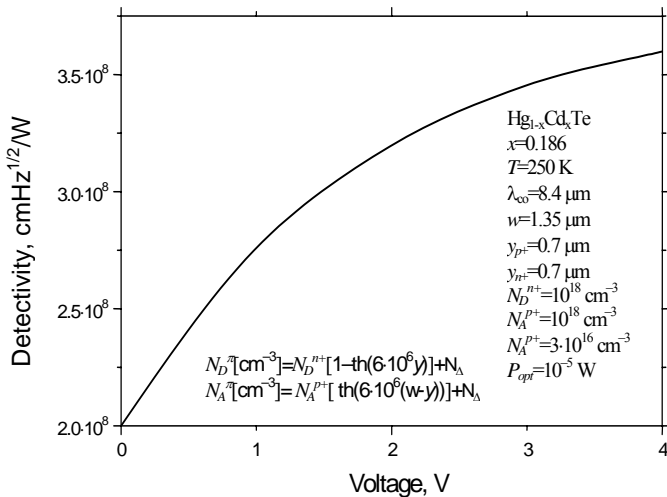

Fig. 6. Specific detectivity of an HgCdTe extraction diode versus applied bias

The frequency dependence of specific detectivity is another crucial parameter. For the extraction diodes the device response speed was assessed by using the drift-time of flight approximation, convenient for charge carriers near the hot carrier region [8]. It should be mentioned that the influence of electronic circuitry was not taken into account. The upper limit of the achievable bandwidth satisfies the requirements for FSO communication. However, as mentioned in Introduction, another frequency limit is posed by the 1/f (flicker) component of noise. Unlike conventional detectors, where the knee (i.e. threshold) frequency of 1/f dependence is of the order of kHz, this value is much larger in all nonequilibrium Auger-suppressed devices. In the case of extraction diodes the knee frequency may reach the values as high as 200 MHz [13]. The practical upper limit of operation is about 2.5 GHz [2]. This means that the "window" of allowed operating frequencies for extraction diodes is narrowed, but wide enough still to enable correct operation of high-speed FSO.

IV. CONCLUSION

We proposed the use of extraction photodiodes for free space optical communications in long-wavelength infrared range. To this purpose we considered Auger generation-recombination rates in mercury cadmium telluride-based devices and the resulting noise and specific detectivity levels. We also calculated the current-voltage characteristics of the devices. It is concluded that extraction-based HgCdTe diodes may be convenient for the LWIR FSO communications.

It is necessary to mention that the results presented in this work were obtained for an extraction structure without any optimization, so that a further improvement of results can be expected for improved devices.

Our further research should include optimized detector design and the use of additional methods for receiver performance improvement, particularly the resonant cavity enhancement and the use of refractive and reflective external light concentrators.

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ETS Method – An Approach to the Analysis of Arbitrarily Shaped Hole in Microstrip Lines

Miodrag Gmitrović and Biljana Stojanović

Abstract – **Analysis of some microstrip lines with a hole is done by Equivalent Thevenin Source (*ETS*) method. A line with an arbitrarily shaped hole is represented by equivalent two-dimensional circuit constructed as cascade-connected uniform lines with different lengths and widths. A few examples with the analysis results are shown here.**

Keywords – **ETS method, microstrip line, cascade connection, hole.**

I. INTRODUCTION

In the earlier published papers [1-5] it is shown on many examples that *ETS* method represents one of efficient ways for analysis of planar microwave structure. Analysis is based on two-dimensional circuit and its decomposition into cascade-connected ladder subnetworks with the same or different number of ports. Each ladder subnetwork can be fully characterized by its transmission matrices. After that, corresponding *ETS* voltage vector and impedance matrix are calculated and that ladder subnetwork is substituted by its *ETS*. That *ETS* are now the excitation of the next cascade-connected ladder subnetwork. Input and output voltages and currents for each ladder subnetwork can be obtained by successive application of this procedure.

In this paper, a complete procedure for analysis of microstrip line with a hole of arbitrary shape is described. This analysis represents one more extension of program *FAMIL* (Frequency Analysis of Microwave Lines). It can lead to a universal and effective computer program capable of solving a wide range of practical problems.

II. MULTI-PORT NETWORK DRIVEN BY CURRENT AND VOLTAGE SOURCES

A terminal behaviour of any ladder subnetwork with $2L$ ports (Fig.1) may be uniquely described by a set of equations. That set relates input voltages and currents of the network (U_1, I_1) to its output voltages and currents (U_2, I_2). The matrix equations are

$$U_1 = A \cdot U_2 + B \cdot I_2, \qquad (1)$$

$$I_1 = C \cdot U_2 + D \cdot I_2, \qquad (2)$$

where $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ are transmission matrices of the network and they are given in the paper [1]. The network is driven by $m1 + m2$ voltage and k current real sources, so $L = m1 + k + m2$.
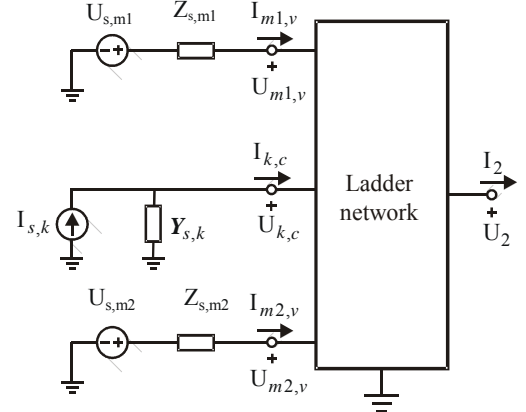
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Fig.1. Multi-port network driven by voltage and current sources.

The input voltage vector of the network according to source disposition is

$$U_1 = \left[U_{m1,v} \mid U_{k,c} \mid U_{m2,v} \right]^T = \left[U_{1,1}\, U_{1,2} \cdots U_{1,L} \right]^T . \quad (3)$$

The first sign of subscripts in the vector indicates the number of the sources and the second one indicates the type of source (v - voltage or c - current source).

Also, the output voltage vector of the network can be divided in the form

$$\mathbf{U}_2 = \left[U_{2,m1} \mid U_{2,k} \mid U_{2,m2} \right]^T = \left[U_{2,1}\, U_{2,2} \cdots U_{2,L} \right]^T . \quad (4)$$

In order to find the voltage vector $\mathbf{U}_{2T}$ for open-ended network and the impedance matrix $\mathbf{Z}_{2T}$ for annulled sources by *ETS* method, it is necessary to form real input vector with known voltage vectors, $\mathbf{U}_{m1,v}$ and $\mathbf{U}_{m2,v}$ and current vector, $\mathbf{I}_{k,c}$. Because of that, the permutation of rows in the existing transmission matrices must be done. After row permutation is done, the equation system (1–2) becomes

$$
\begin{bmatrix} U_{m1,v} \\ I_{k,c} \\ U_{m2,v} \end{bmatrix} = \begin{bmatrix} U_{s,m1} - Z_{s,m1} \cdot I_{m1,v} \\ I_{s,k} - Y_{s,k} \cdot U_{k,c} \\ U_{s,m2} - Z_{s,m2} \cdot I_{m2,v} \end{bmatrix} =
$$

$$
= \begin{bmatrix} A_{m1,m1} & A_{m1,k} & A_{m1,m2} \\ C_{k,m1} & C_{k,k} & C_{k,m2} \\ A_{m2,m1} & A_{m2,k} & A_{m2,m2} \end{bmatrix} \cdot \begin{bmatrix} U_{2,m1} \\ U_{2,k} \\ U_{2,m2} \end{bmatrix} + \quad (5)
$$

$$
+ \begin{bmatrix} B_{m1,m1} & B_{m1,k} & B_{m1,m2} \\ D_{k,m1} & D_{k,k} & D_{k,m2} \\ B_{m2,m1} & B_{m2,k} & B_{m2,m2} \end{bmatrix} \cdot \begin{bmatrix} I_{2,m1} \\ I_{2,k} \\ I_{2,m2} \end{bmatrix}
$$

$$\begin{bmatrix} \boldsymbol{I}_{m1,v} \\ \boldsymbol{U}_{k,c} \\ \boldsymbol{I}_{m2,v} \end{bmatrix} = \begin{bmatrix} \boldsymbol{C}_{m1,m1} & \boldsymbol{C}_{m1,k} & \boldsymbol{C}_{m1,m2} \\ \boldsymbol{A}_{k,m1} & \boldsymbol{A}_{k,k} & \boldsymbol{A}_{k,m2} \\ \boldsymbol{C}_{m2,m1} & \boldsymbol{C}_{m2,k} & \boldsymbol{C}_{m2,m2} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{U}_{2,m1} \\ \boldsymbol{U}_{2,k} \\ \boldsymbol{U}_{2,m2} \end{bmatrix} +$$
$$+ \begin{bmatrix} \boldsymbol{D}_{m1,m1} & \boldsymbol{D}_{m1,k} & \boldsymbol{D}_{m1,m2} \\ \boldsymbol{B}_{k,m1} & \boldsymbol{B}_{k,k} & \boldsymbol{B}_{k,m2} \\ \boldsymbol{D}_{m2,m1} & \boldsymbol{D}_{m2,k} & \boldsymbol{D}_{m2,m2} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{I}_{2,m1} \\ \boldsymbol{I}_{2,k} \\ \boldsymbol{I}_{2,m2} \end{bmatrix} \tag{6}$$

There are no changes in the output voltage and current's vectors after the row permutations. The only changes are in the transmission matrices.

After taking the new signs for transmission matrices with permuted rows $\boldsymbol{A}_P$, $\boldsymbol{B}_P$, $\boldsymbol{C}_P$ and $\boldsymbol{D}_P$ and for matrices

$$\boldsymbol{W}_s = \begin{bmatrix} \boldsymbol{Z}_{s,m1} & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{Y}_{s,k} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{Z}_{s,m2} \end{bmatrix}, \boldsymbol{S} = \begin{bmatrix} \boldsymbol{U}_{s,m1} \\ \boldsymbol{I}_{s,k} \\ \boldsymbol{U}_{s,m2} \end{bmatrix},$$

$$\boldsymbol{S}_{v,c} = \begin{bmatrix} \boldsymbol{I}_{m1,v} \\ \boldsymbol{U}_{k,c} \\ \boldsymbol{I}_{m2,v} \end{bmatrix} \tag{7}$$

the equation system (5-6) can be written

$$\boldsymbol{S} - \boldsymbol{W}_s \cdot \boldsymbol{S}_{v,c} = \boldsymbol{A}_P \cdot \boldsymbol{U}_2 + \boldsymbol{B}_P \cdot \boldsymbol{I}_2, \tag{8}$$

$$\boldsymbol{S}_{v,c} = \boldsymbol{C}_P \cdot \boldsymbol{U}_2 + \boldsymbol{D}_P \cdot \boldsymbol{I}_2. \tag{9}$$

The voltage vector of *ETS* for open-ended network is

$$\boldsymbol{U}_{2T} = [\boldsymbol{A}_P + \boldsymbol{W}_s \cdot \boldsymbol{C}_P]^{-1} \cdot \boldsymbol{S} \tag{10}$$

and the impedance matrix of *ETS* for annulled current and voltage sources is

$$\boldsymbol{Z}_{2T} = [\boldsymbol{A}_P + \boldsymbol{W}_s \cdot \boldsymbol{C}_P]^{-1} \cdot [\boldsymbol{B}_P + \boldsymbol{W}_s \cdot \boldsymbol{D}_P] \tag{11}$$

The relations (10) and (11) are equivalent to the recurrent relations (16) and (17) given in the paper [1], for $k = 1$, $\boldsymbol{U}_s \equiv \boldsymbol{S}$ and $\boldsymbol{Z}_s \equiv \boldsymbol{W}_s$.

III. PROCEDURE FOR THE ANALYSIS OF A HOLE IN MICROSTRIP LINES

Using the equivalent complex network shown in Fig.2 can do the analysis of microstrip lines with an arbitrarily shaped hole by *ETS* method. Number of ports for the networks 1 and 2 are $2L_1$ and $2L_2$, respectively, where $L_1 = m$ and $L_2 = L - n + 1$.

The complete procedures for *ETS* voltage and impedance calculation in case of simple and complex network connections with different number of ports are given in the paper [3].

Solving procedure for the structure depicted in Fig.2:
Cascade-connected planar transmission lines of different widths and lengths can be analysed by *ETS* method as cascade-connected networks with different number of input and output ports [3-5].

1. The first network and the other including the kth network as the last one have $2L$ ports. Voltages and impedances

of the kth network can be recovered from the recurrent relations [1]

$$\mathbf{U}_{2T}^k = [\mathbf{A}_k + \boldsymbol{Z}_{2T}^{k-1} \cdot \boldsymbol{C}_k]^{-1} \cdot \mathbf{U}_{2T}^{k-1}, \tag{12}$$

$$\boldsymbol{Z}_{2T}^k = [\boldsymbol{A}_k + \boldsymbol{Z}_{2T}^{k-1} \cdot \boldsymbol{C}_k]^{-1} \cdot [\boldsymbol{B}_k + \boldsymbol{Z}_{2T}^{k-1} \cdot \mathbf{D}_k]. \tag{13}$$

First k networks are then substituted with their Equivalent Thevenin sources of voltages $\boldsymbol{U}_{2T}^k$ and impedances $\boldsymbol{Z}_{2T}^k$.

The impedance matrix obtained by the equation (13) is full matrix

$$\boldsymbol{Z}_{2T}^k = \begin{bmatrix} Z_{11}^k & \cdots & Z_{1L}^k \\ \vdots & \ddots & \vdots \\ Z_{L1}^k & \cdots & Z_{LL}^k \end{bmatrix}. \tag{14}$$

The voltage vector of *ETS* at the kth open-ended network is full vector

$$\boldsymbol{U}_{2T}^k = \begin{bmatrix} U_{2T,1}^k & U_{2T,2}^k \cdots U_{2T,L}^k \end{bmatrix}^T. \tag{15}$$

2. The next matrices are formed for both $k+1^{st}$ networks [3]

$$\boldsymbol{A}_{k+1}^r = \begin{bmatrix} \boldsymbol{A}_{k+1}^1 & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{A}_{k+1}^2 \end{bmatrix}, \boldsymbol{B}_{k+1}^r = \begin{bmatrix} \boldsymbol{B}_{k+1}^1 & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{B}_{k+1}^2 \end{bmatrix},$$

$$\boldsymbol{C}_{k+1}^r = \begin{bmatrix} \boldsymbol{C}_{k+1}^1 & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{C}_{k+1}^2 \end{bmatrix} \text{ and } \boldsymbol{D}_{k+1}^r = \boldsymbol{1}, \tag{16}$$

where $\boldsymbol{0}$ is zero matrix and $\boldsymbol{1}$ is unitary matrix.

3. The voltage vector given by (15) can be divided in the form according to the network connections

$$\boldsymbol{U}_{2T}^k = \begin{bmatrix} \boldsymbol{U}_{2T,1m}^k \mid \boldsymbol{U}_{2T,m+1,n-1}^k \mid \boldsymbol{U}_{2T,nL}^k \end{bmatrix}^T, \tag{17}$$

where

$$\boldsymbol{U}_{2T,1m}^k = \begin{bmatrix} U_{2T,1}^k & U_{2T,2}^k \cdots U_{2T,m}^k \end{bmatrix}^T, \tag{18}$$

$$\boldsymbol{U}_{2T,nL}^k = \begin{bmatrix} U_{2T,n}^k & U_{2T,n+1}^k \cdots U_{2T,L}^k \end{bmatrix}^T. \tag{19}$$

After corresponding reduction voltage vector becomes

$${}^r\boldsymbol{U}_{2T}^k = \begin{bmatrix} \boldsymbol{U}_{2T,1m}^k \mid \boldsymbol{U}_{2T,nL}^k \end{bmatrix}^T \tag{20}$$

and now it represent the input vector for the next cascade-connected ladder networks.

4. The full impedance matrix given by (14) after the corresponding reduction is

$${}^r\boldsymbol{Z}_{2T}^k = \begin{bmatrix} Z_{11}^k & \cdots & Z_{1m}^k & \mid & Z_{1n}^k & \cdots & Z_{1L}^k \\ \vdots & \ddots & \vdots & \mid & \vdots & \ddots & \vdots \\ Z_{m1}^k & \cdots & Z_{mm}^k & \mid & Z_{mn}^k & \cdots & Z_{mL}^k \\ - & - & - & \mid & - & - & - \\ Z_{n1}^k & \cdots & Z_{nm}^k & \mid & Z_{nn}^k & \cdots & Z_{nL}^k \\ \vdots & \ddots & \vdots & \mid & \vdots & \ddots & \vdots \\ Z_{L1}^k & \cdots & Z_{Lm}^k & \mid & Z_{Ln}^k & \cdots & Z_{LL}^k \end{bmatrix} = \begin{bmatrix} \boldsymbol{Z}_{mm}^k & \boldsymbol{Z}_{mL}^k \\ \boldsymbol{Z}_{Lm}^k & \boldsymbol{Z}_{LL}^k \end{bmatrix}$$
$$\tag{21}$$

5. The voltage vector $\boldsymbol{U}_{2T}^{k+1}$ and the impedance matrix $\boldsymbol{Z}_{2T}^{k+1}$ of the $k+1^{st}$ networks 1 and 2 are calculated from the

relations (16) and (17) given in the paper [3], where are $\boldsymbol{U}_{2T,2}^{k} = {}^{r}\boldsymbol{U}_{2T}^{k}$ and $\boldsymbol{Z}_{22}^{k} = {}^{r}\boldsymbol{Z}_{2T}^{k}$.

The obtained voltage vector is

$$\boldsymbol{U}_{2T}^{k+1} = \left[\boldsymbol{U}_{2T,1m}^{k+1} \mid \boldsymbol{U}_{2T,nL}^{k+1} \right]^{T}. \qquad (22)$$

6. For the other networks in cascade connection till the outputs of networks 1 and 2 the relations (12) and (13) are used.
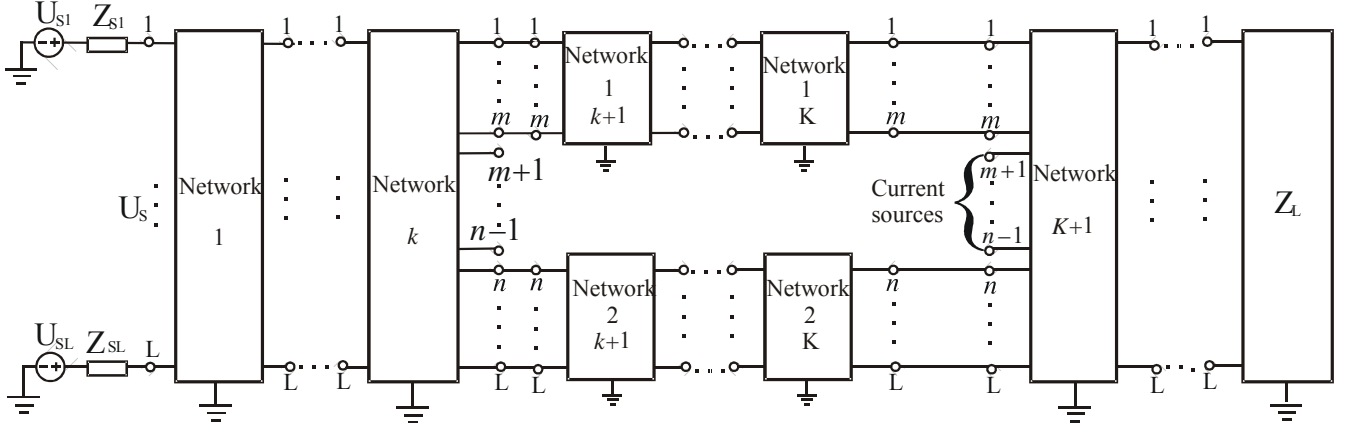
Fig.2. One microstrip structure with complex network connections.

7. The transmission matrices of the $K+1^{st}$ network and the other networks till the end are square matrices of sizes $L \times L$. According to the network junction (K^{th} and $K+1^{st}$ networks) permutation of rows in the transmission matrices only for the $K+1^{st}$ network must be done in the manner shown in the previously given section. In that way new matrices $\boldsymbol{A}_{P}$, $\boldsymbol{B}_{P}$, $\boldsymbol{C}_{P}$ and $\boldsymbol{D}_{P}$ are formed.

8. At the junction between the Kth and $K+1^{st}$ networks, because of the increased number of input ports, it is necessary to increase the vector $\boldsymbol{U}_{2T}^{K}$ and the matrix $\boldsymbol{Z}_{2T}^{K}$. According to the network connection given in Fig.2 the source impedance matrix for the next $K+1^{st}$ network is impedance matrix $\boldsymbol{Z}_{2T}^{K}$ increased as

$$ {}^{i}\boldsymbol{Z}_{2T}^{K} = \begin{bmatrix} \boldsymbol{Z}_{mL}^{K} & | & \boldsymbol{0} & | & \boldsymbol{Z}_{mm}^{K} \\ -- & | & --- & | & -- \\ \boldsymbol{0} & | & \boldsymbol{0} & | & \boldsymbol{0} \\ -- & | & --- & | & -- \\ \boldsymbol{Z}_{Lm}^{K} & | & \boldsymbol{0} & | & \boldsymbol{Z}_{LL}^{K} \end{bmatrix} \begin{matrix} 1 \\ \vdots \\ m \\ m+1 \\ \vdots \\ n-1 \\ n \\ \vdots \\ L \end{matrix} . \qquad (23) $$

$$ 1 \cdots m \mid m+1 \cdots n-1 \mid n \cdots L $$

The voltage vector of *ETS* at the Kth open-ended network is full vector and it can be increased in the form

$$ {}^{i}\boldsymbol{U}_{2T}^{K} = \left[\boldsymbol{U}_{2T,1m}^{k} \mid \boldsymbol{0} \mid \boldsymbol{U}_{2T,nL}^{k} \right]^{T} \qquad (24) $$

$$ 1 \cdots m \mid m+1 \cdots n-1 \mid n \cdots L $$

which represents the source vector of the next $K+1^{st}$ network.

9. The voltage vector, $\mathbf{U}_{2T}^{K+1}$, and the impedance matrix, $\boldsymbol{Z}_{2T}^{K+1}$, of *ETS* for the $K+1^{st}$ open-ended network are given by equations (10) and (11), where $\boldsymbol{S} = {}^{i}\boldsymbol{U}_{2T}^{K}$ and $\boldsymbol{W}_{S} = {}^{i}\boldsymbol{Z}_{2T}^{K}$.

10. For the further calculation, $K+2, K+3,...$, till the load network $\boldsymbol{Z}_{L}$, the relations (12) and (13) can be used for solving the rest of the networks in cascade connection.

IV. EXAMPLE

Several examples of microstrip lines with arbitrarily shaped holes and leaders, which are symmetrically or asymmetrically placed, are shown in this section, Figs. 3-4, 6-7, 9. They are observed as cascade-connected transmission lines with different lengths and increased or reduced widths.

The nominal substrate dielectric constant is $\varepsilon_{r} = 10.2$, the substrate thickness is $h = 635 \, \mu m$ and the strip thickness is $t = 18.03 \, \mu m$.

The lines at the ends (L1) are the $50 \, Ohm$ leader lines. Their widths are $w1 = 586.95 \, \mu m$ and lengths $d1 = 800 \, \mu m$.

The widths of cascade-connected transmission lines are $w2 = 2500 \, \mu m$, $w3 = 250 \, \mu m$, $w4 = 500 \, \mu m$, $w5 = 750 \, \mu m$ and $w6 = w7 = 1000 \, \mu m$. Their lengths are $d2 = 310 \, \mu m$, $d3 = 1000 \, \mu m$, $d4 = 400 \, \mu m$, $d5 = 500 \, \mu m$, $d6 = 300 \, \mu m$ and $d7 = 1200 \, \mu m$.

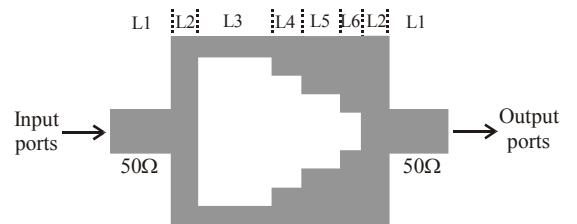The result obtained by program *FAMIL* that is done in MATLAB is shown in Figs. 5, 8, 10.

Fig.3. Example 1 – Line with a hole and symmetrically placed leader lines.
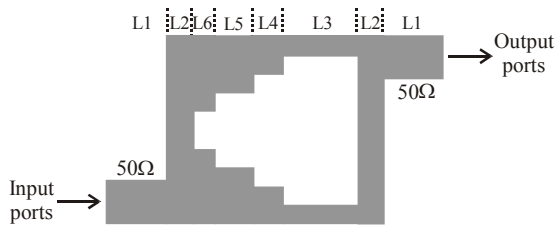
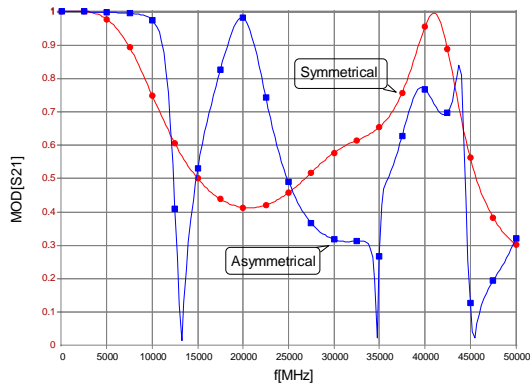Fig.4. Example 1 – Line with a hole
and asymmetrically placed leader lines.
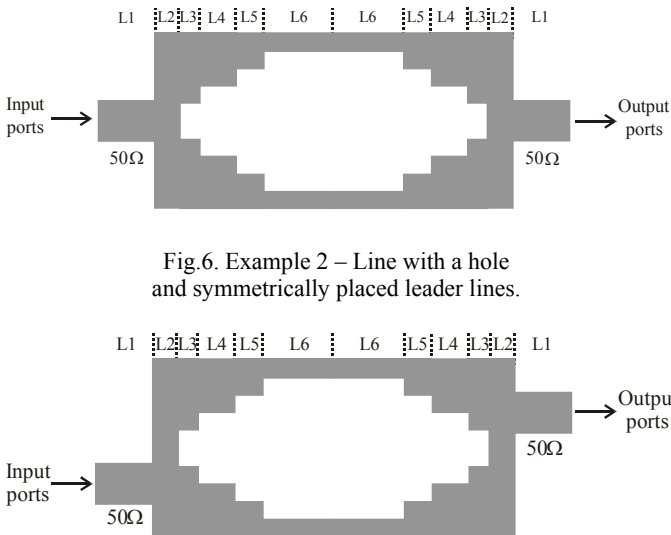

Fig.5. Responses of the lines shown in Example 1.

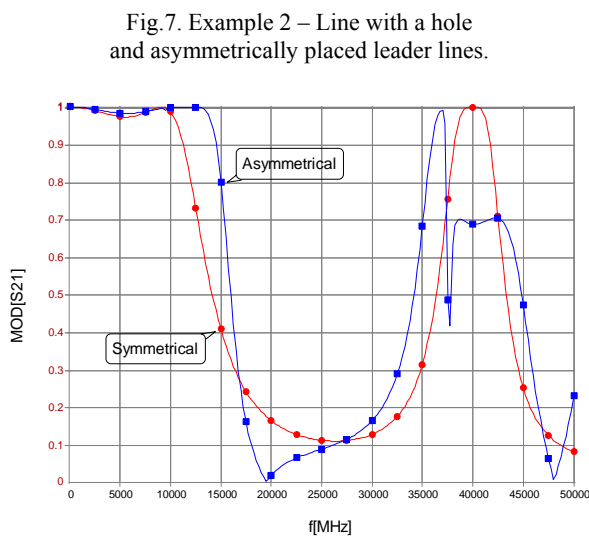Fig.6. Example 2 – Line with a hole
and symmetrically placed leader lines.

Fig.7. Example 2 – Line with a hole
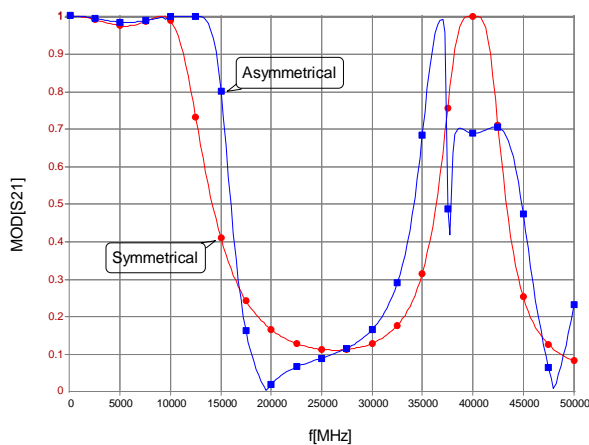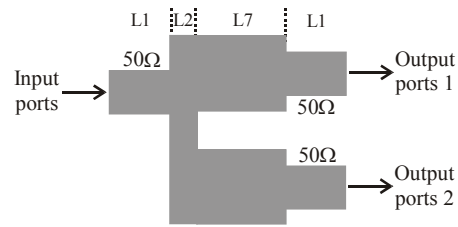and asymmetrically placed leader lines.

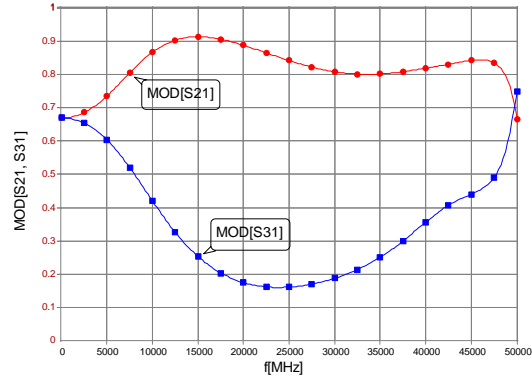Fig.8. Responses of the lines shown in Example 2.

Fig.9. Example 3 – Tree.

Fig.10. Responses of the line shown in Example 3.

V. CONCLUSION

The procedure for frequency analysis of planar microwave structures is completely given in the papers [1-5]. Here, it is extended for the analysis of a microstrip lines with a hole of arbitrary shape.

Several examples of such lines are analyzed in this paper. The shown results are obtained by program *FAMIL* that is done in MATLAB.

The results of analysis obtained here show that the microstrip line with hole have resonant feature. Therefore, this type of circuits can be use for synthesis of various type filters.

ACKNOWLEDGMENT

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Fiber Optic Refractometer Instrument Used for Measurement Practicing in Applied Photonics Multimedia Courseware

Ján Turán[1], Ľuboš Ovseník[1]

Abstract - **This paper presents development work to design multimedia courseware: Applied Photonics. This courseware is based on: 1) multimedia document about the basic theory of Applied Photonics; 2) simulation and measurement supporting multimedia programme package able solving selected CAD and CAE problems in Applied Photonics. As special application of practical session web-based interactive fiber optic instrument is described in details.**

Keywords - **multimedia courseware design, fiber optic refractometer, remote measurement through WWW.**

I. INTRODUCTION

Multimedia and Internet convergence opens of new avenues of methodologies for enhancing the experience of learning as will as expanding educational opportunities for a larger pool of students. Specifically, distance education and non-traditional classrooms have the capability to reach more students using specialised instructions, self-paced learning and virtual laboratories (and/or virtual instruments). Traditionally the integration of Multimedia and Internet with education can be based on the following:

Developing a courseware and course web site to centrally house various online functions and facilitate course management (especially feedback),
Creating a Virtual laboratory to replace physical experiments with multimedia animation or simulation (CAD and CAE multimedia package).

While a good learning experience can be obtained from such a purely simulation systems, in many situations, it is commonly recognised that effective and complete learning, especially in engineering and science, requires a mixture of theoretical (and/or simulation). and practical sessions. To address this very important issue we embedded to our multimedia distance education courseware: Applied Photonics, web-based laboratories that have capability to enable for students to set up parameters to run experiments from a remote location. This capability also is essential from the point of view to effective use of very expensive instruments and limited students time resources.

II. MULTIMEDIA COURSEWARE: APPLIED PHOTONICS

The explosive growth of the photonics market leads to wide up the need for CAD and CAE analysis tools applicable for designers, engineers and university students [1,2,3]. The recent advantage of hardware, software and digital signal processing allow for application of new discipline called multimedia signal processing to be embedded to these tools. This discipline is motivated to the convergence of traditionally separated technologies, namely, digital signal processing, digital image processing, computer vision, computer graphics and document processing [1]. The most innovative way to application this new discipline is the systematic approach to multimedia graphical user interface (GUI) design [2] and efficient interpretation of used multimedia material [3]. Multimedia graphical user interfaces (GUI) are traditionally created by intuition. They are usually designed and developed without exact analysis of multimedia information presentation. The objective of co-operative teleworking among students and teachers (with simultaneously possible using of databases and others multimedia CAD and CAE tools) is the provision of some degree of "telepresence" for geographically distributed persons and teaching, simulation, measurement and design materials in a quality comparable to that of a real-world lecture (conference, co-operation) [2,3]. In the modern multimedia courseware four multimedia GUI have to be designed:

System supervisor GUI – *operator GUI, responsible for the system.*
Teacher (tutor, supervisor) GUI – *responsible for the course content.*
Student GUI – *user (student, designer, engineer) GUI.*
Browser GUI – *GUI for any person interesting about the course.*

The developed Applied Photonics courseware represents an interactive multimedia course based on use of multimedia document and visual simulation CAD and CAE programme package for teleeducation purposes. The course structure and some of its interactive features are noticed in Fig. 1.

Student and teacher have access to an interactive multimedia document stored in a server. Teacher as a master has the possibility of changing this document if necessary. There are possibilities of interactive multimedia communications between student and teacher using various tools (E-mail, White Board, Audio-Video). Teacher has the possibility to supervise of student work and able to monitor his/her progress and interactively change-tailor the course

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content. The basic organisation of the courseware consist from four parts:

Theoretical part - *this is an interactive multimedia document about the theory of Applied Photonics.*
Practical part - *this is an interactive multimedia based simulation and measurement supporting multimedia programme package able to solve CAD and CAE problems in the area of Applied Photonics.*
Part references - *this is a multimedia document about published documents related to Applied Photonics.*
Part tests – *the tests embedded to the courseware are entitled to evaluated the knowledge, routines and working shills obtained by students through the learning process.*

Measurement practising in Applied Photonics for a large number of students is an economic problem. One approach to solve this problem is to create web-based laboratory equipments which are available to students through using standard Internet Protocol procedures on WWW. This approach was choosed in the course for practising measurements in the chapter Fiber Optic Sensors, particularly in application of fiber optics refractometer.
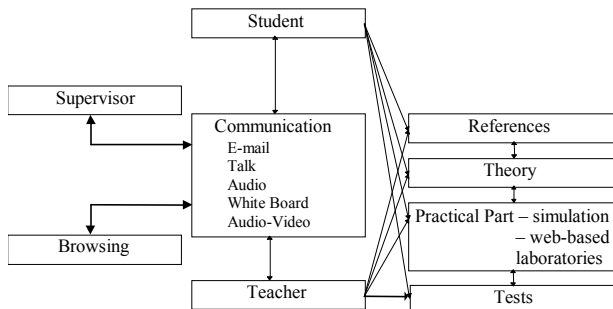
Fig. 1. Co-operative modern teleeducation

III. FEEDBACK IN THE PHOTONICS COURSEWARE

Very important part of the teleeducation courseware is the feedback. The architecture of the feedback used in the fiber optic communication courseware is depicted on the Fig. 2. It consists from five feedback loops, which are realised on the both level of the course (training and expert level). The simplest way of the feedback is the study and practicing solved examples embedded to the courseware. The quality of the courseware and the student progress in the course may be evaluated using predefined Questionnaire and the course statistics available to the teacher (course supervisor). Course statistics deals with registration and multimedia document utilization (users data, data and time using (working) of the courseware, results of evaluation etc.). Course Questionnaire deals with questions about course structure, optimal material selection, multimedia document quality etc. Tests embedded to the courseware are entitled to evaluate the knowledge, routines and working skills obtained by students trough the learning process. The test is structured trough the courseware content and may consist from the questions, unsolved examples and simulation problems. If there is any problem with the student progress in the course the student is able activate a hot line to the teacher, but only in consultation hours. At the present level of development of the courseware and available technology it may be only a E-mail contact with the remote teacher. Outputs from the feedback is

structured, saved and statistically processed to be used for improving the courseware quality in next development step.
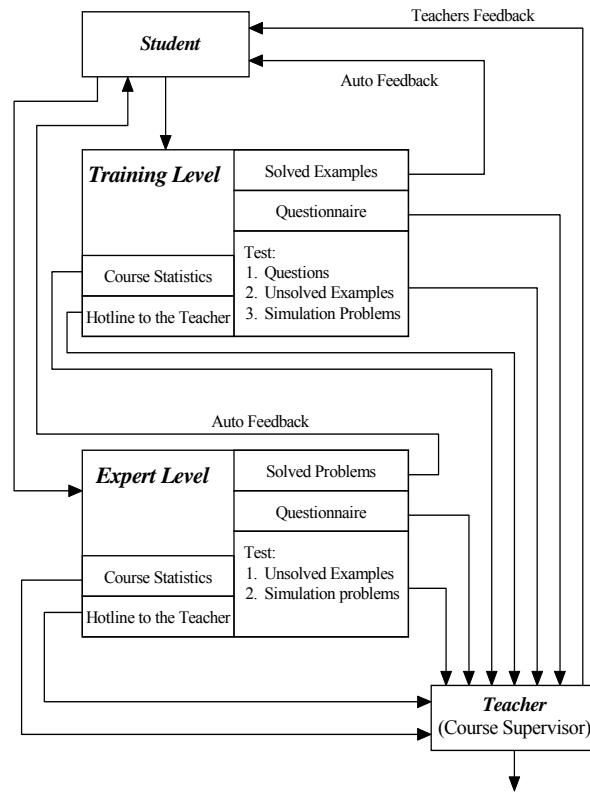

Fig. 2. Feedback in the multimedia courseware

IV. WEB-BASED FIBER OPTIC REFRACTOMETER DESIGN

Almost all currently available classical refractometers employ a prismatic element on which the liquid sample is placed. These instruments yield an output that is based on measuring the critical angle of reflection of a light beam at the liquid-prism interface. In more modern, digital type instruments, the angle of reflection is measured automatically using a linear photodetector array [1,2]. Since the index of refraction is strongly dependent on temperature and also, to a lesser degree, on wavelength, these effects must be corrected for in designing and/or using such instruments. As with any other refractometer, any instrument that employs this fiber optic based transducer must be capable of correcting for the intrinsic temperature dependence of a liquid's index of refraction [1]. In addition, however, for an intensity type fiber optic sensor, other corrections and precautions must be taken especially if, a precision of 1 part in 10.000 is to be attained. It will be necessary to employ low noise electronic circuitry and/or correct for photodetector dark current, especially at higher indices, where the output light intensity is strongly attenuated. It also will be necessary to correct for light source and photodetector temperature sensitivities and for any stray light that might affect the photodetector. In one sense, in terms of capabilities of today's microprocessor controlled "smart" sensor technology, it should be straightforward to design instruments that automatically "massage" the raw transducer data to correct them for each of these effects [3]. Referring to the block diagram in Figure 3a, the basic system, as presently

conceived, consists of the following elements: a light emitting diode (LED) or semiconductor laser diode (LD) light source and its electronic driver/pulser; a monitor photodetector to determine the output light level of the use light source, a second photodetector to record the return light from the transducer; and a microprocessor to automatically control the system and process the data from the various elements. It computes the ratio of the intensity of the transducer output for an unknown liquid and that recorded earlier for a standard liquid, e.g., water. The microprocessor then determines an index value, either by a comparison and

interpolation process between this ratio and those in a calibration data lookup table, or by computation using a transducer response equation. In addition, the temperature of the liquid sample and of the source/detector module is measured simultaneously with the index, to correct for their temperature dependence. The liquid sample temperature is determined using a thermistor, as indicated in Fig. 3a, or using a fiber optic temperature sensor in applications requiring an all dielectric transducer, e.g., for use in explosive or high voltage environments [2,3]. A second system, as outlined in Figure 3b, was also considered in detail.
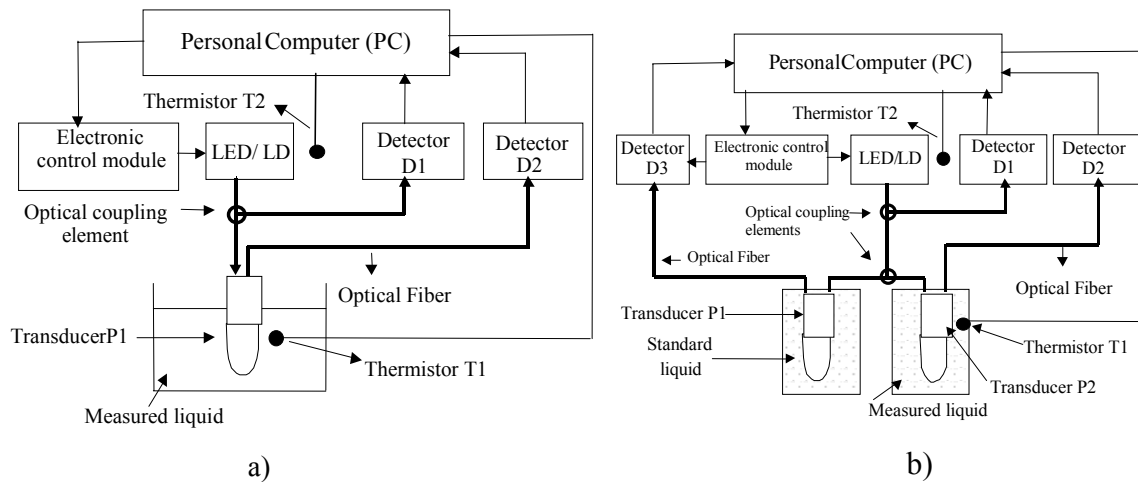
Fig. 3. Block diagram outlining the design of a a) basic and b) differential type fiber optic refractometer
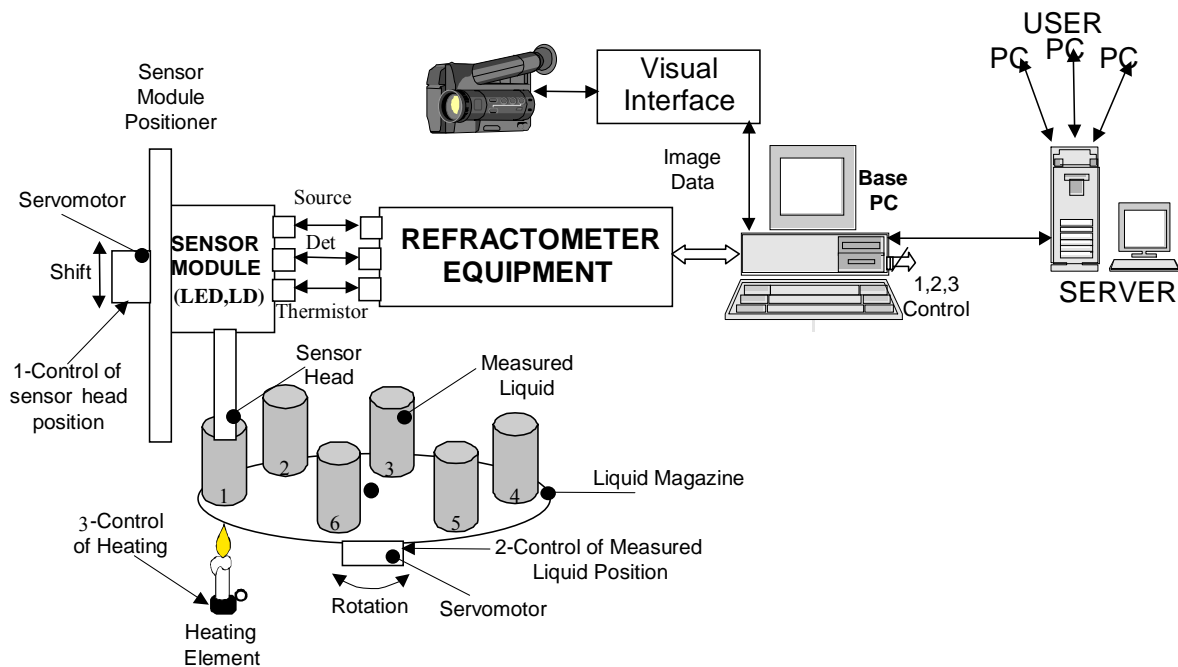
Fig. 4. Block scheme of the interactive web-based fiber optic refractometer instrument
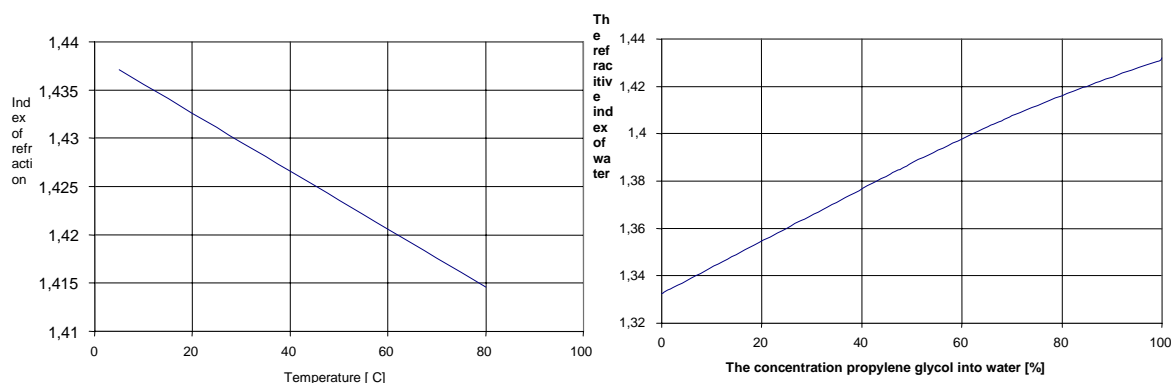
Fig. 5. The refractive index of a) the propyle glycol vs. temperature (°C) and b) the water vs. propyle glycol concentration

Basically, it employs a differential technique and would allow measurements/comparisons of index to a very high precision. Instead of taking comparative readings of index of a known and an unknown liquid at separate time, as would be done with the system outlined in Figure 3a, both readings would be taken simultaneously, using two index of refraction transducers, one in the unknown and the other in a standard liquid sample. For the course laboratory equipment type fiber optic refractometer able to emulate block diagrams described in Fig. 3a and Fig. 3b was choosed. This equipment was furnitured with the appropriate Measured Liquid Magazine, Sensor Module Positioner, Control Servomotors, Heating Element, Visual Camera Feedback, Control and Communication Software (Fig. 4) to create an interactive fiber optic refractometer instrument. Sensor Module

V. EXPERIMENTS AND RESULTS

A) Basic laboratory experiments

- dependence of the refractive index of propylene glycol on temperature (Fig. 5a),
- dependence of the refractive index of water propylene glycol solution on propylene glycol concentration (Fig. 5b).

B) Measurements of petrochemical products of the developed equipment

As field tests we use some petrochemical products of known index of refraction. They make it difficult to clean the sensor face however. We recommend to keep the containers of the mixtures sealed when not in use since they tend to drift in index, though this is not much of a problem. We frequently make up relatively large sample, e.g., 100 to 200 cc, and then use one half for our measurements for while and after a week or two, take a reading in the other half that has been kept well sealed. That way we can determine if there has been any shift in the index of our measurement sample. The results of measured index of refraction are depicted on Tab. 1, and are in very good success as compared with results obtained by classical methods.

Tab.1 Result of petrochemical products measurements

Petrochemical products	Refractive index	Temperature (°C)
Water	1.3333	21
Synthetic alcohol	1.3620	21
Propylen glycol	1.4268	21
Mobil VS-200	1.4399	21
Mobil motor 5W-50	1.4678	21

Positioner controls using servomotor the on (measured) and off (non-measured) position of the sensor head. Measured Liquid Magazine is based on the revolver system controlled by servomotor and provide the change of measured liquid (6 different liquids are possible). Heating Element provide controlled heating of the measured liquid. Visual Camera Feedback was added to the system to provide student with the feeling to be virtually present at the measurement place and also as visual feedback for verify correct function of the mechanical parts of the instrument. Developed multimedia software is able to control the various parts of the instrument, support control remote measurements using standard Internet Protocol procedures through WWW. The control of the refractometer is realised under standard Windows procedures.

Oil drive	1.4757	21
Madit drive	1.4828	21

VI. CONCLUSIONS

Development work related to create a web-based multimedia courseware: Applied Photonics has been presented. The courseware is based on the traditional multimedia learning document and simulation CAD and CAE programme package, with using practical sessions: web-based laboratories. In more detail we describe development and results of web-based fiber optic refractometer. The developed multimedia courseware was tested in teaching MSc. students. Since the number of student taking the course is of the range of 60 the aviable laboratory time slot is limited, and the few aviable expensive instruments are more effectively used to obtain real hands-on experience for the individual students.

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Television Scanning Optical Stereomicroscope for Surface Architectonics of Blood Cells Research

Zenon D. Hrytskiv, Anatolii D. Pedan.

Abstract − **The paper is dedicated to advantages of a television scanning optical stereomicroscope application to surface architectonics of blood cells research. The optical scheme of scanning stereomicroscope and examples of test-object and erythrocytes images received with microscope usage are presented.**

Keywords − **Blood cells architectonics, Scanning optical microscopy, Cathode ray tube, Volume image of micro object.**

I. INTRODUCTION

The television scanning optical microscopy, based on scanning of examined object with the light probe, which one is formed with usage of the cathode-ray tube in a mode of a flying spot, is the effective tool for a signature analysis of microscopic objects [1]. In a number of cases the efficiency of research essentially increases at application of stereomicroscopes. Thereby the new additional capabilities are also opened. The present paper is dedicated to advantages of a television scanning optical stereomicroscope application to surface architectonics of blood cells research.

The study of blood cells surface architectonics, in particular, erythrocytes, enables to observe a physiological ageing process and to investigate influence the different factors on this process. It is especially informative at diseases of a blood system, extreme conditions, conservation of a blood, at finding-out infusions of different transfusion drugs influence onto blood cells.

Now such analysis is realized by a method of a scanning electron microscopy, which one allows to receive in essence new information on features of constitution of a membrane surface, to describe morphologically the different shapes of cells, to define their percentage ratio.

However, the method of a scanning electron microscopy has some eventual shortcomings. As an example we reproduce in Fig. 1 the microphotographs of erythrocytes of a rat peripheral blood obtained with a method of scanning electron microscopy [2].

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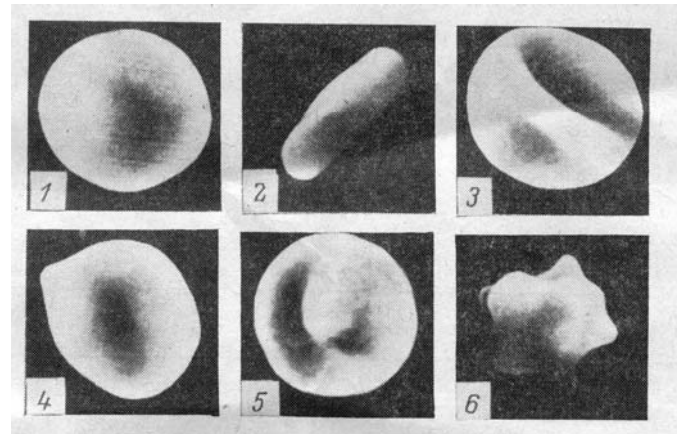
Fig. 1. Microphotographs of a rat peripheral blood erythrocytes (scanning electron microscopy)

II. SHORTCOMINGS OF SCANNING ELECTRON MICROSCOPY

The main source of scanning electron microscopy shortcomings is connected with necessity to put biological object in vacuum. Vacuum guesses long-lived, complicated and expensive preparation of an examined object.

This preparation includes [3] fixing of the object, deprive of water, drying and electrical conductivity enhancement. Long time is necessary (about 3 days) for these stages execution and this time may not be shortened without quality of micro object worsening.

If may be pointed out that scanning electron microscopy may be used without such onerous object preparation. Two possible ways are described in [3] and consist in: the first one – special gas camera installation in the column of electron microscope, and the second one – usage of non standard mode of electron microscope action (low voltage and beam current, short time of image formation, worse signal/noise radio e.t.c.) Both ways are useless for blood cells investigation because of them quick deprive of water.

At the same time, the morphological classification of erythrocytes of the person introduces large value in clinical diagnostic of early stages of disease, therefore creation of widely accessible instrumentation permitting with standard blood preparation to receive operatively the information about surface architectonics of erythrocytes, is apart actual.

III. POSSIBILITIES OF TELEVISION SCANNING OPTICAL STEREOMICROSCOPY

Television scanning optical stereomicroscopy, preserving main idea of scanning with probe, allows to use light probe which is free of destructive influence onto erythrocytes.

As a base for such instrumentation creation, the television scanning optical microscope can be successfully used [1], as its maximum working magnification is 10000x at usage of a lens 40x and spatial resolution the tenth parts of micrometer, allows to find out a relief of erythrocytes surface.

For analysis of erythrocytes surface architectonics it is necessary, that the scanning optical microscope creates a 3-D image of an object. The optical scheme of such stereomicroscope is shown in Fig. 2.
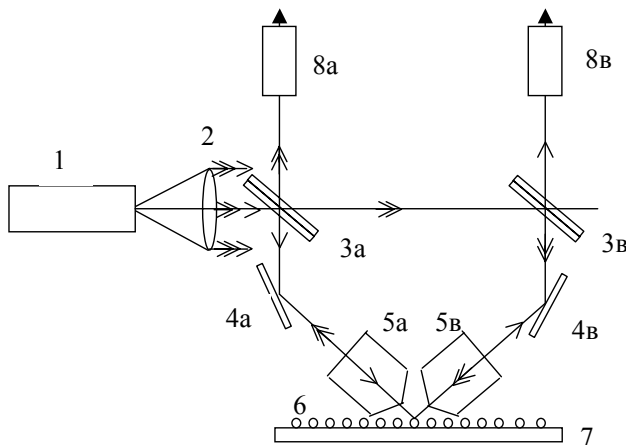
Fig. 2. The optical scheme of scanning stereomicroscope

The scanner 1 on projection cathode-ray tube of high resolution with polychrome luminescence of a screen forms a micro raster, the luminous flux from which one by a lens 2 is transformed to a parallel pencil of rays. The interference light filter [4] 3a reflects one of spectral components on a metallic mirror 4a, which one routes a parallel pencil beam of light to a microscope lens 5a, in a focus of which one there is an investigated object 6 on a substrate 7. Diffused by the object light, collected by a lens 5b, having reflected from a metallic mirror 4b easily permeates the interference filter 3b on a photo multiplier 8b, the signal from which one goes in computer, adapted to stereo images processing and display. The light pencil of beam with other spectral component, passing through the interference filter 3a, is reflected from the filter 3b and mirror 4b, falling in the lens 5b, is dispersed by the object 6, collected by a lens 5a, reflected from a mirror 4a and through the interference filter 3a falls on a photo multiplier 8a, the signal from which one also goes to the computer. Thus, the interference light filters, having split a light pencil of beam on two spectral components, lights the object from two sides, have ensured the information on the object, sufficient for construction 3-D image on the screen of computer monitor. The computer image processing with usage of a software used in a photogrammetry, allows to compound the topographic map of investigated object relief.

In Fig. 3 example of the images, experimentally obtained with microscope action simulation by one-channel television scanning optical microscope usage, are presented. 21x lens was used in microscope. Fig.3a and Fig 3b show test object as orthogonal metallic grid, covered with particles of another metal at different magnification. Dimensions of grid cell is 30×30 μm. The erythrocytes of human's blood (standard fixed and dyed smear for morphological examination) are shown in Fig. 3c. All images were not processed with computer.
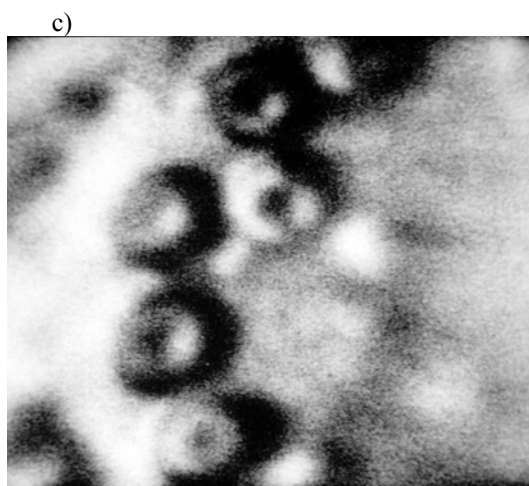
a)

b)

c)
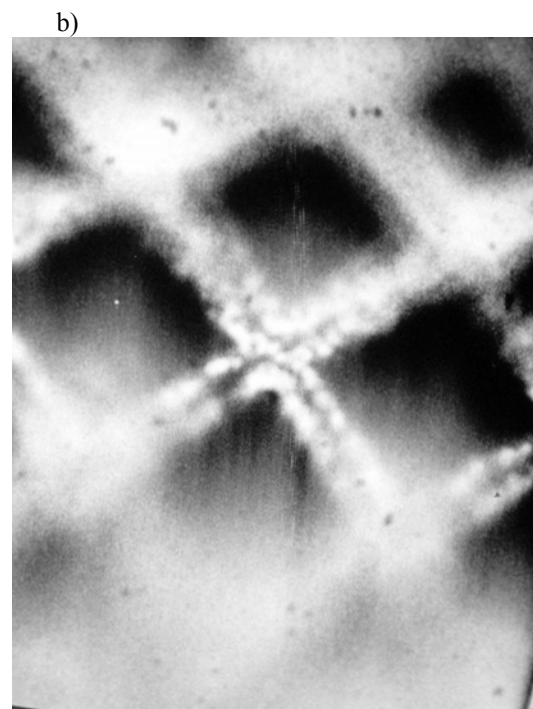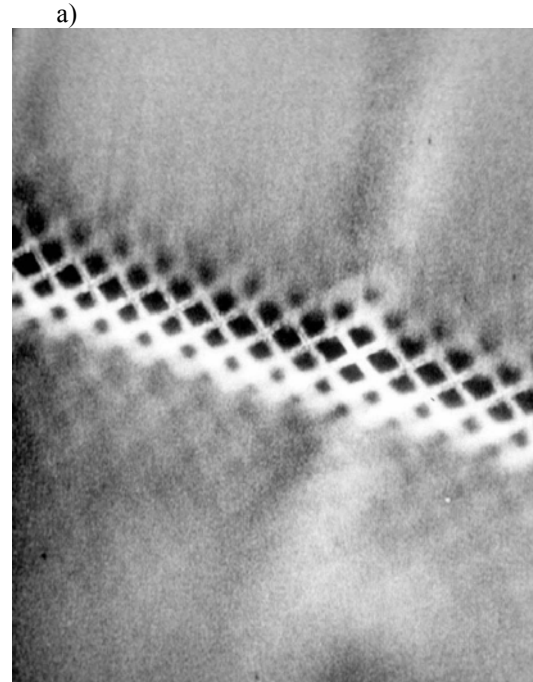
Fig. 3. Images of test object (metallic grid) and erythrocytes
obtained with television scanning optical microscope usage

IV. CONCLUSION

Thus, usage of a television scanning optical stereomicroscope for surface architectonics of blood cells analysis, will allow to expand essentially diagnostic capabilities of microscopic examinations and to make their realization accessible in clinical labs.

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Push-Pull Class-D High Frequency Generator for Industrial Applications

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Abstract - **There are various industrial processes calling for reliable and cheap high frequency energy regulation. High-frequency generators are sources, appropriate for applications of the kind since they are highly efficient reliable and cheap systems. This paper presents the design of a high frequency generator by push-pull scheme class D realized with HEXFET Power MOSFET transistor sets. The transformer output provides galvanic load division. PWM control current scheme and PLL circuit is used.**

Keywords – **High Frequency Generator, Power Supply**

I. INTRODUCTION

The high frequency (HF) power generators are widely used for variety applications such as induction and dielectric heating. For this applications are needed the HF power levels from watts to tens of kWatts and frequencies from kHz to MHz. Different circuits and active devices are used in the HF power generators to produce AC power to the load at a single frequency from a DC input source. The basic structure of this process is shown in Fig. 1. From the AC line with a DC converter and a HF power generator the AC output power at required frequency is detached to the load.
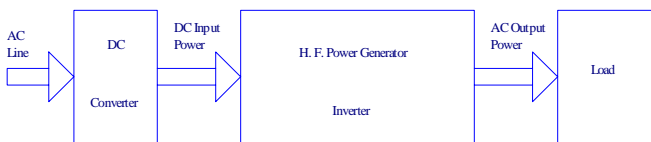
Fig. 1. Basic function of HF Power Generator

Solid state (SS) HF power generators offer a lot of advantages as a low cost, stability, small size and weight, lower operating voltage and control of the output power. To improve efficiency and increase the output power, the solid-state generators operated in the switching mode.

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II. OPERATING PRINCIPLE

In this paper is present SSHF power generator for an induction heating of non-ferrous thin tapes. The block schemeof the HF solid-state power generator is show in Fig. 2. The generator consists of three basic parts: inverter, PLL control and PWM control.
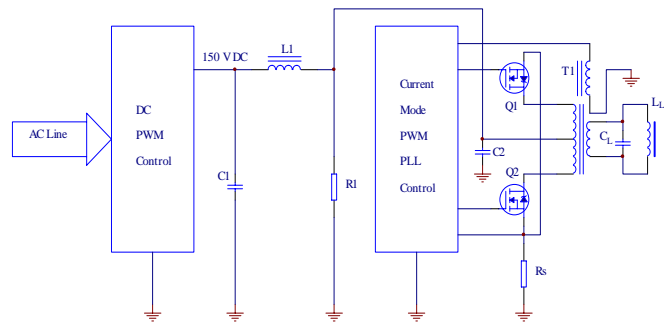
Fig. 2. Block schematic of HF generator

The inverter part in the generator consists of a single-phase half bridge push-pull class D with HEXFET power MOSFET transistors. The resistor R_S is a sensor for the current mode in the MOSFET switches. The output frequency is regulated fro 1 to 1.5 MHz according to the technological process. An output transformer with a transformation ratio 1:6 for the impedance matching on the load is used.

The soldering of the non-ferrous thin tapes is made with an inductor L_L = 3.9 μH, compensated in the resonant parallel circuit from a capacitor C_L = 5.6 nF. The equivalent resonant resistance is $R_e \approx 572$ Ω.

To compensate the alteration of the load and the resonant frequency a PLL circuit is included. . The output power is regulated to P_{out} = 750 W with DC power PWM control at V_{DC} = 150 V.

III. CALCULATION

Using the presented method for calculations in [2], the electric parameters of the solid-state HF generator are the next:

-necessary output voltage for the maximum output power from $750\,W$ is $V_{out} = 655\,V$;

-duty cycle $D_{\max} \approx 90\,\%$;

-the input power is $P_{in} = 1000\,W$

-the efficiency [7] is $\eta = 0.75$;

-the primary RMS current is $I_{p(rms)} = 4.99\,A$;

-minimum voltage in the primary turn is $V_{pri(\min)} = 130\,V$;

-minimum voltage in the secondary turn is $V_{sec(min)} = 656\,V$;

-turns ratio:

$$N = \frac{V_{pri(min)}D_{(max)}}{V_{sec(min)}} = 1:5{,}84 \qquad (1)$$

For a galvanic detached on the load inductor from the AC line and the matching on the load with the output resistance of the inverter the high frequency transformer is used. The turns ratio of the high frequency transformer is approximately 1:6.

The inductance of the second turn with ferrite core 3F4 is $L_{(sec)} = 744\,nH$, the number of the turns is $N_{(sec)} = 12$.
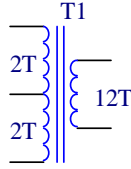
Fig. 3. Transformer Schematic

The minimum cross-sectional core that can be used is calculated from [6] with the following equation for core loss limited applications.

$$A_C = \frac{V_{pri(min)} \cdot Duty_{(max)} \cdot 10^4}{2 \cdot F_{req} \cdot N_{(pri)} \cdot \Delta B} = 1.2 \quad cm^2 \qquad (2)$$

To minimize the eddy current losses and skin effects in high frequency magnetic design from [3] is calculated the penetration

$$d_{pen} = \frac{7.5}{\sqrt{F_{req}}} = \frac{7.5}{\sqrt{1.5 \cdot 10^6}} = 6.12 \cdot 10^{-3}\,cm \qquad (3)$$

For low current windings and the skin effects the several strands of thin Litz wire is used. The practice in the industry is to operate at 450 amps (RMS) per centimeter squared, or $2.22 \bullet 10^{-3}$ cm/A..

Area required for primary area is $A_{xp} = 1.1 \cdot 10^{-2}\,cm^2$ and for secondary area is $A_{xs} = 2.56 \cdot 10^{-3}\,cm^2$.

For the primary turn is used copper foil 2 cm wide.

The necessary cross-sectional area of the secondary turn is

$$\frac{A_{xs}}{\#conductors} = \frac{2.56 \cdot 10^{-3}}{2} = 1.28 \cdot 10^{-3}\,cm^2 \qquad (4)$$

For the secondary turn is used a Litz wire with cross-sectional area of $2.46 \bullet 10^{-3}$ cm^2.

The total transformer power losses are consisting from the copper losses and the ferrite losses.

$$P_{CU} = P_{Rpri} + P_{Rsec} \approx 1\,W \qquad (5)$$

The ferrite losses can be calculated as a multiplication on the core volume $U\ cm^3$ with the losses per cubic centimeter

$$P_{core} = B \cdot c = 2.75\,W \qquad (6)$$

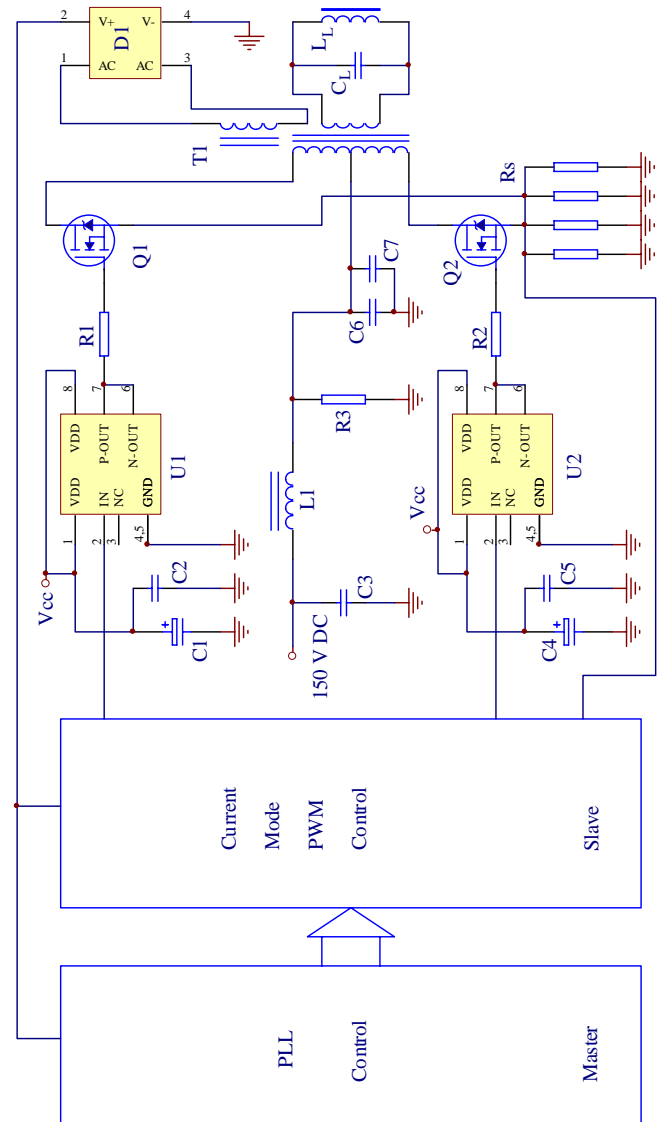Fig. 4. Function schematic of HF generator

The total transformer power losses are

$$P_{HFTr} = P_{CU} + P_{CORE} = 3.75\,W \qquad (7)$$

The HF generator losses include the sensor resistor R_s

$$P_{Rs} = I_p^2 \cdot R_s \cdot D_{max} = 5.48 \, W \qquad (8)$$

and the losses in the switching transistors

$$P_{Sw\,Tr} = 2 \cdot P_{dc} = 26 \, W . \qquad (9)$$

The total HF generator losses are

$$P_{total\,losses} = P_{Rs} + P_{Sw\,Tr} + P_{HFTr} = 35.23 \, W . \qquad (10)$$

III. EXPERIMENTAL RESULTS

Fig. 4 shows the push-pull configuration with the driver for the inverter part, PLL and current mode PWM control of the HF generator. The inverter is operated in class D mode using HEFET power MOSFET transistors. The switching mode of the power MOSFET transistors is set from the drivers EL 7104 CN.

The waveforms of the voltage V_{GS} of the power transistors are shown in Fig. 5.
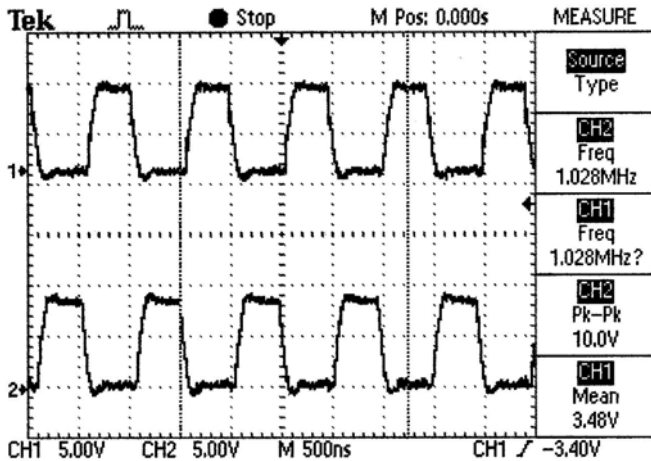
Fig. 5. Waveforms of the voltage V_{GS}

To obtain tuned to the working frequency and the switching mode a current PWM control is used. For this purpose the controller ML 4825 get information from the current in the resistor R_S. When the When the current in the resistor R_S is increased over the critical level the controller switch off the power MOSFET transistors and the generator. As a first step for the tuning of the generator is used an active load. The waveforms of the current I_D and the voltage V_{DS} on the power transistors are shown in Fig. 6.
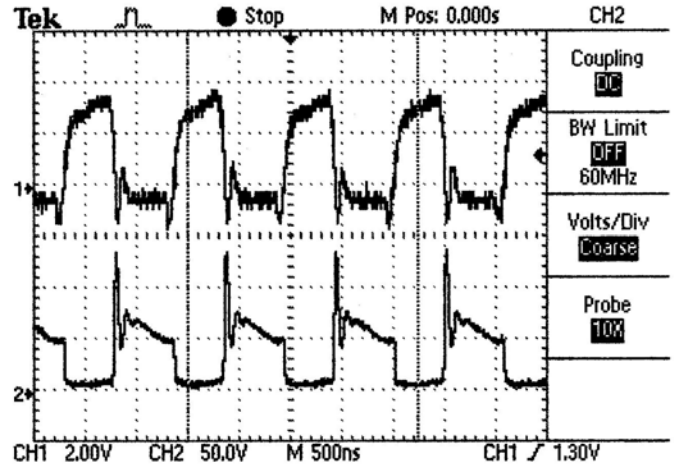
Fig. 6. Waveforms of the current I_D and the voltage V_{DS}

The generator works is constructed for an induction heating of the non ferrous thin tapes. The wave forms of the current I_{R_S} in the resistor R_S and voltage V_{L_L} are shown in fig. 7.
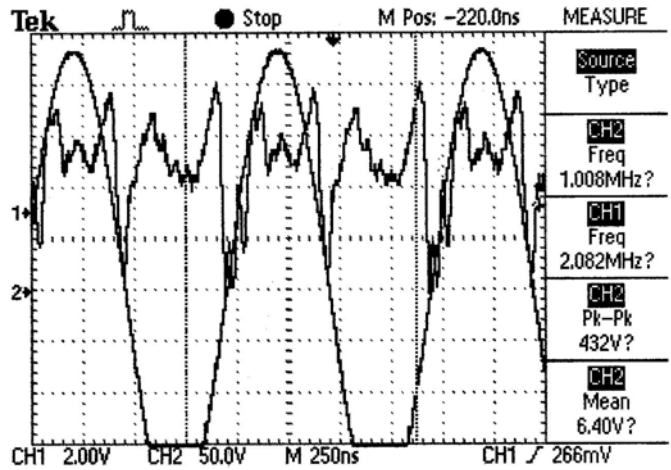

Fig. 7. Waveforms of the current I_{R_S} and the voltage V_{L_L}

IV. CONCLUSION

The parameters of the load of the generator and its resonant characteristic are shown in Fig. 8. The resonant characteristic has a narrow band and consequently, the mode of the generator have to be tuned to the resonant frequency.

The maximum output power in the load we receive with help of the PLL controller in synchronization with Current mode PWM control in the system Master-Slave.

From the output power in the load and the losses in the
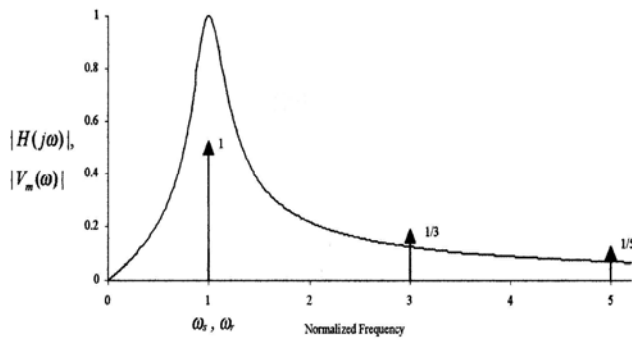
$$L_L = 3.9\ \mu H, \quad C_L = 5.6\ nF, \quad \rho \approx 26\ \Omega, \quad Q \approx 26$$

Fig. 8. Resonant characteristic

MOSFET transistors is calculated the efficiency of the generator approximately of 95%. The investigated generator may be used for different purposes in the induction heating.

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INSTRUCTION FOR AUTHORS

Name of the author/s, Affiliation/s

Abstract: *Short instruction for authors is presented in this paper. Works that are to be printed in the review "Electronics" should be typed according to this instruction.*
Keywords: *Review Electronics, Faculty of Electrical Engineering in Banjaluka, Instruction for authors.*

1. INTRODUCTION

In the review "Electronics", we publish the scientific and professional works from different fields of electronics in the broadest sense like: automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. In addition to the scientific and professional works, we present new products, new books, B. Sc., M. Sc. and Ph.D. theses.

In order to enable the unification of the technical arrangement of the works, to simplify the printing of the review "ELECTRONICS", we are giving this instruction for the authors of the works to be published in this professional paper.

2. TECHNICAL DETAILS

2.1. Submitting the papers

The works are to be delivered to the editor of the review by the E-mail (elektronika@etfbl.net) or on floppy (or CD) by post mail to the address of the Faculty of Electrical Engineering (Elektrotehnicki fakultet, Patre 5, 78000 Banja Luka, Republic of Srpska, Bosnia and Herzegovina).

2.2. Typing details

The work has to be typed on the paper A4 format, 8.27" width and 11.69" height (21.0x29.7 cm), upper margin of 1" (2.54 cm) and lower margin of 0,59" (1,5 cm), left and right margins of 1,57" (2 cm) and 0,39" (1cm) (mirrored margins). The header and footer are 0,5" (1.27cm) and 57" (2 cm). The work has to be written in English language. Our suggestion to the authors is to make their works on a PC using the word processor MS WORD 97/2000, and for the figures to use the graphic program CorelDraw, if the graphs are not going from the original programs, i.e., from the programs received (like MATLAB).

The title of the work shall be written on the first page, in bold and 12 pt. size. Also, on the first page, moved for one line spacing from title, the author's name together with the name of his institution shall be printed in the letter size (10pt, *Italic)*. The remaining parts of the manuscript shall be done in two columns with 0.5cm distance. The work shall be typed with line spacing 1 (Single) and size not less than 10 pt (like as this instruction). After the title of the work and the name of the author/s, a short content in English language follows, written in italics. The subtitles in the text shall be written in bold, capital letters of the size as in the text (not less than 10 pt.). Each work shall, at the beginning, comprise a subtitle INTRODUCTION, and, at the end, the subtitles CONCLUSION and BIBLIOGRAPHY / REFERENCES.

The operators and size marks that do not use numerical values, shall be written in common letters. The size marks that can use numerical values shall be written in italics. The equations shall be written in one column with right edge numeration. If the breaking of equations or figures is desired, those may be placed over both columns.

Illustrations (tables, figures, graphs etc.) may be wider than one column if necessary. Above a table there shall be a title, for instance: Table 2. *The experimental measuring results.* The same applies to figures and graphs but the accompanying text comes underneath the figure of graphs, for instance: Fig.3: *Equivalent circuit diagram...*

The work should not be finished at the beginning of a page. If the last manuscript page is not full, the columns on that page should be made even. Number of pages should not go over 6.

3. CONCLUSION

This short instruction is presented in order to enable the unification of technical arrangement of the works.

4. REFERENCES

At the end of work, the used literature shall be listed in order as used in the text. The literature in the text, shall be enclosed in square brackets, for instance: ...in [2] is shown ...

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