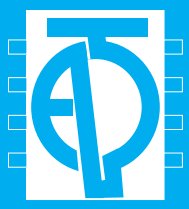

ELEKTROTEHNIČKI FAKULTET
UNIVERZITETA U BANJOJ LUCI

FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITY OF BANJALUKA

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Часопис "Електроника" у издању Електротехничког факултета у Бањој Луци ослобођен је плаћања пореза на промет на основу мишљења Министарства науке и културе Републике Српске, број 06-75/97 од 20. новембра 1997. године

PREFACE

Dear Reader,

In this issue of the Electronics we are following, one may say, the tradition established by the Editor, to pay exceptional attention and to promote the scientific events that were organized in the near past. In this issue we will follow two events. The first one is the Second Small Systems Simulation Symposium, SSSS'05, that took place on March, 28-29, 2005, at the Faculty of Electronic Engineering of the University of Niš. This meeting happens with low frequency and here comes its importance. The second event, that we are representing here, is the Industrial Electronics Symposium, INDEL 2004, (12-13.11.2004) that takes place biannually at the Faculty of Electrical Engineering in Banja Luka.

The SSSS'05 symposium is a unique specialized event that gathers European researchers working in the field of simulation. It was used as opportunity for young researchers originating from this region, but now working in the western world, to represent their results and to keep the connection with their fellow researchers that remained home. Participants from several western and eastern European countries presented their result at this event.

The subject of simulation being interesting and always challenging offered to the participants an overview of the results and paved research directions for future work. At this event, especially, electronic simulation was dominating. Subjects related to microelectronic modelling, artificial intelligence, circuit simulation, logic simulation, system modelling and simulation, including control systems, were prevailing topics. In addition non-electrical and non-technical simulation subjects such as stock market simulation were presented. Thanks to the courtesy of the Editor of Electronics, prof. Dokić, ten selected papers from the proceedings of the SSSS'05 are reprinted in this issue.

The second event is the traditional INDEL conference. This conference, as it is now well known, is dedicated to industrial electronics, one of the most important application areas of the electronic technology. The term industrial gives rise to many aspects of electronics that is why a variety (by subject) of papers were selected by Prof. Dokić and the reprints given here. In fact INDEL 2004 was working in six tracks and a paper from averz track was selected for publication in Electronics.

I hope that you will find the contentent of this issue interesting to read and representative enuogh to show the scientific level of the symposia under consideration.

Sincerely

Prof. V. Litovski

SHORT BIOGRAPHY OF GUEST EDITOR

Dr Vančo B. Litovski, full prof.

Prof. Litovski was born in 1947, in Rakita, South Macedonia, Greece. His basic education was in Bitola, Macedonia. He entered the university of Niš, Faculty of Electronic Engineering, in 1965, and graduated in 1970. Just after, he joined the University of Niš as teaching assistant. He received the MSc. And Ph.D. From the University of Niš, Faculty of Electronic Engineering, in 1974, and 1977, respectively in the class of Prof. B. Racović. He was elected a full professor for Electronics and CAD of Electronic Circuits in 1978. In 1999 he was elected a Visiting Professor at the University of Southampton, England. He is now serving as Prof. Litovski id married and has two grown up children.

The research work of Prof. Litovski is related to CAD of electronic circuits and systems. His previous interest was in development of algorithms, methods, and software for CAD for electrical and electronic filters for telecommunications. Later prof. Litovski's interest encompassed the broad field of CAD of electronic circuits including CAD of integrated circuits. To his name and work are related the first Serbian software packages for electronic circuit simulation and for integrated circuit design, and the first designed integrated circuits in Serbia. The first domestic software system for design of gate-arrays (custom integrated circuits) was developed and implemented. Also, the first domestic gate-array circuit was designed and produced in collaboration with "Elektronska Industrija", "Rudi Čajavec", and Elektronski Fakultet.

Prof. Litovski is author or co-author of more that 300 scientific papers with more than 40 of them published in the most recognised international scientific periodicals. He has papers published at best recognised international conferences too. He wrote (alone or in a team) textbooks, problem solvers, and laboratory guides for any subject he thought. He published more than 15 such books one of them in Great Britain in English language.

Prof. Litovski was the founder and the first editor of the scientific journal “Facta Universitatis, series: "Electronics and Energetics”.

Prof. Litovski is member of "The Institute of Electrical and Electronic Engineers", "The Association for Computing" and ETRAN. Prof. Litovski gave the initiative for the establishment and is the current president of the Yugoslav Simulation Society established on February 1999. He is a full member of the Academy of Engineering Sciences of Serbia and Montenegro.

He received several Awards from the City Council of Niš and The University of Niš for distinguished results in studying and exceptional contributions to the development of The Faculty of Electronic Engineering and The University of Niš. Similar recognition came from the Faculty of Electrical Engineering of the University of Banja Luka. He got recognition from the Scientific Journal "Tehnika" on the occasion of the 25th anniversary of the journal for contribution to the development of the journal. He was awarded the best paper award in the track of Electronics by the ETAN Conference in 1986. He received (1994) the "Tesla" award for outstanding engineering and technological achievements, by the independent "Tesla" association. Finally he (and a group of co-authors) was awarded The Savastano Award given by The European Federation of Simulation Societies for the best paper published in the period 1995-1997.

TESTING OF THE DEVICE FOR COMMUNICATION IN THE TOOL FOR MEASUREMENT OF PIPE DIAMETER AND FLUID FLOW IN THE BOREHOLE

Miloš Slankamenac, Miloš Živanov, Fakultet tehničkih nauka, Univerzitet u Novom Sadu
Krešimir Knapp, Hotwell Ges. m. b. H. Klingenbach, Austria

Abstract: *In this paper an implementation and test of the device for communication between Telemetry system and Surface unit with the tool for measurement of pipe diameter, fluid velocity and direction of flow in the borehole (Calliper-Fullbore Flowmeter - CFF) are presented. This communication is done according to SIPLOS (Simultaneous Production Logging String) protocol and it is used by Hotwell company [1] as a part of a larger system for borehole investigations.*

Keywords: Communication protocol, Borehole, Measurement, Logging tools.

1. INTRODUCTION

Systems for borehole investigation consist of: A Surface unit for analysis and presentation of measurement results, logging tools, a cable for mechanic and communication link between logging tools and the Surface unit and equipment for relocating tools (Fig. 1).

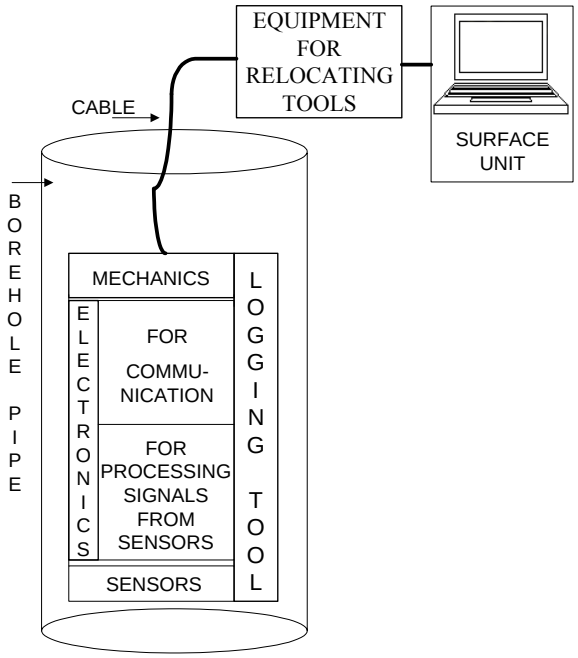


Fig. 1. *Block diagram of a system for borehole investigation.*

Digital systems for borehole measurement measure more parameters at the same time than analogue systems. Because of this advantage, the process of logging is much shorter and cheaper. Establishing digital systems complex of processing data from sensors and communication between tools and the Surface unit are larger. At the same time, more parameters are measured and processed data are sent to the Surface unit. Because of larger number of sensors and electric devices for processing data and smaller dimensions of digital tools than analogue tools, projecting of mechanical parts and PCBs (Printed Circuit Board) are much more difficult. Digital logging strings are smaller, more reliable and more effective for processing and storing data than analogue logging strings.

The digital system for borehole investigation – SIPLOS consists of a Surface unit (Fig. 2), Telemetry tool (Fig. 3) and other tools in a logging string. The SIPLOS is projected to work in high temperature conditions, up to 180ºC and under high pressure, up to 103.4 MPa (15000 psi). Logging tools have to be very reliable because these measurements are very expensive, take a lot of time and should be done in the first attempt.

The Surface unit is located in a special motor vehicle near the borehole pipe, where the measurement is performed. It provides, via a cable, DC supply for logging tools. The Surface unit consists of a computer with Warior software which collects, processes and shows graphical and numerical formats of data. There is also a control table for display of the voltage that supplies the tools and current that is necessary for the tools. Warior is a universal program for display of data from various types of tools. In addition, there is a possibility for calibrating and adjustment of data received from boreholes.

There are also programs for analyzing measured values. Based on this analysis, the final report of a borehole potential is done.

Fig. 2. *The Surface unit of the SIPLOS system and motor vehicle.*

The Telemetry tool is the first and the only necessary tool in the string of production tools and it is connected to the top of the cable head. It has capability for logging of CCL (Casing Collar Locator), internal temperature, external temperature, pressure, fluid identifier and gamma ray. The Telemetry tool sends synchronization bits for all other tools in the string.

Fig. 3. *The Telemetry tool.*

The Telemetry tool is the first and the only necessary tool in the SIPLOS system, whilst all other tools are optional. In addition, there is all necessary electronics (amplifiers, signal conditioners, DC/DC converter, line driver, etc.) inside the Telemetry tool. On the bottom of the Telemetry tool there is a single connector with line voltage where it is possible to connect other tools in the string for simultaneous production logging [2].

CFF tool combines a two axis (X-Y) calliper with a fullbore flowmeter in a single device. Fig. 4 depicts connection of the Telemetry and CFF tool.

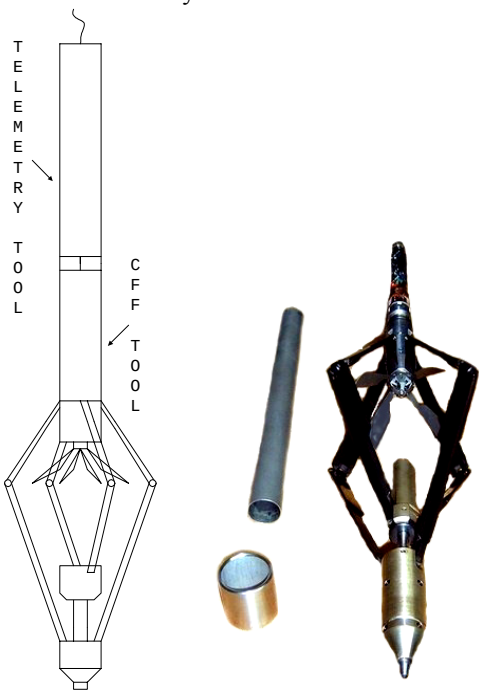


Fig. 4. *The Telemetry and the CFF tool.*

The CFF tool, shown in Fig. 4, measures pipe diameter in range 2½"-7" (6.35-17.8 cm). X-Y calliper is designed for downhole pipes diameter measurements in two axes, X-Y. The pipe diameter that is sensed by the calliper arms is magnetically transferred to a linear position sensor. The position sensor is a part of electronics that converts linear position to the output pulses. Flowmeter performs bi-directional measurement of the rotational speed and direction of a turbine wheel (spinner or impeller), in relation to fluid flow inside the well [3]. The four-arm CFF device is designed to provide autonomous displacement in X and Y-axis, and uniquely allows the spinner to rotate whilst partially closed.

The protocol device has to provide an accurate and reliable communication between the CFF tool with the Telemetry tool and the Surface unit in very difficult conditions for measurement in a borehole. The main problem is high and variable temperature (up to 180 ºC) causing significant drop of frequency of the oscillator in microcontroller and changes characteristics of some electronic components.

2. SENSORS PART OF THE CFF TOOL

Fig. 5 represents a CFF calliper block diagram. The calliper arm position is measured by using a transformer based position LVDT sensor.

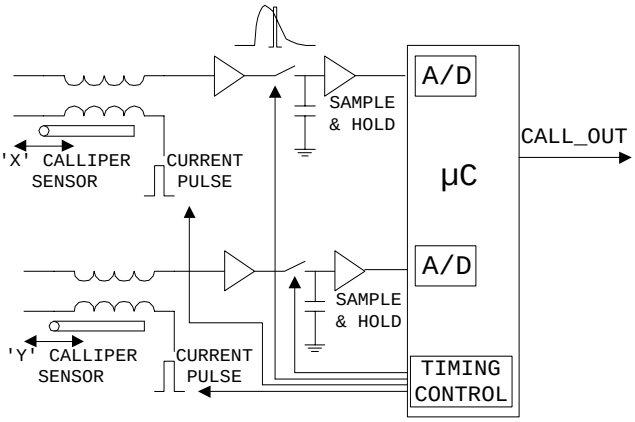


Fig. 5. *CFF calliper block diagram.*

When a diameter of a pipe is changed, a metal rod is moved within the transformer core that has the effect of varying the coupling between transformer's primary and secondary (Fig. 6).

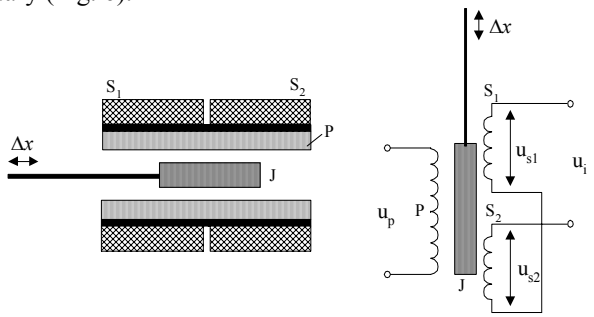


Fig. 6. *Concept of constructing and schematic representation of a LVDT sensor [4]*

The transformer primary is driven by a fixed amplitude voltage pulse and the degree of coupling is determined by measuring the resultant signal in the transformer secondary. Thus the amplitude of the detected secondary signal is proportional to the arm position and hence to the diameter of the well-bore. The complete calliper system is controlled by a microcontroller PIC 16F876. It controls timing of the primary drive signals and uses an internal A-D converter to sample the transformer secondary signals. In operation, voltage pulses are applied to the transformer primary. The voltage across the transformer secondary will rise sharply with the rising edge of the pulse and then decay at a rate dependent on the inductance of the transformer system. This inductance depends on the position of the sensor rod within the transformer core. If the decay waveform is sampled at a precise time after the rising edge of the primary pulse, the magnitude of the sampled voltage will be linear proportional to the rod position. This voltage is measured by the A-D converter. The processed data are transmitted by UART to the CFF protocol device in standard RS232 format (1 start bit, 8 data bits and 1 stop bit) with rate of 115,2 Kbaud.

The flowmeter uses an array of five fixed Hall effect sensors operated by a rotating magnet assembly containing two outward facing poles (Fig. 7). This results in 10 sensor operations per revolution of the impeller. The sequence of sensor operations indicates the direction of rotation. The rate of sensor operations is proportional to the flow rate. The flow rate and direction signals are sent by microcontroller PIC 16F876 to the CFF protocol device.

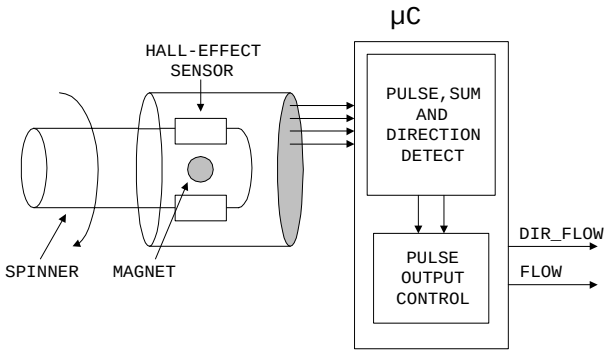


Fig. 7. *CFF flowmeter block diagram*

4. CFF PROTOCOL DEVICE

All tools, which are connected together, send packets of processed data from sensors during 200 ms according to SIPLOS protocol, which is described in detail in [2].

Fig. 8 depicts block diagram of hardware realization of CFF tool's part for communication between sensors and surface system according to pulses from the Telemetry tool.

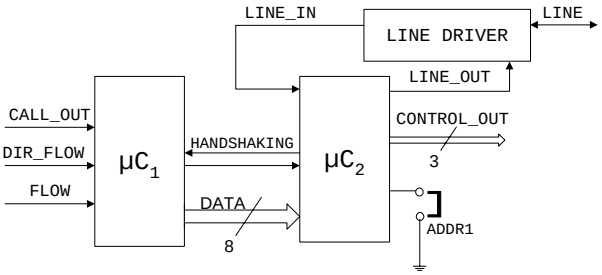


Fig. 8. *Block diagram of CFF protocol device.*

A microcontroller PIC 16F627 (μC_1 and μC_2) are chosen for realization of CFF protocol device [5], because it has: a large number of programmable pins, serial UART port, internal pull-ups and it works on higher temperature very reliably, which is tested experimentally.

LINE is bi-directional signal from Telemetry tool that consists of a line voltage (70V) from the Surface unit and negative pulses (START, STOP, SYNC) from the Telemetry tool and CFF protocol device (DATA bits). Telemetry tool transmits START, STOP and SYNC pulses to all other tools. DATA bits are transmitted by all measuring tools to surface unit in determined interval of time. LINE DRIVER is a device that converts line voltage into CMOS voltage level, discriminates pulses from LINE signal and makes LINE_IN signal. LINE_IN signal contains START, STOP and SYNC pulses that determine timing for sending DATA from CFF to surface unit. LINE DRIVER receives LINE_OUT signal from μC_2 that is converted into corresponding pulses, positioned in the middle of a data-bit frame, whose duration is 50μs ± 10% and sends it to surface unit. CONTROL_OUT are signals for verification purpose, which contain an error signal and two signals for verification of synchronization. μC_1 receives signals CALL_OUT, DIR_FLOW and FLOW from sensors. CALL_OUT contains information about pipe diameter from calliper in RS232 protocol form. DIR_FLOW and FLOW contain information about flowmeter impeller direction and frequency given in a pulse form.

Algorithms for programmes of both microcontrollers, which are shown in [2], respect possible obstruction and changes in time intervals because of high and variable temperature conditions.

5. RESULT OF SIMULATIONS

Simulations of work of microcontrollers PIC 16F627 were performed successively by MPLAB IDE [6] AND PIC IDE. Simulator Stimulus options were used to simulate input signals. DIR_FLOW, ADDR, and HANDSHAKING signals were simulated by Asynchronous Stimulus option where it is possible to change state of particular pins during the simulation.

LINE_IN signal is programmed before a start of a simulation using Pin Stimulus option. LINE_IN signal, which represents START and STOP pulses from the Telemetry tool and Data pulses from other tools, is simulated by making files in a textual format. In this way some SIPLOS sequence '0' and '1' are presented.

When a signal is programmed in a textual format, it should be started in simulator at desirable moment. There is a possibility of temporary stop of the simulation of some signals, which is very useful for testing functionality of some parts of the program.

FLOW signal, which presents pulses from Hall sensors, is shown as periodical signal of equal pulses. It is done by Clock Stimulus option, using a lot of pulse sequences of various duration, which simulates change in rate of impeller. During this time, temporaries that count number of revolution for two directions are observed.

CALL_OUT signal is simulated by setting the duration of sequence '0' and '1' in RS232 form for 115,2 kbaud rate protocol.

Program PIC IDE, unlike MPLAB, has more options for simulation of serial communication, A/D conversion and simulator is more descriptive.

Output signals, SFR registers and memory content were observed during the simulation step by step. All of input signals were simulated for ideal and the worst temperature conditions [3] and expected output signals were obtained.

6. EXPERIMENTAL RESULTS

Fig. 9 shows a scheme of a test board, which was used before final version of PCB is made. Serial port of a computer and program PIC IDE are used for generating CALXY signal. Parallel port of a computer and program SIPSIM are used for generating LINE_IN signal.

This manner of testing, with generating test signals that send sensors from the CFF tool and the Telemetry tool, is used because the tools were not always accessible during the testing. In addition, this method provides checking of accuracy of communication for known sequences.

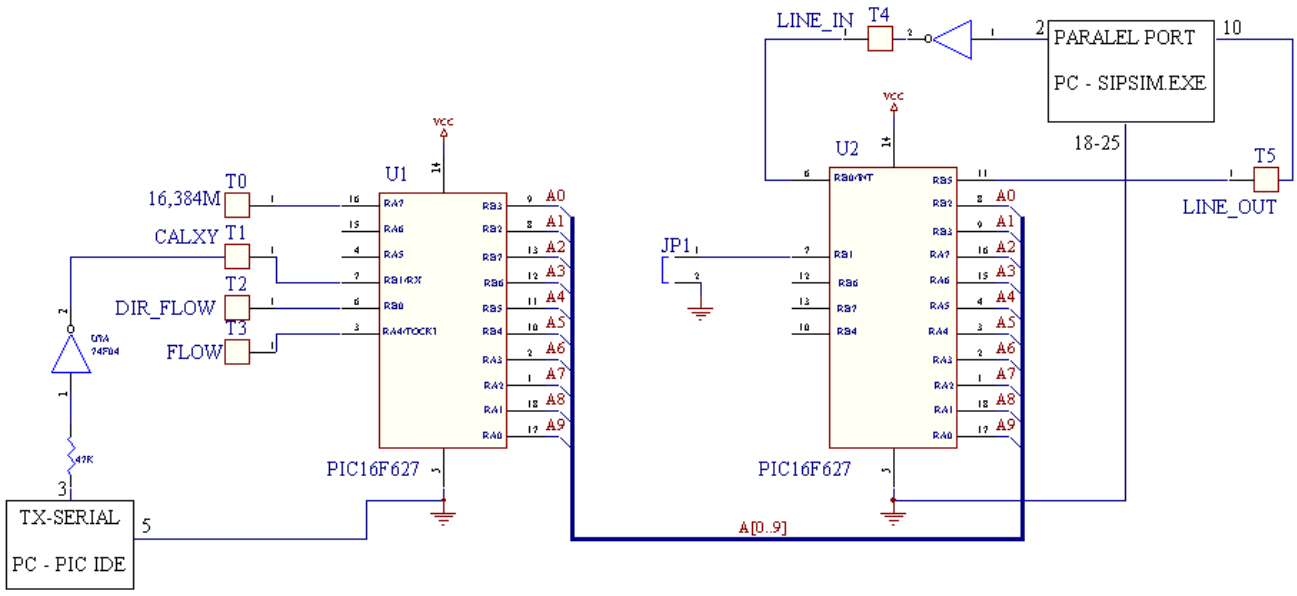


Fig. 9. *Block diagram of test board*

Fig. 10 depicts the appearance of a test board with connectors and cables for connection with a computer. You can also see wires with labeled name of signals, which are observed by oscilloscope or they are supplied by signals from a function generator.

Program SIPSIM sends LINE_IN signal to the second microcontroller via parallel port and receives LINE_OUT signal from it. Duration of all pulses from LINE_IN signal is possible to change simultaneously via keyboard. In this manner, checking of work of microcontroller is done for occasion when frequency of oscillator is changed because of the increase of temperature. On the monitor of a computer number values of data are displayed, which are sent according to the SIPLOS protocol. If synchronization is not correct or there are some wrong pulses, program will show a message that indicates a mistake. FLOW signal is supplied via function generator in pulse form. Table 1 shows the number of pulses during 200 ms, for various frequency of FLOW signal.

Table 1. *Review of increment values of FLOW signal by SIPSIM program.*

FLOW (Hz)	INCREMENT (during 200ms)
10	1-2
50	10
100	20
300	60
500	101-102
1k	205-206

Testing of serial communication on real hardware via serial port of a computer is provided by using *PCs serial port terminal* option in PIC IDE program. Particular bytes and sequences are sent at desirable rate to RS232 microcontroller serial port (UART). In this manner CALXY signal is generated and correctness of the communication with the sensors for measurement of a pipe diameter is inspected.

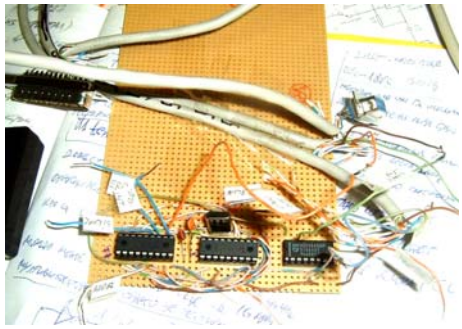


Fig. 10. *Test board with connectors and cables.*

Fig. 11 shows the devices used for testing work of a microcontroller PIC 16F627 on high temperatures. The microcontroller is located in an oven. Some particular pins are welded with high-temperature tinol to wires isolated by teflon. These wires are connected to voltage supply, a tact generator (if external tact for microcontroller is used) and a digital oscilloscope. The temperature of the microcontroller is measured by a universal instrument.

The program in the microcontroller sends pulses, whose frequency is four times less than clock frequency of the microcontroller on the output pin. This signal is observed on an oscilloscope during the heating of the microcontroller.

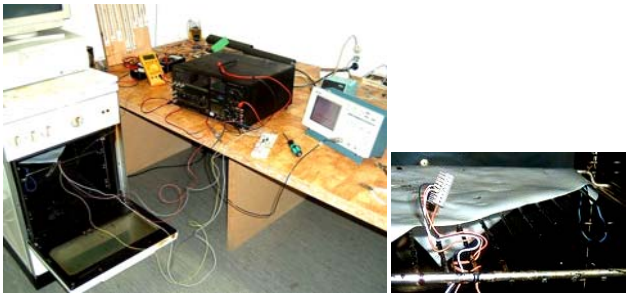


Fig. 11. *Testing of works the microcontroller on high temperatures.*

Testing of the microcontroller on high temperatures is performed by increasing the temperature gradually up to 180°C, and then this temperature is hold for two hours.

During these experiments the supply of the microcontroller is turned on and off, to check the correctness of the work of the microcontroller. It is very important to check, because, in well-bores, momentary turning off of a supply might happen.

The microcontroller was tested for three different configurations of clock frequency. The first configuration was internal clock with 4 MHz frequency, which was very good for the microcontroller operation. At the second configuration output, crystal quartz 16 MHz frequency was used and it was very bad. Problems were already on 80°C, where the clock frequency changed quickly. During turning off and on the supply the oscillator did not work. At the third configuration output, an unstable multivibrator with about 16 MHz frequency is used. In this case the work frequency decreased gradually with increasing of the temperature. The greatest drop of the frequency was 6%, whereas there was no problem after turning off and on the supply of the microcontroller.

Fig. 9 shows the first microcontroller U1 with output clock with 16,384 MHz frequency, whilst the second microcontroller U2 has internal clock with 4 MHz frequency. The first microcontroller works on higher clock frequency, because it receives data by serial communication from sensor's part of the CFF tool with rate of 115,2 kbaud.

Figures 12 and 13 show devices for testing the work of the Telemetry and the CFF tool on high temperatures and pressures. At first, the Telemetry and the CFF tool are connected together and link to the Surface unit. Then all tools are put into the oven which is like a chest (Fig. 13) and has switches for adjusting desirable temperature. Characteristic signals are observed by digital oscilloscope (Fig. 12 and 14) and they are connected by wires to the CFF tool. A device between the oscilloscope and the Surface unit on Fig. 12 controls the pressure, which is 103.4 MPa (15000 psi) maximally for these tools.

Fig. 12. *Devices for testing the work of the Telemetry and the CFF tool.*

Fig. 13. *Testing the work of the Telemetry and the CFF tool.*

Testing the work of the flowmeter and in the CFF tool is done by a compressor, which turn over the impeller by directional air beam. Fig. 13 (right) shows the manner of turning over the impeller while the tools are heating. On the display of the Surface unit (Fig. 2) values, which are presented in number of revolution per second, for both direction of rotate of the impeller, are observed. The compressor with a nozzle is located at different sides of the oven to check the work for both direction of rotating.

Checking the work of caliper in the CFF tool is done by metal pipes with known diameter, where the tool is put. During the heating it is very important that , on all temperatures, the Surface unit displays adequate equal value (nearly constant) for one sort of a pipe.

The result of testing during two hours, for all characteristic sorts of checking, was regular on temperatures up to 180°C.

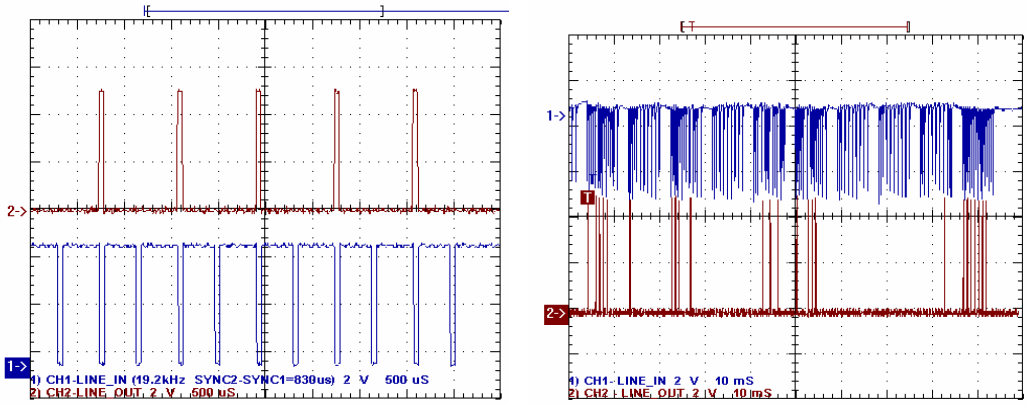


Fig. 14. *Review of signals LINE_IN i LINE_OUT with a digital oscilloscope.*

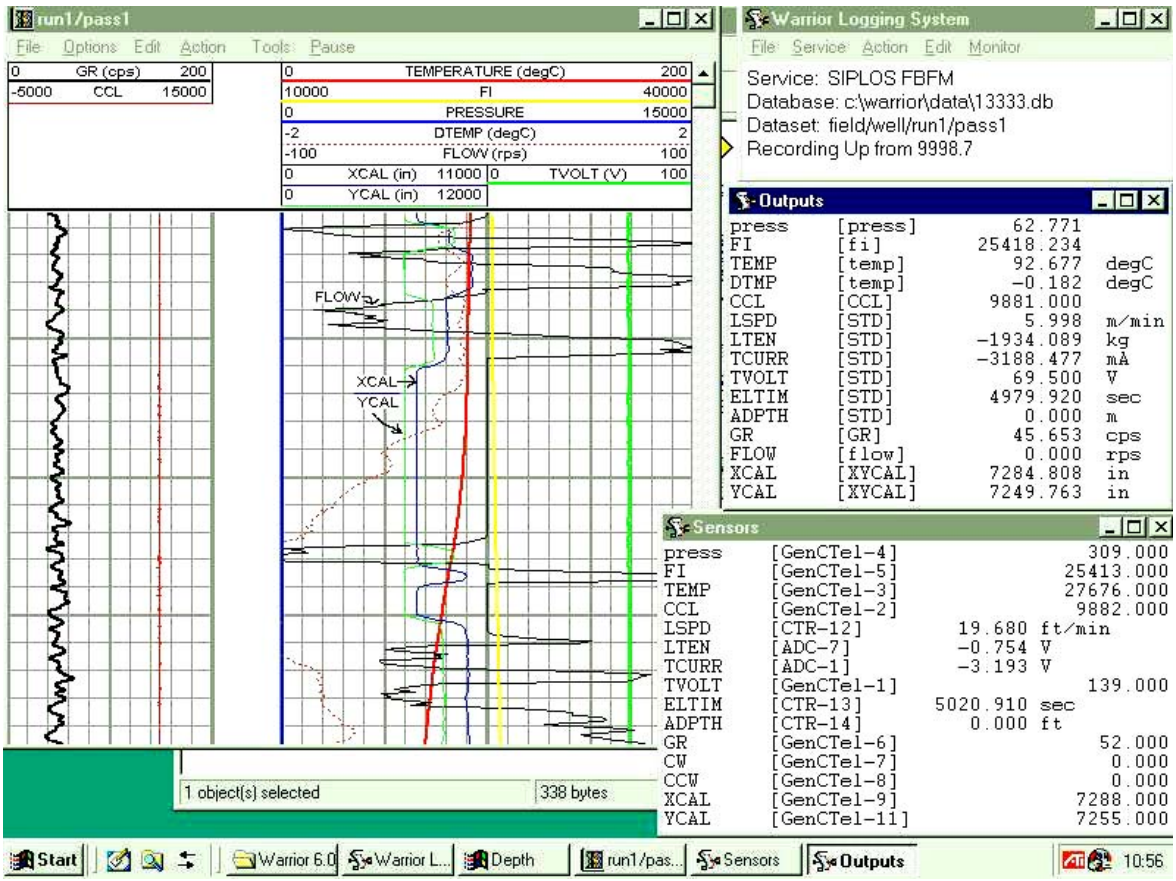


Fig. 15. *Review of grafical and numerical measured values on the Surface unit.*

7. CONCLUSION

In this paper the problem of measurement of the diameter and fluid flow inside boreholes is considered under high pressure (up to 103.4 MPa) and temperature conditions (up to 180°C).

Problem of transfer of measured data to the surface computer, which is used for collecting and displaying data and control of measurement, exists in boreholes. SIPLOS protocol is used where the possibility of appearance of a mistake during the transfer is minimized, by putting synchronization during sending each bit.

The control of synchronization of connected digital tools with the Surface unit is done by the Telemetry tool. The communication system that collects, processes and sends data from measured sensors to the Surface unit according to SIPLOS protocol has been realized. Program for communication has been written and tested by the simulators and the test board. Realized communication system inside the CFF tool (connected with the Telemetry tool) has been tested on the room temperature, then on high temperatures (up to 180 °C). It has been noticed that correct results, which are similar to those obtained by simulators, has been obtained.

The first serial of PCBs has been made and complet measurement system has started working in practise. The first results are very good.

8. REFERENCES

[1] Website: www.hotwell.at

[2] M. Slankamenac, Krešimir Knapp, M. Živanov, "Uređaj za komunikaciju između telemetrijske sonde i senzora u bušotinskim mernim uslovima", Konferencija ETRAN 2004, Srbija i Crna Gora, Čačak, 7-10. juna 2004. godine.

[3] V. Bilas, D. Vasić, "SIPLOS Flowmeter – technical documentation", Hotwell Ges.m.b.H, Austria, 2003.

[4] Dragan K. Stanković, "Fizičko tehnička merenja - senzori", Univerzitet u Beogradu, Beograd, 1997.

[5] N. Matić, "PIC mikrokontroleri" Beograd, MikroElektronika, 2002.

[6] Microchip Technology Inc., "MPLAB IDE User's Guide", 2001.

3D NUMERICAL SIMULATION AND EQUIVIVALENT CIRCUIT MODEL FOR ELECTRICAL MODELING OF HALL SENSOR

Elva Jovanović, Tatjana Pešić, Nebojša Janković, Dragan Pantić, *Faculty of Electronic Engineering in Niš*

Abstract - A three-dimensional (3D) process and device simulations of cross-shaped Hall magnetic sensor fabricated in the standard 0.8μm CMOS technology have been described. The consistent 3D doping profiles are obtained by data interpolation from several 2D doping profiles generated by simulation of sensor cross-sections along main device axes of symmetry. In addition, a novel equivalent circuit model of cross-shaped Hall sensor is developed and implemented in SPICE, and the results obtained from 3D device simulation and from novel circuit model are compared with measured sensitivity characteristics of practical cross-shaped Hall sensor.

1. INTRODUCTION

Solid-state electron magnetic devices whose principle of operation is based on the Hall effect are included in many products, ranging from computers to sewing machines, automobiles to aircraft, and machine tools to medical equipment [1,2]. Achieving high sensitivity of Hall sensors demands usage of non-standard technologies that significantly increases fabrication costs. Even though it is possible to realize good sensitivity performance Hall sensor using standard CMOS technologies [3,4], it requires special attention in structure and layout designing since process parameters cannot be changed. The realization of high sensitive Hall sensors with electronics on the same chip lowers a production cost and improves sensor performances

A cross-shaped Hall sensor (Fig.1) belongs to the majority of Hall devices that, owning to theirs geometry cannot be properly simulated without the inclusion of 3rd dimension. Restriction to 1D or 2D analytical profiles in the simulation domain can severely degrade the accuracy of simulation results. On the other hand, the 3D process and device simulations of sensor devices are rarely reported due to highly demanding simulation tasks tied to software (complex process models, discretization methods, numerical techniques) and hardware limitations ("slow" processors for discretization grids of that size and corresponding numerical operations). In this paper, DIP (*Data Interpolation Package*) software tool, a part of ISE TCAD software package [7], designed to exchange dataset between grids of different dimensions and types is used for incorporating 2D- and 3D doping profiles into one consistent 3D model [6].

In complex structure of Hall sensor fabricated in CMOS technology active region is highly non-uniform. It means that charge carriers distribution varies significantly in all three-axis direction so analytical methods cannot be applied. Very efficient method [5] of performing the numerical analysis is to construct a device equivalent in the form of an electrical circuit and than solve it using circuit simulation program. In this way, approximate values of macroscopicall voltage and current quantities can be acquired. In this paper that approach was used in order to construct Hall sensor equivalent circuit suitable for incorporating with another circuits. A network of identical basic cells, consisting of conventional circuit elements, using circuit simulation program SPICE, simulates the whole device.

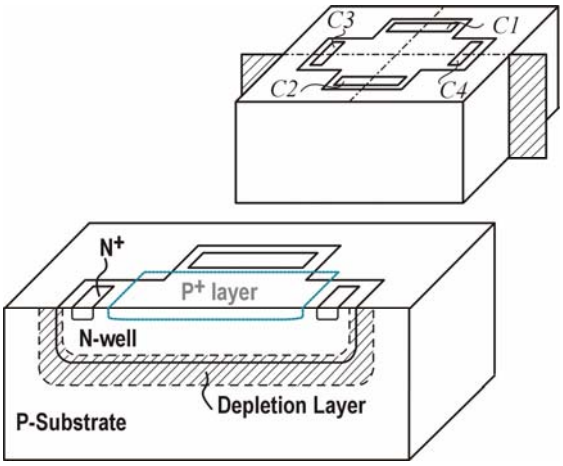


Fig.1. Cross-shaped Hall sensor in AMS 0.8μm HV-CMOS technology: general view and view with the middle cross/section [5].

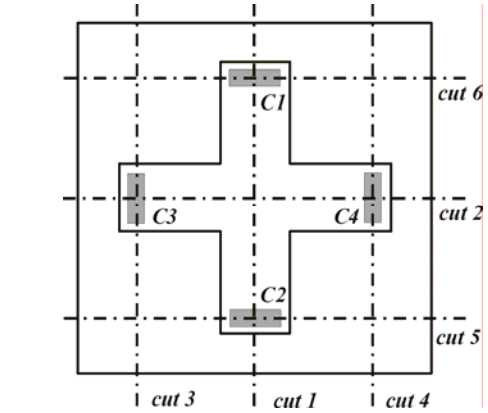
2. 3D SIMULATION

Cross-shaped Hall sensor is a four-contact, 90° rotation symmetrical device, sensitive to magnetic filed perpendicular to a device surface. It has four contacts: two opposite for biasing and the other two for Hall voltage detection and measuring. Its active region is weekly doped n-well region isolated from the p-type substrate by the reverse-biased well/substrate p-n junction, while for n+ contact regions source and drain formation processing steps are used. When biased, structure of junction-isolated Hall sensor forms isolating depletion layer around the well/substrate p-n junction, which thickness depends on local electrical potential along the current flow axes. The modulation of the device thickness due to junction field effect is a source of non-linearity, and it depends on device structure and biasing conditions. Besides mentioned, resistance of the active part of cross-shaped Hall sensor will be non-linear as a function of a biasing current, which is a result of non-uniform (*Gaussian*) profile of n-well region.

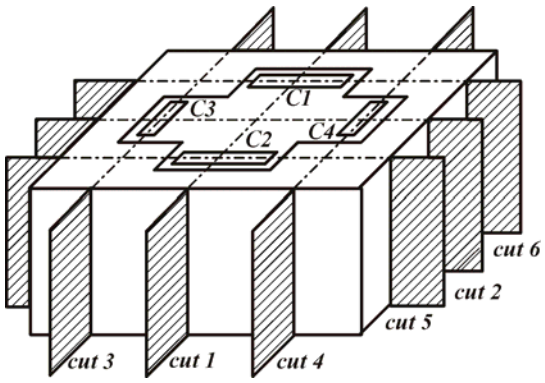
a) Process simulation

The complete fabrication process flow of cross-shaped Hall sensor was simulated using parameters of AMS 0.8μm CMOS technology [8]. Since preconditions for achieving high sensitivity are low-doped active area profiles, it is easy to understand why this exact technology was the first choice. In our particular case, we selected n-well area thickness of 5μm. Fig. 2 illustrates position of 2D layout cuts (2.a), as well as 3D incorporation regions (2.b) formatted according to the position of cuts. Process simulator DIOS [7], as a part of the ISE TCAD software package, was used, and the obtained 2D doping profiles for cut 1-2 and cut 3-6 are shown on Fig. 3.a and b, respectively. Simulation tool DIP was designed to build consistent 3D doping profile from a number of two-

dimensional profiles (cuts). It requires set of input files necessary for constructing 3D structure: set of data files containing 2D grid and doping distribution (process simulator DIOS), 3D geometry file containing layer structure (boundary generator PROSIT), DIP input file which governs interpolation process (layer editor PROLYT) and mashing criterion command file.



(a)



(a)

Fig.2. Layout (a) and structure cutting illustration (b) of Hall sensor with contacts placements (C1 and C2 sensitive, C3 and C4 biasing contacts) and cutting planes selected for 2D simulation.

Basic property of applied incorporation method is that it computes the value at 3D point by combining values from the sides of the region according to the certain rule called incorporation rule. Since a 2D profile is attached to each side of incorporation region, the main task of DIP is to provide consistency of doping profile within the region with respect to the boundary conditions of side points. For that purpose user is supposed to define interpolation criteria for each region. In our case, for the creation of cross-shaped Hall sensor consistent 3D doping profile six 2D doping profiles in the cuts denoted on Fig. 3 are used. Final 3D geometry of the whole device, with illustration of adaptive discretization mesh obtained by DIP and MESH software tools is shown on Fig. 3.c.

b) Device simulation

Simulations of electrical characteristic were performed by program DESIS, multidimensional, electothetmal, mixed mode device and circuit simulator. It incorporates advanced physical models and robust numerical methods for the simulation of semiconductor devices and has implemented necessary models for galvanomagnetic effects simulation.

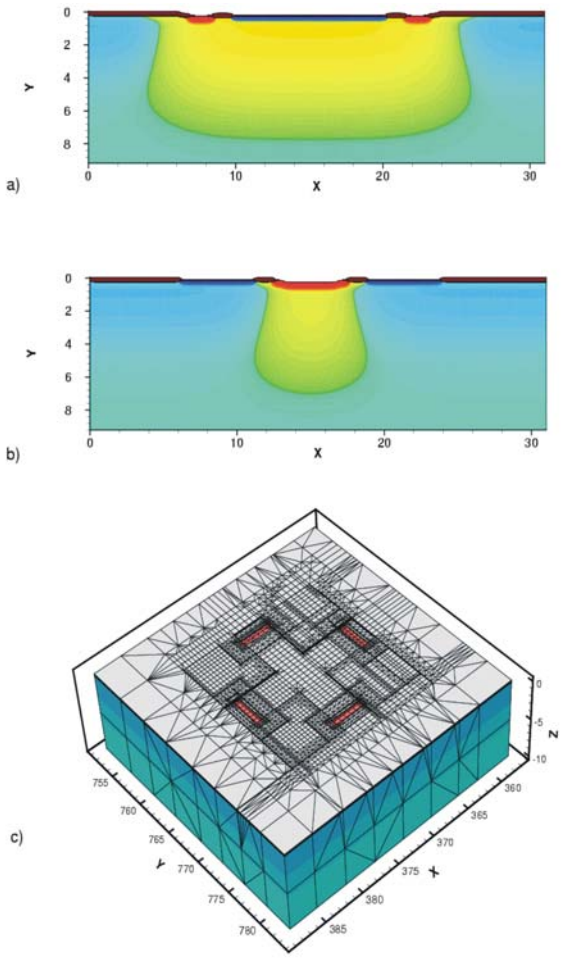


Fig. 3. Process simulation results: a) 2D doping profiles in the middle planes (cut 1-2), b) 2D doping profiles in side planes (cut 3-6), c) discretization grid the whole 3D simulation domain obtained by DIP and MESH software tools.

Device simulations were conducted using the drift-diffusion model. Modeling of electron and hole current densities in presence of magnetic field is based on augmentation of magnetic field dependent terms accounting for the Lawrence force on the motion of the carriers:

$$\vec{J}_n = -\sigma_n \nabla \phi_n - \sigma_n \frac{1}{1+(\mu_\alpha^* B)^2}[\mu_n^* \vec{B} \times \nabla \phi_n + \mu_n^* \vec{B} \times (\mu_n^* \vec{B} \times \nabla \phi_n)] \quad (1)$$

Here, σ_n denotes the electrical conductivity, μ_n doping dependent Hall mobility, ϕ_n quasi-Fermi potential and B magnetic induction. In case of $B \neq 0$, σ_n becomes tensor of rank 2 with two principal components.

Mobility was considered via doping dependence formula while recombination processes were taken to

account via Shockley-Read-Hall and Auger model. Sensing contacts were connected to two identical voltmeters with input resistance of 10MΩ. For sensor biasing voltage generator was applied between contacts C3 and C4 while sensing contacts C1 and C2 were connected to two identical voltmeters with input resistance of 10MΩ. 3D potential distribution for V_{in}=2.54V and B=0.21mT are shown on Fig. 4.

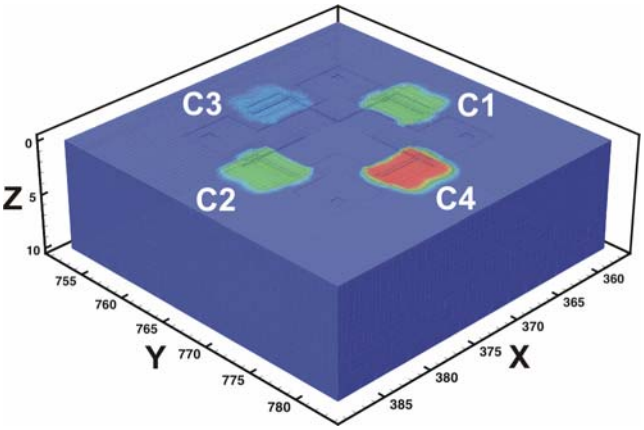


Fig.4. 3D potential distribution for $B = 0.21mT$ *and* $V_{in} = 2.54V$ *.*

2D electron current density in *cut1* and *cut2* cross for the same biasing conditions are shown on figure 5. The influence of p^+ layer is obvious – current is pushed down. In this way surface effects are minimized and sensitivity characteristics are improved due to decreased losses on the Si/SiO2 interface. Current distribution in XY plane for Z=1μm is shown on Fig. 6. Streamlines are non-symmetrically distributed which is direct consequence of magnetic field influence on quazi-free carrier transport.

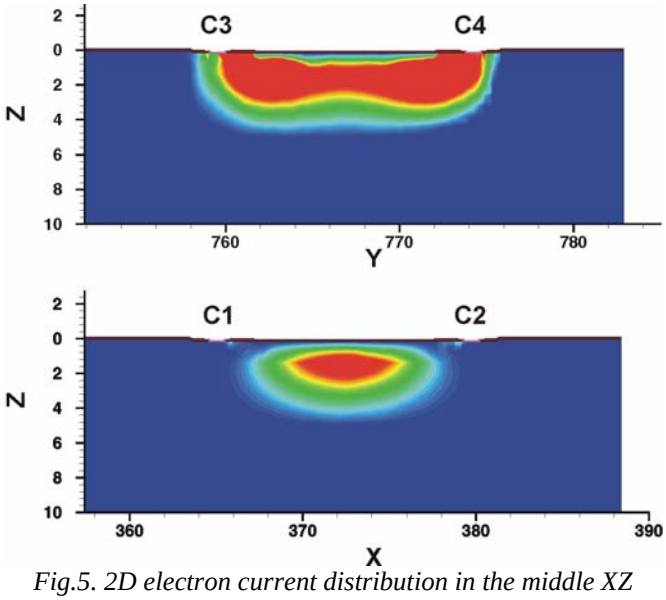


Fig.5. 2D electron current distribution in the middle XZ plane - cut2 (up) and middle YZ plane - cut1 (down).

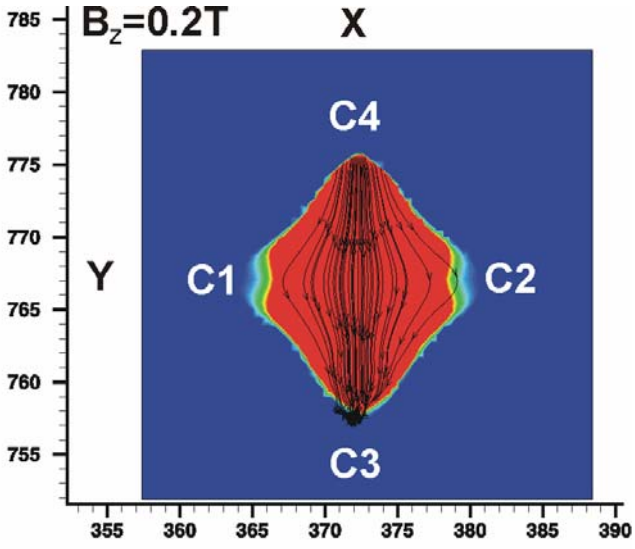


Fig.6. Electron current distribution in XY plane.

3. EQUIVALENT CIRCUIT

Development of the equivalent circuit model of cross-shaped Hall sensor is based on strong correlation with most important physical effects in the device and material as well as technology parameters. For proposed symmetrical circuit model of a cross-shaped Hall sensor (Fig.7) only conventional circuit components were used.

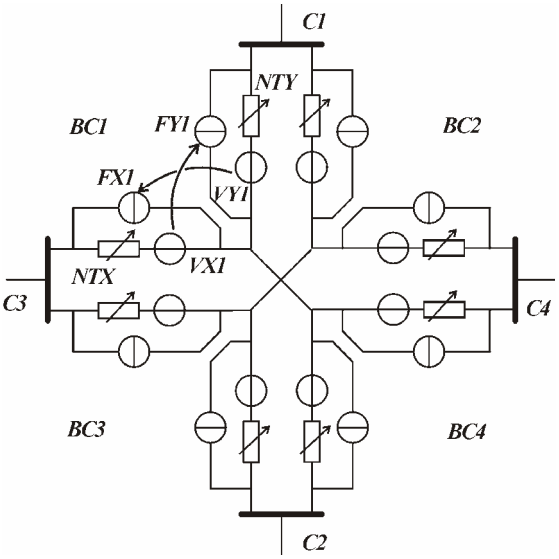


Fig.7. Equivalent circuit model with voltage control non-linear resistors R_{NT} *of cross-shaped Hall sensor.*

Presence of biasing voltage gives rise to the position dependent depletion region width of the n-well/substrate pn junction. This means that active region resistivity exhibits modulation as a function of device geometry and applied voltage, which is one of the most important, causes of non-linear sensitivity characteristics.

Position dependent resistance of an active part of the CMOS integrated Hall sensor was modeled by using non-linear resistors R_{NT} (NTX and NTY on Fig.7) with voltage controlled resistivity. Since the value of R_{NT} resistivity is the

function of potential difference on its ends, ideal voltmeter is placed in parallel with each non-linear resistor. The polynomial nature of this functionality is modeled by:

$$R_{NT} = a + b \cdot \exp\left(\frac{V_{NT}}{c}\right) \quad (2)$$

Where V_{NT} denotes voltage drop between resistors ends. Parameters a, b and c figuring in the equation (2) were acquired by current-voltage characteristics fitting. For that purpose devise simulation results (DESSIS) were used. For this particular sensor structure values are: $a = 680.62\Omega$, $b = 2113.8\Omega$ and $c = 3.55V$. Elements F_{XY1} and F_{YX1} (Fig.7) represent current sources controlled by currents "measured" with corresponding ideal ampermeters V_{XY1} and V_{YX1}. (Correspondence is arrow marked on Fig.7).

X and Y current components must be multiplied with "gain" factor according to the relations:

$$K_{xy} = \mu_n B \frac{\Delta x}{\Delta y} \quad (3)$$

$$K_{yx} = \mu_n B \frac{\Delta y}{\Delta x} \quad (4)$$

Where Δx/Δy denotes the length to width ratio for each resistor [9].

Comparison of simulated (3D ISE TCAD simulation and SPICE simulation) and experimental results for cross-shaped Hall sensor is shown on figure 8., which represents Hall voltage V_H to bias voltage dependency for three different values of magnetic field intensity. In order to make this comparison possible experimental results had to be modified – just a useful portion of the signal is extracted, simply by subtracting offset voltage (B=0) from the full output value.

Figure 9. shows current-related sensitivity as a function of supply voltage for $B = 127mT$. Simulation results exhibit very good agreement with experimental measurements due to implementing most important effects that govern non-linearity of cross-shaped Hall sensors in the equivalent circuit model.

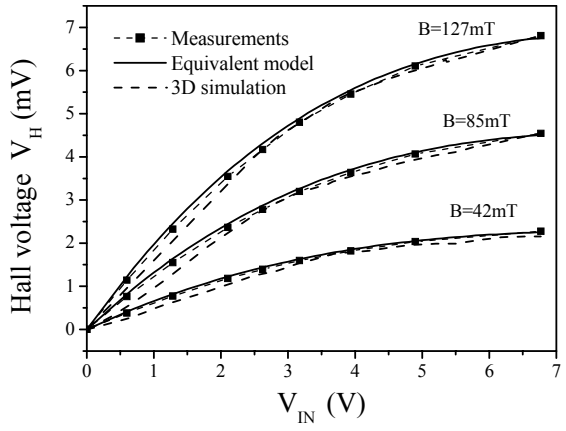


Fig.8. Hall voltage vs. supply voltage for different values of magnetic field.

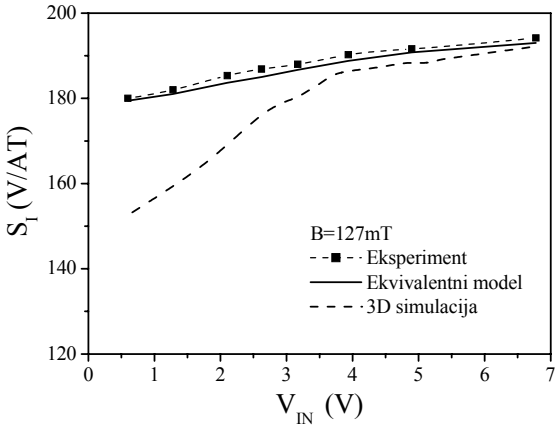


Fig.9. Current related sensitivity vs supply voltage.

4. CONCLUSION

The complete technology process flow and electrical characteristics of cross-shaped Hall sensor in AMS 0.8μm CMOS technology have been accurately simulated in 2D and 3D using ISE TCAD system. Interpolation methods were used in order to obtain consistent 3D doping profile, which was generated by exchanging data between several 2D doping profiles. Equivalent circuit model of cross-shaped Hall sensor with voltage control non-linear resistors was suggested. The model includes most important physical effect that causes non-linearity of output characteristic. Finally, results acquired by 3D electrical characteristic simulations using ISE tool DESSIS and equivalent-circuit analyses using program SPICE were compared with experimental measurements.

5. REFERENCES

[1] C.L. Chin, C.R. Westgate (editors), The Hall effect and its applications, Plenum Press, New York, 1979, p. 535.

[2] M. Epstein, et al. "Principles and applications of Hall-effect devices," *Proceedings of the National Electronics Conference*, vol. 15, p. 241, 1959, p. 241.

[3] H.P. Baltes, R.S.Popovic, "Integrated semiconductor magnetic field sensors," *Proc. IEEE*, vol. 74, 1986 p. 1107.

[4] H. Blanchard, F. De Montmollin, J. Hubin, R.S. Popović, "Highly sensitive Hall sensor in CMOS technology," *Sensors and Actuators 82*, pp. 144-148, 2000.

[5] R.S. Popović, Hall Effect Devices, Second edition, IOP Publishing Ltd, Bristol and Philadelphia, 2004.

[6] E. Jovanović, T. Pešić, D. Pantić, "3D simulation of cross-shaped Hall sensors and its equivalent circuit", *Proc. of 24th International Conference on Micoelectronic – MIEL*, pp. 235-238, 2004.

[7] ISE TCAD – Users Manual, Release 7.0, Integrated System Engineering AG, Zurich, Switzerland.

[8] 0.8μm HV-CMOS Process Parameters, Austria Mikro Systeme International AG, Document #9933013, 1999.

[9] R.S. Popović, "Numerical analysis of MOS magnetic field sensors" *Solid-State Electronics*, vol. 28, no. 7, pp. 711-716, 1985.

PERFOMANCE OF OPTICAL TELECOMMUNICATION SYSTEM IN THE PRESENCE OF CHIRPED AND TIME SHIFTED INTERFERENCE

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Abstract: *The positive influence of nonlinear effects in optical fiber that works under anomalous dispersive regime are presented in this paper. Interferences are often present in optical systems and their influence can be great and it is reason for studding interference chirp influence on performance of IM-DD optical systems when interference appears at the beginning of optical fiber. All these influences are considered by pulse shape at the end of nonlinear-dispersive optical fiber for SIR (signal-to-interference ratio) =10dB and by bit error probability for SIR=10dB and 20 dB. The pulse shape along the optical fiber is determined by solving Schrödinger equation by symmetrical "split-step" Fourier method.*

Keywords: *Gaussian signal, Chirped interference, Nonlinear Schrödinger equation, Bit error probability.*

1. INTRODUCTION

A chromatic dispersion results from refractive index and mode propagation constant frequency dependence and it leads to pulse deformity when pulse propagates along an optical fiber, i.e. pulse broadening [1]. Dispersion coefficient, parameter β_2, shows the magnitude of the dispersion and defines dispersive regime of an optical fiber. When $\beta_2>0$, an optical fiber works under the normal dispersive regime. However, when $\beta_2<0$, we say that an optical fiber is exposed to anomalous dispersion [1]. It is optimal that optical fiber works under anomalous dispersive regime because then influence of dispersion can be reduced and soliton propagation can be realized under specific conditions in such optical fiber. Kerr's nonlinearity, as kind of nonlinear effects, decrease influence of dispersion. They are consequence of refractive index depends on the intensity of pulse that propagates along optical fiber [1]. If signal propagates along optical telecommunication system at high data rate and at long distance, the influence of nonlinear effects should be taken into consideration because signal intensity is big enough not to allow for the disregard of the intensity dependence of refractive index.

Inband interference is kind of disturbance that appears in optical telecommunication system and it is the consequence of crosstalking, reflection, etc... [2,3,4]. At the detection process, inband interference is more problematic than outband interference because it cannot be isolated by optical filtering. It is the reason why such a kind of interference influence on performance IM-DD (Intensity Modulation and Direct Detection) optical telecommunication systems is discussed in this paper.

2. PULSE PROPAGATION ALONG NONLINEAR OPTICAL FIBER IN THE PRESENCE OF CHIRPED INTERFERENCE

Cognition of pulse shape at the receiver is needed to determine IM-DD optical telecommunication system performance. A signal that has got Gaussian envelope is very often found as a useful signal in optical telecommunication systems and it can be written as [4,5]:

$$U(0,\tau) = a\exp(-\tau^2/2) \tag{1}$$

where the value of parameter a depends on the transmitted information (1 or 0). A useful signal at the beginning of optical fiber is:

$$s(0,\tau) = U(0,\tau)\cos\omega_r\tau \tag{2}$$

$\omega_r = \omega T_0$ is a normalized frequency, T_0 is half-width, i.e. the time when the signal power declines to $1/e$ of its top value.

Inband interference is of the same frequency as a useful signal and it is time and phase shifted in relation to a useful signal. Interference at the place of its appearance is:

$$\begin{aligned} s_i(z_i,\tau) &= U_i(z_i,\tau)\cos(\omega_r\tau+\varphi), \\ U_i(z_i,\tau) &= a_i\exp(-(1+iC_i)(\tau-b)^2/2) \end{aligned} \tag{3}$$

where b and φ are the time and phase shift, respectively. z_i is the place along an optical fiber where interference appears, C_i is chirp of interference and the value of parameter a_i depends on the magnitude of the interference. Interference can be chirped although useful signal is not linearly chirped and it depends on the kind of interference.

Pulse propagation along a nonlinear-dispersive optical fiber can be described by the equation that is well known in literature as nonlinear Schrödinger equation:

$$\frac{\partial U}{\partial z} = -i\frac{\operatorname{sgn}(\beta_2)}{2L_D}\frac{\partial^2 U}{\partial\tau^2} + \frac{i}{L_{NL}}|U|^2 U \tag{4}$$

Optical losses are neglected in (4), i.e. α=0. L_D is dispersive length and L_{NL} is nonlinear length.

The new parameter is introduced to determine interaction between nonlinear and dispersive effects in optical fiber:

$$N^2 = L_D/L_{NL} = \gamma P_0 T_0^2/|\beta_2| \tag{5}$$

When $N^2<<1$, dispersive effects dominate an optical fiber. In case of $N^2\approx1$, dispersive and nonlinear effects establish a mutual balance [1].

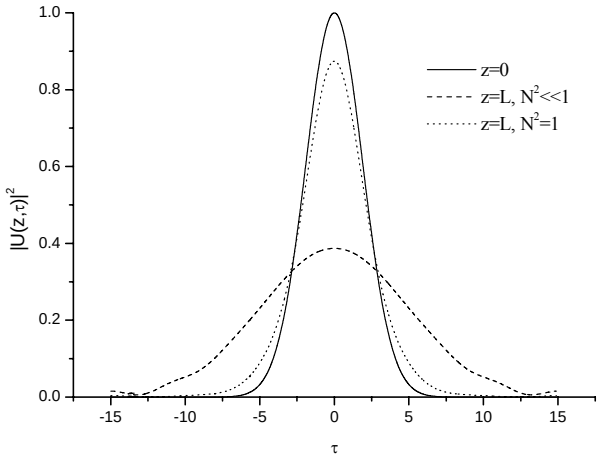
There are many methods for solving of Schrödinger equation, numerical and analytical. Numerical "split-step" Fourier method has great accuracy and it is very fast. Because of that it is used in this paper [1]. Pulse shape along the optical fiber is got by solving equation (4) with this method. In the presence of interference, initial conditions of Schrödinger equation evaluation are modified, at the place of interference appearance. The envelope and phase of the resulting signal on the place where interference appears are [4,5,6]:

$$U_r(z_i,\tau) = \sqrt{U^2(z_i,\tau)+2U(z_i,\tau)U_i(z_i,\tau)\cos\varphi+U_i^2(z_i,\tau)} \tag{6}$$

$$\psi(z_i,\tau) = arctg\frac{U_i(z_i,\tau)\sin\varphi}{U(z_i,\tau)+U_i(z_i,\tau)\cos\varphi} \tag{7}$$

Figure 1 shows Gaussian pulse shape at the end of optical fiber in the presence of interference at the beginning

of fiber for the worst case, i.e. b=0 and $\varphi=\pi$. This result has already represented in paper [7] but it is made in this paper for other value of parameters, i.e. for T_0=4 ps, β_2=-23 ps^2/km and $L=6L_D$. Figure 1(*a*) confirms above mention fact that nonlinear effects can decrease influence of dispersion in anomalous dispersive optical fiber. Comparison of figures 1(*a*), 1(*b*) and 1(*c*) shows that nonlinear effects do not have such great positive influence in the presence interference at the beginning of optical fiber. It is needed to determine bit error probability of IM-DD optical system to see real influence of chirped and time shifted interference on this system performance, whereas time and phase shifts are random values.



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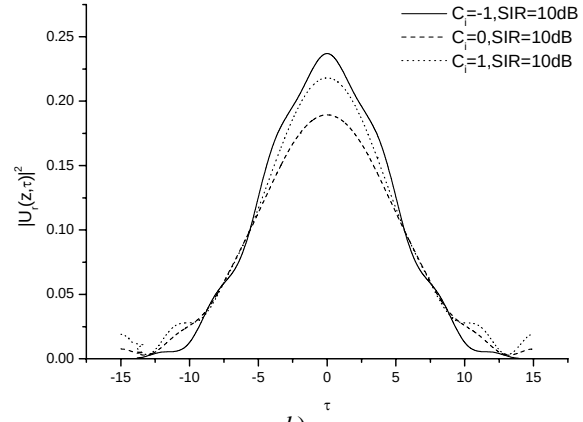

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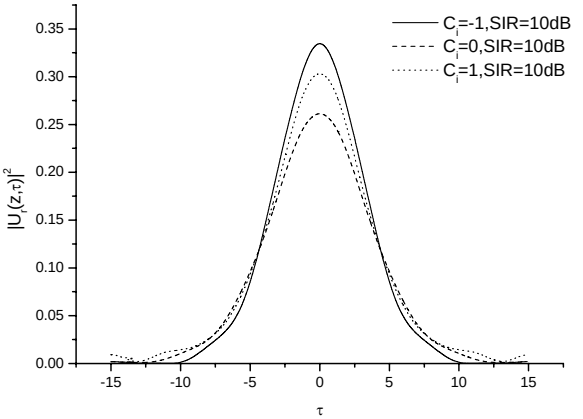


c)

Fig. 1. (*a*) *Gaussian pulse shape at the end of optical fiber without the presence of interference*
(*b*) *Gaussian pulse shape at the end of linear optical fiber in the presence of chirped interference* (z_i=0)
(*c*) *Gaussian pulse shape at the end of nonlinear optical fiber in the presence of chirped interference* (z_i=0)

3. BIT ERROR PROBABILITY OF IM-DD OPTICAL SYSTEMS IN THE PRESENCE OF CHIRPED AND TIME SHIFTED INTERFERENCE

Optical telecommunication systems with intensity modulation and direct detection, so called IM-DD systems, are prevalent because of their simplicity and because of fact that they are pay off economically. Beside signal, there are different kinds of noises (laser intensity noise, thermal noise, quantum noise…) at the receiver of these systems. According with "central limit theorem", addition of great number of independent random variables has Gaussian probability density, regardless individual density of addends. Based on this theorem, density of total noise at the receiver is Gaussian. Bearing this rule and rule for determining probability density function of statistical independent processes (signal, interference and noises) in mind, we get [8]:

$$p_1(y/\varphi)=\frac{1}{\sqrt{2\pi}\sigma_1}\exp\left(-\frac{(y-\bar{y}_1)^2}{2\sigma_1^2}\right) \tag{8}$$

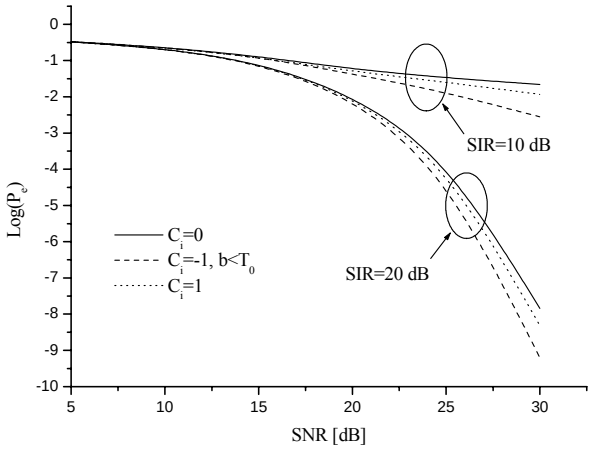
$$p_0(y/\varphi)=\frac{1}{\sqrt{2\pi}\sigma_0}\exp\left(-\frac{(y-\bar{y}_0)^2}{2\sigma_0^2}\right) \tag{9}$$

If it is assumed that sending probability of 1 equals sending probability of 0, then conditional bit error probability is:

$$P_{e/\varphi}=\frac{1}{2}\left[\int_{V_p}^{+\infty}p_0(y/\varphi)dy+\int_{-\infty}^{V_p}p_1(y/\varphi)dy\right] \tag{10}$$

where threshold of decision is defined as:

$$V_p=\frac{\bar{y}_1\sigma_0+\bar{y}_0\sigma_1}{\sigma_0+\sigma_1} \tag{11}$$



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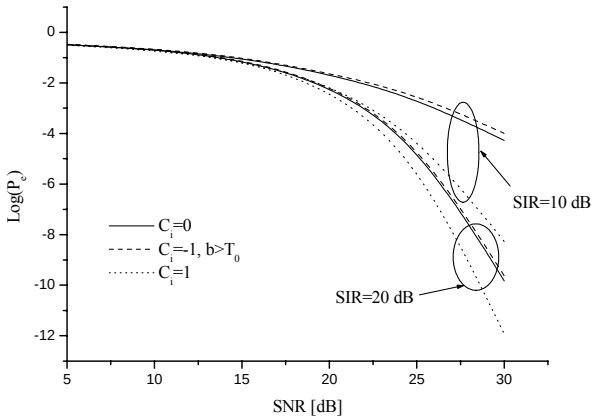
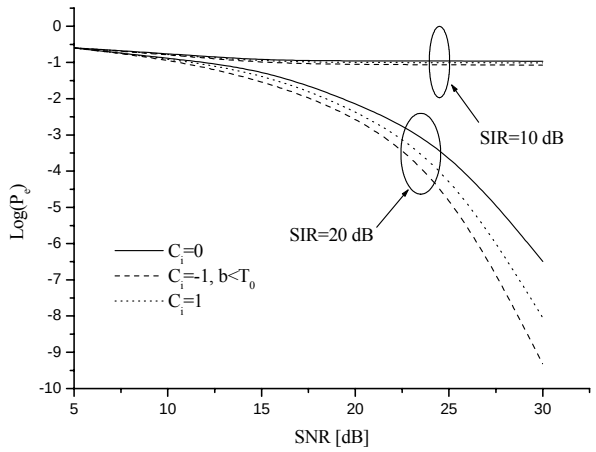


b)

Fig. 2. *Bit error probability as function of SNR for case of dispersive effects ascendancy* (N^2<<1).
(*a*) $b<T_0$; (*б*) $b>T_0$



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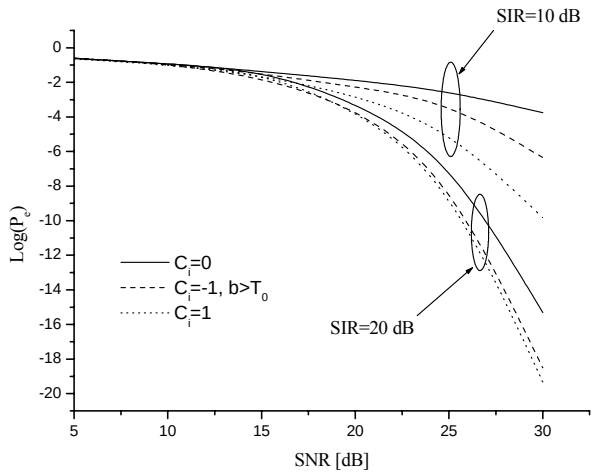

.*b*)

Fig. 3. *Bit error probability as function of SNR for case of balance between nonlinear and dispersive effects* ($N^2\approx1$).
(*a*) $b<T_0$; (*б*) $b>T_0$

Unconditional bit error probability is obtained by averaging of relation (10), where $p(\varphi)$ is uniform probability density function of phase:

$$P_e = \int_{-\pi}^{\pi} P_{e/\varphi}\, p(\varphi) d\varphi \qquad (12)$$

Bit error probability of IM-DD optical systems as function of SNR (signal-to-noise ratio) is shown in figure 2 (ascendancy of dispersive effects) and in figure 3 (balance between nonlinear and dispersive effects). It is known from literature [1] that if chirped useful signal propagates along optical fiber larger pulse deformation happens for case $\beta_2 C>0$ than for $\beta_2 C<0$. The least deformation happens for unchirped pulse propagation. However, there is deviation in the presence interference, because resulting signal at the beginning of optical fiber in the presence of unchirped interference (z_i=0) has the most sharpness edge and it affects width of spectrum, i.e. pulse broadening. In that case resulting signal has the largest deformation. Illustrated pulse shapes (figure 1) at the end of optical fiber for SIR (Signal-to-Interference ratio) =10 dB are agreeable with graphs of bit error probability. Regardless working regime of optical fiber, for $b<T_0$ the most and least pulse deformation happen in the presence unchirped interference and interference with negative chirp, respectively. We can conclude from comparison of figures 2 (*a*) and 3 (*a*) that positive influence of nonlinear effects on Gaussian pulse propagation are negligible in the presence of interference. Nevertheless, for time shift of interference that is larger than pulse width, positive influence of Kerr's nonlinearity is noticeable (fig. 2 (*b*) and fig. 3 (*b*)). For this case, the great deformation happens for negative than for positive chirp of interference.

4. CONCLUSION

Dispersion and interference are one of the most important factors that preclude "ideal" transmission through the optical telecommunication system. It was reason for studding of their influence on optical system performance in this paper. Pulse shapes shown in figure 1 affirmed that nonlinear effects can reduce influence of dispersion. Figures 2 and 3 showed that this positive influence is reduced with wane of interference time shift and wane of SIR. Results of paper reveal that the largest pulse deformations happen in the presence of unchirped interference at the beginning of optical fiber. Influence of chirped interference depend on magnitude of interference time shift. All these foregoing results are obtained by solving nonlinear Schrödinger equation using "split-step" Fourier method.

5. REFRENCES

[1] Govind. P. Agrawal, *Nonlinear Fiber Optics*, Academic Press INC., Boston-San Diego-New York-London-Tokyo-Toronto, 1995.

[2] P. J. Legg, M. Tur, I. Andonović, ″Solution Paths to Limit Interferometric Noise Induced Performance Degradation in ASK/Direct Detection Lightwave Networks″, Journal of Lightwave Technology, Vol. 14, No. 9, p. 1943-1954, September, 1996.

[3] J. Wangg, A. Yongacoglu, ″Performance of Trellis Coded-8PSK with Cochannel Interference″, Transaction on Communications, Vol. 42, No. 1, p. 6-10, January, 1994.

[4] Stefanović M., *Perfomance of Digital Telecommunication Systems*, Faculty of Electronic Engineering, University of Niš, 2000.
[5] Lukatela G., *Statistical Telecomunication Theory and Information Theory*, Građevinska knjiga, Belgrade, 1981.
[6] Stefanović M., Drača D., Panajotović A., Spalević P., "The influence of crosstalk signal interference to signal propagation along nonlinear and dispersive fiber", *Journal of Optical Communications*, German, 2002 (accept for printing, JOC #844).
[7] Drača D., Panajotović A., Jovanović A., Martinović D., ″Influence of Interference Chirp on Gaussian Signal Propagation along Nonlinear Dispersive Optical Fiber″, TELFOR 2003, Belgrad, 2003.
[8] Marinčić A.., *Optical telecommunication*, University of Belgrade, Belgrade, 1997.
[9] Krejić N., Herceg Đ., *Matematika and Mathematica*, Computers in Academic Practice, Novi Sad, 1993.

SINUSOIDAL VOLTAGE-SOURCE INVERTER WITH DUAL CURRENT MODE CONTROL

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ABSTRACT

In this study are presented examination of single-phase sinusoidal voltage-source inverter (1kVA). Output voltage has been obtained and his waveform, amplitude and frequency have been maintained in requested limits by means ***dual current mode*** *control, which is based on control of output filter current (current mode control). The main distinctions of dual current mode are: constant switching frequency, simple implementation and excellent performances of equipment*.

1. INTRODUCTION

Hundred millions of computers, communication, medicines and the other computed based equipments for witch a high reliability is mandatory, request supplying with clear sinusoidal voltage with stable amplitude and frequency in all working conditions.

Even in *USA* where the quality of mains voltage is good, one computer, during the year, meet with approximately 289 disturbances, from blackout to impulse disturbances (more then one per a working day). Problems in power mains cause of data losing, damage or destroying of equipment (losing of money). Solving of problems is using *UPS*. Main part of *UPS* is inverter. [1]

Fast dynamic response, excellent static accuracy of output voltage and reduced level of distortion in the presence of nonlinear loads (diode bridge rectifier with capacitive filter) are the fundamental characteristics of this kind of equipments. It is desirable to have a control system that is very fast and has a high gain. In the case of the *DC-DC* converters, this can be achieved by using current mode control with constant frequency. In this study was represent modification of this kind of control, suitable for inverters, called ***dual current mode*** control.

Nominal desirable characteristics of inverter[2]:

Power	***1 – 5 kVA***
Power factor (cosφ)	***0.8 ind***
Input voltage	***110 / 220 V ; -10 , +20 %***
Output voltage	***220 (110) V***
- static accuracy	***± 1 %***
- dynamic accuracy	***4 – 8 %***
- frequency	***50 Hz ; ± 0, 1 %***
- waveform	***sinusoidal***
- THD	***< 3% lin. , < 5% nonlin.***
-harmonics	***2% of fundamental***
Switching frequency	***> 10 kHz***
Galvanic isolation input/output	***yes***
Current limit	***adjustable***
Crest factor of load	***2.5 - 3***
Efficiency	***> 90 %***

2. REALIZATION OF INVERTER

In realization of inverter special attention is dedicated on:

- Integration of input filter and power stage because of stray inductance elimination to where the snubber circuits is unnecessary.
- Optimal *MOSFET/IGBT* driving with short circuit protection and soft turn-off.
- Using of current mode control with constant frequency for fast dynamic response, excellent static accuracy of output voltage and reduced level of distortion in the presence of nonlinear loads.

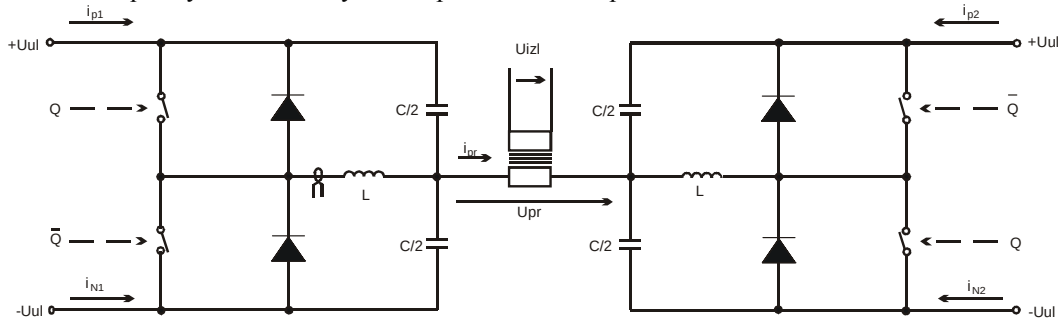

Fig. 1. Full-bridge inverter with output filter and transformer

Circuit, showed on Fig. 1., is suitable for practical realization because it make possible integration of inverter power stage (transistors H-bridge), input filter and output filter capacitors (C/2) on the printed board with simplification of complete inverter construction. This integration and output filter inductors (L), wounded on ferrite core, with small dimensions and weight, make possible realization of compact inverter.

2.1 CONTROL ELECTRONICS OF INVERTER

Control electronics of inverter had to be: simple, reliable, inexpensive, easy for assembling and servicing, and is realized as a electronic module with four functional blocks with tasks as follow:

- Generation supply voltages
- Adapting and measuring of input signals
- Signalization
- Output voltage forming and control

2.1.1 FORMING AND CONTROL OF OUTPUT VOLTAGE

Output sinusoidal voltage of inverter is obtained after filtration of bridge voltage that is in rectangular pulse waveform. Harmonics contents of this voltage should be good as much possible (as much as possible fundamental component and less harmonics), for simplification of filtering and satisfied contradictions demands for reduced level *THD* and fast dynamic response of output voltage.
Block for forming and control of output voltage (and current) have to provide such control pulses for power switches in power stage witch (after filtration), on output of inverter are forming sinusoidal voltage which amplitude and frequency stay in requested limits in all anticipated operational conditions (for all changes of input voltage and load). This function and very efficient current limit are realized by *dual current mode control* and use of standard, cheep and easy procurable components.

2.1.2 CURRENT MODE CONTROL IN *DC-DC* CONVERTERS [3]

Current mode control in *DC-DC* converters has many advantages related to usual *PWM* as follow: automatic feed-forward, automatic correction of asymmetric, natural current limit, simply compensation, excellent response on load changes and capability for parallel operation.
There are two way of current mode control in *DC-DC* converters:

1. Power switch is closed by clock and opens when current reaches error voltage (clocked turn-on, stable for $D<0.5$),
2. Power switch is opened by clock and closes when current fall down error voltage (clocked turn-off, stable for $D>0.5$).

Inverter have to use control which provide stable operation over entire duty-cycle range (0 to 1). It will be obtained by using current mode control with clocked turn-on operation for $D<0.5$, and with clocked turn-off operation for $D>0.5$.

2.1.3 *DUAL CURRENT MODE* CONTROL [4]

A modulator, capable of automatically changing between clocked turn-on and clocked turn-off when $D=0.5$, with stable operation over the entire duty-cycle range and suitable for four quadrant (inverter) operation with saved all advantages of current mode control with constant frequency, exists and its name is *dual current mode* modulator. The operation principle of that modulator is presented on Fig. 2. Constant voltage V_A is added and subtracted to the error voltage V_ε. The sampled current signal $K_iR_SI_L$, which is proportional to inductor filter current, is compared with both $V_\varepsilon+V_A$ and $V_\varepsilon-V_A$ in the comparators *K1* и *K2*. *RS FF*, who drive switch S, is set (*log 1*) either when a clock pulse *CLKA* occurs, or when $K_iR_SI_L$ reaches $V_\varepsilon-V_A$, and reset (*log 0*) when either $K_iR_SI_L$ reaches $V_\varepsilon+V_A$, or when a clock pulse *CLKB* occurs. The two clocks signals have constant frequency and one has a delay with respect to the other of a half period.

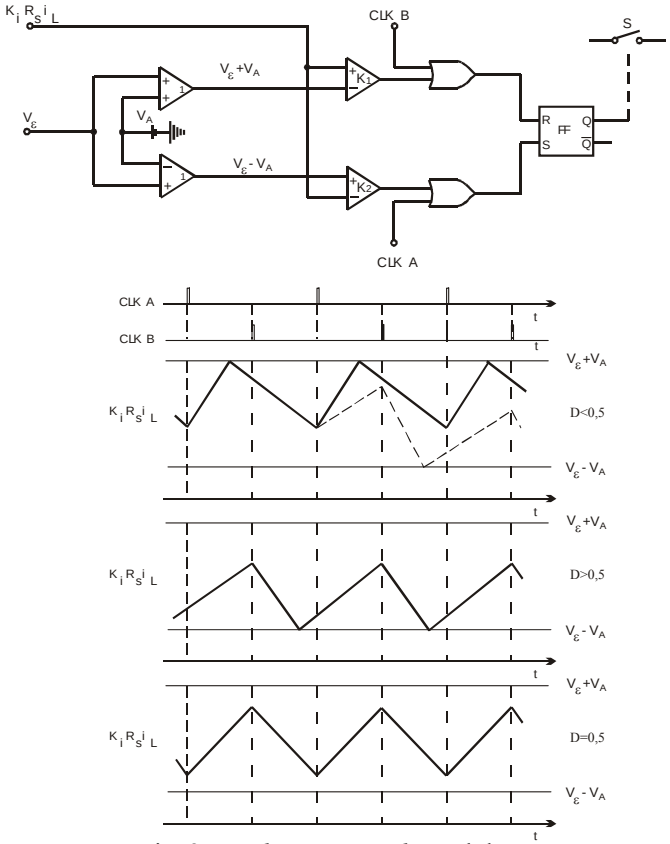

Fig. 2. *Dual current mode* modulator

The circuit on Fig. 2. can have the three modes of operation, shown on the figure, depending on whether $D<0.5$, $D>0.5$ or $D=0.5$.

- ***D<0.5*** **:** Power switch S is closed by clock pulses *CLKA*, and opens when $K_iR_SI_L$ reaches $V_\varepsilon+V_A$ (*CLKB* has no effect on the performance since, when its pulses occurs, *FF* is already reset). Since this is a clocked turn-on mode and $D<0.5$, converter is (for the suitable value of the loop gain).
- ***D>0.5*** **:** In this case, the power switch closes when $K_iR_SI_L$ reaches $V_\varepsilon-V_A$, and is open by clock pulses *CLKB*. (*CLKA* has no effect on the performance since, when its pulses occurs, *FF* is already set). This is clocked turn-off mode with $D>0.5$ and converter is stable.
- ***D=0.5*** **:** The switch is operated by the two clocks (closed by *CLKA* and opened by *CLKB*).

When slopes of waveform $K_iR_SI_L$ change (as a consequence of a change of V_{out}/V_{in}), the modulator can change automatically from one mode of operation to the other (dashed line superimposed to the waveform on Fig. 2.).
Condition for stable operation of bridge converter, over the entire range of D is:

$$V_A > K_i \cdot R_s \cdot \frac{U_{ul} \cdot T_r}{4 \cdot L} \qquad (1)$$

Voltage $2V_A$ must be larger then maximum (*peak-to peak*) ripple of $K_iR_SI_L$. If the $2V_A$ is not large enough the operation

of modulator is not proper. The modulator operates almost as a hysteric current mode circuit, switching on and off when. $K_iR_SI_L$ reaches the two comparison voltages $V_\varepsilon+V_A$ and $V_\varepsilon-V_A$. Some switching due to clocks also occurs, leading to an apparently no periodic operation (average value of current is not affected).

The use of an excessive value for $2V_A$ should be avoided since it introduces a large domain of uncontrolled output current when $D=0.5$ and the system travels between clocked turn-on and clocked turn-off operation.

The voltage V_A in control electronics is stable and adjustable for elimination irregular conditions of modulator operation.

The output current is limited by saturation voltage of error amplifier:

$$I_{omax} \approx \pm V_{\varepsilon sat}/K_iR_S \quad (2)$$

In order to provide an effective limitation of the output current, it is necessary to limit the saturation voltage of the summing amplifiers (Fig. 2.) to values below the saturation voltages of the current amplifier.

The power stage of inverter is realized as H-bridge (Fig. 1.) Pulses for switches driving are obtained from one modulator where Q output of *RS FF* is used for driving switches in one, and $\overline{Q}$ in other diagonal of H-bridge. That kind of driving gives two level modulation voltage on the output of bridge.

Limit of bridge current (output current) and other functions of modulator (clocks generation, *RS FF,* comparators etc.) are realized according description and basic part circuit.

3. EXPERIMENTAL RESULTS [2]

Experimental results of investigation of sinusoidal voltage-source inverter are presented in form oscillograms of characteristics voltages and currents obtained by means *TEK 2230* oscilloscope, *PC* computer and small *GWBASIC* program, and they are looking better in reality that on showed pictures.

Fig. 3. shows output voltage of inverter with nominal resistive load (higher oscillograms) and referent sinusoidal voltage from excellent functional generator *HP3314A* (lower oscillogram). From picture is clear that waveform and contents of harmonics (*THD*) of inverter output voltage are satisfied requested input demands.

Fig. 4. shows that inverter output voltage is stable with step change of input *DC* voltage of 50V (measured absolute error is 0.43V on 110 V).

Influence of step change load (0,100%,0) is showed on Fig. 5. Like in previous case, voltage is stable.

Inverter passing over from voltage to current source on Fig. 6. is showed. All passing over are quit natural and control electronics and power stage of equipment do not have any problem. As current do not came over max. setting value there is no time limit for this situation. In overload situation, voltage and current have trapezoidal waveform. Increasing of overload bring that voltage decrease (to 0), when current stays constant

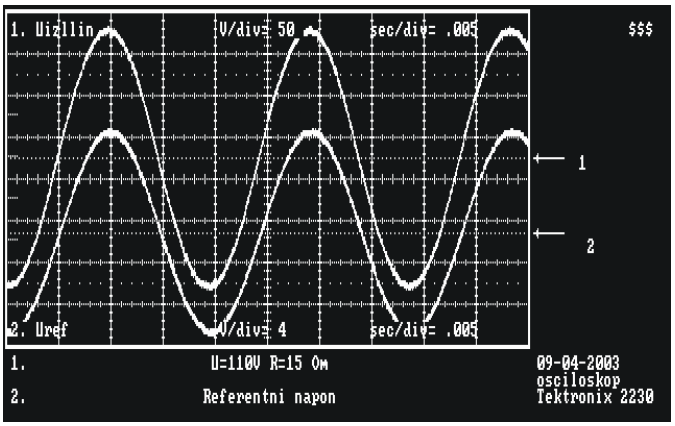

Fig. 3. Resistive load

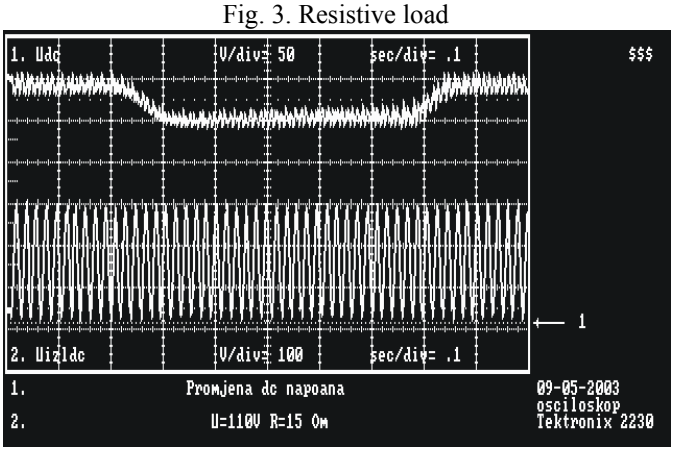

Fig. 4. Influence of input *DC* voltage on output voltage

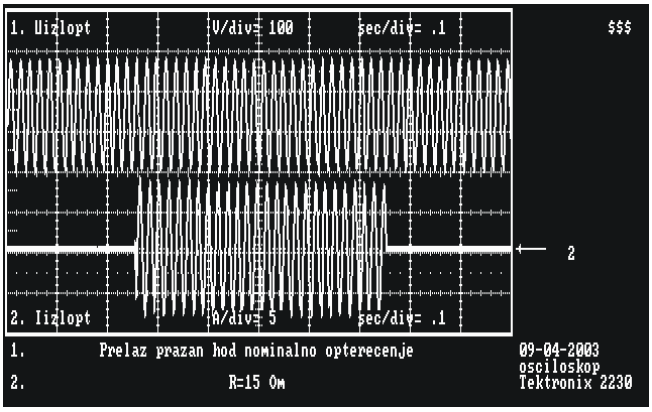

Fig. 5. Influence of load change on output voltage

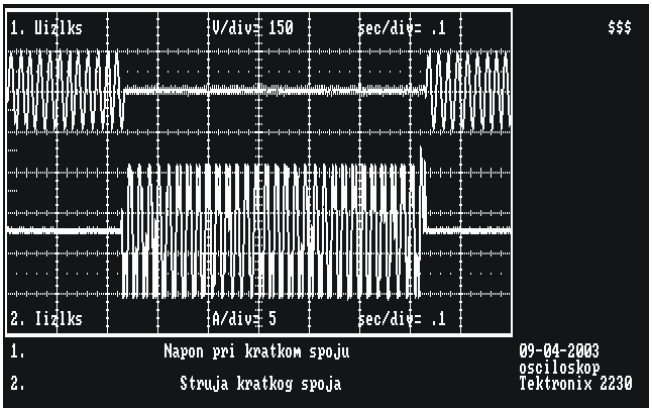

Fig. 6. Output voltage and current in short-circuit condition

4. CONCLUSION

Results of sinusoidal voltage-source inverter development (1kVA), obtained in oscillogram form, show that inverter has a little *THD*, excellent static and dynamic accuracy of output voltage in anticipated changes of input *DC* voltage and load. Very important is capability of permanent work with short circuit on output, with totally natural passing over from voltage to current source. This results are improved that developed equipment are satisfied requested input demands at all, and that using of dual current mode control was justified

REFERENCES

[1.] Best Power : *UPS Product Catalogue*, 1999.
[2.] K-INEL : *Technical documentation*, 1999-2004.
[3.] UNITRODE : *Modelling, Analysis and Compensation of the Current-Mode Converter*, 1997.
[4.] A.Victor Anunciada, Manuel M. Silva : *A New Current Mode Control Process and Applications*, 1991.
[5.] S.Buso, S.Fasolo, L.Malesani, P.Mattavelli : *A Dead-Beat Adaptive Hysteresis Current Control*, 2000.
[6.] S.Buso, S.Fasolo, P.Mattavelli : *Uninterruptible Power supply Multiloop Control Employing Digital Predictive Voltage and Current regulators*, 2001.
[7.] K.Miyashita, H.Hara, S.Shimogata, T.Yokoyama : *Multirate Deadbeat Control for PWM Inverters using FPGA based Hardware Controller*, 2002.
[8.] Timothy L. Skvarenina : *The Power Electronic Handbook*, CRC PRESS, 2002.

COMPACT MAC ARCHITECTURE OF HILBERT TRANSFORMER IN SOLID-STATE ENERGY METER

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Abstract: *Two implementations of two MAC (Multiplier and ACcumulator) architectures of a Hilbert transformer used in solid-state energy meter have been considered in this paper. The general feature of basic MAC architecture is smaller chip area comparing to other architectures. A new compact form of MAC architecture, that improves savings in chip area and efficiency, is suggested in this paper. Both MAC architectures (basic and compact) are described in VHDL, verified by simulations and synthesized using AMI Semiconductor CMOS 0.35μm technology library.*

Keywords: *Hilbert transformer, energy measurement, MAC architecture, FIR filter design*

1. INTRODUCTION

Hilbert transformer is a digital filter used for phase-shifting input signal for 90°. It is usually implemented as a FIR system with asymmetrical impulse response. There are several architectures and optimization criteria used for filter implementation: chip area, speed and power consumption. The main optimization criterion during Hilbert transformer design for solid-state energy meter was small chip area and as low power consumption as possible.

Hilbert transformer within the solid-state energy meter described in [1], should introduce a constant phase shift of 90° in voltage signal at line frequency of 50 Hz. That signal is necessary to calculate reactive power. Sampling frequency of the input and output signals is 4096 Hz. Hilbert transformer incorporated in the current prototype of the solid-state energy meter was implemented as a direct form with CSD (Canonical Signed Digit) representation of coefficients, [2]. In that architecture multipliers are not used and multiplication is implemented by adders, subtracters and shifters. CSD representation enables minimal number of additions and subtractions. The advantages of this architecture are small power consumption, high speed and simple implementation. In this paper is described implementation of Hilbert transformer using MAC architecture that gives smaller chip area comparing to CSD architecture. The disadvantages of MAC architecture are increased power consumption and restriction in speed determined by ratio between sampling frequency and basic clock frequency.

In this paper modification of basic MAC architecture is suggested in order to overcome mentioned disadvantages together with additional reduction in chip area. Therefore, in the rest of the paper such improved MAC architecture will be called *compact* MAC architecture.

In the next section characteristics of Hilbert transformer are given. After that, in the subsequent two sections basic and compact MAC architecture and their hardware implementations are described. Simulation and synthesis results conclude the paper.

2. HILBERT TRANSFORMER FEATURES

The measurement of consumed reactive power is one of tasks of the solid-state energy meter. The simplest way to use the same hardware already implemented for measuring consumed active power, is to repeat calculation using voltage signal phase-shifted for 90°. It is important to provide that near line frequency of 50 Hz amplitudes of input and shifted signal have the same values. Hilbert transformer is used to achieve such signal transformation. Additional challenge in the filter design is relatively high sampling frequency comparing to line frequency that gives very sharp amplitude response in LF band. Implementation of such filter function requires approximating function of high order, i.e. big number of filter coefficients.

The coefficients of Hilbert transformer are determined using MATLAB, [11]. Afterwards, obtained decimal values are converted into binary code with precision of 15 bits. Satisfactory results are achieved by the filter with 31 taps. Amplitude response of Hilbert transformer is shown in Figure 1, while its coefficients are given in Table 1. Coefficients are asymmetrical around central, h(15), and all odd coefficients are equal to zero. Therefore, impulse response of the filter can be described by the following equation (1) :

$$y(n) = \sum_{k=0}^{7} h(2k)[x(n-2k) - x(n-30+2k)]. \qquad (1)$$

Amplitude response around frequency of 50 Hz is shown in Figure 2. As it can be seen, around line frequency of 50 Hz there is an acceptable small amplification of 0.1855 dB. Better amplitude response can be achieved only by increasing number of filter taps. In that case, CSD architecture is inappropriate because it requires significant increase in hardware. However, MAC architecture provides savings in chip area and that enables Hilbert transformer design with better amplitude response.

3. BASIC MAC ARCHITECTURE

FIR filters implemented as MAC architectures use the following algorithm for output samples calculation.

The pairs coefficient/corresponding_input *signal*_sample represent inputs to a multiplier. Multiplication result is loaded into accumulator and added to multiplication result of previous pairs. Calculation is finished when multiplication result of the last pair is loaded into accumulator. Then, the output from accumulator is loaded into output capture register, reset signal is applied to accumulator, and calculation cycle is repeated.

Block diagram of the basic MAC architecture is shown in Figure 3. This digital system consists of several subsystems: Addressable Buffer (U1), Address Generator (U2), ROM module (U3), Subtracter (U4), MAC Unit (U5),

Output Capture Register (U6), Register Array (U7) and Controller (U8).

Table 1. *Hilbert transformer coefficients*

h(n)	Value	Binary code
h(0) = -h(30)	0.710938	0101101011111111
h(1) = -h(29)	0	
h(2) = -h(28)	0.260742	0010000101100000
h(3) = -h(27)	0	
h(4) = -h(26)	-0.0488892	1111100110111111
h(5) = -h(25)	0	
h(6) = -h(24)	-0.223145	1110001101101111
h(7) = -h(23)	0	
h(8) = -h(22)	-0.272461	1101110100100010
h(9) = -h(21)	0	
h(10) = -h(20)	-0.207031	1110010110000010
h(11) = -h(19)	0	
h(12) = -h(18)	-0.0189819	1111110110010001
h(13) = -h(17)	0	
h(14) = -h(16)	0.554443	0100011011110111
h(15)	0	

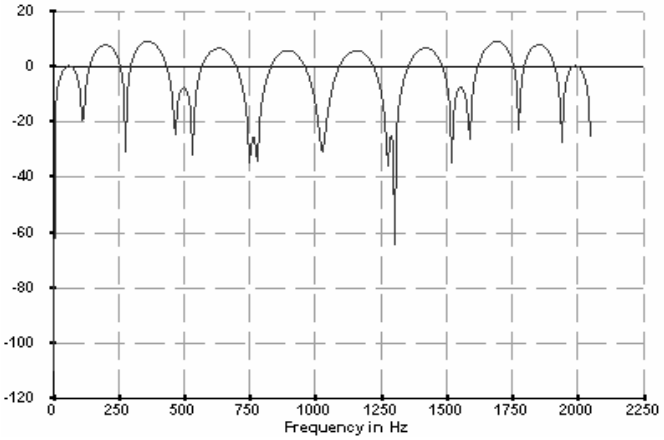

Figure 1: *Hilbert transformer amplitude response*

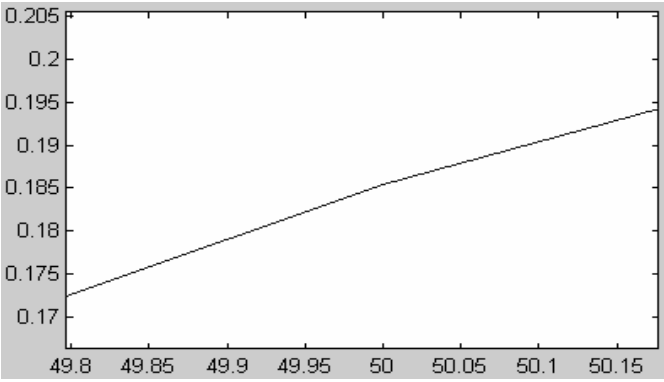

Figure 2: *Amplitude response around frequency of 50 Hz*

The system has the following ports: basic clock signal *clk* with frequency of 4.194.304 Hz, clock signal *clk1* for clock frequency of 4096 Hz (sampling frequency), *reset* used to asynchronously setup the system to initial state, input buses *In_V(15:0)* and *In_C(20:0)* for voltage and current signal, respectively, output bus *Out_Hil(15:0)* for output voltage signal, output buses *Delay_V(15:0)* and *Delay_C(20:0)* for delayed voltage and current signal, respectively.

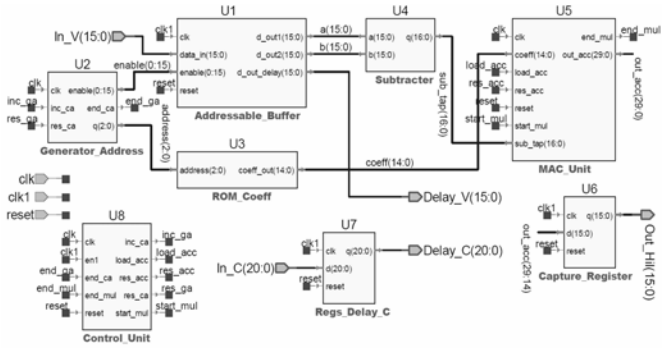

Figure 3: *Block diagram of basic MAC architecture of Hilbert transformer*

Addressable buffer consists of registers for delay implementation of input voltage signal samples and three-state buffers used to select the appropriate register content. At the rising edge of clock signal *clk1* a new input signal sample is loaded into the first register in array and simultaneously, the content of each register is shifted to the right in the next register. Addressable buffer consists of p 16-bit registers (p=31, filter order) and q 16-bit three-state buffers (q=16, the number of non-zero coefficients). Three-state buffers are divided into two groups. Both groups consist of 8 16-bit three-state buffers. Outputs of the first group are connected to the bus *a(15:0)*, while outputs of the second group are connected to the bus *b(15:0)*. As shown in equation (1), the corresponding input signal samples, *x(n-2k)* and *x(30-n+2k)* are subtracted and generated difference is multiplied by corresponding coefficient (multiplications by zero coefficients are not performed). Subsystem *Generator_Address* generates addresses for ROM module where coefficients are stored and enable signals for three-state buffers in addressable buffer.

Multiplier in MAC unit uses Booth algorithm for multiplication of 2's complement numbers [3]. For multiplication of one pair coefficient/corresponding_signals_difference, 15 clock cycles are necessary (the number of bits in the coefficient). The multiplier implementation details are shown in Figure 4.

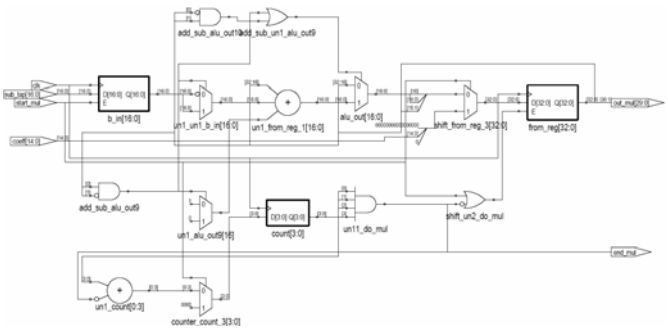

Figure 4: *Booth multiplier implementation*

Hilbert transformer output signal, *Out_Hil* is phase-shifted for 90° comparing to input voltage signal. In FIR

filter theory it is known that linear phase FIR filter of order M (with M taps) has the $delay = \frac{M-1}{2}$ (in samples). In order to synchronize results of active and reactive power calculation it is necessary to delay signals in voltage and current channel for the same value. Therefore, input voltage and current signals are passed through an array of 15 registers and signals *Delay_V* and *Delay_C*, respectively are generated. However, addressable buffer causes one additional delay as well as output register *Capture_Register*, so input current signal is passed through the array of 17 registers (delayed current signal, *Delay_C* is at *Regs_Delay_C* output). Voltage signal delay is not implemented by special registers, but addressable buffer registers are used, so delayed voltage signal, *Delay_V* is output signal from 17th addressable buffer register.

The control unit manages the work of the whole system. It is implemented as Moor FSM (Finite State Machine) with 8 states. It receives status signals from all subsystems (for example, when multiplication is finished) and generates control signals necessary for their function (for multiplication start, for accumulator load, etc.).

4. COMPACT MAC ARCHITECTURE

Compact MAC architecture has the following improvements comparing to the described (basic) MAC architecture:

- RAM modules used as memory elements instead of registers occupy smaller area on the chip.
- Gated clock signals are applied [4] in order to decrease dissipation.
- Modified Booth algorithm is implemented [5] in order to reduce the number of clock cycles necessary for multiplication.
- Overlapping technique is applied in order to speed up output sample calculation.

The most important improvement giving smaller chip area is the way of storing voltage and current signal samples. Instead of registers (*Addressable_Buffer* and *Regs_Delay_C*) RAM modules are used. They occupy smaller chip area than mentioned subsystems. Block diagram for this architecture is shown in Figure 5.

Subsystem *Datapath* is described in VHDL while Verilog models of RAM modules *SPS4_64x24* (U2 and U3) are supplied by technology vendor. Memories are accessed synchronously at rising edge of the clock.

RAM modules require additional control logic in subsystem *Datapath*. However, chip area necessary for this logic is significantly smaller than the area for registers implemented using standard flip-flop cells.

Address generator for memories is more complex comparing to the one in the basic MAC architecture. Its implementation is shown in Figure 6. The generator consists of blocks *Address_Shift* and *Address_Mul*. Their outputs are connected to inputs of a multiplexer. Subsystem *Address_Shift* is used to shift the memory cells content (i.e. voltage and current signal samples). It is implemented as FSM and works as the following:

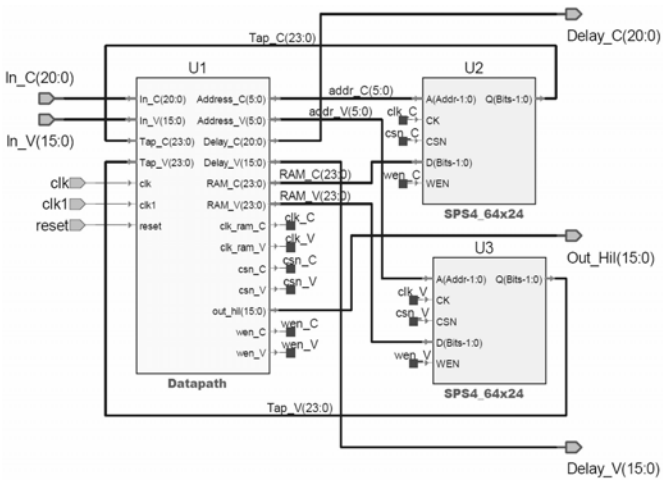

Figure 5: *Block diagram of compact MAC architecture of Hilbert transformer*

Initially, the address "29" is generated and the content of corresponding memory location is read. Then, the address "30" is generated and the content of memory location with address "29" is written at the address "30". This procedure continues and finally, in location "0" is stored the content of the register where current voltage signal sample is stored. Inputs of the multiplexer that is in front of the memory data input are connected to memory output and the mentioned register output (Figure 7).

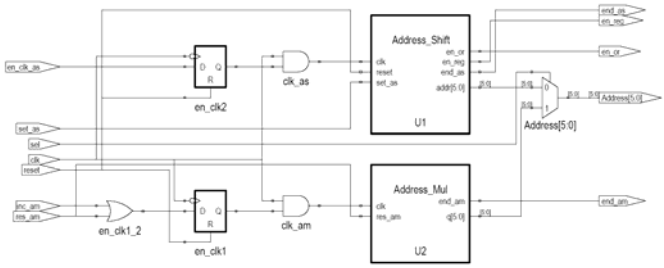

Figure 6: *Address generator implementation details*

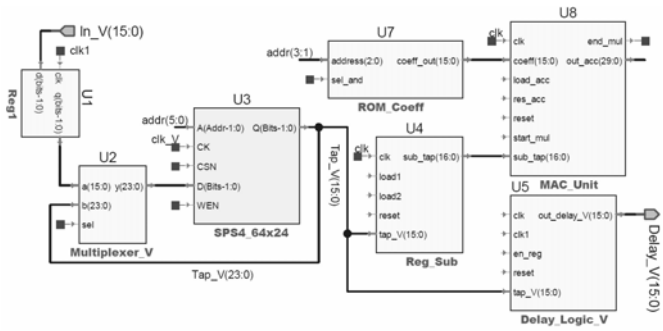

Figure 7: *Datapath subsystem block diagram*

Subsystem *Address_Mul* shown in Figure 6 generates

addresses during multiplication of pairs coefficient/samples_difference. Appropriate samples *x(n-30+2k)* and *x(n-2k)* are read from RAM (U3 in Figure 5) and loaded into registers *Reg_Sub*, shown in Figure 7. Then, the register contents are subtracted (coefficients are asymmetrical). Subsystem implementation details are shown in Figure 8.

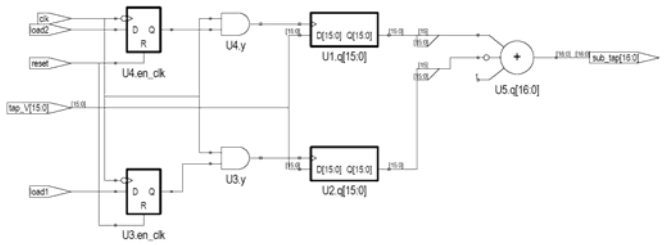

Figure 8: *Reg_Sub implementation*

Subsystems *Delay_Logic_*V and *Delay_Logic_*C generate delayed signals *Delay_V* and *Delay_C*, respectively at subsystem *Datapath* output.

Delay_Logic_V implementation is shown in Figure 9. The content of memory location "15" is written into the first register, and then the content of the first register is written into the second register. The second register clock frequency is 4.096 Hz (sampling frequency). Subsystem *Delay_Logic_C* is implemented in a similar way.

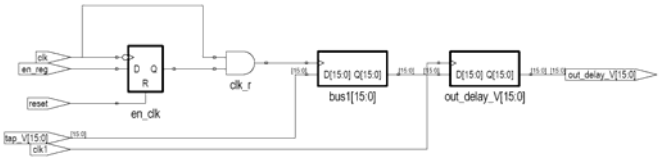

Figure 9: *Delay_Logic_V implementation*

In order to reduce power consumption in the system (i.e. dynamic dissipation), all sequential elements in the subsystem *Datapath* are clocked by gated clock signals. These clocks are used for the memories as well. To enable correct functioning of the system, it is very important to avoid glitches during the clocks generation. Figure 10 shows the block used for gated clock signals generation [6].

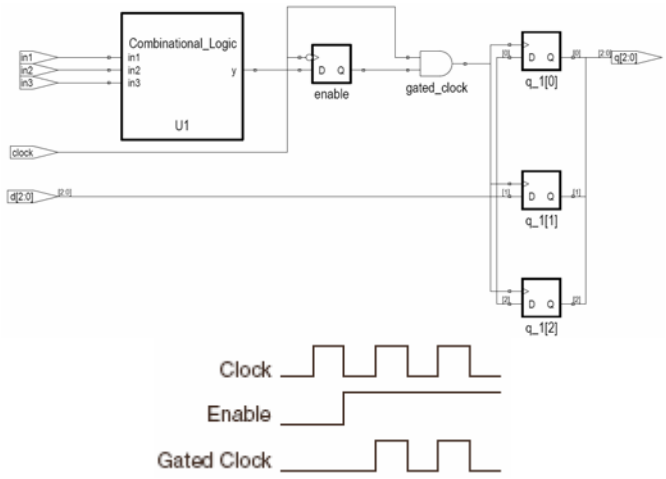

Figure 10: *Gated clock signals generation*

During the clock falling edge the flip-flop placed between combinational logic and AND gate generates enable signal for glitch-free clock signal. When *enable* is '1', AND gate passes the clock to flip-flops triggering at rising edge. Since both clock edges are used for triggering of flip-flops, one must pay attention on the duty cycle of the clock and delay through the logic that generates enable signal, because the enable signal must be generated in half the clock cycle. This situation might cause problems if the logic that generates enable signal (block *Combinational_Logic* in Figure 10*)* is complex, or the clock with asymmetrical (severely unbalanced) duty cycle is used. Therefore, it is important to control duty cycle of the clock very carefully.

Modified Booth algorithm enables decrease in the number of clock cycles necessary for multiplication. These modification is based on filter coefficient transformation called radix-4 recoding [5]. Transformation is shown in Table 2, while the process of multiplier recoding is shown in Figure 11. If n is the number of bits in multiplier (n should be an even number), $n/2$ clock cycles is necessary for multiplication. Since filter coefficients are 16-bit numbers, 8 clock cycles are needed for multiplication of coefficient/samples difference. Modified multiplier implementation details are shown in Figure 12.

Table 2. *Radix-4 recoding*

Original bits $y_{2i+1}y_{2i}y_{2i-1}$	**Recoded bit** y_i'
000	0
001	1
010	1
011	2
100	-2
101	-1
110	-1
111	0

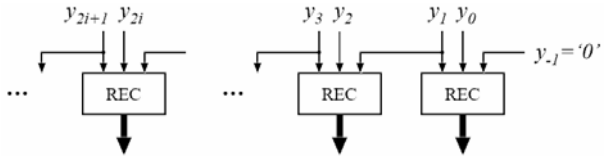

Figure 11: *Radix-4 recoding*

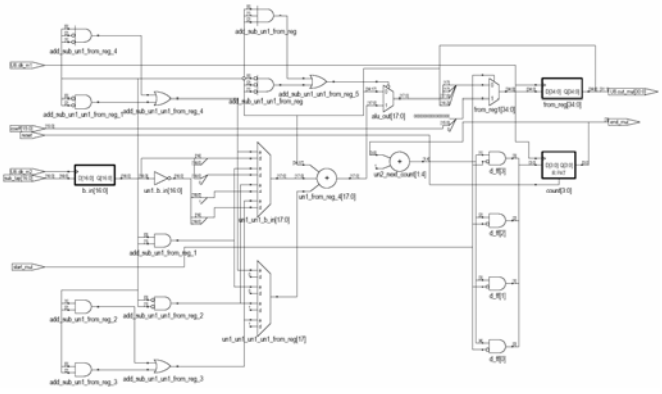

Figure 12: *Modified Booth multiplier implementation*

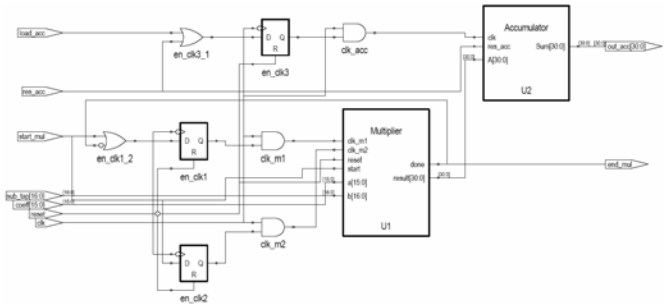

Figure 13: *MAC_Unit implementation*

In order to speed up output sample calculation, overlapping technique is applied together with modified Booth algorithm (this technique is used in pipelined microprocessors) [7]. The output sample calculation can be divided in two phases. During the first phase input signal samples are read from the memory, loaded into registers and then register contents are subtracted (subsystem *Reg_Sub*). In the second phase the pair coefficient/input_signal_samples_difference is multiplied and the result is written in accumulator (*MAC_Unit* module). These phases can be overlapped in time. Therefore, the fetching of new samples from the memory can begin at the moment when multiplication of one pair starts,. Figures 14 and 15 show sequential and overlapping operations, respectively. OF (*Operand Fetching*) denotes fetching of input signal samples from RAM, while MAC (*Multiply and ACcumulate*) denotes multiplying by the coefficient and loading in the accumulator.

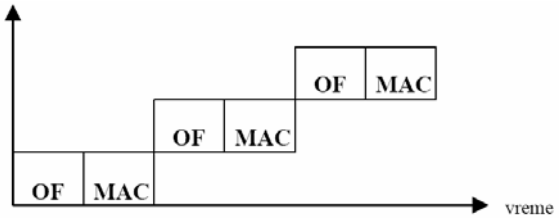

Figure 14: *Sequential operation*

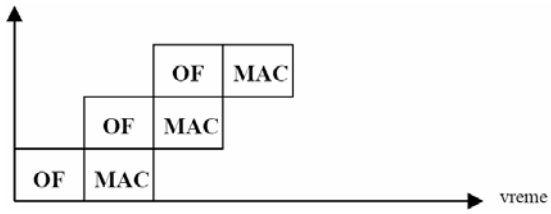

Figure15: *Overlapping operation*

Figure 16 shows clock signals triggering flip-flops in multiplier (*clk_m1* and *clk_m2*), accumulator (*clk_acc*) and registers in the subsystem *Reg_Sub* (*clk_l1* and *clk_l2*) generated during simulations. As it can be seen, there is an overlapping in time between clock signals *clk_l1*, *clk_l2* and *clk_m2*. Obviously this shortens the time interval between two successive multiplication cycles.

Modified Booth algorithm and overlapping technique enable reduction in the number of clock cycles necessary for MAC operations for about 40% (from 152.5 to 94.5). In that way the number of clocks for shifting of RAM content is compensated, and maximal number of filter taps that can be achieved using the same hardware is increased.

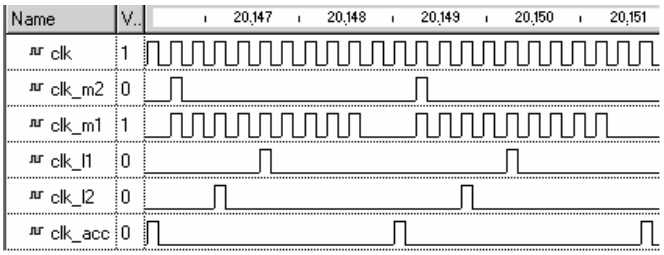

Figure 16: *Overlapping technique*

5. SIMULATION AND SYNTHESIS RESULTS

Hilbert transformer VHDL description is verified using *Active HDL* simulator [8]. Input sequence for verification is taken from FIR filter outputs (voltage and current). Figure 17 shows simulation results for signals *Delay_V*, *Delay_C* and *Out_Hil*. These signals are sinusoidal in time domain like "analog" signals, but they are actually values of 16-bit (*Delay_V* and *Out_Hil*) and 21-bit (*Delay_C*) output signals.

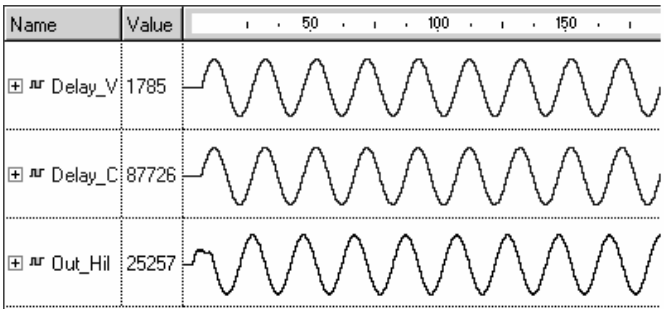

Figure 17: *Hilbert transformer simulation results*

After that, Hilbert transformer VHDL descriptions are synthesized using AMI Semiconductor 0.35um C035M-D technology library in the program *Ambit Build Gates* that is a part of Cadence package [9, 10]. Chip areas for both MAC architectures and CSD architecture are shown in Table 3. Compact MAC architecture is implemented using 64x24 RAM cells that are much bigger than it is necessary for 31 tap filter implementation.

Table 3. *CSD and MAC architecture areas after synthesis*

Architecture	Area in number of NAND gates	Area in um^2
CSD	10286.41	555466.14
Basic MAC	6418.97	346624.38
Compact MAC	5690.34	307278.36

After synthesis, generated VHDL netlist is simulated in order to verify synthesis results. Simulation results (Hilbert

transformer output) are imported in MATLAB [11] and FFT (*Fast Fourier Transform*) is calculated. Power spectrum of Hilbert transformer input and output signal is shown in Figures 18 and 19. Obviously, filter performances remained unaffected (SFDR>100dBc).

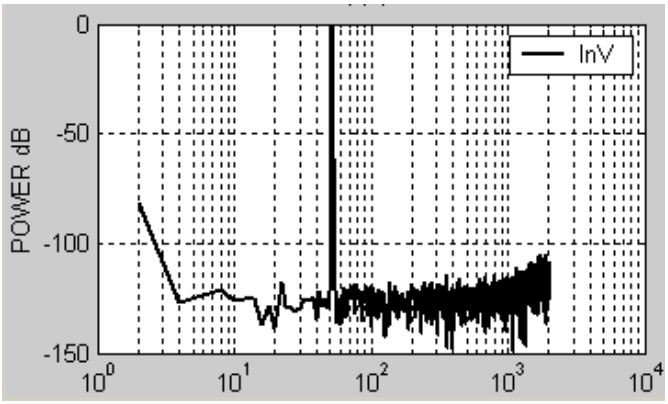

Figure 18: *Power spectrum of Hilbert transformer input signal*

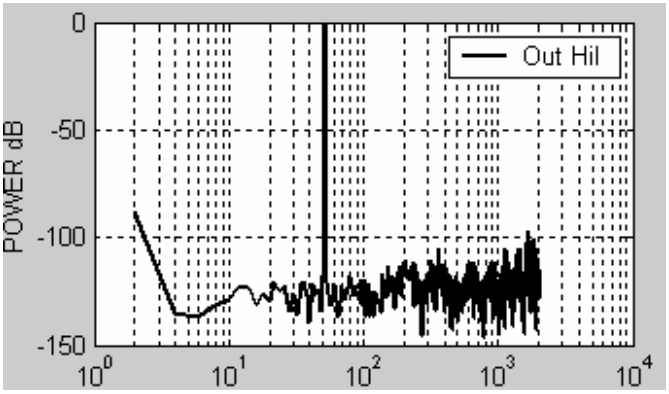

Figure 19: *Power spectrum of Hilbert transformer output signal*

6. CONCLUSION

Two implementations of Hilbert transformer MAC architecture (basic and compact) are described in this paper. Both implementations are realized as macro blocks using AMI Semiconductor CMOS 0.35um C035M-D standard cells technology library. It was shown that MAC architecture gives smaller chip area comparing to CSD architecture. Both MAC architectures are verified by VHDL simulations and FFT analysis.

Compact MAC architecture is realized by modification of basic one using:

- RAM memory cells instead of registers,
- Gated clock signals,
- Overlapping technique,
- Modified Booth algorithm.

In that way the following improvements are achieved:

- Smaller chip area,
- Decreased power consumption,
- Increase in calculation speed.

Besides this, compact MAC architecture enables to increase filter order (number of taps) by minimal increase in hardware. Bigger number of taps requires significant increase in hardware for basic MAC architecture and especially for CSD architecture. One should notice that 64x24 RAM cells are used, i.e. bigger than it is necessary for 31 tap filter implementation.

7. REFERENCES

[1] Nikolić, M., Andrejević, M., Savić, M., Anđelković, B., "Top-Level Layout Design of Solid-State Energy Meter", Proc. of XLVIII Conference of ETRAN, Vol. I, pp. 13-16

[2] Bojan Anđelković, Milunka Damnjanović, „Design Of Hilbert Transformer For Solid-State Energy Meter", Proc. of XLVIII Conference of ETRAN, Vol. I, pp. 83-86

[3] Z. Huang, "High-Level Optimization Techniques for Low Power Multiplier Design", Ph.D. Thesis, University of California, Los Angeles, 2003.

[4] Emnett F., Biegel M., "Power reduction through RTL clock gating", Synopsis Users Group, SNUG, Papers and Presentations, San Jose, 2000.

[5] http://www.ecs.umass.edu/ece/koren/arith/simulator

[6] Altera 2002 Documentation, Application Note 238, http://www.altera.com.

[7] M. Stojčev, "RISC, CISC i DSP procesori", Univerzitet u Nišu, Elektronski fakultet, 1997 (in Serbian).

[8] "*Active-HDL, ver.5.1. User's Manual*", ALDEC Inc., 2002.

[9] Cadence 2003 Documentation, http://www.cadence.com.

[10] AMI Semiconductor CMOS 0.35um Technology Documentation.

[11] *" MATLAB and SIMULINK Users Guide"*, The MathWorks, Inc., Natich, MA, 1997.

BLACK-BOX APPLICATION IN MODELING OF MICRO-ELECTRO-MECHANICAL SYSTEMS

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Mark Zwolinski, University of Southampton

Abstract: *New concepts of modeling and simulation of micro-electro-mechanical systems (MEMS) are proposed, intended to boost the time to market and dependability of such systems. Black-box modeling of non-electronic parts is introduced using artificial neural networks, so enabling radically faster simulation without concurrent algorithms and parallel computation. A lumped model of the capacitive transducer, being the part of a micro-electro-mechanical capacitive pressure sensing system, is created using an artificial neural network (ANN).*

Keywords: *Black-box Modeling, Artificial Neural Networks, Micro-Electro-Mechanical Systems.*

1. INTRODUCTON

Advances in semiconductor technology and related economic developments strongly point to the rapid emergence and significant potential of the new silicon-infrastructure, or design-for-manufacturability, market. The DFM market ex-tends from design implementation, mask synthesis, and adva-nced lithography techniques. According to [1] in 2003, ana-lysts projected the market to grow 64% to USD 220 million.

Some of the ultimate goals of DFM include isolating designers from process details and making designs foundry--independent. In that regard, the industry has seen a limited number of DFM platforms emerging to date. An ideal DFM platform should include all data including design, lithography, and production manufacturing, and a design system connecting all these phases is still far from reality.

When a model is available and characterised, a design automation solution will be able to allow a designer to extract, analyze, simulate, and optimize the circuit prior to the handoff to manufacturing. This will provide some confidence that the design will function.

This more comprehensive model requires a new infrastructure that supports a feedback loop between designer and manufacturer. The feedback loop should include a means of defining and relaying manufacturing constraints, verifying IC layouts, and demonstrating manufacturing-related issues to the designer.

Simulation, in our opinion, is one of the key issues in the development of such a model. In this paper, new concepts for coping with new challenges will be implemented. Our ideas relating to these concepts are briefly expressed below.

2. MEMS SIMULATION

Consider the problem of simulating the simple circuit depicted in Fig. 1. This is a micro-electro-mechanical capacitive pressure sensing system. It consists of an electro-mechanical part that is a capacitor with a deflectable membrane such that a change in pressure results in a change in capacitance, and an electronic switched-capacitor network that generates a pulse train of fixed frequency. The pulse amplitude at the output is related to the capacitance value, so that the whole system converts pressure into pulse amplitude.

For simulation of this and other similar systems we have implemented "Alecsis-the simulator for circuits and systems" [2], [3], [4], [5], [6], [7], [8], [9]. It is a mixed-signal (analogue and discrete), mixed-level (or mixed-abstraction) (system-level analogue and digital, device-level electrical and gate-level digital, grid-level mechanical), and mixed description (behavioural digital, behavioural analogue, circuit-electrical, gate-digital, algebraic logic and electrical, and partial equation with a set of facilities for boundary condition management). A library of built-in models has been provided.

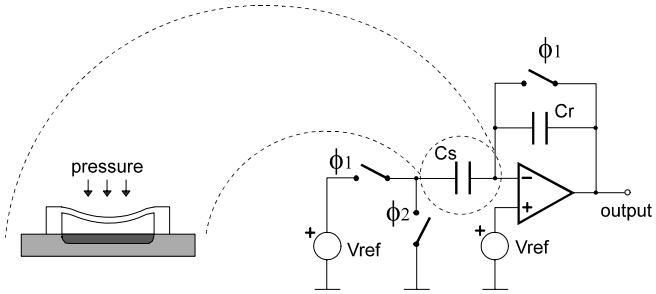

Fig. 1. *Micro-electro-mechanical capacitive pressure sensing system*

In addition, a hardware description language named AleC++ was developed as a superset of C++ in order to make the description of the models tractable [10], [11], [12], [13].

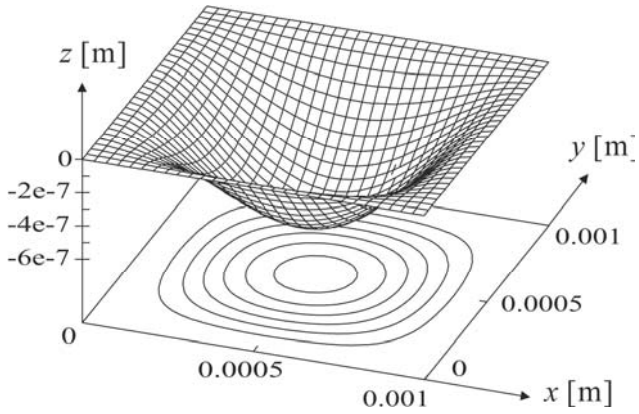

Fig. 2. *Displacement of the sensor membrane for simulation time instant 0.0004s*

Partial differential equation for the sensor membrane is:

$$D\left(\frac{\partial^4 w}{\partial x^4}+2\frac{\partial^4 w}{\partial x^2\partial y^2}+\frac{\partial^4 w}{\partial y^4}\right)=p+\rho h\frac{\partial^2 w}{\partial t^2}+k\frac{\partial w}{\partial t} \quad (1)$$

where x, y are spatial coordinates, p is effective pressure, w is membrane displacement, ρ is material density, h is membrane thickness, k is dumping coefficient and D is bending rigidity. Equation (1) is applicable only to isotropic materials. Also, it

cannot be solved in closed form, numerical solution is necessary.

If the membrane of the rectangular shape is clamped at its edges, than the boundary conditions are:

$$w(x=0 \wedge x=L)=0, \qquad \frac{dw}{dx}(x=0 \wedge x=L)=0$$
$$w(y=0 \wedge y=W)=0, \qquad \frac{dw}{dy}(y=0 \wedge y=W)=0 \tag{2}$$

L and W are length and width of the membrane, respectively. Boundary conditions can be changed if bending of the membrane rim is significant and has to be modeled.

For capacitance modeling, a parallel plate approxi–mation is used. Capacitance in Alecsis is modeled by the following expression:

$$C = \varepsilon \int_{x=0}^{L} \int_{y=0}^{W} \frac{dxdy}{l - w(x,y)} \tag{3}$$

where C is capacitance, ε is dielectric constant of the capacitor dielectric material, and l is distance between the ground plane and the unloaded membrane.

The coupling between mechanics and electronics is modeled according to equation:

$$i = \frac{dQ}{dt} = C\frac{dv}{dt} + v\frac{dC}{dt} \tag{4}$$

where Q is total charge at the capacitor sensor, i is electrical current through its contact terminals, and v is voltage across the capacitor plates.

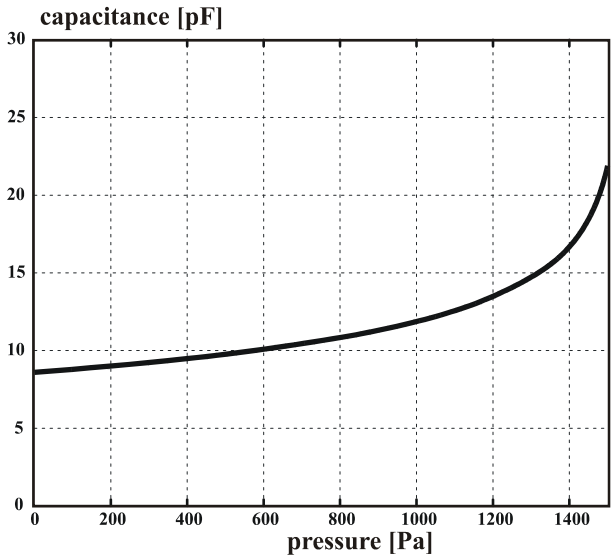

Fig. 3. *The capacitance of the membrane of Fig. 1 expressed as a function of pressure. This dependence is also obtained using the ANN structure from Fig. 5*

Considering these equations, Alecsis simulation is performed, and dependence of capacitance on applied pressure is presented in Fig. 3.

As an example of MEMS simulation, circuit presented in Fig. 1 is used. Time domain simulation results for the system are given in Fig. 4.

The mechanical and the electrical part are modeled within a single description and the simulation performs simultaneous evaluation of all system variables that are (in this case) displacements, voltages, currents, and states.

The concept proposed in this simulation system has been widely recognized [14], [15], [16], and [17].

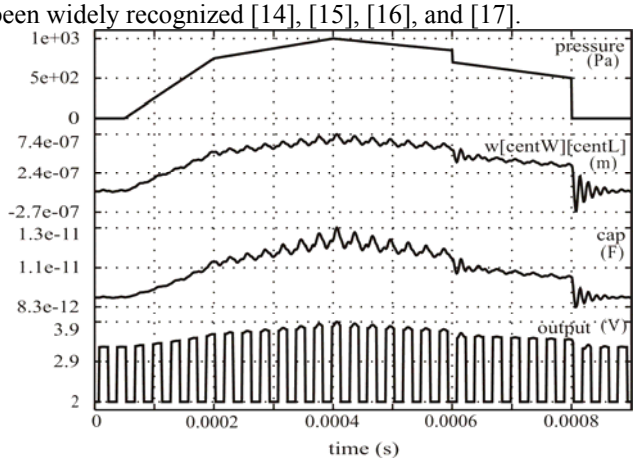

Fig. 4. *Time-domain simulation results for the system given in Fig. 1. The traced signals are pressure, displacement of the pressure sensor centre, sensor capacitance, and the output voltage.*

3. BLACK-BOX MODELING

To start with, an ANN was created to get a lumped model of the capacitive transducer. The ANNs here are considered universal approximators [18], convenient for black-box device modeling. The process starts with the extraction of the $C(p)$ dependence from the "Alecsis" simulation of the system in Fig. 1., given in Fig. 3.

The structure of the ANN used is depicted in Fig. 5. It is a simple feed-forward ANN with only one hidden layer. The hidden neurons have sigmoidal activation functions, while the output neuron is linear. Table 1 contains the weights and thresholds of the ANN obtained after training with a standard algorithm.

The $C(p)$ dependence obtained using this neural network is the same as in Fig. 3.

Table 1: *Weights and thresholds of the ANN used to approximate the curve of Fig. 3*

Hidden layer neurons	Output layer neurons
w(1,1)(2,1) = 33.1034	w(2,1)(3,1) = 2.32691
w(1,1)(2,2) = 3.92046	w(2,2)(3,1) = 17.8609
w(1,1)(2,3) = 4.04654	w(2,3)(3,1) = -15.9505
θ (2,1) = -35.6658	θ (3,1) = 0.354662
θ (2,2) = -3.88227	
θ (2,3) = -3.88324	

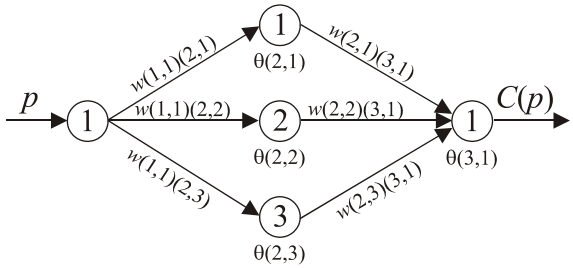

Fig. 5. *The ANN structure used for approximation of the curve of Fig. 3. (w stands for weight and θ for threshold)*

The capacitor constitutive equation

$$i_C = C(p)\frac{dv_C}{dt} \tag{5}$$

was implemented according to [5]. Discretization was performed first:

$$i_c^{n+1} = C(p^{n+1})\cdot(A\cdot v_c^{n+1} + B_v^n) \tag{6}$$

where A and B are constants derived from the discretization rule. n stands for the time instance counter.

After that, linearization was applied in order to implement Newton's method for nonlinear analysis. This yields

$$\begin{aligned} i_c^{n+1,m+1} = i_c^{n+1,m} + G_v^{n+1,m}\cdot(v_c^{n+1,m+1} - v_c^{n+1,m}) + \\ + G_p^{n+1,m}(p^{n+1,m+1} - p^{n+1,m}) \end{aligned} \tag{7}$$

where

$$i_c(p^{n+1,m}) = i_c{}^{n+1,m} = C(p^{n+1,m})\cdot(A\cdot v_c^{n+1,m} + B_v^n), \tag{8}$$

$$G_v^{n+1,m} = \left.\frac{\partial i_C}{\partial v_C}\right|_{v_C = v_c{}^{n+1,m}} = A\cdot C(p^{n+1,m}), \tag{9}$$

and

$$\begin{aligned} G_p^{n+1,m} = \left.\frac{\partial i_C}{\partial p}\right|_{p = p^{n+1,m}} = \\ = (A\cdot v_c^{n+1} + B_v^n)\cdot\left.\frac{\partial C(p)}{\partial p}\right|_{p = p^{n+1,m}} \end{aligned} \tag{10}$$

The discretized and linearized model of the nonlinear capacitor represented by (7) may be expressed in a circuit form as depicted in Fig. 6. Note that, to apply this model we write code to calculate the response of the ANN that is $C(p)$, and its derivative with respect to p.

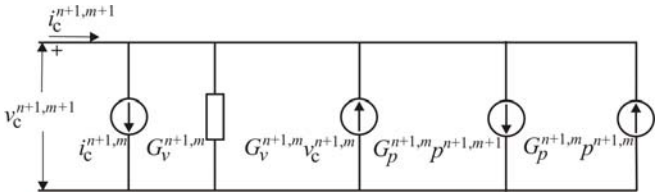

Fig. 6. *The linearized and discretized model of the capacitor controlled by pressure*

4. SIMULATION RESULTS

Fig. 7. shows an excerpt from Fig. 4., repeating for convenience the input (pressure) signal to the transducer. A new simulation is performed now for the original circuit in the Fig. 1., but with the membrane substituted by a lumped model of the capacitor expressed by the ANN. The simulation results, as shown in Fig. 8., are in excellent agreement with those obtained earlier.

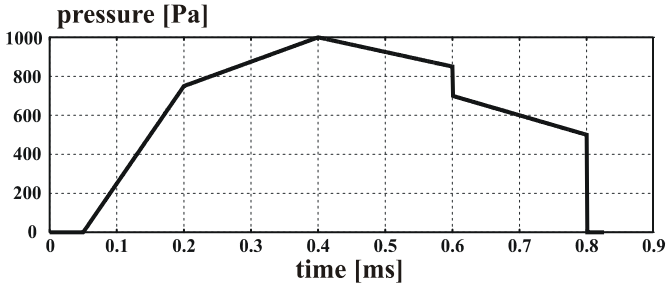

Fig. 7. *Part of Fig. 3. redrawn for convenience*

What is the difference? To obtain the result in Fig. 8. we need to simulate a circuit described by 5 (five) network variables only, compared with 1005 to describe the original circuit. This enables inexpensive repetitive simulation of the system when faults are inserted.

Such simulations are presented in Figs. 9. and 10.

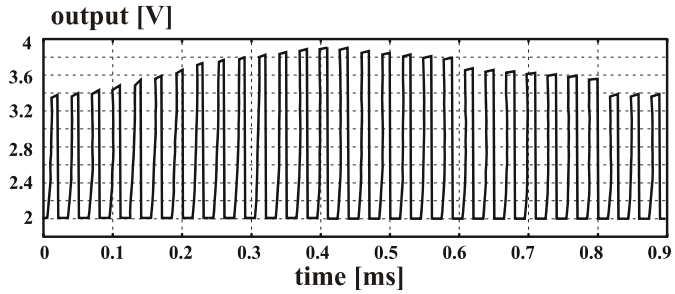

Fig. 8. *Simulation results of the circuit of Fig. 1. with the membrane substituted by a lumped capacitor*

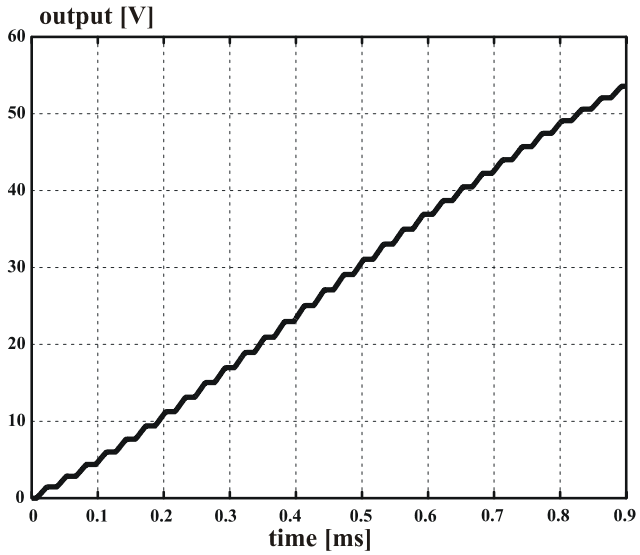

Fig. 9. *Response of the faulty circuit in the presence of the "feed-back switch of the operational amplifier stuck-at-open" fault*

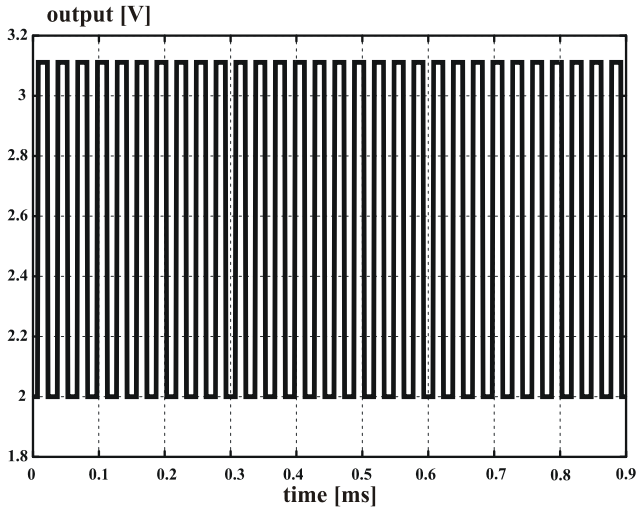

Fig. 10. *Response of the faulty circuit in the presence of the "membrane stuck-at-flat" fault*

Note that, while fault model insertion in the electronic part (both digital and analogue) is well understood and easy to implement [6], [9], there is still much research to be done for mixed-signal electronic circuits and, unfortunately, even more work for non-electronic structures, the membrane being almost the simplest example.

5. CONCLUSIONS

Concepts and research tasks are proposed for a new radically improved concept of MEMS simulation, intended to boost the time to market and dependability of such systems. It conforms to the new design for manufacturability concept that stresses the testing and diagnostic aspects of the design cycle. Ideas are proposed that can make modeling and simulation into a routine tasks performed within a short time. As shown by a simple example these ideas are feasible.

6. REFERENCES

[1] Vandenberg, C., "*Back to basics: The IC Industry's reintegration and dynamics of a newly emergent full-chip, design-for-manufacturability infrastructure*", IEEE Design and Test of Computers, Vol. 21, No. 3, 2004, p. 180.

[2] Jakovljević, M., Mrčarica, Ž., Fotiu, P., Detter, H., Litovski, V., "*Implementation of Finite Elements Using An A-HDL Environment*", Numerische Simulation in Feinwerk-/Mikrotechnik und Elektronik, Munchen, Germany, March 4-5, 1998.

[3] Litovski, V., and Zwolinski, M., "*VLSI circuit simulation and Optimization*", Chapman and Hall, London, 1997.

[4] Maksimović, D., and Litovski, V., "*Tuning the logic simulator for timing simulation*", Electronic Letters, Vol. 35, No. 10. May 1999, pp. 800-802.

[5] Maksimović, D., Litovski, V., "*Logic simulation methods for longest path delay estimation*", IEE Proceedings Computers and Digital Techniques, Vol. 149, No. 2, 2002, pp. 53-59.

[6] Milovanović, D., and Litovski, V., "*Fault models of CMOS Circuits*", Microelectronics Reliability, Vol. 34, No. 5, 1994, pp. 883-896.

[7] Mrčarica, Ž., Glozić, D., Litovski, V., Detter, H., *"Simulation of Microsystems Using A Behavioural Hybrid Simulator Alecsis"*, in: Adey, R.A., Lahrmann, A., Lemboe Ilmann, C., editors, "*Simulation and Design of Microsystems and Microstructures*", Computational Mechanics Publication, Southampton, GB, 1995.

[8] Mrčarica, Ž., Risojević, V., Lenczner, M., Jakovljević, M. and Litovski, V. "*Integrated simulator for MEMS using FEM implementation in AHDL and frontal solver for large-sparse system of equations*", Proc. of Design and Test of Microsystems, Paris, March 1999, pp. 271-278.

[9] Petković, P., Milovanović, D., Litovski, V., *"Symbolic Fault Modeling and Test Generation of MOS Circuits"*, Microelectronics and Reliability, Vol. 37, No. 1, 1997, pp. 137-157.

[10] Damnjanović, M., Dimić, Ž., Litovski, V., and Glozić, D., "*Hardware description language for Alecsis simulator*", Proc. of the 20th Conf. on Microelectronics, 1995, Vol. 2., pp. 525-528.

[11] Litovski, V., Maksimović, D., and Mrčarica, Ž., "*Mixed-signal modeling with AleC++: Specific features of the HDL*", Simulation Practice and Theory, Vol. 8, 2001, pp. 433-449.

[12] Mrčarica, Ž, Ilić, T., Glozić, D., Litovski, V., and Detter, H., "*Mechatronic Simulation Using Alecsis: Anatomy of the Simulator*", Proc. of the Eurosim'95, Vienna, Austria, Sept. 1995, pp. 651-656.

[13] Mrčarica, Ž., Litovski, V., Detter, H., *"Modeling And Simulation of Microsystems Using Hardware Description Language"*, Research Journal on Microsystem Technologies, Vol. 3, No. 2, Feb., 1997, pp. 80-85.

[14] Chappel, B., "*The fine art of IC design*", IEEE Spectrum, Vol. 36, No. 7, July 1999., pp. 30-34.

[15] Endemano, A., et al. "*VHDL-AMS modeling and simulation of a planar electrostatic micromotor*", J. of Micromechanics and Microengineering, Vol. 13, 2003, pp. 580-590.

[16] Haase, J., Schwarz, P., Trappe, P., und Vermeiren, W. "*Erfahrungen mit VHDL-AMS bei der Simulation heterogener Systeme*", ITG/GI/GMM Workshop, "Methoden und beschreibungssprachen zur modellirung und verifikation von Schaltungen und Systemen", Frankfurt/M, 28-29.02.2000, pp. 167-175.

[17] Senturia, S. D., "*CAD challenges for Microsensors, Microactuators, and Microsystems*", invited paper, Proceedings of the IEEE, Vol. 86, No. 8, August 1998., pp. 1611-1626.

[18] Scarselli, F., and Tsoi, A. C., "*Universal approximation using feed-forward neural networks: A survey of some existing methods and some new r*esults", Neural Networks, Elsevier, Vol. 11, No. 1, 1998, pp. 15-37.

An Example of Hardware-In-the-Loop-Simulation using Mission Level Designer Simulator

Borisav Jovanović, Volker Zerbe

Abstract – A system with fluid level sensors, pumps and control unit was designed as an example of Hardware-in-The-Loop Simulation in Mission Level Designer simulator. For realization of a proposed system multi domain simulation is used.

Keywords – System with sensors and pumps, multi domain simulation, Hardware-in-The-Loop-Simulation.

I INTRODUCTION

With capabilities provided by today's graphic based software, such as ML Designer, systems can be rapidly developed using system level concepts by a single control engineer. In this development environment, the engineer does no programming at all from his perspective; he simply draws the design on the computer screen as a system of interconnected blocks. Therefore, an engineer can focus entirely on design issues eliminating the need for code development and debugging and he can complete more design iterations in a shorter period of time.

For most of real systems, there are characteristics that are unknown or too complex to be modeled by pure simulation. Good system engineering practice should begin with a pure simulation. Later, as components become better defined (with the aid of simulation), they can be fabricated and replaced in the control loop. Once physical components are added to the loop, un-modeled characteristics can be investigated, and controls can be further refined. The use of HILS eliminates expensive and lengthy iterations in machining and fabrication of parts, and speeds development towards a more efficient design.

With the HILS approach we now have the advantage that the control design has been proven with the actual hardware, and the design has been well defined. Since we know the control algorithm, we also know the computational load, and can select an appropriate processor - neither under nor over-rated to accomplish the task.

II SYSTEM WITH SENSORS AND PUMPS

B. *System overview*

An example of Hardware–In-the-Loop system consists of the pool filled with fluid (it can be water), two fluid pumps (P0 and P1 shown in Fig.1), four sensors (S0, S1, S2, and S3) and control subsystem that turns on and off the pumps. Also, the pool has valve through which it can be emptied. The amount of fluid coming out from pool's valve can be changed.

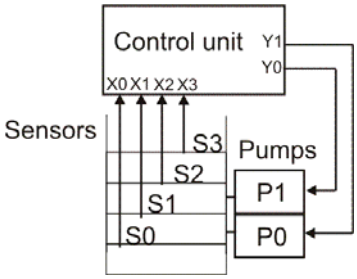

Fig. 1. Block diagram of a system that consists of sensors, pumps and control unit

The pumps have electrical inputs to turn pumps on and off (Y1 and Y0) and their activity can be easily controlled by control unit (shown in Fig.1).

Inside the pool, there are four sensors (S0, S1, S2, S3) fixed on different levels, measuring the level of fluid. Sensor S0 has the lowest level or level with the greatest depth. Sensor S3 is fixed on the highest level. All four sensors have electrical outputs (X3, X2, X1, X0 shown in Fig.1) that are inputs of the Control unit. When water level exceeds the level of some sensor, its output is set to 5V. Otherwise, its output is 0V signal.

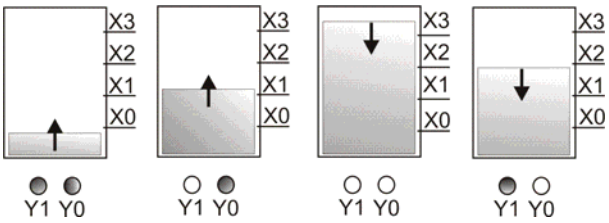

Fig. 2. Pump's functioning

Sensors produce output to the control unit which, in response, controls the pumps. The pumps functioning should be as follows:

If water level drops below X0 level, both pumps should be turned on (Fig 2.a). The pumps will stay in active state until water level exceeds X1 (Fig 2.b) when one pump is turned off and the other remains working. For example, let the pump which is turned off be P1 and the other that is left turned on be P0. If the water level is raising again, in the moment when it gets over X3 level (Fig 2.c), P0 pump is turned off. Then both pumps are turned off. This situation is changed when water level gets under X2 level (Fig 2.d). Then only one pump should be turned on and the other turned off. If previously pump P0 was working alone, now, the other pump, P1, is working.

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B. Mission Level Modeling and Simulation

First, in order to develop and simulate mission level design models, the tool MLDesigner is used [3]. Modelling is simplified by providing a graphical editor for creating block diagrams and a huge library of built-in primitives letting designers to concentrate on modeling instead of programming. It is also possible to develop own primitives in a C/C++ like language [4]. The overall system model consists of functional module Controller FSM and environmental components and it is shown in Fig. 3.

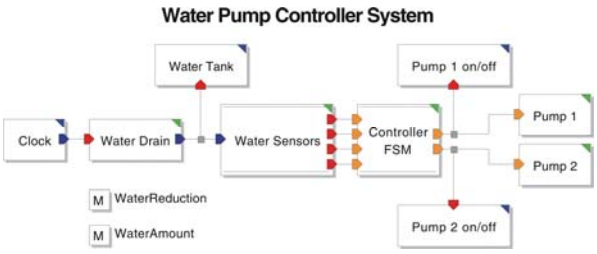

Fig. 3. The overall model of Water Pump Controller System

The complete system is heterogenous and consists of components from different domains. MLDesigner supports the description of such systems where modules from different domains can be combined together. An integrated multi-domain simulator enables simulation and verification of an entire system model and generated simulation results can be evaluated by appropriate plot and animation tools. Different domains for modeling and simulation are supported: Discrete Event, Dynamic Data Flow and Synchronous Data Flow. These primary domains are augmented by two subdomains: Finite State Machine and Higher Order Functions. Models in subdomains are always incorporated into systems in other MLDesigner domains.

The control function for the described system has to be developed by using MLDesigner finite state machine (FSM) models. Three different implementations of control function were made. One of them is shown in Fig. 4. The complete function can be decomposed into a pump controlling FSM and an automaton that handles their equal distribution. A Pump Control FSM and a Pump Distribution FSM instances are then interconnected inside a higher level FSM module that also defines input/output interface of the controller.

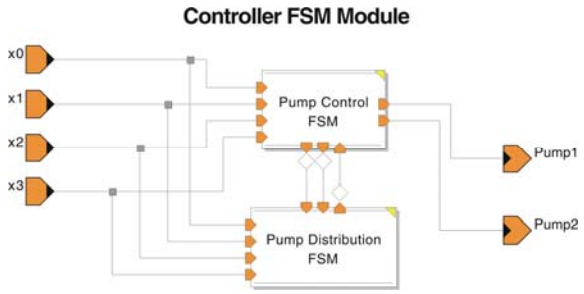

Fig. 4. Controller FSM Module

III HARDWARE-IN-THE-LOOP-SIMULATION

A. Hardware-In- the-Loop- Simulation Overview

After high-level simulations in ML Designer, system's parts had to be checked in real conditions. Because the designing all three full implementations require much time and effort, only one of them had to be chosen for final implementation. Instead of doing all three full design implementations, decision which implementation is the right one was brought much time earlier using simulation in ML Designer while respecting the real time influences and conditions.

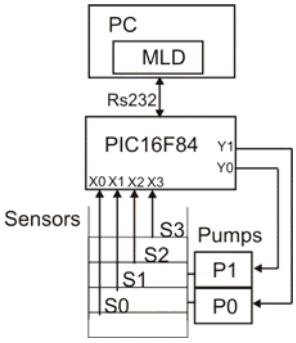

Fig. 5. Block diagram of a HILS

Sensors and actuators, modeled previously in MLD, were replaced by real hardware, shown in Fig. 6. The main part of the system – the control unit was left implemented in MLD. In the real-time simulation, MLD program running on PC receives information from external sensors and transmits commands to pumps. The PIC microcontroller is used as interconnection between PC, and the sensors and pumps on the other side. PIC receives the commands from MLD, and then turn on or off pumps. Also, it gives back to MLD the measurement results for further processing. For the communication between ML Designer and PIC controller, RS232 serial communication was used.

Fig. 6. Sensors and pumps

The system functioning is described as follows: PIC controller periodically (period time can be set to 25ms for example) determines state of sensors X0 to X3 (shown in Fig.1). After it sends this information to MLD program using its RS232 routines implemented in Assembler. FSM in ML Designer receives sensor's information and gives the appropriate respond on its outputs. After that, this respond, in form of a command, is sent back to PIC controller which turns on or off the pumps.

B. Communication module implemented in MLD

The RS232 communication module was implemented in MLD in Discrete Event domain. It was written in Ptolemy language as a primitive called comRS232. The module provides C++ routines for opening the communication port, setting important parameters including baud rate and parity, reading data from the serial port and writing data to the port.

The developed module sends and receives string data packets over RS232 serial communication. It has following input and output ports: inputs OpenPort, Read, PsOutput and outputs Displa**y** and PsResponse as is shown in Fig. 7.

Any float type data particle that comes on OpenPort opens the serial port and enables the RS232 communication..

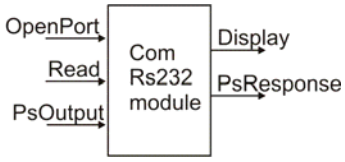

Fig. 7. Interface of the module for RS232 communication

Reading operation: port Read is used to set the comRS232 into reading mode. After some non-zero float type particle comes on Read, module comRS232 will wait for the incoming new characters. Wait state will remain active until at least one character is read. When characters get received they appear in form of string on psResponse output.

While writing operation, string type data packets coming on psOutput port are transferred over RS232. The output port Display is used for displaying all necessary information like which port is open, what are the speed rate, the number of bits in data packets, parity and other RS232 parameters. Also, Display shows the characters that have been received or sent.

The communication module comRS232 has three parameters: sPortNumber**,** BaudRate and Config. The first parameter, sPortNumber**,** defines the number of serial port over which the communication is established. Since MLD program is running under Linux, default value of parameter sPortNumber, 0, opens the port /dev/ttyS0. If the value of sPortNumber is 1, the other port, /dev/ttyS1, is opened.

The BaudRate, parameter with integer type, has default value of 9600. It represents the speed of the serial data steam as a number of ones and zeroes that can be sent in one second. It can have one of following values: 110, 300, 1200, 2400, 4800, 9600, 19200, 38400.

The third parameter called Config determines the parity and number of bits in data packets. It has one of the following string values: 8N1, 7N1, 7O1 and 7E1.

C. Part of a HIL system realized in MLD

Beside previously explained comRS232 module the software part of a HIL system consists of several other modules: Slave, FSM and Text displays Received Message, Sent Message, and Display as shown in Fig. 8.

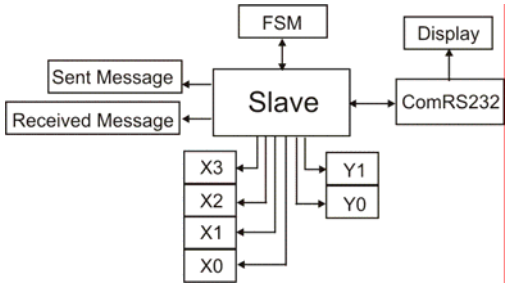

Fig. 8: Block diagram of a part of a system implemented in MLD

The system's functioning is described as follows: the Slave module periodically receives 8-bit sensor's data from comRS232. When received, it is shown on Received Message display (shown in Fig. 8). After, FSM calculates new pump's states and sends it back over comRS232 module to PIC microcontroller.

The Slave module's input and output ports are shown on Fig. 9. The Slave module receives new sensor's status on its psResponse input (shown on Fig. 9). Since received data is 8-bit character and FSM gets on its input integer value in range from 0 to 1000 (representing fluid level in the pool), received input data has to be transformed. Slave module can send the FSM module over its Water Level port one of following values: 100, 300, 500, 700 or 900.

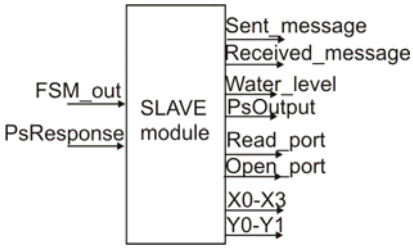

Fig. 9. Interface of the SLAVE module

If sensors are not active, Slave sends to FSM the minimal value 100. If only the lowest sensor X0 is active, then sends number 300; if X0 and X1 are active - number 500; when X0, X1 and X2 are active – 700; and finally, when fluid level is over all the four sensor, number that FSM module receives from Slave module is 900. Also, after receiving new sensor's value, Slave produces received information on output ports **X0** to **X3** to be further displayed on TclTk Show Values displays.

After new pump states Y1 and Y0 are determined (within FSM), Slave module receives this information on its FSM_out input and generates new command to be sent over psOutput port to comRS232. Also, this command is sent to Sent Message TclTk display (shown on Fig. 8). Finally, new float type particle is generated on Read output requesting information from comRS232.

D. Circuit interconnecting PC, sensors and pumps

The circuit interface between PC on one side, and sensors and actuators on the other, is shown in the diagram Fig.10.

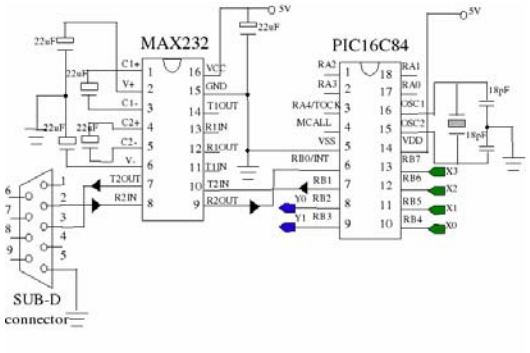

Fig. 10. Connection between PC, sensors and pumps

As it can be seen, sensors X0 to X3 are connected to PIC16C84 PortB pins RB4 to RB7 respectively which had to be configured as input pins in a assembler program code. PortB pins RB3 and RB2 control fluid pump and are connected to inputs Y1 and Y0 respectively.

To connect a microcontroller to a serial port on a PC computer, the level of the signals had to be adjusted. The signal level on a PC is -10V for logic zero, and +10V for logic one. Since the signal level on the microcontroller is +5V for logic one and 0V for logic zero, we need an intermediary stage that will convert the levels. One chip specially designed for this task is MAX232. This chip receives signals from -10 to +10V and converts them into 0 and 5V (and vice versa).

For receiving data from PC, pin 2 of Sub-D connector (called RX) is connected to input pin 8 of MAX232 (R2IN). Then, output pin 9 of MAX232 (R2OUT) is then connected to pin 6 of PIC16C84 (RB0/INT) which is configured in assembler code as a input port.

For sending data to PC, pin7 of PIC16C84 (pin RB1) was chosen. This pin is connected then to pin 10 of MAX232 (pin T2IN). MAX232 output pin for transmitting serial data, pin 7 (T2OUT) is then connected to pin 3 of Sub-D connector (called TX).

As it can be seen on Fig.10, of all input and output ports of used PIC16C84, only PortB is used (for sensor acquisition, pump managing, data sending and receiving data over RS232). PortA was not used and it is left unconnected.

IV. Conclusion

This paper presents research results after praxis at University in Ilmenau. First, the module for RS232 communication was developed in MLD. After, communication module was used in the example of Hardware-In-the-Loop simulation. The system with sensors and pumps was developed. First, whole system was described in MLD and after sensors and pumps models were replaced with real hardware. For interconnection between sensors, pumps and MLD program, PIC microcontroller is used. It receives signals form sensors and sends sensor status over RS232 communication to the MLD program. Finite State Machine in MLD generates the new pumps states and over RS232 sends back new commands to PIC microcontroller which turns on and off the pumps.

References

[1] V. Zerbe, "Mission Level Design of Complex Autonomous Systems", in *Proc. XLVII ETRAN Conference*, Herceg Novi (Montenegro), 2003, pp. 55-59

[2] M. Jevtić, V. Zerbe, S. Brankov, "Multilevel Validation of Online Monitor for Hard Real-Time Systems", *IEEE 24th Conference on Microelectronics* (*MIEL 2004*), (accepted)

[3] http://www.mldesigner.com

[4] MLDesigner Documentation, version 2.4, 2003.

[5] V. Zerbe, "Systematischer Entwurf paralleler digitaler Systeme", in *Proc. Workshop Boolesche Probleme,* Freiberg (Germany), 07. Oct. 1994, pp.73-79

Implementation of the Component Characteristic Curve Tracer Using PC-based Acquisition Card

Marko Dimitrijević and Vančo Litovski

Abstract – The component characteristic curve tracer consists of hardware and software parts. Hardware part is a PC-based acquisition card mounted in standard personal computer. Software part is developed in National Instruments LABVIEW package. The tracer can be used for educational purposes, as well as in science purposes, for testing semiconductor or any other nonlinear electronic component.

Keywords - The component characteristic curve tracer, PC-based acquisition card.

I. INTRODUCTION

Computer based acquisition instruments followed development in personal computer industry. There are several types of acquisition equipment from various vendors. Most new implementations of legacy instruments like oscilloscopes, AVΩ-meters and spectrum analysers have interface for connection with computer and software for data acquisition and manipulation. New types of stand-alone instruments and measurement equipment are embedded systems with adapted operating systems and acquisition software.

Measurement equipment based on computer hardware is realised as PCI card for desktop or rack-mounted computers or PCMCIA acquisition card for portable or PDA computers. The acquisition card needs device driver for operating system that runs on host machine and application software which provides data acquisition and manipulation.

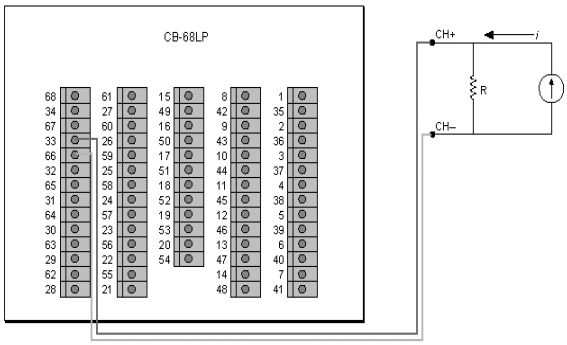

Fig. 1. CB-68LP connection block

The component characteristic curve tracer is implemented using *National Instruments NIDAQ PCI-6014* acquisition card [1]. This card has 16 analog inputs with 200kS/s sampling rate, two analog outputs with 10kS/s sampling rate, 8 digital I/O channels and two 24-bit counters. PCI-6014 is PCI based acquisition card. External signals or devices under testing can be connected with acquisition card using CB-68LP block panel (figure 1) and SH68-68-EP cable.

Software part is developed in LABVIEW package. LABVIEW provides intuitive developing interface with possibility of developing GUI applications. *National Instruments* provides other development platforms such as *Measurement Studio* for Microsoft Visual Studio, and ANSI compatible LABWINDOWS. The operating system driver is common for all developing packages. It provides basic application interfaces, and elementary functions for configuring acquisition card.

II. HARDWARE

The analog outputs are used as DC voltage generators for power supply and stimulus voltage. Maximal DC output voltage is limited to ±10V. This voltage is adequate for power supply, polarisation and measurement of static characteristics of the semiconductor components (figure 2).

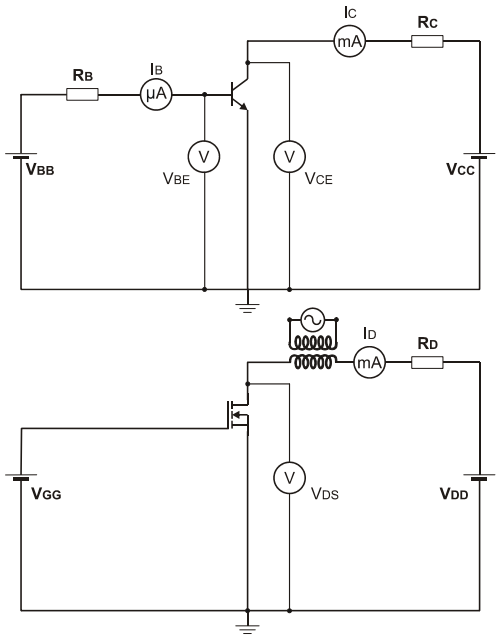

Fig. 2. Circuits for BJT and MOSFET characteristic measurement

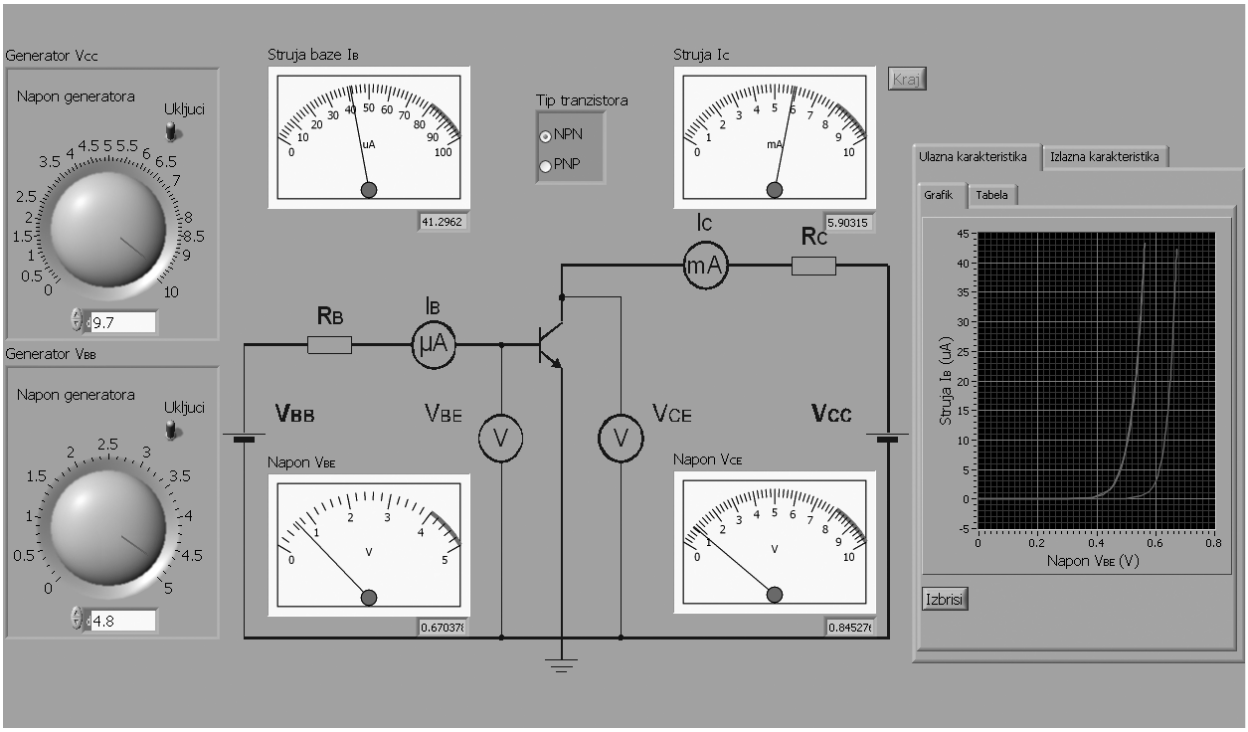

Fig. 3. User interface – measurement of BJT input characteristic

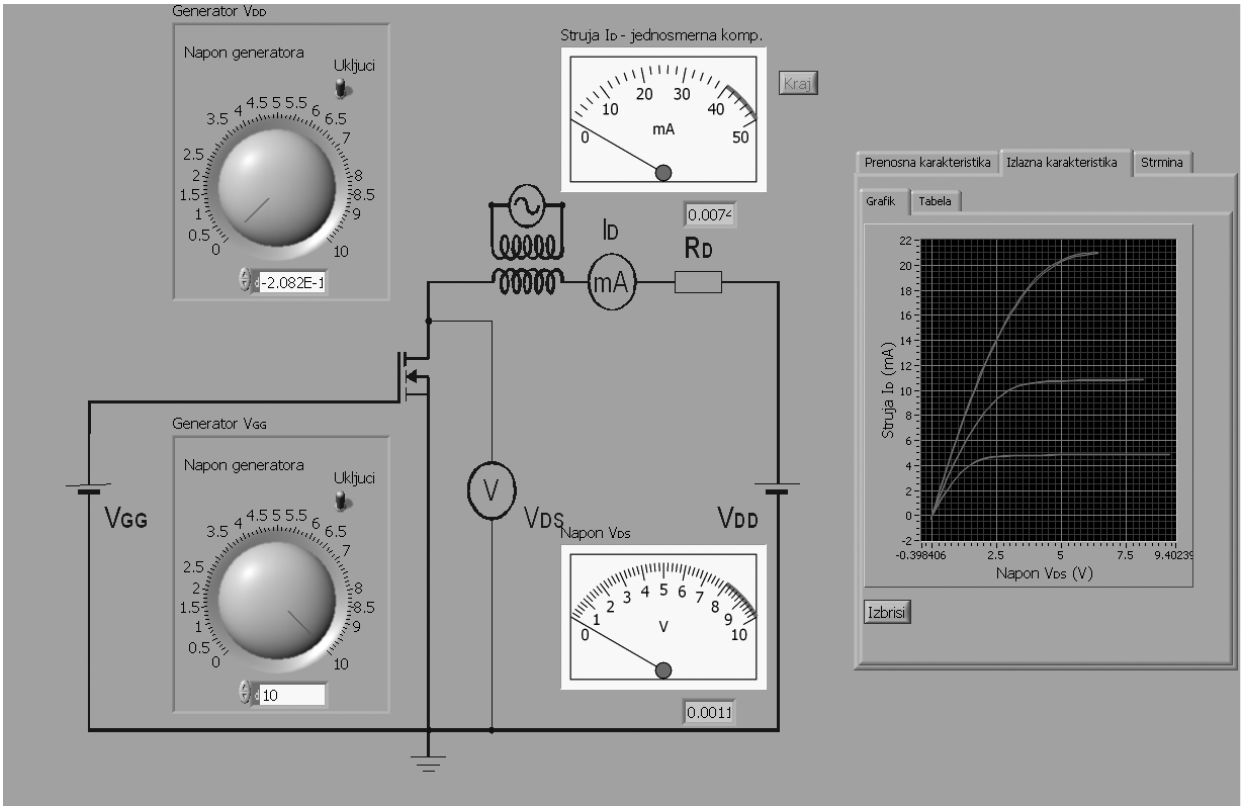

Fig. 4. User interface – measurement of MOSFET output characteristic

The analog inputs can be connected using NRSE – non-referenced single-ended, RSE – referenced single-ended and differential measurement method. Differential method is used in implementation of the characteristic curve tracer, in order to decrease noise and increase the CMRR. This noise influences to measurement precision of small current and voltage values, such as saturation current of the germanium diode. Both of the connection points of a differential system are tied to instrumentation amplifier. There are no terminals connected to a fixed reference. With differential method, the number of analog inputs is limited to 8. In order to increase CMRR, a resistor can be connected between inverted input of instrumentation amplifier and ground. The resistance must have value of hundred equivalent Thevenin's resistance

between connection points (inverted and non-inverted terminal of instrumentation amplifier). It is also possible to connect the second resistor between non-inverted terminal and ground. This configuration provides greater CMRR, but there is a systematic error in measurement caused by serial connection of resistors.

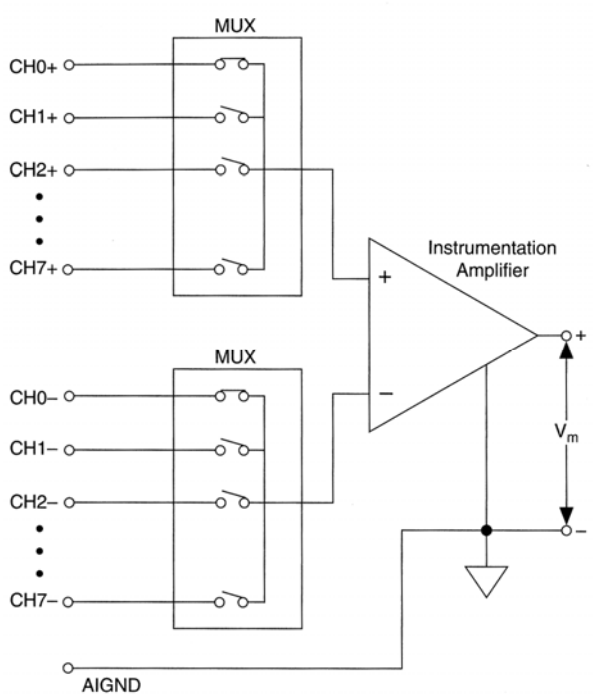

Fig. 5. Differential measurement method

The measurement of voltages can be performed directly. Maximum input voltage is limited to ±10V. The measurement of currents can be performed only indirectly, by transforming current into voltage using parallel resistor. In this implementation we used 100Ω, 1% tolerance metal-film resistor, due to better precision of measurement. Consequently, the value of 1mA is equivalent to 0.1V. The value calculation is performed as software function.

III. SOFTWARE

Software part of the characteristic curve tracer is realized in National Instruments LABVIEW developing package, which provides simple realization of virtual instruments. Virtual instruments consist of interface to acquisition card and application with graphic user interface.

Interface to acquisition card is realized as device driver. PCI 6013/6014 cards are supported by *Traditional* NI-DAQ and NI-DAQmx drivers. All the measurements are performed using *virtual channels*. A virtual channel is collection of property settings that can include name, a physical channel, input terminal connections, the type of measurement or generation, and scaling information. A physical channel is a terminal or pin at which an analog signal can be measured or generated. Virtual channels can be configured globally at the operating system level, or using application interface in the program. Every physical channel on a device has a unique name.

When using NI-DAQmx drivers, a number of similar virtual channels can be aggregated into a *task*. A task is a collection of one or more virtual channels with the same timing, triggering, and other properties. A task represents a measurement or generation process. As well as virtual channels, tasks can be configured globally at the system level, as well as using application interface.

The user interface (figure 3 and figure 4) of the component characteristic curve tracer consists of visual controls and indicators. It provides basic functions for measurement. Visual controls – knobs and switches – provide control of analog signal generation. The indicators – gauges and graphs – show measured values. All measured values are placed in a table, and after the measurement process in appropriate file. User interface also provides controls for data manipulation and saving measured values.

For better performance, the main application has been separated in two threads. The first thread has functions for file manipulation and saving measured values (figure 6). All measured values will be saved in HTML file format.

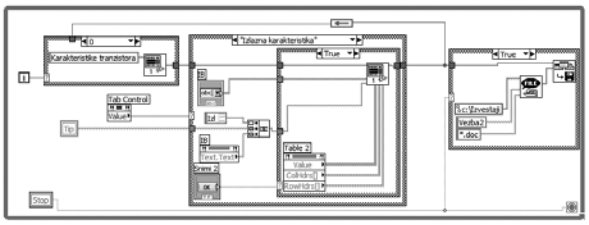

Fig. 6. Data manipulation and saving thread

Main thread (figure 7) performs the measurement process. It is a connection between user interface and low level device driver which controls acquisition card. Processes of signal generation and acquisition are controlled by DAQ Assistant. Main thread also includes

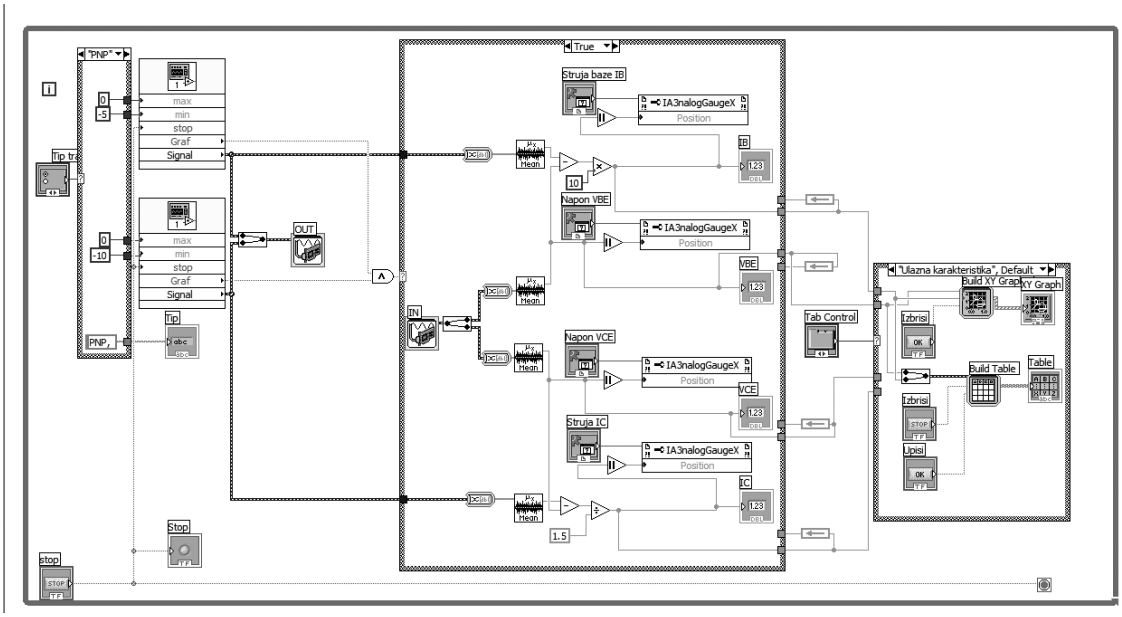

Fig. 7. Main thread

functions for signal manipulations, range calculations, calculations of measured current, building data table and characteristic graphs.

IV. Conclusion

The component characteristic curve tracer has educational purpose. It is a part of computer system for laboratory exercises in Electronics [2 and 3]. The main goal of this system is to simplify manipulation of instruments, faster measurement and notation of the results, providing students to concentrate on measurement essence.

This system can also be used in science purposes for characteristics measurement of low-power semiconductor electronic components.

References

[1] *National Instruments PCI 6014* Product Data Sheet, http://ni.com.

[2] Dimitrijević M., Litovski V., Jovanović S., „Računarski sistem za izvođenje laboratorijskih vežbi iz Elektronike“, V simpozijum Industrijska Elektronika Indel 2004, Banja Luka, 11-12 novembar 2004, pp.156-160.

[3] Litovski V., Petković P., Milenković S., Milovanović D., Glozić D., Mrčarica Ž., Maksimović D., Ranđelović Z., „Praktikum laboratorijskih vežbi iz Elektronike I“, šesto izdanje, Elektronski fakultet Niš, 1998.

Performance Simulation of Ultra-Short (10nm) NMOSTs with Dual-Gate and Lightly Doped Source/Drain

Nebojša D. Janković, Alastair G. Armstrong

Abstract - In this paper, the operation and performance of 10nm Dual Gate (DG) NMOST with lightly doped drain/source (LDDS) regions is investigated in details by means of two-dimensional numerical device simulations. It is found that 10nm LDDS DG NMOST on 20nm "thick" Si film can be optimised to yield superior DC characteristics compared to the identical conventionally designed device requiring an ultra-thin 3nm Si layers. The trade-off is lower maximum cut-off frequency of LDDS device mainly due to the enhanced gate overlapping capacitances.

Keywords – Dual-Gate, NMOST, SOI.

I. INTRODUCTION

According to the 2002 International Technology Roadmap for Semiconductors (ITRS) [1], CMOS technology with channel lengths approaching 10nm will be of primary importance for electronics after 2010. SOI MOSFETs with ultra-thin fully depleted silicon layers are regarded as the most promising option for rigorously scaled CMOS transistors [2,3]. In particular, because of their superior immunity to short-channel effects (SCEs), double-gate (DG) SOI MOSFETs with intrinsic doped channels and mid-gap metal electrodes [2-5] become mainstream candidates for future SOI CMOS technology. According to DG device scaling theory [6],[7], an optimised 10 nm DGNMOST with good control of SCEs including low drain induced barrier lowering (DIBL) parameter and near-ideal sub-threshold swing (S), requires an extremely thin Si layer in the range 3 - 5 nm and a gate oxide in the range 0.5 -1.5 nm. While future uses of high-k dielectrics straightforwardly alleviate gate oxide tunnelling problems [8], there is not an easy solution to high source/drain (S/D) sheet resistance inherent to ultra-thin 3nm Si films. Traditional methods of decreasing S/D resistance involve silicidation [9] and/or thickening of S/D regions after spacer formation [10]. Both methods, however, will contribute considerably to SOI CMOS complexity, which, in conjunction with difficulties in fabricating uniform ultra-thin SOI films, represent the challenging tasks for process engineers.

Apart from technology issues, the excessive thinning of Si films bellow 10nm thickness also brings some fundamental physical drawbacks such as the degradation of carrier mobility [11,12] and/or the increase of band-to-band tunnelling leakage currents [13]. Consequently, obtaining high performance fully depleted DG MOSTs on relatively "thick" SOI films would be favourable from device physics, as well as from a device fabrication points of view.

In that respect, a possible approach in avoiding the need for ultra-thin SOI films for future 10nm DG MOSFETs could be the implementation of lightly doped drain/source (LDDS) design. Owning to the presence of drain extension, it is intuitively clear that the LDDS DG NMOS devices would exhibit smaller SCEs for any given Si layer thickness in comparison with identical conventional highly-doped S/D devices. However, beside the beneficial influence on mitigating SCEs, the LDDS device exhibits some well-known drawbacks compared to its conventional counterpart with highly-doped S/D designs. It includes higher total S/D resistances and enhanced overlapping Miller capacitance, which can degrade to some extent device output drive currents and limit maximum operational frequencies. Hence, it is important to evaluate a net effect that the LDDS concept would have on the electrical characteristics when applied to fully depleted DG NMOST devices.

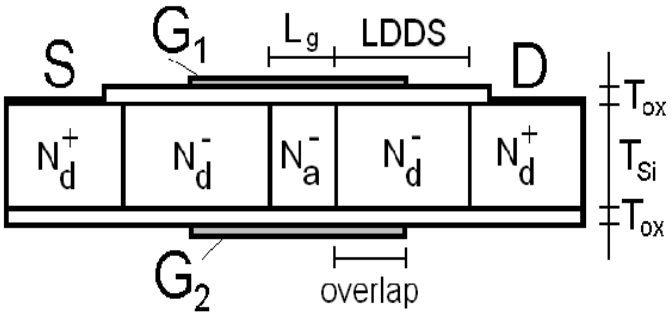

Fig. 1. Cross-section of simulated DG NMOST with LDDS regions.

In this paper, the potential performances of a 10nm LDDS DG NMOST on "thick" 20nm Si films is investigated in detail by means of two-dimensional numerical device simulations. The D.C. and A.C. parameters of optimised LDDS device on 20nm are extracted from simulated output characteristics and their values compared with the parameters of identical conventionally designed 10nm device on a 3nm Si film. It is worthwhile to point out that, to the best of our knowledge, the implication of LDDS concept in SOI MOSFETs has been analysed so far only with respect to single-gate (SG) SOI devices [14-16].

II. THE DG NMOST STRUCTURE

Fig.1 shows the LDDS DG NMOST structure with geometry parameters Lg, Tox, TSi, LDDS and OVERLAP. For convenience, the units of OVERLAP are given in % of LDDS parameter . An ideal DG NMOSTs with L_g = 10 nm, T_{Si} = 20nm T_{ox}= 1.5nm, $N_d^+ = 10^{20}$ cm^{-3}, $N_d^- = 10^{14}$ cm^{-3} and gates with work functions Φ_{ms} = 4.55V is assumed in 2D numerical simulations. The parameters N_d^- , LDDS and OVERLAP are varied within the ranges of 10^{15} cm^{-3} - 10^{18}cm^{-3} , 0 - 50nm and 0 – 100 %, respectively. The length of N_d^+ region of 50 nm with ideal 40nm long S/D metal contacts placed on top of N_d^+ regions are also assumed. Note that, in simulations, a conventional DG NMOST structure is obtained as a special case of LDDS device by putting LDDS = 50nm, OVERLAP = 0, and =1020cm3 .

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III. SIMULATION METHOD

A drain current of 10nm DG NMOST is mainly determined by near-ballistic carrier transport along the channel [18]. Recently, Granzner et al [19] have obtained excellent agreement between transfer characteristics of DG MOSFETs with Lg scaled down to 10nm simulated with DD and Monte-Carlo models. It was achieved by modifying ATLAS default parameters beta and vsat.n of Caughey-Thomas high field mobility model [20] as:

$$vsat.n = \frac{1.5 \cdot L_g + 21.6}{L_g + 2.7} \cdot 10^7 \left(\frac{cm}{\sec} \right), beta = 1 \qquad (1)$$

where Lg is in nm. Following Grazner et al [19] method, we also employed Fermi-Dirac statistics, Klaassen unified mobility model, Shockley-Read-Hall recombination and Lombardi et al. [21] transverse field mobility model. Some of the reasons laying behind the success of Granzer's empirical simulation method can be found in [18],[19]. It is worth pointing out, however, that the employed mobility models can realistically describe carrier transport in the low-doped and narrow LDDS regions. In this case, the electron mobility of LDDS regions has similar field dependence to that of the inversion layer, since carrier concentration of the accumulated layers greatly exceeds and the Coulombic scattering dominates mobility. The effective electron mobility degradation with Si film thinning (found to occur for T_{Si} < 20nm [11],[12]), was not modelled in our simulations bearing in mind recently described counter effect of volume inversion [22]. The band-to-band and source barrier quantum tunnelling effects can be neglected in present analysis, since they contribute less then a few percent to I_{off} in 10nm DG MOSFETs, as shown in [13], [23] and [24].

For proper prediction of drain current of 10nm DG NMOSTs on thin Si layers, we must also include the influence of quantum effects (QEs) [22-27]. In order to quantify QEs in DG NMOSTs , we have simulated low-frequency C-V curves of DG SOI capacitor on 3 nm and 20 nm p-type Si layers using the one-dimensional Schrodinger-Poisson self-consistent numerical solver SCHRED [25]. Results are shown in Fig.2.

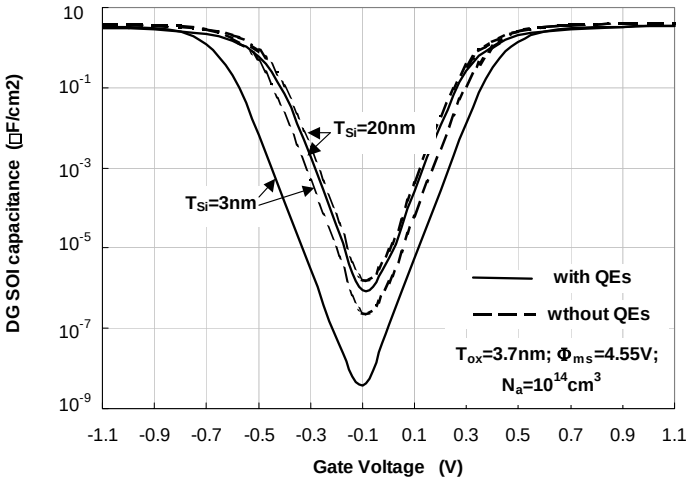

Fig.2 Low-frequency capacitance versus gate voltage of DG SOI capacitor on 20nm and 3 nm p-type Si films, simulated with and without quantum effects (QEs) by 1D Poasson-Schredinger solver SCHRED [25]

Beside the extremely low minimum capacitance value of thin silicon DG SOI capacitors, Fig.2 also shows a substantial positive parallel shift of 3nm C-V curve in the inversion region due to the influence of QEs. It implies that QEs can be approximately incorporated in DD modelling by the effective enhancement of flat-band parameter Φ_{ms} . It actually represents the effective quantum increase of V_t that has already been observed in previous studies of ultra-thin SOI devices [27]. Results in Fig.2 clearly show that the same quantum shift is much less in case of 20nm Si layer device. Consequently, as the first order approximation, the influence of QEs can be neglected in DD simulations of DG NMOST with TSi=20nm.

The validity of our DD modelling approach is illustrated in Fig.3. It shows comparison between transfer characteristics of a conventional 10nm DG NMOST on 3nm Si film simulated with our ATLAS DD modified model and NanoMOS2.5 [26] programs. The latter employs a self-consistent quantum-ballistic (QB) model solving the carrier ballistic transport with quantum corrections [26]. A good agreement between DD and QB modelling was achieved with parameters Φ_{ms} = 4.75V and beta = 1, vsat.n= 2.8x107 cm/s (calculated from eq.(1)) in the DD model and Φ_{ms} = 4.55V in the QB model. A 200mV difference of representing V_t quantum enhancement is larger than the one observed in Fig.2, probably due to the influence of two-dimensional effects encompased by NanoMOS2.5 [26].

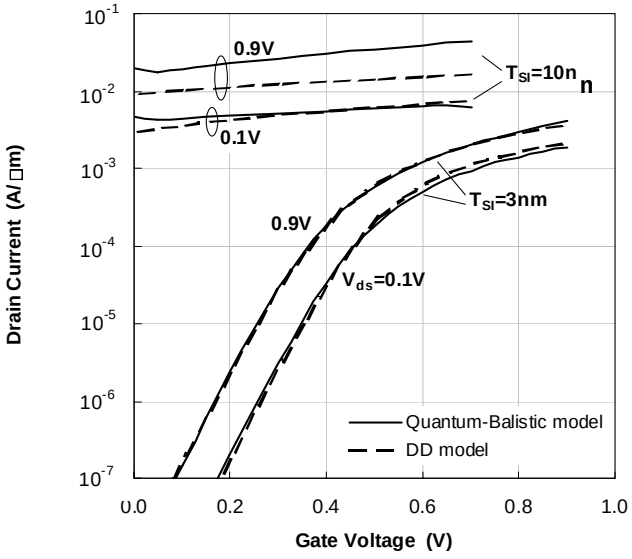

Fig.3 Transfer characteristics of a conventional 10nm DG NMOSTs on 3nm and 10nm Si films simulated by ATLAS Drift-Diffusion [17] and NanoMOS2.5 [26] Quantum-Ballistic programs

The simulated transfer characteristics of identical DG NMOST on 10nm Si layer are also shown in Fig.3. Both DD and QB models yield degraded transfer characteristics, indicating that severe SCEs already dominate device performance. A good fit between DD and QB results is obtained for V_{ds}=0.1V using Φ_{ms}=4.67V in DD modelling. A notable difference occurs at high drain currents (Vds=0.9V) because of the increased influence of finite S/D parasitic resistances that are inherently included in ATLAS 2D

simulations [17], but assumed zero in NanoMOS2.5 program [26]. Degraded transfer characteristics clearly confirm the need for the implementation of the LDDS concept in order to obtain useful electrical characteristics of 10 nm DG NMOSTs on "thicker" Si films.

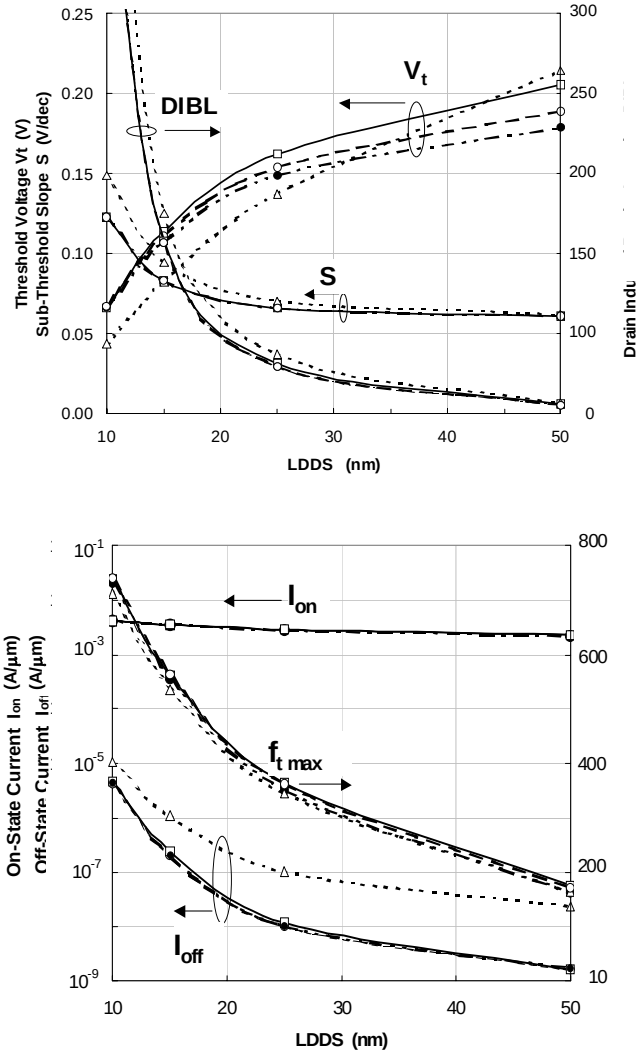

Fig.4 The DC and AC parameters of 10nm DG NMOSTs with T_{Si}=20nm and OVERLAP=100% versus the *LDDS* parameter for N_d^- = 10^{15}cm^{-3} (●); 10^{16}cm^{-3} (○); 10^{17}cm (□); 10^{18}cm^{-3} (△)

IV. LDDS DESIGN OPTIMISATION

The sensitivity of device electrical characteristics on-state drive current I_{on} , off-state leakage current I_{off} , drain induced barrier-lowering DIBL, sub-threshold slope *S* , threshold voltage V_t and maximum cut-off frequency f_t on the variation of LDDS, OVERLAP and N_d^- parameters are shown in Fig.4 and Fig.5. Note that, in order to avoid the influence of high S/D resistance, V_t is defined at the point of maximum slope of I_{ds}-V_{gs} curve following standard method of Yang and Li [28] . The $f_{t.max}$ parameter represents maximum value of unity gain cut-off frequency f_t found from ATLAS AC simulations over the bias range 0.2 <V_{gs} < 1 and V_{ds} = 1V. Fig.4.a shows that DIBL, S, V_t

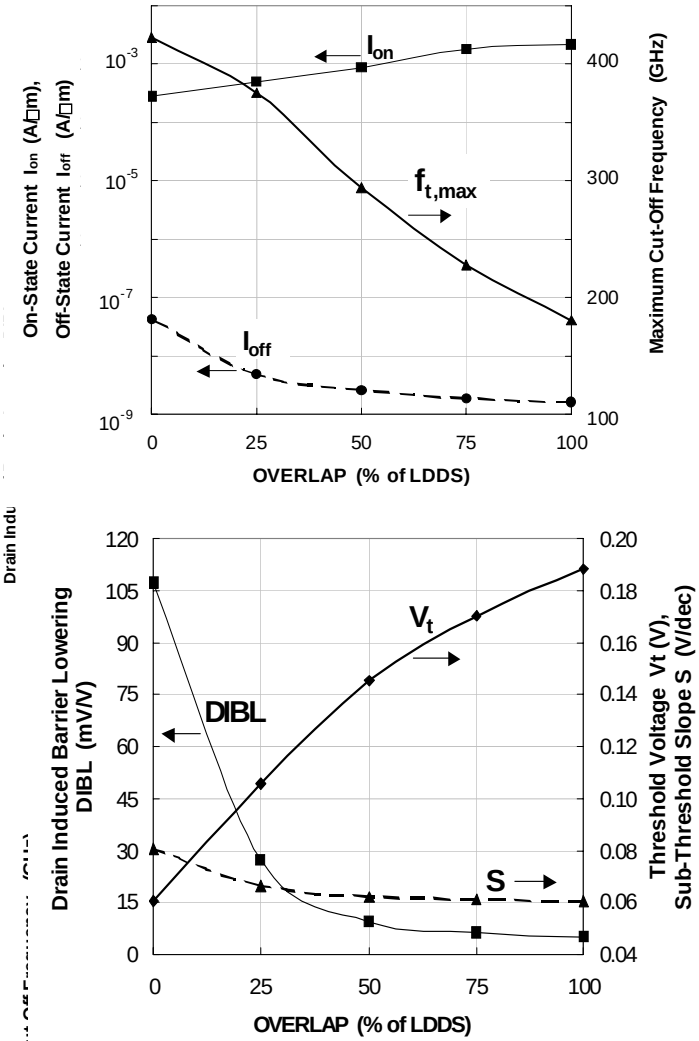

Fig.5 The DC and AC parameters of 10nm DG NMOST with T_{Si}=20nm, LDDS=50nm and N_d = 10^{16}cm^{-3} versus the *OVERLAP* parameter.

and I_{off} strongly improve with increasing LDDS, whereas I_{on} exhibits a slight degradation. These improvements are offset by a three fold decrease of $f_{t.max}$ when keeping OVERLAP =100%. As for the influence of N_d^-, simulations yields a weak sensitivity of all parameters up to N_d^- =10^{18}cm^{-3} , except I_{off} exhibiting a sharp increase for N_d^- >10^{17}cm^{-3}. Hence, N_d^- =10^{17}cm^{-3} represents the upper limit of LDDS doping for achieving low-leakage midgap metal DG NMOST on 20 nm Si film. The influence of variation in OVERLAP is illustrated separately in Fig.5 by maintaining LDDS = 50nm and N_d^- = 10^{16}cm^{-3}.

A better insight into the beneficial influence of OVERLAP parameter on overall SCEs is given in Fig.6. It shows 2-D distributions of electron current density simulated at Vgs = Vds = 1V for three OVERLAP values e.g. 0%, 50% and 100%. As can be noticed, the peak current density is always confined to the gate edge overlapping the drain as well as to the middle of Si film due to the dual-gate symmetry. Bearing in mind that the spatial position of peak current density must coincide with the position of maximum electric field, the

increase of OVERLAP parameter actually moves the peak field away from the channel region within the drain depletion region. It in turn decreases the longitudinal potential gradient in the channel yielding smaller SCEs and better DC parameter ratings. Unlike the increase of LDDS degrading I_{on}, the increase of OVERLAP improves ***all*** DC parameters (including I_{on}). It widens the N_d^- depletion region at the expense of the LDD ohmic area, which in turn decreases drain ohmic resistance. However, although the increase of OVERLAP improves D.C. characteristics, it also increases the input gate capacitances, degrading $f_{t.max}$. It is confirmed in Fig.5.b showing that the increase of OVERLAP from 0% to 100% for constant LDDS yields approximately a two-fold decrease of $f_{t.max}$.

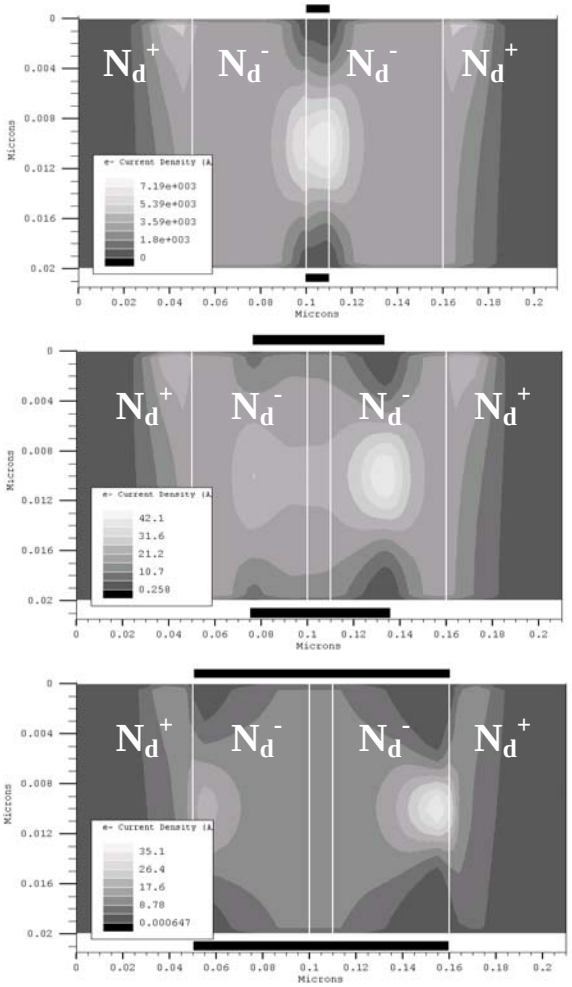

Fig.6 Electron current density distribution in 10nm LDDS DG NMOST on 20nm Si film with parameters LDDS=50nm, N_d^- = $10^{16}cm^{-3}$ and OVERLAP = 0%, 50%, and 100% (from the top).

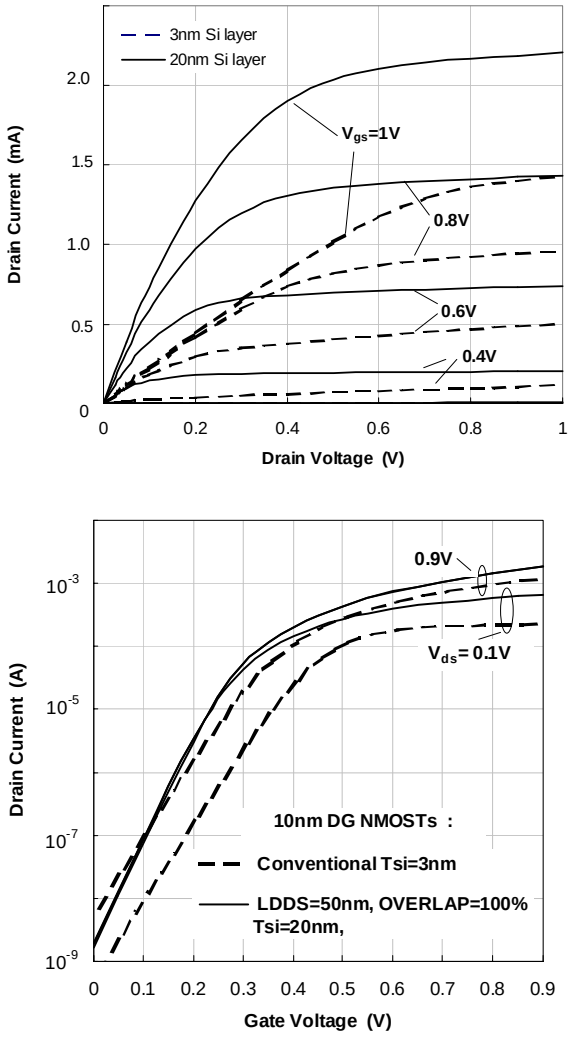

Fig.7 Comparisons between simulated (a) transfer characteristics; and (b) output characteristics of conventional DG NMOST on 3nm Si layer and LDDS DGNMOSTs with *LDDS*=50nm, *OVERLAP*=100% on 20 nm Si film.

V. LDDS VERSUS CONVENTIONAL DESIGN

Comparisons between simulated transfer characteristics and output electrical characteristics of a 10 nm LDDS DG NMOST on 20 nm Si film and a conventional DG NMOST device on a 3nm Si are shown in Fig.7. It clearly shows that an LDDS device on a "thicker" Si film has superior DC characteristics compared with the conventional DG NMOST on ultra-thin Si layer. It can be mainly attributed to smaller total S/D resistances and lower SCEs of LDDS device. However, although LDDS device with OVERLAP>0 exhibits higher transconductance g_m as shown in Fig.6.b, it has also higher gate-drain C_{gd} and gate-source C_{gs} overlapping capacitances then the conventional device design. Bearing in mind that:

$$f_t \approx g_m \cdot \{\ 2\pi(C_{gs} + C_{gb} + C_{gd})\ \}^{-1} \qquad (2)$$

there is obviously a room for LDDS device design optimisation. Table 1 shows a comparison of DC and AC parameters extracted for two conventional devices with two different gate lengths and Si layers as well as for two LDDS

devices with optimised LDDS design parameters. The LDDS device in column 3 is optimised for low-speed, but with DC performance superior to the conventional device in column 2. The second LDDS device example in column 4 is optimised for high speed, but with moderate output drive current I_{on}. Its $f_{t.max}$ parameter is about three times smaller then the maximum frequency of conventional device in column 2, mainly due to the increased input gate capacitance. The 75nm gate device in column 1 is shown to illustrate a minimal gate length of conventional device on 20nm Si that can still maintain D.C parameters comparable to that of 10nm gate LDDS device. It has, however, much smaller $f_{t.max}$ in comparison with optimised high-speed LDDS device shown in column 4. Note that high theoretical $f_{t.max}$ of the intrinsic device predicted in this study is likely to be limited in practice, as our simulation ignores the effects of extrinsic device areas and external parasitics, such as the contact resistances and the interconnect capacitances.

TABLE I
THE DC AND AC PARAMETERS OF CONVENTIONAL AND LDDS DG NMOST STRUCTURES EXTRACTED BY 2-D SIMULATIONS

	Conv. Lg=75nm T_{Si}=20nm	Conv. Lg=10nm T_{Si}=3nm	LDDS Lg=10nm, T_{Si}=20nm LDDS=50nm OVERLAP=90%	LDDS Lg=10nm, T_{Si}=20nm LDDS=40nm OVERLAP=33%
I_{off} (nA/um) (V_{ds} = 0.1V)	3	0.5	1.6	7.7
I_{on} (mA/um) (V_{ds} = 0.1V) (V_{ds} = 1V)	0.53 1.74	0.23 1.4	0.73 2.20	0.16 0.78
$V_{t(low)}$ (V) @V_{ds} = 0.1V	0.16	0.29	0.19	0.12
DIBL(mV/V) (ΔV_{ds} = 0.9V	12	102	5.2	28
S (mV/dec)	62	78	61	66
f_t max (GHz)	194	1399	200	470

VI. CONCLUSIONS

Based on two-dimensional numerical simulations with calibrated device simulator, it is found that 10nm DG NMOSTs on 20nm Si film with lightly-doped drain/source (LDDS) design can be optimised to yield superior DC parameters compared to the identical conventionally designed devices requiring an ultra-thin 3nm Si films. The trade-off is lower maximum cut-off frequency of LDDS devices mainly due to the enhanced gate overlapping capacitances. By subtle control of the degree of overlap of the gate electrode, LDDS DG NMOSTs can be optimised for either low power or high frequency performance. Scaling of LDDS devices also allows the utilization of substantially thicker SOI layer compared to scaling-down conventional devices. This particular feature of LDDS design can be advantageous in obtaining reproducible 10nm device characteristics having in mind serious potential problems of fabricating uniform ultra-thin SOI layers down to several nanometres.

REFERENCES

[1] International Technology Roadmap for Semiconductors, 2001 Edition, 2002 Update [Online]. Available: http://public.itrs.net/

[2] H.-S. P. Wong," *Beyond the conventional transistor*", IBM Journal of Research and Development , Vol. 46, No. 2/3, pp. 169-180, 2002

[3] G. K. Celler and S. Cristoloveanu "*Frontiers of silicon-on-insulator* ", Journal of Applied Physics, Vol 93, No 9, pp 4955-4978 (2003)

[4] V. P. Trivedi and J. G. Fossum, "*Scaling fully depleted SOI CMOS"*, IEEE Trans. Elec. Devices, Vol.50, No 50, pp.2095-2103 (2003)

[5] H. Shang, and M. H. White, *An ultra-thin mid-gap gate FDSOI MODFET*, Solid-State Electronics, Vol. 44, pp 1621-1625 (2000)

[6] D.J. Frank, Y. Taur, and H.-S.P. Wong, "*Generalized scale length for two-dimensional effects in MOSFETs"*, IEEE Electron Device Letters, Vol.19 , pp. 385-387, Oct 1998

[7] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, *" Scaling theory for double-gate SOI MOSFET's"*, IEEE Transactions on Electron Devices ,Vol. 40 pp. 2326-2329, 1993

[8] C. M. Osburn, I. Kim, S. K. Han, I. De, K. F. Yee, S. Gannavaram, S. J. Lee, C.-H. Lee, Z. J. Luo, W. Zhu, J. R. Hauser, D.-L. Kwong, G. Lucovsky, T. P. Ma, and M. C. Öztürk, " *Vertically scaled MOSFET gate stacks and junctions: How far are we likely to go?*" IBM Journal of Research and Development , Vol. 46, No. 2/3, 2002 pp. 299-316.

[9] H.I. Liu, J.A. Burns, C.L. Keast, and P.W. Wyatt, *"Thin silicide development for fully-depleted SOI CMOS technology "*, IEEE Transactions on Electron Devices, Vol. 45, No. 5, pp. 1099-1104, May 1998

[10] M. Chan, F. Assaderaghi, S. A. Parke, C. Hu, and P. K. Ko *" Recessed-channel structure for fabricating ultrathin SOI MOSFET with low series resistance"*, IEEE Electron Device Letters, Vol. 15, No.1, pp. 22-24, Jan 1994

[11] F. Gamiz, J.A. Lopez-Villanueva, J. B. Roldan, J. E.Carceller, and P. Cartujo, *"Monte Carlo simulation of electron transport properties in extremely thin SOI MOSFET's*" IEEE Transactions on Electron Devices, Vol. 45, pp.1122-1126, 1998

[12] B. Majkusiak, T. Janik, and J. Walczak, *"Semiconductor thickness effects in the double-gate SOI MOSFET"* IEEE Transactions on Electron Devices, Vol. 45, pp. 1127-1134, 1998

[13] T. Ishiyama and Y. Omura*," Influences of Superficial Si Layer Thickness on Band-to-Band Tunneling Current Characteristics in Ultra-Thin n-Channel Metal-Oxide-Semiconductor Field-Effect-Transistor by Separation by IMplanted Oxygen (nMOSFET/SIMOX)"* Jpn. J. Appl. Phys. Vol.36, Part 2, No.3A, pp. L264-L267 , March 1997

[14] C.-G. Chyau, S.-L. Jang, and C.-J. Sheu ,"*A physics-based short-channel SOI MOSFET model for fully-depleted single drain and LDD devices "*, Solid-State Electronics, Vol 44 pp. 487-499 (2000)

[15] S. Pidin and M. Koyanagi*," Parasitic series resistance extraction and impact ionization current modelling for SOI MOSFETs "*, Microelectronics Journal, Vol. 29,

pp.31-41, 1998

[16] A. S. Nicolett, J. A. Martino, E. Simoen and C. Claeys, *"Extraction of the lightly doped drain concentration of fully depleted SOI NMOSFETs using the back gate bias effect ",* Solid-State Electronics , Vol. 44, No. 4 , pp. 677-684, April 2000,

[17] ATLAS User's Manual-Device Simulation Software: SILVACO International Inc., 2000

[18] K. Banoo and M.S. Lundstrom, *"Electron transport in a model Si transistor",* Solid-State Electronics, Vol 44, pp. 1689-1695 February, 2000)

[19] R. Granzner V.M. Polyakov, F. Schwierz, M. Kittler, and T. Doll, *"On the suitability of DD and HD models for the simulation of nanometer double-gate MOSFETs*", Physica E 19 (2003) 33 – 38.

[20] D.M. Caughey, and R.E. Thomas, *"Carrier mobilities in silicon empirically related to doping and field*", Proc. IEEE 52 (1967) pp. 2192.

[21] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, *" A physically based mobility model for numerical simulations of non-planar devices",* IEEE Trans. Computer-Aided Design, vol.7, pp. 1164-1171, Nov. 1988

[22] L. Ge and J.G. Fossum, *"Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs",* IEEE Transactions on Electron Devices, Vol. 49 , pp.287- 294, 2002

[23] H. Nakajima, S. Yanagi, K. Komiya, and Y. Omura, *"Off-leakage and drive current characteristics of sub-100-nm SOI MOSFETs and impact of quantum tunnel current"* , IEEE Transactions on Electron Devices, Vol. 49, pp. 1775- 1782, 2002

[24] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, and J. Fossum, *"The ballistic nanotransistor: a simulation study"*, Electron Devices Meeting, 2000. IEDM Technical Digest. International , 10-13 . 2000 , pp. 715 -718

[25] D.Vasileska and Z. Ren, SCHRED-2.0 Manual Purdue Univ., West Lafayette, IN, Feb. 2000

[26] Z. Ren, R. Venugopal, S. Goasguen,, S. Datta, and M. S. Lundstrom, *"NanoMOS 2.5: A two-dimensional simulator for quantum transport in double-gate MOSFETs"* , IEEE Trans. on Electron Devices Vol. 50, pp. 1914- 1925, Sept. 2003

[27] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, *" Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs",* IEEE Electron Device Letters, Vol. 14, No. 12, pp. 569-571, Dec 1993

[28] P. C. Yang and Sheng S. Li, *" Analysis of current-voltage characteristics of fully depleted SOI MOSFETs "* Solid-State Electronics, Vol. 36, No 5 , pp.685-692, May 1993

[29] H.-S. P. Wong *et al.*, *"Nanoscale CMOS," Proc. IEEE*, Vol. 87, pp.537–570, Apr. 1999.

[30] D. J. Frank, S. E. Laux, and M. V. Fischetti, *"Monte Carlo simulation of a 30 nm dual-gate MOSFET: How short can Si go?," IEDM Tech. Dig.*, pp. 553–556, 1992

Integrated Power Meter IC Calibration

Milunka Damnjanović, Predrag Petković, Borisav Jovanović

Abstract - Calibration has a big impact on all the other results that Integrated Power Meter IC provides (RMS values of voltage and current, active and reactive power and energy). Calibration hardware within a DSP unit dedicated for an Integrated Power Meter and full calibration procedure are explained in this paper.

Keywords – Calibration of Integrated Power Meter

I. INTRODUCTION

High accuracy Integrated Power Meter IC works at frequency of 4.194 MHz and has four operation modes: reset (RST), initialization (INI), normal operation (NOM) and testing mode (TST). During NOM, with the accuracy less than 0.1% it calculates root mean square values for voltage Vrms and current Irms, mean values for active Pav and reactive power Qav, apparent power S, active Ea and reactive energy Eq, power factor and frequency. It satisfies dynamic range in current channel from 10 mA RMS to 100 A RMS, and voltage up to 300V RMS.

Generally, it is a mixed signal system that consists of analog CMOS blocks and digital signal processing blocks shown in Figure 1. Communication between IC and external micro controller is done through a Communication Serial Port (CSP shown in Fig.1) and allows the user to calibrate various components of a meter including gain, offset and phase errors in the initialization mode and read the measured results in normal operation and testing mode. All registers in the memory are available through CSP.

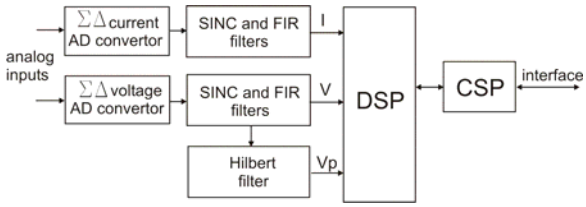

Fig. 1. Block diagram of Integrated Power Meter IC

One programmable energy-to-frequency converter provides pulse response to consumed power. This output allows direct interfacing with an electronic or mechanical counter. By means of a programmable register one can determine the ratio between the active energy and output's pulse frequency. In other words, the meter constant is programmable.

Programmable calibration registers allow compensating gain and offset errors. One can calibrate the Integrated Power Meter by writing appropriate data into the internal registers. The necessary data can be entered via micro controller or any device that provides the clock and data signals.

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II. CALIBRATION HARDWARE AND PROCEDURE

A. DSP's operation

As one can see in Fig. 1, analog current and voltage signals are processed within appropriate sigma-delta modulators. Sampled current signal passes through a third order sigma-delta modulator while voltage signal passes through the second order modulator. Then, decimation of sampled signals from 528.288 kHz to 4.096 kHz is performed within appropriate decimation filters. Besides, Hilbert digital filter produces 90 degrees phase-shifted voltage signal. Data rate of current, voltage and phase-shifted 24 bit digital samples that enter DSP part is exactly 4.096 kHz.

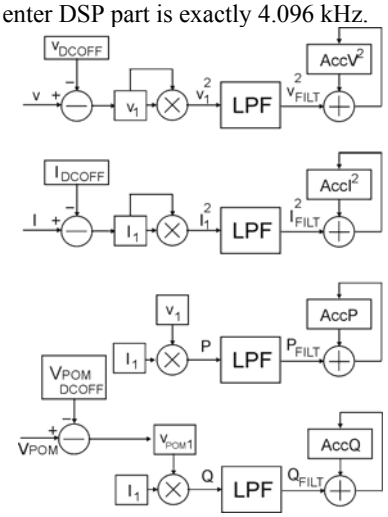

Fig. 2. Data processing chain executing 4096 times in a second

4096 times during 1 second during the normal operation mode, DSP performs following operations: at the beginning of each sequence, 24 bit instantaneous waveform samples of current, voltage and phase-shifted voltage are transferred from Hilbert and decimation filter's outputs, modified with the appropriate DC offset correction and stored into the memory (values I1, V1 and Vp1 shown in Fig.2). After that, instantaneous sample of current is squared in multiplication unit. Then, square is passed thought a single pole Low Pass Filter with a cut-off frequency of 10Hz and then accumulated into a 48-bit register $AccI^2$. LPF details and DSP operation are explained in [1]. The same procedure is repeated with the same hardware for square voltage, active and reactive power integration. The only difference is in operands while multiplying. Data processing chain for integration of current and voltage square, active and reactive power is given in Fig 2.

After every second in NOM, RMS voltage Vrms, current Irms, mean active Pav and reactive power Qav are calculated using accumulated squares of instantaneous current and voltage, accumulated instantaneous active and reactive power during the last second, and this data processing chain is given in Fig.3.

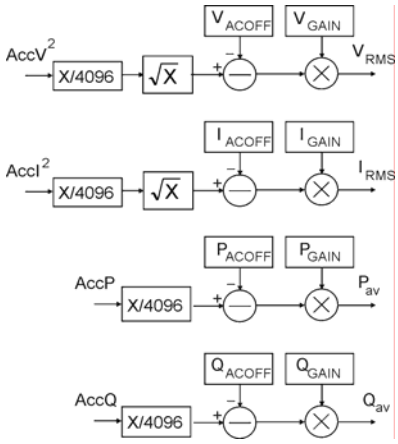

Fig. 3. Data processing chain executing once after every second

The calibration register provides the facility to calibrate and to program the whole metering system. The calibration registers store data needed for the following tasks:

- DC offset calibration of instantaneous current and voltage signals (Idcoff, Vdcoff)
- AC offset calibration for RMS current and voltage signals (Iacoff, Vacoff)
- Calibration of gain error for RMS voltage and current calculation (Igain, Vgain)
- Active and reactive power offset calibration (Pacoff, Qacoff)
- Active and reactive power gain calibration (Pgain, Qgain)

Instantaneous values of current I, voltage V, phase-shifted voltage Vp, root mean square of current Irms, voltage Vrms, average values active Pav, reactive Qav, and apparent power S, and their AC and DC offsets Idcofft, Vdcofft, Iacofft, Vacofft, Pacoff, Qacoff are all represented as 24-bit signed two's complement values with a specific data format given in Figure 4.

Its range is from -1 to 1 and is normalized to appropriate full-scale value. For voltage (V, Vp, Vrms, Vdcoff, Vacoff) full-scale value is $\sqrt{2}$ 300V, for current (I, Irms, Idcoff, Iacoff) is $\sqrt{2}$ 100A, for power (Pav, Qav, S, Pacoff, Qacoff) is 2*100A*300V =60kW.

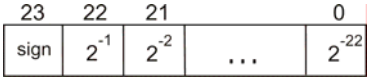

Fig. 4. Data format 1

Gain corection values that should be derived after power meter calibration (Igain, Vgain, Pgain,Qgain), power factor Cos(φ) and power line frequency F are also represented by 24-bit signed two's complement values in range from –2 to 2 and have data format given in Figure 5:

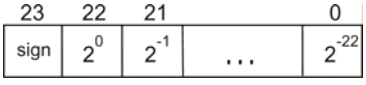

Fig. 5. Data format 2

B. DC offset Calibration

Fig. 6 shows the effect of offsets on active power calculation. As can be seen, an offset of voltage and current will contribute a DC component after multiplication. Since this DC component is extracted by LPF and used to generate the active power information, this offsets will have contributed the constant error to active power calculation. This problem can be easily avoided by introducing the HPF in one of the channels. It is obvious that after multiplication, error terms with AC component cos(wt) will be removed by LPF.

$$(V\cos(\omega t)+Vos)\times(I\cos(\omega t)+Ios)=\frac{VxI}{2}+Vos\times Ios$$
$$+Vos\times I\times\cos(\omega t)+V\times Ios\times\cos(\omega t)+\frac{VxI}{2}\times\cos(2\omega t) \quad (1)$$

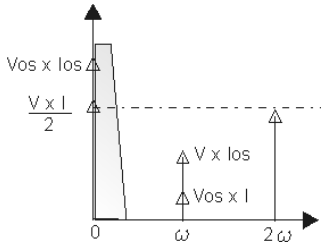

Fig. 6. Effect of channel offsets on the active power calculation

Since Integrated Power Meter is intended to be used for measuring non-sinusoidal signals with significant DC component, as well, the HPF solution for DC offset compensation is rejected. The other way to eliminate the DC offset is using calibration.

DC offset calibration start with shorted inputs that should result with zero values of instantaneous values of voltage V, current I and phase-shifted voltage Vp coming out from decimation filters. Because of offsets, these values are not equal to zero (can be either positive or negative) and are stored into appropriate DC offset registers. If, for example, voltage channel is being calibrated, result of DC offset calibration is stored into VDCOFF register. After calibration, in NOM, instantaneous voltage samples V are subtracted with the content of VDCOFF register (as shown on Fig.2). It has to be mentioned that offset has a big impact on all the other results (RMS values of voltage and current, active and reactive power and energy).

Precision of offset calculation can be improved with repeated offset measurements and accepting the mean value.

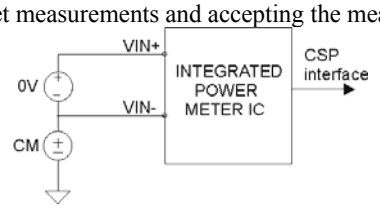

Fig. 7. DC offset calibration setup

Offset calibration setup is shown in Fig.7. The calibration method is as follows:

First, after Power-on Reset, DC offset calibration registers are set to zero by default. After, differential inputs of AD converter are shorted, several instantaneous values of current (or voltage) are read via CSP, their mean value is calculated and stored into appropriate offset register.

C. AC Offset Calibration

AC offset calibration is necessary in order to eliminate the noise from measurement results. Noise can have zero average value but its RMS value can be greater than zero. AC offset calibration is subsequent and similar to DC calibration. In fact one more thing has to be done. According to data processing chain shown on Fig. 3, gain correction value 1.0 has to be stored into gain correction register. The default value of gain correction registers are given in Table 1. Default values for AC and DC offset corrections are set to zero.

Results of calibration - calculated RMS value is stored into appropriate AC offset register and this value can be only positive.

AC Offset calibration setup is same as DC offset calibration setup. Before the measurement start, all correction values should be stored into appropriate registers (AC and DC offset and GAIN). When RMS value is going to be calculated (voltage or current RMS once after every second of NOM), after square-rooting operation is performed, derived product of square rooting operation is subtracted with AC offset value and then, derived result multiplicated with gain correction value (shown on Fig. 3).

D. Gain correction

Despite to offset that has two registers for storing DC and AC correction, every channel has only one gain correction register. It stores the value that affects dynamic range. While the offset calibration assures the transfer function to cross the zero when there is no input signal, the gain correction modifies the transfer function slope.

It can be done in two ways. One method is applying DC signal on AD converter differential inputs. This kind of calibration is called DC gain calibration. The other is AC gain calibration where AC signal has to be applied on ADC's inputs. Independently on the chosen method, maximal allowable input signal should be applied on external ports. Therefore, user can get grater signal range on AD converter output and more precisely determine gain correction value.

The both methods require similar calibration procedure. First, DC and AC offset calibrations have to be performed with gain correction value set to1.0 stored into appropriate gain correction register. Then one should apply the maximal AC or DC signal to inputs. The obtained RMS result is used for gain correction calculation (voltage RMS for voltage and current RMS for current gain correction procedures).

DC gain calibration is performed with maximal DC signal applied on input in order to achieve the Full Scale value. For current gain correction measurement, if DC 250mV signal is applied on inputs, DSP produces Full Scale value (that is stored in Irms register) represented by 24 bit signed number with most significant bit 0 followed by all ones. Full Scale value for current is 100*sqrt(2)= 141.4A. If 250mV DC signal is considered too large and not allowed, calibration can be performed with some smaller signal value. Let x be value of DC signal applied on inputs (represented in mV) and y the value read from RMS Current register and translated in Ampere units. Gain correction can be calculated according to the following formula:

$$Igain = \frac{x}{250mV}\frac{\sqrt{2}\,100A}{y} \qquad (2)$$

For instance, if input signal is x=230mV and the obtained result y=120A, the new gain correction value should be Gain=1.08423039.

For voltage channel the gain correction Full Scale value is 300*sqrt(2)=424.26V represented by 24 bit signed number with most significant bit 0 followed by all ones. If x is DC voltage applied to ADC inputs (represented in mV) and y is the value read from RMS voltage register calculated in V units, then voltage gain correction is calculated according to:

$$Vgain = \frac{x}{250mV}\frac{\sqrt{2}\,300V}{y} \qquad (3)$$

AC gain calibration provides that that the maximal allowed input AC signal corresponds to RMS value equal to the Full Scale value divided by the number equal to square root of number 2. For current gain calibration, if AC signal with amplitude of 250mV is applied, Irms register value should be equal 100. (Full Scale value for current is 141.24A) Let x be the value of AC signal applied on inputs (represented in mV) and y be the value read from RMS Current register translated in Ampere units. Then, gain correction can be calculated according the following formula:

$$Igain = \frac{x}{250mV}\frac{100A}{y} \qquad (4)$$

Similar formula stands for AC gain correction of voltage signals:

$$Vgain = \frac{x}{250mV}\frac{300V}{y} \qquad (5)$$

Fig. 8. shows the results of gain calibration when AC signals are applied to the AD converter inputs.

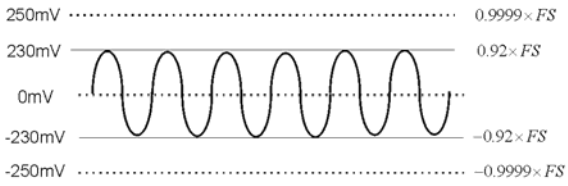

Fig. 8. Results of gain calibration

E. Active power offset calibration

At a first sight, one can say that there is not need to compensate offset for active power if instantaneous voltages and currents have already been calibrated. Unfortunately, that is not the case. Namely, because of RF interference between two analog channels within AD converter, the crosstalk may appear and cause power offset. Therefore the following power-offset calibration procedure is necessary.

First, value 0 has to be stored into Poffset register and value 1 has to be stored into the gain calibration register (it will be explained in detail later). One of the channels should be shorted and on the other, some signal has to be applied. Usually, the current channel is shorted and AC signal applied to voltage input pins. Result calculated by DSP, used for power offset calibration is stored in register for mean active power. This value should be read from that register and written into Poffset register. Precision of offset calculation can be improved with several repeated offset measurements. This value should be experimentally determined taking into account different signal amplitudes on voltage AD converter differential inputs. The similar procedure stands for Qoffset calibration. One of the channels should be shorted and on the other, some signal has to be applied. Reactive power value

calculated by DSP represents the new Qoffset value. One should note that current and voltage DC offsets have to be calibrated before starting Poffset or Qoffset calibration.

F. Active power gain calibration

Active power gain calibration assures that maximal DC signals (250mV DC) applied on voltage and current differential ADC inputs cause Full Scale value of Active power. If Full-scale signal for current corresponds to 141.24A and Full-scale signal for voltage corresponds to 424.24V, Full-scale value for active power is 60kW. It is represented by 24 bit signed value with zero on most significant bit followed by all ones.

Of course, calibration can be done using smaller signals than Full-scale. Active power gain calibration can use either AC or DC signals. When using only AC signals for Active Power gain calculation, signals with the same phase must be used. For reactive power gain calculation, only AC signals should be applied with the 90 degrees phase shift.

TABLE I Default correction values

	Reg. value	value
Igain	54A748	1.3227
Vgain	545567	1.3118
Pgain	6F8C86	1.7429
Qgain	92CDE8	-1.7061

For example, let x1 and x2 (represented in mV) be values of AC signals (which have the same phase) applied on the ADC inputs and y is the value read from P register and represented in Watt units. Gain correction for Active power can be calculated according to the following formula:

$$Gain = \frac{x1}{250mV}\frac{x2}{250mV}\frac{30kW}{y} \qquad (6)$$

The same formula stands for reactive gain calculation if the phase shift of 90 degrees between current and voltage input is achieved. Correspondence between the sign of calculated reactive power and phase is explained in detail in [2].

For both P and Q gain calibrations, stands that first offset calibrations should be performed; after gain correction value 1.0 stored into appropriate gain correction register and then AC or DC signal applied to inputs.

IV. Conclusion

Calibration has a big impact all the other results that Integrated Power Meter IC provides (effective values of voltage and current, active and reactive power and energy). The chip provides calibrations for: DC offset of instantaneous current and voltage signals; AC offset of RMS current and voltage signals; gain error for RMS voltage and current calculation; active and reactive power offset; active and reactive power gain.

References

[1] Jovanović, B., Damnjanović, M., Petković, P. *"Digital Signal Processing for an Integrated Power Meter"*, Conference Proceedings of 49. Internationales Wissen-schaftliches Kolloquium Technische Universitat Ilmenau 27-30 September 2004, Vol. 2, pp. 190-195.

[2] Damnjanović, M., Jovanović, B., "*Energy Calculation in Power Meter IC*", Zbornik radova sa V simpozijuma industrijske elektronike INDEL 2004, pp. 126-131

Acceleration of MEMS Fault Simulation Using ANNs

Vančo Litovski, Miona Andrejević and Mark Zwolinski

Abstract - New concepts for micro-electro-mechanical systems (MEMS) simulation under fault-free and faulty conditions are proposed, in order to decrease the time to market and increase the dependability of such systems. Black-box modelling of non-electronic parts using artificial neural networks (ANNs) is introduced, so enabling radically faster simulation. A lumped model of a capacitive transducer, part of a micro-electro-mechanical capacitive pressure sensing system, is created using an ANN. Faults are then introduced to the sensing system and simulation of the fault-free and faulty circuits is demonstrated. Fault coverage is verified for the chosen signal and fault dictionary creation is enabled.

Keywords - Micro-electro-mechanical systems, Artificial neural networks, Fault simulation

I. Introduction

Since the product development cycle in microsystem technology, or more specifically in Micro-Electro-Mechanical System (MEMS) technology, rarely takes less than 5 years, design for manufacturability [1] is becoming of prime importance. Inefficient design automation tools become a limiting factor for new applications of MEMS. Compared with digital, analogue or even mixed signal products, poor tools may slow-down the product development cycle by orders of magnitude. Such delays are mainly created from a great number of trial-and-error steps caused by, among other things, immature simulation tools and inappropriate modelling methodologies.

This problem becomes even more drastic when testing and diagnosis are considered. Repetitive analyses are needed not only to verify and optimize the design but also for fault coverage verification and fault dictionary creation. One should not forget that we are speaking about systems on chip that encompass analogue and digital electronics and different (mostly mechanical) components described by specific models (most frequently by partial differential equations). An incomparably larger number of faults is expected in the electronic parts, meaning a vast number of simulations is expected. One cannot afford to simulate the mechanical parts at the lowest level. We need models of MEMS at a higher level in order to avoid the repetitive solution of systems of partial equations.

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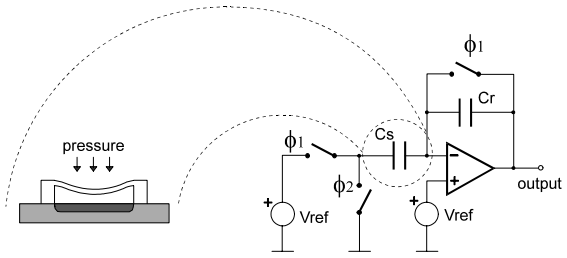

Fig. 1. Micro-electro-mechanical capacitive pressure sensing system

In the next section we will exemplify the standard approach to the MEMS simulation. Than we will introduce black-box modelling by Artificial Neural Networks and apply this to a linear capacitor whose capacitance is controlled by pressure in a nonlinear manner. This model is then implemented in a behavioural system and circuit simulator to demonstrate the effectiveness of the idea.

II. MEMS Simulation

Consider the problem of simulating the simple circuit depicted in Fig. 1. This is a micro-electro-mechanical capacitive pressure sensing system. It consists of an electro-mechanical part that is a capacitor with a deflectable membrane such that a change in pressure results in a change in capacitance, and an electronic switched-capacitor network that generates a pulse train of fixed frequency. The pulse amplitude at the output is related to the capacitance value, so that the whole system converts pressure into a pulse amplitude.

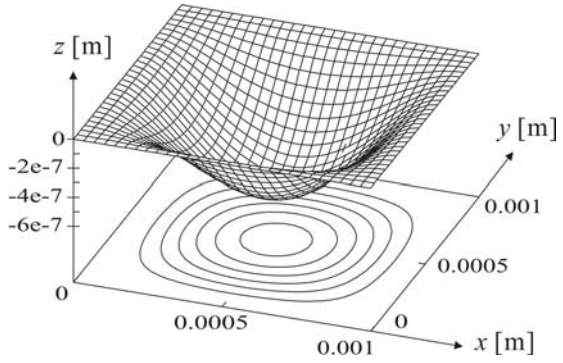

Fig. 2. Displacement of the sensor membrane for simulation time instant 0.0004s

For simulation of this and other similar systems we have previously implemented "Alecsis – the simulator for circuits and systems" [2-4]. It is a mixed-signal (analogue and discrete), mixed-level (system-level analogue and digital, device-level electrical, gate-level digital and grid-level mechanical), and mixed-description (behavioural digital, behavioural analogue, circuit-electrical, gate-digital,

algebraic logic and electrical and partial equation with boundary condition management) simulator. A library of built-in models has been developed.

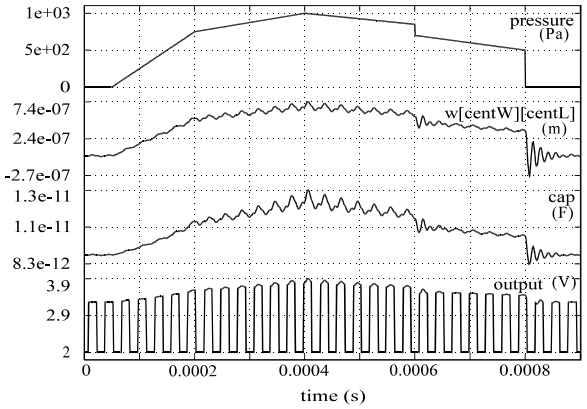

Fig. 3. Time-domain simulation results for the system of Fig. 1. The displayed signals are pressure, displacement of the pressure sensor centre, sensor capacitance, and the output voltage

In addition, a hardware description language named AleC++ was developed as a superset of C++ in order to make the description of the models tractable.

Fig. 2 and Fig. 3 show some simulation results of the system depicted in Fig. 1. The mechanical and the electrical part are modelled within a single description and the simulation performs simultaneous evaluation of all system variables that are (in this case) displacements, voltages, currents, and states.

The concept proposed in this simulation system has been widely recognized [5-10]. In some cases this strategy was adopted as a base for further developments [11].

III. Fault Simulation

During the life-cycle of a product, testing is performed in both the production phase and the implementation phase. We claim, however, that the sustainability of a product is strongly influenced by the design phase. So, to make a sustainable product, one should design the test procedure and synthesize test signals early in the design phase.

It is frequently possible to perform functional verification of the system. That, most frequently, happens when a small number of input/output terminals is present. In the majority of cases however, full functional testing becomes time consuming and is not acceptable. So, we use defect-oriented (structural) testing.

We consider testing to be: the selection of a set of defects regarded as the most probable; the description of a set of measurements; the selection of a set testing points (or output signals); and most importantly, the synthesis of optimal testing signals that will be applied at the system inputs for detecting and observing the listed fault effects. Here, "optimal" means that one test signal covers as many faults as possible.

After selection of test signals, the fault coverage has to be evaluated. To do that, as many replicas of the original circuit as the number of predicted faults have to be created. For large complex systems containing mechanical, analogue and digital parts, the number of replicas becomes huge. Each replica has one fault inserted. The fault coverage is evaluated after simulation of the faulty systems by comparing the results thus obtained with the response of the fault-free system. If these two differ, the fault is covered and the corresponding entry in the fault list can be removed.

As already mentioned, simulation of the system under consideration is time consuming per se. Thus, should we repetitively simulate at the PDE level – the most time consuming part – when faults occur within the analogue or the digital part of the system?

We avoid this by black-box modelling of the non-electronic parts (mechanical, optical, electromagnetic etc.), capturing their properties and so enabling *radically* faster simulation. We capture this black-box behaviour by using artificial neural networks (ANNs). As already proven elsewhere [19-24] this approach has been very successful in modelling non-linear dynamic electronic systems.

In the next section, we show how the system of Fig. 1 may be simplified by substituting the membrane with a lumped (nonlinear with respect to the pressure) capacitor modelled using an ANN. Faults will be introduced and simulation of the fault-free and faulty circuits will be demonstrated.

IV. Black-box Modeling

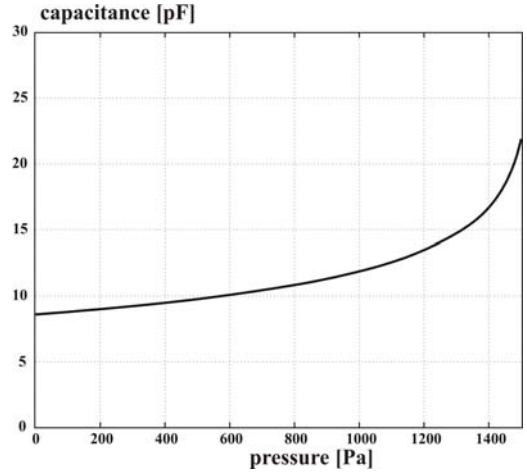

Fig. 4. The capacitance of the membrane of Fig. 1 expressed as a function of pressure

To start with, an ANN was created to characterize a lumped model of the capacitive transducer. The ANNs here are considered universal approximators [17], convenient for black-box device modelling. The process starts with the extraction of the $C(p)$ dependence from the "Alecsis" simulation of the system in Fig. 1. Here C stands for capacitance while p denotes pressure. For this extraction the third trace of Fig. 3 was used and Fig. 4 was created.

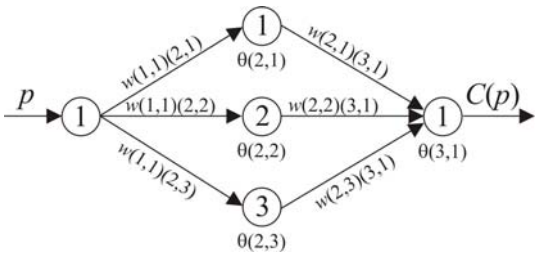

Fig. 5. The ANN structure used for approximation of the curve of Fig. 4. (w stands for weight and θ for threshold)

The structure of the ANN used is depicted in Fig. 5. It is a simple feed-forward ANN with only one hidden layer. The hidden neurons have sigmoidal activation functions, while the output neuron is linear. Table 1 contains the weights and thresholds of the ANN obtained after training with a standard algorithm, e.g. [18].

TABLE I
WEIGHTS AND THRESHOLDS OF THE ANN USED TO APPROXIMATE THE CURVE OF FIG. 4

Hidden layer neurons	Output layer neurons
w(1,1)(2,1) = 33.1034	w(2,1)(3,1)= 2.32691
w(1,1)(2,2) = 3.92046	w(2,2)(3,1) = 17.8609
w(1,1)(2,3) = 4.04654	w(2,3)(3,1)=-5.9505
θ(2,1) = -35.6658	θ(3,1) = 0.354662
θ (2,2) = -3.88227	
θ (2,3) = -3.88324	

The capacitor constitutive equation

$$i_c = C(p)\frac{dv_c}{dt} \tag{1}$$

was implemented according to [19]. Discretization was performed first:

$$i_c^{n+1} = C(p^{n+1})\cdot(A\cdot v_c^{n+1} + B_v^n) \tag{2}$$

where *A* and *B* are constants derived from the discretization rule. *n* stands for the time instance counter.

After that, linearization was applied in order to implement Newton's method for nonlinear analysis. This yields

$$\begin{aligned} i_c^{n+1,m+1} = i_c^{n+1,m} + G_v^{n+1,m}\cdot(v_c^{n+1,m+1} - v_c^{n+1,m}) + \\ + G_p^{n+1,m}(p^{n+1,m+1} - p^{n+1,m}) \end{aligned} \tag{3}$$

where

$$i_c(p^{n+1,m}) = i_c{}^{n+1,m} = C(p^{n+1,m})\cdot(A\cdot v_c^{n+1,m} + B_v^n), \tag{4}$$

$$G_v^{n+1,m} = \left.\frac{\partial i_c}{\partial v_c}\right|_{v_c = v_c{}^{n+1,m}} = A\cdot C(p^{n+1,m}), \tag{5}$$

and

$$\begin{aligned} G_p^{n+1,m} = \left.\frac{\partial i_c}{\partial p}\right|_{p = p^{n+1,m}} = \\ = (A\cdot v_c^{n+1} + B_v^n)\cdot\left.\frac{\partial C(p)}{\partial p}\right|_{p = p^{n+1,m}} \end{aligned} \tag{6}$$

The discretized and linearized model of the nonlinear capacitor represented by (3) may be expressed in a circuit form as depicted on Fig. 6. Note that, to apply this model we write code to calculate the response of the ANN that is *C*(*p*), and its derivative with respect to *p*.

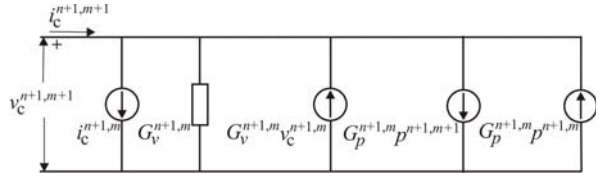

Figure 6. The linearized and discretized model of the capacitor controlled by pressure

V. SIMULATION RESULTS

Fig. 7 shows the input (pressure) signal to the transducer used in the black-box model simulations (repeated from Fig. 3). A new simulation is performed now for the fault-free circuit (the same as Fig. 1) but with the membrane substituted by a lumped model of the capacitor expressed by the ANN. The simulation results, as shown in Fig. 8, are in excellent agreement with those obtained earlier, shown in the fourth trace of Fig. 3.

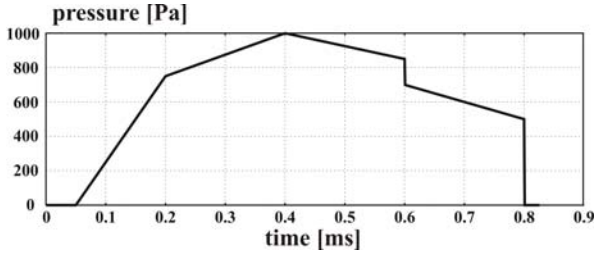

Fig. 7. Input to simulations

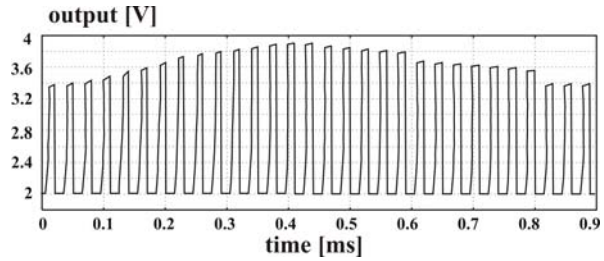

Fig. 8. Simulation results of the circuit of Fig. 1 with the membrane substituted by a lumped capacitor

What is the difference between the two traces? *To obtain the result of Fig. 8 we need to simulate a circuit described by 5 network variables only, compared with 1005 to describe the original circuit.* This enables inexpensive repetitive simulation of the system when faults are inserted.

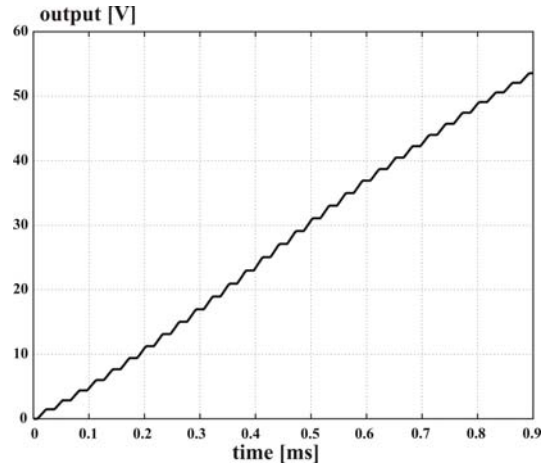

Fig. 9. Response of the faulty circuit in the presence of the "switch stuck-at-open" fault

Simulation for testing and diagnosis will be considered next.

For simplicity only five faults were selected as likely to occur:

1. S_1-On: The feed-back switch of the operational amplifier stuck-at-closed
2. C_r+: The feed-back capacitor incremented by +20%

3. S_1-Off: The feed-back switch of the operational amplifier stuck-at-open

4. C_r-: The feedback capacitor incremented by -20%

5. C_s-flat: The membrane stuck-at-flat (for some reason the membrane does not sense the pressure signal).

The simulation results for the third and fifth defect inserted in the circuit are given on Fig. 9 and Fig. 10.

As a specific simulation example, Fig. 11 shows the response of a faulty circuit with two faults present simultaneously: C_r+ and S_1-Off. This is to assure that simulation is inexpensive and any designer's idea may be easily verified.

Note that, while fault model insertion in the electronic part (both digital and analogue) is well understood and easy to implement [20], there is still much research to be done for mixed-signal electronic circuits and, unfortunately, even more work for non-electronic structures, the membrane being almost the simplest example.

Implementation of the above concept, however, allows for fast creation of a fault coverage list for a broad set of test signals and at the same time for creation of complex fault dictionaries needed to implement any diagnostics.

Table 2 contains the data that constitutes the fault dictionary for a single fault model. After the fault description, in the first column, the fault code is stated. There are five faults to be diagnosed. Accordingly, the fault dictionary has six rows enumerated from zero to five, the zeroth representing the fault-free (FF) system. These numbers are referred to as the fault codes. The last column in Table 2 shows the system response (DC voltage at the output, V_{oDC}) for the fault-free and the faulty circuits.

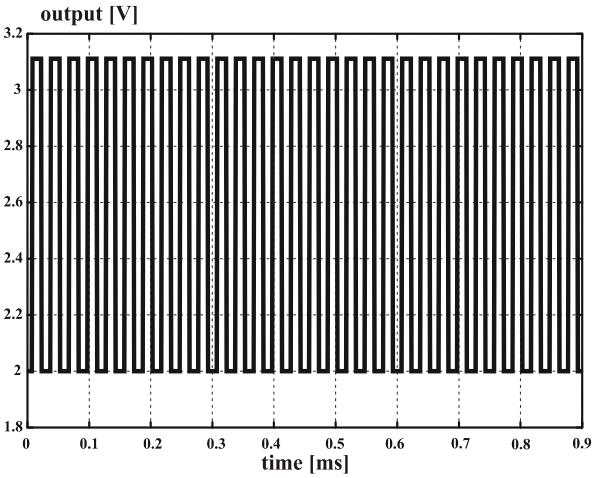

Fig. 10. Response of the faulty circuit in the presence of the "membrane stuck-at-flat" fault

TABLE II
FAULT DICTIONARY

Type	Code	V_{oDC} [V]
FF	0	2.829738
S_1-On	1	2.0
Cr +	2	2.691447
S_1-Off	3	26.8489
Cr -	4	3.037174
C_s - flat	5	2.555527

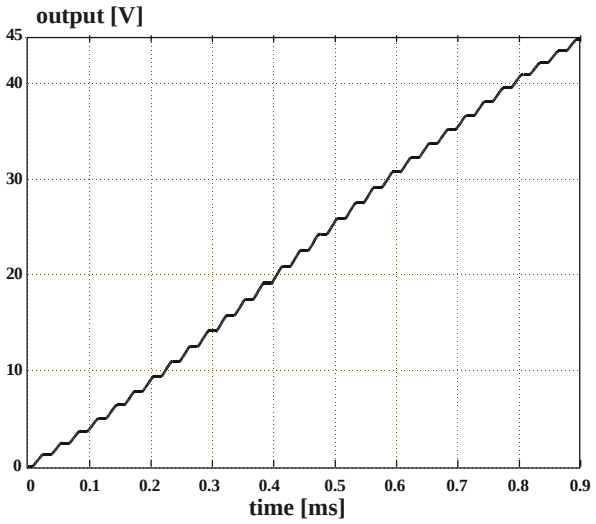

Fig. 11. Response of the faulty circuit in the presence of two: C_r+ and S_1-Off faults

VI. CONCLUSIONS

In order to decrease the time to market and increase the dependability of MEMS, tools are needed for the modelling, simulation and diagnosis of the entire system. To date this has only been possible by modelling the mechanical parts at the level of PDEs. This has led to excessive simulation times and has made fault simulation effectively impossible.

Here, we have demonstrated that accurate black-box modelling of the micro-mechanical parts is possible and, most significantly, that such models may be effectively characterized using ANNs.

Such an approach leads to rapid simulation and fault simulation and allows the further development of integrated design tools for entire Micro-Electro-Mechanical Systems.

REFERENCES

[1] Vandenberg, C., "Back to basics: The IC Industry's reintegration and dynamics of a newly emergent full-chip, design-for-manufacturability infrastructure", *IEEE Design and Test of Computers*, Vol. 21, No. 3, 2004, p. 180.

[2] Litovski, V., Maksimović, D., and Mrčarica, Ž., "Mixed-signal modeling with AleC++: Specific features of the HDL", *Simulation Practice and Theory*, Vol. 8, 2001, pp. 433-449.

[3] Mrčarica, Ž, Ilić, T., Glozić, D., Litovski, V., and Detter, H., "Mechatronic Simulation Using Alecsis: Anatomy of the Simulator", *Proc. of Eurosim'95*, Vienna, Austria, Sept. 1995, pp. 651-656.

[4] Mrčarica, Ž., Litovski, V., Detter, H., "Modeling And Simulation of Microsystems Using Hardware Description Language", *Research Journal on Microsystem Technologies*, Vol. 3, No. 2, Feb., 1997, pp. 80-85.

[5] Chappel, B.,"The fine art of IC design", *IEEE Spectrum*, Vol. 36, No. 7, July 1999., pp. 30-34.

[6] Endemano, A., et al. "VHDL-AMS modeling and simulation of a planar electrostatic micromotor", *J. of Micromechanics and Microengineering*, Vol. 13, 2003, pp. 580-590.

[7] Gerlach, G., Schroth, A., and Klein, A., "Modellirung nichtelektrischer Komponenten in heterogenen und komplexen Mikrosystemen", *Workshop: Methoden und Werkzeuge zum Entwurf von Microsystemen*, Frankfurt

a.M., Jun 1996, pp. 12-21.

[8] Haase, J., Vermeiren, W., Clauss, C., und Schwarz, P.,"Erste Erfahrungen mit der simulation von Mixed-Signal-Schaltungen mit einem VHDL-AMS-Simulator", *ASIM-Tagung, Simulationstechnik*, Weimar, 17.09. 1999, Praxisforum, pp. 33-38.

[9] Haase, J., Schwarz, P., Trappe P., und Vermeiren, W. "Erfahrungen mit VHDL-AMS bei der Simulation heterogener Systeme", *ITG/GI/GMM Workshop, "Methoden und beschreibungssprachen zur modellirung und verifikation von Schaltungen und Systemen"*, Frankfurt/M, 28-29.02.2000, pp. 167-175.

[10]Senturia, S. D., "CAD challenges for Microsensors, Microactuators, and Microsystems", *Proceedings of the IEEE*, Vol. 86, No. 8, August 1998., pp. 1611-1626.

[11]Zhang, T., Chakrabarty, K., and Fair, R. B., "Behavioral modeling and performance evaluation of microelectrofluidics-based PCR systems using SystemC", *IEEE Trans. on CAD of Integrated circuits and Systems*, Vol. 23, No. 6, June 2004, pp. 843-858.

[12]Andrejević, M., Litovski, V., "Electronic Modeling Using ANNs For Analogue and Mixed-Mode Behavioural Simulation", *Journal of Automatic Control*, Vol. 13, No. 1, 2003, pp. 31-37.

[13]Litovski, V., Rađenović, J., Mrčarica, Ž., Milenković, S., "MOS Transistor Modeling Using Neural Network", *Electronics Letters*, Vol. 28, No. 18, August, 1992, pp. 1766-1768.

[14]Litovski, V. B., Andrejević, M., Petković, P., Damper, R., "ANN Application to Modeling of the D/A and A/D Interface for Mixed-Mode Behavioural Simulation", *Journal of Circuits, Systems and Computers*, Vol. 13, No. 1, February 2004, pp. 181-192.

[15]Mikulchenko, O., Mayaram, K. "Neural network design for behavioral model generation with shape preserving properties" IEEE/ACM International Workshop on Behavioral Modeling and Simulation, 2000, pp. 97-102

[16]Zwolinski, M., Brown A.D., "Behavioural Modelling Of Analogue Faults In VHDL-AMS — A Case Study", *ISCAS*, Vancouver, Canada, 2004.

[17]Scarselli, F., and Tsoi, A. C., "Universal approximation using feed-forward neural networks: A survey of some existing methods and some new results", *Neural Networks*, Elsevier, Vol. 11, No. 1, 1998, pp. 15-37.

[18]Zografski, Z., "A novel machine learning algorithm and its use in modeling and simulation of dynamical systems", *Proceedings of 5th Annual European Computer Conference, COMPEURO'91*, Bologna, Italy 1991, pp. 860-864.

[19]Litovski, V., and Zwolinski, M., *VLSI Circuit Simulation and Optimization*, Chapman and Hall, London, 1997.

[20]Petković, P., Milovanović, D., Litovski, V., "Symbolic Fault Modeling and Test Generation of MOS Circuits", *Microelectronics and Reliability*, Vol. 37, No. 1, 1997, pp. 137-157.

Passive Image Rejection Filters Optimised for Telecommunication Applications

Srdjan Milenković and Vančo Litovski

Abstract – This paper analyses the complete design flow of passive filters, starting from transfer function optimisation to the final implementation and measurement. Poles and zeros of the transfer function are determined by simultaneously optimising amplitude response and group delay variation. This approach produces the filtering functions with better group delay performance while maintaining similar selectivity when compared to Chebyshev class of filters. Cascade network synthesis is used to determine the circuit architecture and component values. Final S parameter based simulation and measured results are analysed in the context of telecommunication applications. Two approaches are proposed to compensate for the loss of performance due to component nonidealities.

Keywords – Passive filters, amplitude response, flat group delay, simultaneous optimisation, synthesis, implementation.mm

I. Introduction

Analogue filters design techniques were extensively studied back in 1970's for more than a decade. A lot of things have changed since then. We have witnessed enormous increase in available computing resources. Object oriented programming languages offer a lot more flexibility in application development. And finally, technology of the passive components, especially inductors, has also improved. The aim of this paper is to analyse each phase of the passive filter design flow, starting with transfer function optimisation to the final implementation and measurement and answer few key questions: Can we get better performing analogue filters in the context of telecommunication applications using the technology improvements mentioned above? If not, what are the alternatives to improve the performance?

Digital circuits together with digital signal processing (DSP) techniques are heavily used in todays telecommunication systems due to their flexibility, programmability, robustness, insensitivity to noise, accurate arithmetic functions, etc. However, before transmission, digital signal yet has to be converted into analogue domain, upconverted into proper RF frequency band and amplified, as shown in Figure 1. Digital to analogue conversion is done by the DAC module followed by low pass analogue filter (LPF). DAC output spectrum is affected by zero hold effect. Apart from analogue equivalent of the digital signal there are the images centred at integer multiples of the clock frequency. Hence the requirement for the so called image rejection filter. Due to the same effect, DAC amplitude response is not flat. It follows sinx/x envelope which has to be compensated by inverse sinc filter. Inverse sinc filter is in fact digital filter and can be considered as part of DSP block of Figure 1.

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As far as the communication link quality is concerned, image rejection filter mainly affects two figures: output spectrum and bit error rate (BER) which are both strictly regulated by the communication standards. The same figures are also affected by other analogue blocks of Figure 1. However, LPF input and output signals are still in the base band and as such it is much easier to predict and compensate for its imperfections during the design phase. This is unfortunately not the case with RF analogue blocks such as mixers or power amplifier stages. For this reason, more stringent specifications are usually put on image rejection filter in order to relax the design of RF stages.

LPF can contribute to unnecessarily widening the transmit spectrum if images are not attenuated to the required level. This problem is however easy to resolve by careful planning, i.e. by choosing proper clock frequency, and/or selecting higher order analogue filter. On the other hand, bit error rate is directly related to in-band amplitude ripple and group delay variation which means it depends on many factors such as filter type, optimisation method, components used to build the filter, etc.

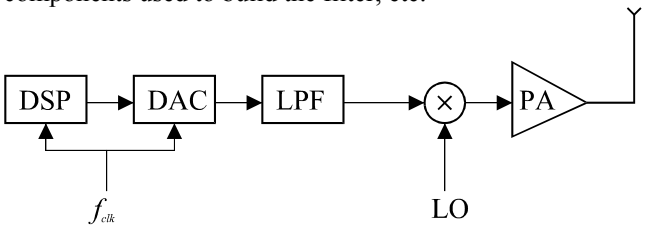

Figure 1: Simplified block diagram of the transmit chain in digital wireless communication system

As mentioned above, to design the filter suitable for telecommunication applications one should minimise in-band amplitude ripple and group delay variation while maintaining the filter selectivity. Obviously, it can be considered as simultaneous optimisation of multiple criteria. The idea of simultaneously optimising amplitude response and group delay variation is not new. Back in 1970's however it was not widely accepted since it was computationally intensive [1-3]. There is no reason not to use it now and it is adopted for the study presented in this paper. Detailed explanation of the approach is given in Section II.

After the optimisation phase, transfer function coefficients as well as the pole and zero locations are known and circuit component values can be calculated. To accomplish that, we use the so called cascade synthesis [1, 4, 5] which is explained in Section III.

Finally, in order to illustrate the performance of the developed analogue filter design procedure, simulation and measured results of a low pass filter are presented in Section IV.

II. Transfer Function Optimisation

A. Low Pass Prototype Transfer Function

The form of the filtering transfer function has direct impact on the resulting circuit architecture and the kind of components the circuit is composed of. Passive lossless filters can be built using capacitors, inductors, mutual inductors and transformers. Each class of the components has its own parasitic effects which cause the performance degradation when the filter is finally implemented. In this respect, the best performing components are capacitors. Mutual inductors and transformers are difficult to tune and their performance is far from the ideal models. The same applies to inductors, however, LC is minimum set we need to construct the filters. For these reasons, the analysis in this paper is limited to LC filters only. Besides, LC filters are also more cost effective than the filters using the whole variety of passive components.

If the target circuit architecture is limited to LC network than low pass transfer function can have the following kind of poles and zeros: a pair of complex poles:

$$p_i = -a_i^2 \pm jb_i ,$$

which define the complex pole subsection of the transfer function:

$$H_{cp}^{(i)}(s) = \frac{s^2 + 2a_i^2 s + (a_i^4 + b_i^2)}{a_i^4 + b_i^2}, \quad (1)$$

real pole:

$$p_i = -c_i^2 ,$$

$$H_{rp}^{(i)}(s) = \frac{s + c_i^2}{c_i^2}, \quad (2)$$

and a pair of real frequency (imaginary) zeros:

$$p_i = \pm jd_i ,$$

$$H_{iz}^{(i)}(s) = \frac{s^2 + d_i^2}{d_i^2}. \quad (3)$$

Note that poles of the transfer function are limited to left half plane by definition.

Hence, low pass prototype transfer function can be defined as:

$$H(s) = \frac{\prod_{k=1}^{Niz} H_{iz}^{(k)}(s)}{\prod_{k=1}^{Nrp} H_{rp}^{(k)}(s) \prod_{k=1}^{Ncp} H_{cp}^{(k)}(s)}, \quad (4)$$

where:

$$2N_{iz} \le N_{rp} + 2N_{cp} .$$

For *H(s)* we define amplitude, phase and group delay functions as below:

$$A(\omega) = |H(j\omega)|, \qquad \varphi(\omega) = \arg H(j\omega), \qquad \text{and}$$

$$\tau(\omega) = -\frac{d\varphi(\omega)}{d\omega}.$$

B. Filtering Function Transformations

Let us assume that we have synthesised low pass transfer function *H(p)*, where $p = \alpha + j\beta$. We introduce new complex variable $s = \sigma + j\omega$. Low pass prototype filter can be transformed into some other type by replacing *p* in *H(p)* with *p=T(s)*, in which case transfer function of the new filter becomes:

$$H_T(s) = H(T(s)) .$$

Real frequency of the low pass prototype filter, β, is related to the real frequency of transformed filter, ω, as below:

$$\beta = \frac{T(j\omega)}{j} .$$

Amplitude, phase and group delay of the transformed filter then can be easily calculated from its prototype as:

$$A_T(\omega) = A(\beta)\Big|_{\beta = T(j\omega)/j}, \quad (5)$$

$$\varphi_T(\omega) = \varphi(\beta)\Big|_{\beta = T(j\omega)/j}, \quad (6)$$

$$\tau_T(\omega) = \frac{d\beta}{d\omega} \cdot \tau(\beta)\Big|_{\beta = T(j\omega)/j} . \quad (7)$$

In this paper, we will limit the analysis to low pass and band pass designs, hence, only low pass to low pass and low pass to band pass transformations are considered. Low pass to low pass transformation is straightforward. In fact, there is no transformation, hence *p=T(s)=s*. In the case of band pass filter, the desired frequency transformation is:

$$p = T(s) = \frac{s^2 + \omega_o^2}{Bs}, \quad (8)$$

where ω_o is geometric centre frequency of the target band pass filter and *B* is its bandwidth.

C. Cost Function

In order to optimise both amplitude response and group delay variation of the filter the following cost function should be minimised:

$$\varepsilon = \frac{\lambda_A}{2}\sum_{l=1}^{P_A} W_A(\omega_l)\left(A_s(\omega_l)A_T(\omega_l) - A_d(\omega_l)\right)^2 + \frac{\lambda_\tau}{2}\sum_{l=1}^{P_\tau} W_\tau(\omega_l)\left(\tau_T(\omega_l) - \rho\right)^2 + \frac{\lambda_m}{2}\sum_{l=1}^{P_A} \max(0, A_T(\omega_l) - 1)^2 \quad (9)$$

where:

$\lambda_A, \lambda_\tau, \lambda_m$	represent the penalty factors,
ω_l	are discretised frequency samples,
W_A, W_τ	amplitude and group delay weighting functions,
A_s	is the spectrum of input signal,
A_T, τ_T	represent amplitude and group delay of the transformed filtering function as defined by (5) and (7),
A_d	is the desired amplitude response and
ρ	represents constant group delay.

Assuming that the filter is driven by a signal the spectrum of which is $A_s(\omega)$, first term in (9) reflects the requirement that spectrum of the filter output, $A_s(\omega)A_T(\omega)$, is as close as possible to some desired response $A_d(\omega)$. In other words, first term of (9) defines filter amplitude response constrain. The approach is slightly different from the traditional one which is usually based on pass band and stop band definition. In order to illustrate the advantage this approach can offer, let us consider Figure 2. The figure shows DAC output spectrum where signal pass band and clock frequency are normalised to 1 and 10, respectively. Images are affected by sinx/x roll off while in the signal pass band we assume that the same effect is compensated by inverse sinc filter. Effectively, Figure 2 shows the spectrum of the filter input signal and the desired output should be to keep the signal while images should be removed. The example is simple and still can be well represented by pass band/stop band definition. However, let us imagine that on top of the images generated by the DAC zero hold effect, some other unwanted components may appear in the input signal. Such components can be generated by the digital interpolation process within the DSP block of Figure 1 for example. In this case, optimisation process itself can fit the transition band amplitude response much better than we can do by inspection.

The purpose of having second term in the cost function (9) is quite obvious. When minimised to zero, it gives ideally flat group delay filter. Note that constant group delay ρ is not known a priori and has to be considered as the optimisation parameter. It is also worth mentioning that group delay constrain of (9) assumes ideally linear phase input signal. We know that digital stage can provide such a signal.

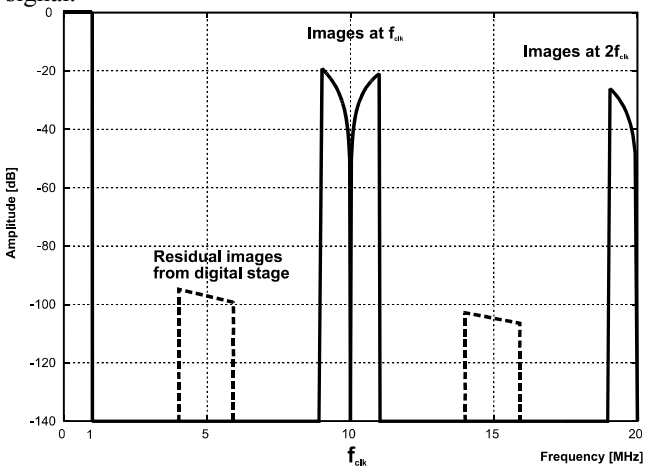

Figure 2: Spectrum of the DAC output

As mentioned before, the analysis presented in this paper is restricted to passive filters only. In this case, the gain, i.e. amplitude response of the filter can not be greater than 1. Hence the third term in (9).

To summarise this section let us emphasise that filter transfer function is optimised in the following way. In both low pass and band pass designs, low pass prototype function (4) is optimised with a_i, b_i, c_i and d_i in (1), (2) and (3) being the optimisation parameters. However, if the target is band pass filter then transformations (5), (6) and (7) are taken into account.

III. Cascade Synthesis of Lossless Four Pole Networks

Once the filter transfer function is optimised one may proceed with the network synthesis. Passive networks synthesis is usually implemented in the following way: Having the desired filter transfer function ready, calculate the reflection coefficient [6]. Use the reflection coefficient to determine input impedance of the network being synthesised [6]. Find the normalised component values of the network which implements the prescribed impedance function [1, 4, 5]. Unnormalise the components having in mind real source resistance and cut-off frequency [6]. In case of band pass filters, low pass prototype is synthesised first and then transformed into band pass equivalent at the circuit level. This section describes the implementation details of the above procedure.

A. Reflection Coefficient

For doubly terminated passive network shown in Figure 3 we can define voltage transfer function:

$$T(s) = \frac{U_{out}(s)}{U_S(s)}. \quad (10)$$

If the desired filter transfer function *H(s)* is designed

according to the constrain:

$$|H(j\omega)| \le 1, \ \forall\omega ,$$

than we can define the synthesis problem as finding the network with the following voltage transfer function:

$$T(s) = \frac{R_L}{R_S + R_L} H(s) . \qquad (11)$$

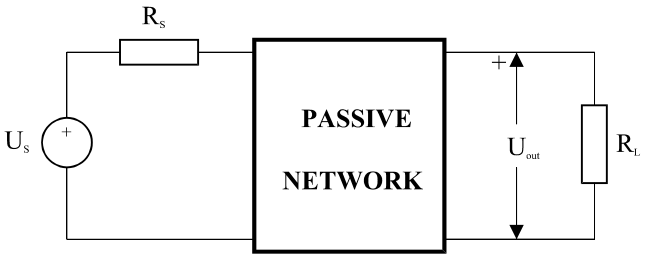

Figure 3: Doubly terminated passive network

Squared magnitude of the reflection coefficient is defined as the ratio of the reflected power to the maximum power available from the source:

$$|\rho(j\omega)|^2 = \frac{P_s - P_{out}}{P_s} .$$

Having in mind that maximum power voltage source of the resistance R_S can supply is:

$$P_s = \frac{|U_S(j\omega)|^2}{4R_S} ,$$

and the power at the output load is:

$$P_{out} = \frac{|U_{out}(j\omega)|^2}{R_L} ,$$

reflection coefficient can be expressed as:

$$|\rho(j\omega)|^2 = 1 - 4\frac{R_S}{R_L}\frac{|U_{out}(j\omega)|^2}{|U_S(j\omega)|^2} ,$$

or, according to (10):

$$|\rho(j\omega)|^2 = 1 - 4\frac{R_S}{R_L}|T(j\omega)|^2 . \qquad (12)$$

In s-domain, the above equation can be rewritten as:

$$\rho(s)\rho(-s) = 1 - 4\frac{R_S}{R_L}T(s)T(-s) ,$$

which, after substituting $T(s)$ with (11) becomes:

$$\rho(s)\rho(-s) = 1 - \alpha H(s)H(-s) , \ \alpha = 4\frac{R_S \| R_L}{R_S + R_L} . \qquad (13)$$

Note that in case of equal termination (R_S=R_L), (13) simplifies to:

$$\rho(s)\rho(-s) = 1 - H(s)H(-s) .$$

If we express both reflection coefficient and transfer function as rational functions:

$$\rho(s) = \frac{P_\rho(s)}{Q_\rho(s)}, \ H(s) = \frac{P_H(s)}{Q_H(s)} ,$$

(13) can be transformed into:

$$\frac{P_\rho(s)}{Q_\rho(s)}\frac{P_\rho(-s)}{Q_\rho(-s)} = 1 - \alpha\frac{P_H(s)}{Q_H(s)}\frac{P_H(-s)}{Q_H(-s)} = \frac{Q_H(s)Q_H(-s) - \alpha P_H(s)P_H(-s)}{Q_H(s)Q_H(-s)}$$

which gives two important equations to identify the reflection coefficient:

$$P_\rho(s)P_\rho(-s) = Q_H(s)Q_H(-s) - \alpha P_H(s)P_H(-s) \qquad (14)$$

$$Q_\rho(s) = Q_H(s) . \qquad (15)$$

As indicated by (15), denominator of $\rho(s)$ is equal to the denominator of $H(s)$. Hence, reflection poles are the same as the poles of the transfer function and have to be in the left half plane (LHP). However, for the reflection zeroes there is no such restriction. They can be located into left half plane, right half plane (RHP), at zero as well as on the imaginary axis.

To identify numerator of $\rho(s)$ we have to solve (14). The procedure starts with first finding the roots of the right hand side polynomial of (14). Then half of the roots are chosen to construct $P_\rho(s)$. Polynomial (14) is squared polynomial with real coefficients. Its roots are symmetrically located around imaginary axis. To construct $P_\rho(s)$ we have three options. If we chose LHP roots, the resulting network will have minimum sensitivity to the source resistor variation. On the other hand, if we chose RHP reflection zeroes, the circuit sensitivity to the load resistor variation is minimised. There is also an option to alternate LHP and RHP zeroes while constructing $P_\rho(s)$ in which case, depending on the circuit architecture, resulting network can be symmetrical or antimetrical.

Polynomial (14) is squared which means all odd coefficients are equal to zero. In this case we can replace $s^2 = p$, which reduces the polynomial order to half, solve for the roots with respect to p and then recalculate the roots of the original polynomial as $s_{1,2} = \pm\sqrt{p}$.

B. Input Impedance

In order to determine input impedance, the circuit of Figure 4 will be analysed in sinusoidal steady state. The input impedance has both real and imaginary components:

$$Z_{in}(j\omega) = R_{in} + jX_{in} .$$

The network is driven by the input current:

$$I_{in}(j\omega) = \frac{U_S(j\omega)}{R_S + Z_{in}(j\omega)} .$$

If the network is lossless then the power supplied to the input terminals is equal to the power supplied to the load, hence:

$$R_{in}|I_{in}(j\omega)|^2 = \frac{|U_{out}(j\omega)|^2}{R_L} ,$$

which, after substituting input current, becomes:

$$\frac{R_{in}\left|U_S(j\omega)\right|^2}{\left|R_S+Z_{in}(j\omega)\right|^2}=\frac{\left|U_{out}(j\omega)\right|^2}{R_L}.$$

The above equation can be rearranged to express the voltage transfer function:

$$\left|T(j\omega)\right|^2=\frac{\left|U_{out}(j\omega)\right|^2}{\left|U_S(j\omega)\right|^2}=\frac{R_L R_{in}}{\left|R_S+Z_{in}(j\omega)\right|^2}$$

Using (12) we can calculate the reflection coefficient as follows:

$$\begin{aligned}\left|\rho(j\omega)\right|^2&=\rho(s)\rho(-s)\Big|_{s=j\omega}\\&=1-4\frac{R_S}{R_L}\frac{R_L R_{in}}{\left|R_S+Z_{in}(j\omega)\right|^2}\\&=\frac{\left|R_S-Z_{in}(j\omega)\right|^2}{\left|R_S+Z_{in}(j\omega)\right|^2}\end{aligned}$$

which can be used to separate $\rho(s)$ from $\rho(-s)$ giving:

$$\rho(s)=\pm\frac{R_S-Z_{in}(s)}{R_S+Z_{in}(s)}.$$

Finally, solving the above equation for Z_{in} results in:

$$Z_{in}(s)=R_S\frac{1\pm\rho(s)}{1\mp\rho(s)}. \qquad (16)$$

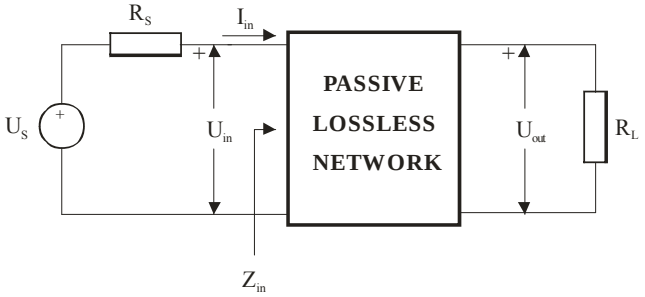

Figure 4: Lossless network

As (16) indicates, we have two solutions for Z_{in}:

$$Z_{in}(s)=R_S\frac{1+\rho(s)}{1-\rho(s)}, \text{ and} \qquad (17)$$

$$Z_{in}(s)=R_S\frac{1-\rho(s)}{1+\rho(s)}. \qquad (18)$$

The synthesis of one or another will give us the same filter transfer function and the two networks are so called dual. The question is which one is more appropriate from the practical point of view? The answer is, the network with less number of inductors. In case of low pass filers, (18) is favourable since it produces minimum inductor solution.

During the synthesis procedure we can assume that source resistor is normalised to unity, i.e. R_s=1 Ω, hence (18) becomes:

$$Z_{in}(s)=\frac{1-\rho(s)}{1+\rho(s)}.$$

Once the normalised circuit element are found, source resistance can be easily unnormalised, as will be shown later.

Having in mind (14) and (15), input impedance is finally calculated as:

$$Z_{in}(s)=\frac{P_{zin}(s)}{Q_{zin}(s)}=\frac{Q_H(s)-P_\rho(s)}{Q_H(s)+P_\rho(s)}. \qquad (19)$$

where $Q_H(s)$ represents denominator of the synthesised transfer function $H(s)$ and $P_\rho(s)$ is the numerator of the reflection coefficient determined by solving (14).

C. Extracting Transmission Zeroes of the Low Pass Prototype Filter

Cascade synthesis of passive networks is in fact iterative process. In each iteration, starting with the input impedance $Z(s)$, we calculate element values of the section which implement one of the transmission zeroes and the remaining impedance $Z_1(s)$, as shown in Figure 5. The process ends when all transmission zeroes, including transmission zeroes at infinity, are examined.

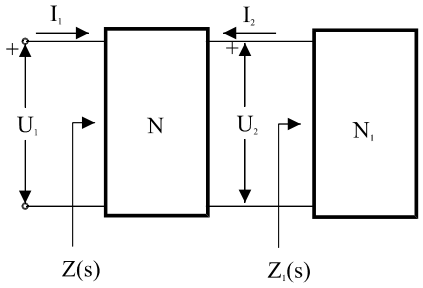

Figure 5: Extracting the section which implements transmission zero $s=s_o$

Depending on the state of $Z(s)$ and the kind of transmission zero, we will extract sections with different topologies, which is explained in more detail in the following section.

C.1. Zero at Infinity

In this case transfer function $H(s)$ is zero when s approaches infinity ($H(\infty)=0$) while input impedance can have either pole or zero for $s\to\infty$. The case when input impedance has the pole at infinity:

$$Z(\infty)=\infty, \qquad (20)$$

is implemented by extracting series inductor as shown in Figure 6. Input impedance is rational function of two polynomials:

$$Z(s)=\frac{P_Z(s)}{Q_Z(s)}=\frac{\sum_{k=0}^{m}a_k s^k}{\sum_{k=0}^{n}b_k s^k}. \qquad (21)$$

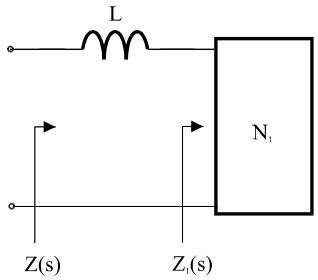

Figure 6: Implementation of zero at infinity when $Z(\infty) = \infty$

Since (21) is imittance function, polynomial orders of $P_Z(s)$ and $Q_Z(s)$ can not differ for more than one. On the other hand, (20) indicates that $m > n$, hence:

$m = n + 1$.

and $Z(s)$ can be expressed as:

$Z(s) = sL + Z_1(s)$,

where:

$$L = \frac{a_m}{b_n}. \tag{22}$$

The remaining impedance is then given by:

$$Z_1(s) = \frac{P_{Z1}(s)}{Q_{Z1}(s)} = \frac{P_Z(s) - sL\,Q_Z(s)}{Q_Z(s)}. \tag{23}$$

Similarly, when input impedance has zero at infinity, $Z(\infty) = 0$, we extract shunt capacitor as shown in Figure 7, where:

$$C = \frac{b_n}{a_m}, \tag{24}$$

and the remaining admittance is then given by:

$$Y_1(s) = \frac{Q_{Z1}(s)}{P_{Z1}(s)} = \frac{Q_Z(s) - sC\,P_Z(s)}{P_Z(s)}. \tag{25}$$

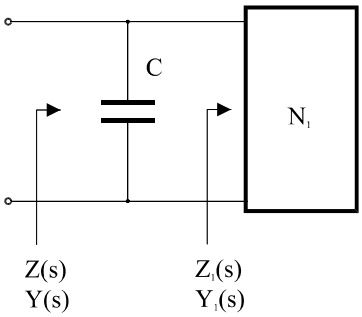

Figure 7: Implementation of zero at infinity when $Z(\infty) = 0$

C.2. Trivial Case of Real Frequency Zero

This section considers the extraction of real frequency transmission zero ($s = \pm j\omega_o$) when input impedance has either pole or zero at the same frequency. Let us assume that input impedance has the pole at $s = \pm j\omega_o$:

$$Z(j\omega_o) = \infty. \tag{26}$$

Such kind of transmission zero can be implemented by extracting series LC circuit as shown in Figure 8.

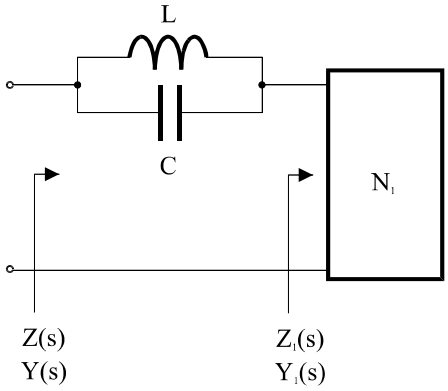

Figure 8: Implementation of transmission zero $s = \pm j\omega_o$ when $Z(j\omega_o) = \infty$

Having in mind (26) and:

$$Z(s) = \frac{P_Z(s)}{Q_Z(s)},$$

one may conclude that denominator of the input impedance has zero at $s = \pm j\omega_o$:

$$Q_Z(j\omega_o) = 0. \tag{27}$$

Also, as Figure 8 shows, input impedance can be expressed as:

$$Z(s) = \frac{sL}{1 + s^2/\omega_o^2} + Z_1(s), \tag{28}$$

where:

$$\omega_o^2 = \frac{1}{LC}. \tag{29}$$

Inductor value can be determined from (28) as a residue of the pole $s = \pm j\omega_o$. We can write:

$$Z(s)\Big|_{s \approx j\omega_o} = \frac{sL}{1 + s^2/\omega_o^2},$$

or:

$$Y(s)\Big|_{s \approx j\omega_o} = \frac{1 + s^2/\omega_o^2}{sL}.$$

If we calculate first derivative of $Y(s)$:

$$Y'(s)\Big|_{s \approx j\omega_o} = \frac{s^2/\omega_o^2 - 1}{s^2 L},$$

and evaluate it for $s = j\omega_o$:

$$Y'(j\omega_o) = X'(\omega_o) = \frac{2}{\omega_o^2 L},$$

we can use it to determine the inductor value:

$$L = \frac{2}{\omega_o^2 X'(\omega_o)}. \tag{30}$$

The capacitor is calculated from (29):

$$C = \frac{1}{\omega_o^2 L} = \frac{X'(\omega_o)}{2}, \tag{31}$$

while remaining impedance is given by:

$$Z_1(s) = \frac{P_{Z1}(s)}{Q_{Z1}(s)} \tag{32}$$
$$= \frac{\left[P_Z(s) - sLQ_Z(s)/(1+s^2/\omega_o^2)\right]/(1+s^2/\omega_o^2)}{Q_Z(s)/(1+s^2/\omega_o^2)}.$$

Note that both numerator and denominator of (32) are divided by $(1+s^2/\omega_o^2)$ which reduces the polynomial order by 2.

The case when input impedance has zero at $s = \pm j\omega_o$, $Z(j\omega_o) = 0$, is implemented by shunt LC circuit as shown in Figure 9. The component values and the remaining admittance are calculated as follows:

$$C = \frac{2}{\omega_o^2 X'(\omega_o)}, \tag{33}$$

$$L = \frac{1}{\omega_o^2 C} = \frac{X'(\omega_o)}{2}, \tag{34}$$

$$Y_1(s) = \frac{Q_{Z1}(s)}{P_{Z1}(s)} \tag{35}$$
$$= \frac{\left[Q_Z(s) - sCP_Z(s)/(1+s^2/\omega_o^2)\right]/(1+s^2/\omega_o^2)}{P_Z(s)/(1+s^2/\omega_o^2)},$$

where, $X'(\omega_o) = Z'(j\omega_o)$.

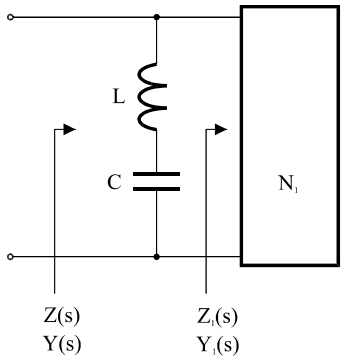

Figure 9: Implementation of transmission zero $s = \pm j\omega_o$ when $Z(j\omega_o) = 0$

C.3. General Case of Real Frequency Zero

In this case input impedance has neither pole nor zero at the transmission zero. However, real part of the impedance is zero at transmission zero, hence:

$$\left[Z(s) + Z(-s)\right]\Big|_{s=\pm j\omega_o} = 0. \tag{36}$$

Following the usual procedure, we extract the section which implements transmission zero, shown as network N in Figure 5. It is more convenient here to use transfer matrix as the section representation:

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A'(s) & B'(s) \\ C'(s) & D'(s) \end{bmatrix} \begin{bmatrix} U_2 \\ -I_2 \end{bmatrix}.$$

If the section implements real frequency transmission zero then its transfer matrix has to be presentable in the following way:

$$\frac{1}{f(s)} \begin{bmatrix} A(s) & B(s) \\ C(s) & D(s) \end{bmatrix}, \tag{37}$$

where *f(s)* represents the polynomial containing only transmission zero that is being extracted. In this particular case we have:

$$f(s) = 1 + s^2/\omega_o^2. \tag{38}$$

Having N represented by (37), the remaining impedance $Z_1(s)$ in Figure 5 can be calculated as:

$$Z_1(s) = \frac{D(s)Z(s) - B(s)}{A(s) - C(s)Z(s)}, \tag{39}$$

or, if we use polynomial representations of $Z(s)$ and $Z_1(s)$:

$$Z_1(s) = \frac{P_{Z1}(s)}{Q_{Z1}(s)} = \frac{D(s)P_Z(s) - B(s)Q_Z(s)}{A(s)Q_Z(s) - C(s)P_Z(s)}. \tag{40}$$

Transfer matrix (37), and consequently element values of the section, should be determined so that the real part of remaining impedance $Z_1(s)$ has no zero at $s = \pm j\omega_o$. According to (36), real part of $Z(s)$ has the form:

$$Z(s) + Z(-s) = f(s)R(s). \tag{41}$$

where $R(s)$ is not zero at $s = \pm j\omega_o$. Combining (39) and (41), real part of the remaining impedance can be calculated as below:

$$Z_1(s) + Z_1(-s) = \tag{42}$$
$$= \frac{f^3(s)R(s)}{\left[A(s) - C(s)Z(s)\right]\left[A(s) - C(s)Z(s) + C(s)f(s)R(s)\right]}$$

The above equation is derived having in mind that $A(s)$ and $D(s)$ are even while $C(s)$ and $B(s)$ are odd functions of s. Obviously, real part of $Z_1(s)$ is not going to have zero at $s = \pm j\omega_o$ if:

$$\Phi(s) = A(s) - C(s)Z(s), \tag{43}$$

has double zero at $s = \pm j\omega_o$. Hence:

$$\Phi(s)\Big|_{s=\pm j\omega_o} = 0, \text{ and } \frac{d\Phi(s)}{ds}\Big|_{s=\pm j\omega_o} = 0, \tag{44}$$

represent starting point to determine the element values.

Having in mind that (43), which is in fact denominator of (39), has double zero at $s = \pm j\omega_o$, numerator and denominator of (40) can by divided by $f^2(s)$ in order to reduce the polynomial order:

$$Z_1(s) = \frac{P_{Z1}(s)}{Q_{Z1}(s)} = \tag{45}$$
$$= \frac{\left[D(s)P_Z(s) - B(s)Q_Z(s)\right]/f^2(s)}{\left[A(s)Q_Z(s) - C(s)P_Z(s)\right]/f^2(s)}$$

Real frequency transmission zero of the low pass filter is implemented by the section whose transfer matrix has

the form:

$$\frac{1}{f(s)}\begin{bmatrix} A(s) & B(s) \\ C(s) & D(s) \end{bmatrix} = \frac{1}{1+s^2/\omega_o^2}\begin{bmatrix} 1+as^2 & bs \\ cs & 1+ds^2 \end{bmatrix}. \quad (46)$$

As mentioned before, real part of the input impedance *Z(s)* is zero for $s = \pm j\omega_o$, hence

$$Z(s)\Big|_{s=j\omega_o} = jX(\omega_o),$$

is pure imaginary while:

$$\frac{dZ(s)}{ds}\Big|_{s=j\omega_o} = X'(\omega_o),$$

is pure real. Using (44), *a* and *c* coefficients of (46) can be calculated as:

$$a = \frac{\omega_o X'(\omega_o) + X(\omega_o)}{\omega_o^2\left[\omega_o X'(\omega_o) - X(\omega_o)\right]},$$

$$c = \frac{2}{\omega_o\left[\omega_o X'(\omega_o) - X(\omega_o)\right]}. \quad (47)$$

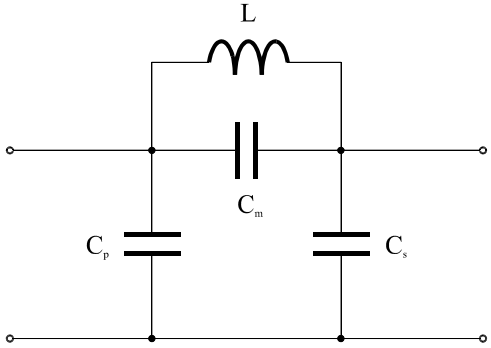

Figure 10: Π section implements real frequency zero

In order to implement transfer matrix (46) Π section shown in Figure 10 can be used. Its ABCD parameters are:

$$A(s) = 1 + s^2L(C_m + C_s), \quad B(s) = sL,$$
$$C(s) = s(C_p + C_s) + s^3L[C_mC_p + C_mC_s + C_pC_s],$$
$$D(s) = 1 + s^2L(C_m + C_p), \quad f(s) = 1 + s^2LC_m$$

Transfer matrix obviously does not fit into (46) form with *C(s)* being the problem. However, if we introduce the following constrain:

$C_mC_p + C_mC_s + C_pC_s = 0$, or

$$\frac{1}{C_p} + \frac{1}{C_m} + \frac{1}{C_s} = 0, \quad (48)$$

which is the same, transfer matrix becomes:

$$\frac{1}{1+s^2LC_m}\begin{bmatrix} 1+s^2L(C_m+C_s) & sL \\ s(C_p+C_s) & 1+s^2L(C_m+C_p) \end{bmatrix},$$

in which case we have:

$$\omega_o^2 = \frac{1}{LC_m},\ a = L(C_m + C_s),\ b = L,$$
$$c = C_p + C_s \text{ and } d = L(C_m + C_p)$$

Element values of the section can be determined as:

$$C_m = \frac{ac\omega_o^2}{\left(1 - a\omega_o^2\right)^2},\ L = \frac{1}{\omega_o^2 C_m},$$
$$C_p = \frac{c}{1 - a\omega_o^2},\ C_s = \frac{ac\omega_o^2}{a\omega_o^2 - 1} \quad (49)$$

Both (48) and (49) indicate that one of the capacitors, C_p or C_s, has to be negative. However, if we cascade this section with the section which ends, or starts, with the positive shunt capacitor, negative C_p or C_s can be absorbed, making the overall circuit realisable.

C.4. Extraction Order of the Transmission Zeroes

As we could see so far, there are many different circuit architectures which can implement the same transfer function. For example, we can choose LHP or RHP zeroes to construct the reflection coefficient. Also, selecting one or another sign for input impedance (equation (16)) leads to two different networks with the same transfer function. Moreover, when we have different transmission zeros, their order of extraction also generates different circuit topologies. Does an optimum order of extraction exist?

In case of low pass filter, real frequency transmission zeroes should be ordered by their magnitude ($\omega_i > \omega_{i-1}$), then the extraction order which minimises both the range of required component values as well as the sensitivity to component tolerances is:

$\omega_n, \omega_{n-2}, ..., \omega_1, ..., \omega_{n-3}, \omega_{n-1}$

or:

$\omega_{n-1}, \omega_{n-3}, ..., \omega_1, ..., \omega_{n-2}, \omega_n$

with *n* being the number of real frequency zeros.

D. Low Pass to Band Pass Transformation at the Circuit Level

Low pass to band pass transformation, explained in section II.B can easily be implemented at circuit level. Having in mind (8), the impedance of low pass prototype inductor *L* can be expressed as:

$$pL = \frac{s^2 + \omega_o^2}{Bs}L = s\frac{L}{B} + \frac{1}{s\dfrac{B}{\omega_o^2 L}},$$

which is equivalent to serial LC circuit with the following band pass component values:

$$L_{BP} = \frac{L}{B} \text{ and } C_{BP} = \frac{B}{\omega_o^2 L}. \quad (50)$$

Similarely, for the admitance of low pass capacitor *C* we have:

$$pC = \frac{s^2+\omega_o^2}{Bs}C = s\frac{C}{B} + \frac{1}{s\dfrac{B}{\omega_o^2 C}},$$

which is equivalent to parallel LC circuit with the following band pass components:

$$C_{BP} = \frac{C}{B} \text{ and } L_{BP} = \frac{B}{\omega_o^2 C}. \quad (51)$$

Therefore, low pass filter is transformed into band pass one by replacing each inductor with serial LC circuit (50) and each capacitor with parallel LC one (51).

E. Impedance and Frequency Scaling

Let us first consider the normalisation of an arbitrary network. Its driving point impedance can be calculated as:

$$Z_{ii}(s) = \frac{\Delta_{ii}(s)}{\Delta(s)}, \quad (52)$$

where $\Delta(s)$ is determinant of the admittance matrix [Y] and $\Delta_{ii}(s)$ is determinant of the same matrix with *i*-th column and *i*-th row removed. Each term of [Y] is of the form:

$$Y_{ij}(s) = \frac{1}{R_{ij}} + \frac{1}{sL_{ij}} + sC_{ij}.$$

We can introduce magnitude and frequency normalising constants R_o and ω_o, to yield the rearranged admittance element:

$$Y_{ij}(s) = \frac{1}{R_o}\left[\frac{1}{\dfrac{R_{ij}}{R_o}} + \frac{1}{\dfrac{s}{\omega_o}\dfrac{\omega_o L_{ij}}{R_o}} + \frac{s}{\omega_o}\omega_o R_o C_{ij}\right].$$

Making the change in variable $p=s/\omega_o$ and defining the normalised element values as:

$$r_{ij} = \frac{R_{ij}}{R_o},\ l_{ij} = \frac{\omega_o L_{ij}}{R_o},\ c_{ij} = \omega_o R_o C_{ij}, \quad (53)$$

we now find that:

$$Y_{ij}(s) = \frac{1}{R_o}\left[\frac{1}{r_{ij}} + \frac{1}{pl_{ij}} + pc_{ij}\right] = \frac{1}{R_o}Y'_{ij}(p), \quad (54)$$

where $Y'_{ij}(p)$ is a normalised admittance element. Substituting (54) in (52) we see that:

$$Z_{ii}(s) = \frac{\dfrac{1}{R_o^{n-1}}\Delta'_{ii}(p)}{\dfrac{1}{R_o^n}\Delta'(p)} = R_o Z'_{ii}(p), \quad (55)$$

where $\Delta'(p)$ and $\Delta'_{ij}(p)$ are normalised determinants and $Z'_{ii}(p)$ is the driving point impedance of the normalised network.

The equations (53) and (55) clearly indicate that if we have synthesised the normalised network, with R_o and ω_o being normalising resistance and frequency, than unnormalised component values can be simply determined by solving (53):

$$R_{ij} = R_o r_{ij},\ L_{ij} = \frac{R_o}{\omega_o} l_{ij},\ C_{ij} = \frac{1}{\omega_o R_o} c_{ij}. \quad (56)$$

IV. Design Example

A. Synthesis

In order to illustrate the procedure explained in the previous sections an all-pole fifth order low pass filter is designed. Using the same notation as in (9), filter transfer function is optimised according to amplitude and group delay specifications given in Tables I and II. It is assumed that filter is driven by the signal of the spectrum shown in Figure 2 without residual images from the digital stage. Poles of the resulting filter are given in Table III. The circuit components are unnormalised having in mind 15MHz cut off frequency and 50Ω doubly terminated network. The component values are given in Table IV while Figure 11 shows the circuit diagram. Amplitude response, in band amplitude ripple and group delay of the new filter are shown in Figures 12-14.

TABLE I
AMPLITUDE SPECIFICATION

	Pass band	Transition band	Stop band
Frequency band	0.0-1.0	1.1-8.9	9.0-11.0
Desired response A_d	1.0	0.0	0.0
Weighting factor W_A	1.0	1.0e7	1.0e6

TABLE II
GROUP DELAY SPECIFICATION

	Pass band
Frequency band	0.0-1.0
Weighting factor W_τ	1.0

TABLE III
POLES OF THE RESULTING FILTER

Pole	Q factor
-0.219046467949926 ± j 1.240413036376161	2.8752
-0.584692777260911 ± j 0.756906141176324	0.817897
-0.731291589403377 ± j 0.0	

TABLE IV
COMPONENT VALUES OF THE NEW AND CHEBYSHEV FILTER

	New filter	Chebyshev
C_1	181.917 pF	243.361 pF
L_2	678.369 nH	727.451 nH
C_3	334.612 pF	419.109 pF
L_4	677.984 nH	727.451 nH
C_5	181.022 pF	243.361 pF

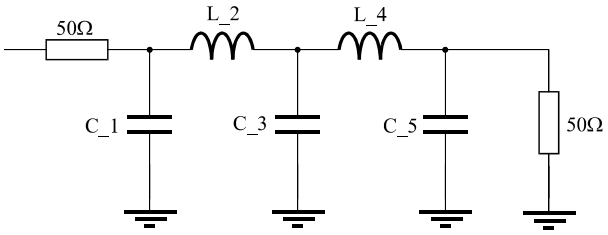

Figure 11: Circuit diagram

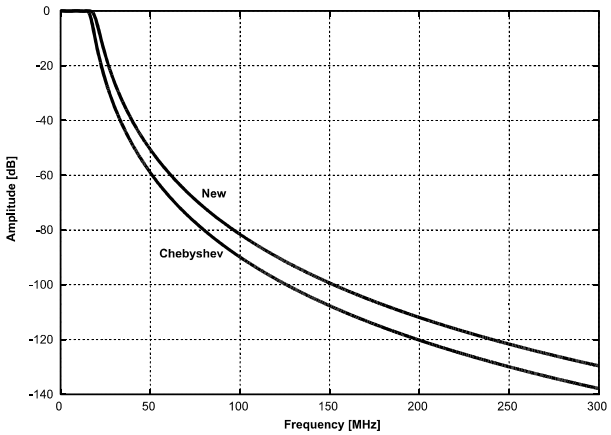

Figure 12: Amplitude response

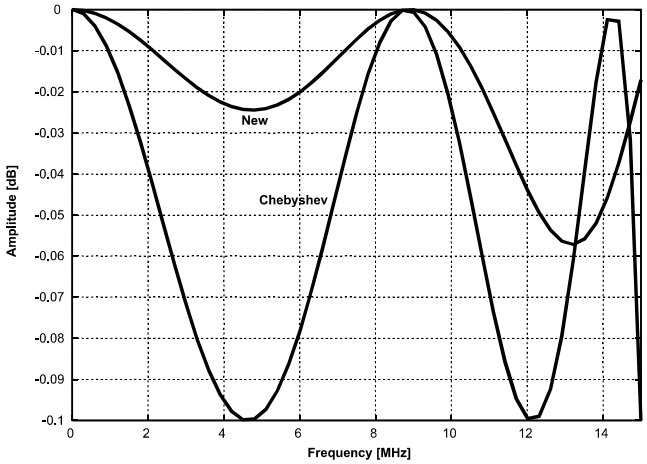

Figure 13: In band amplitude ripple

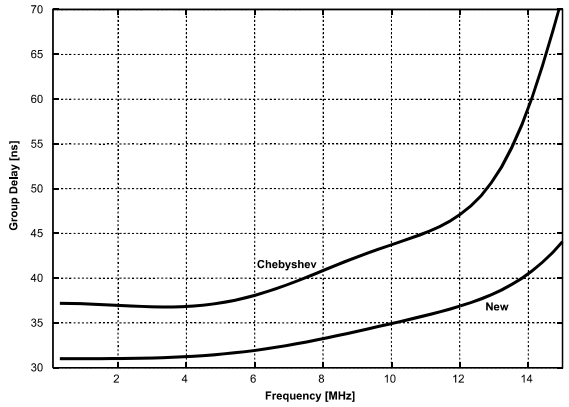

Figure 14: Group delay

The new filter response is compared to the fifth order Chebyshev filter designed using similar specifications. The component values of the Chebyshev filter are also given in Table IV. Having in mind Figures 12-14, one may conclude that new filter has slightly worse selectivity, better in band amplitude ripple but most importantly almost three times less group delay variation.

B. Implementation and Measurement

Before final implementation, synthesised components are first rounded to the nearest available values as shown in Table V. Next, one more simulation is performed using more realistic, S parameter based, LC models. S parameters are measured and provided by the component manufacturers. Finally, the filter is implemented and its amplitude response is measured. Simulation and measured results are plotted in Figures 15-17. Layout and size of the resulting filter are also shown in Figure 15.

Figures 15-17 show that there is almost no performance degradation caused by rounding. Also, we have excellent agreement between S parameter based simulation and measured response having in mind that test and measurement setup accuracy is about 0.1dB. S parameter based simulation and measured results indicate that filter selectivity as well as group delay are not significantly affected by the component parasitics. As expected, the most affected figure is in band amplitude ripple mainly caused by Eddy's current and skin effect in the inductors. In fact, both effects behave as frequency depended parasitic resistance, hence almost linear drop of the in band amplitude response.

TABLE V
SYNTHESISED AND ROUNDED COMPONENT VALUES

	Synthesised	Rounded
C_1	181.917 pF	180 pF
L_2	678.369 nH	680 nH
C_3	334.612 pF	330 pF
L_4	677.984 nH	680 nH
C_5	181.022 pF	180 pF

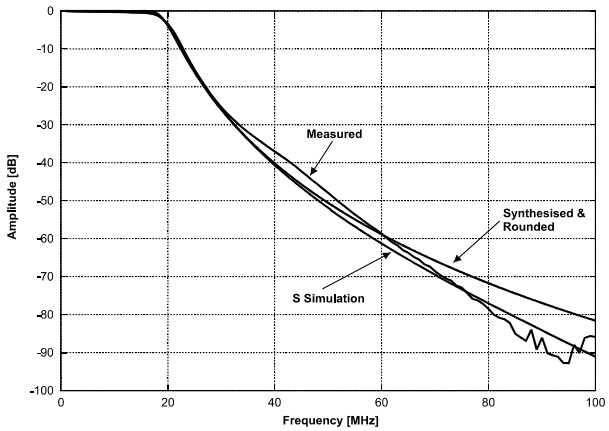

Figure 15: Amplitude response

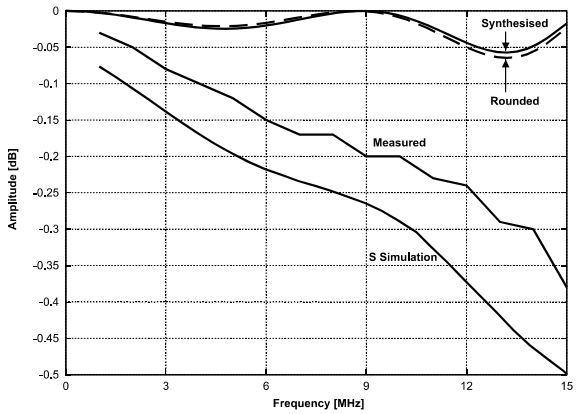

Figure 16: Inband amplitude ripple

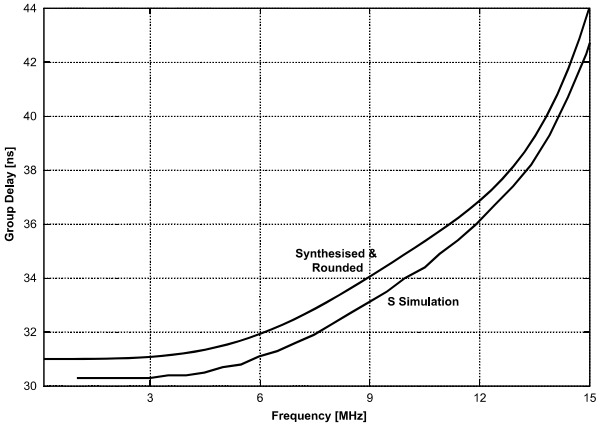

Figure 17: Group Delay

V. CONCLUSION

The design procedure presented so far produces analogue filters with reduced group delay variation while maintaining similar selectivity when compared to classic type of filters. It is also shown that in band amplitude response of the implemented filter is highly affected by inductor nonidealities which are difficult to take into account during the optimisation process.

If the performance of the resulting filter in terms of group delay variation and in band amplitude ripple is still not good enough for some telecommunication applications, then there are three possible solutions we can apply.

The first one is quite obvious. With the inductors being one of the problems we can use continuous time active filters. Although this can reduce in band amplitude ripple, group delay figure unfortunately will stay the same.

Second approach is based on the fact that RF stage amplitude response is band pass in nature. By carefully choosing DSP/DAC clock frequency in Figure 1, we can position the images within the stop band of RF stage. In this case, residual images which may not be attenuated to the required level will be positioned out of transmit band. This can relax filtering requirements or even eliminate the need for low pass image rejection filter [7].

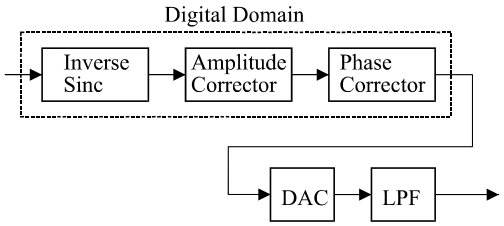

Figure 18: Proposed amplitude and phase correction

Although the above solution seams attractive, there is one major drawback. The flexibility in choosing the clock frequency, i.e. frequency planning, is lost and we still may need simple low pass filter to further attenuate the residual images. To overcome these problems the solution of Figure 18 is proposed. As mentioned before, in band amplitude response of the implemented filter falls down almost linearly with the frequency (Figure 16). Based on numerous simulations, we have seen that this behaviour scales with the cut off frequency. On the other hand, group delay (Figure 17) is not significantly affected by inductor nonidealities. However, it scales with the cut of frequency as well which means that both amplitude and phase distortion introduced by analogue image rejection filter can be compensated in digital domain as suggested by Figure 18. Eventually, inverse sinc filter, amplitude and phase correctors can be integrated into single digital filter performing all three functions.

REFERENCES

[1] V. B. Litovski, *"Selective, Monotonic Passband Filters with Constant Group Delay"*, PhD Thesis, Faculty of Electronic Engineering, University of Ni{, Yugoslavia, 1977, in Serbian.

[2] V. B. Litovski, *"Synthesis of Monotonic Passband Sharp Cutoff Filters with Constant Group Delay Response"*, IEEE Transactions on Circuit and Systems, Vol. CAS-26, No. 8, pp. 597-602, August 1979.

[3] N. Damera-Venkatta, B. L. Evans, *"An Automated Framework for Multicriteria Optimization of Analog Filter Designs"*, IEEE Transactions on Circuit and Systems – II, Analog and Digital Signal Processing, Vol. 46, No. 8, August 1999.

[4] M. Hibino, Y. Ishizaki, H. Watanbe, *"Design of Chebyshev Filters with Flat Group-Delay Characteristics"*, IEEE Transactions on Circuit Theory, Vol. CT-15, No. 4, pp. 316-325, December 1968.

[5] J. D. Rhodes, M. Z. Ismail, *"Cascade Synthesis of Selective Linear-Phase Filters"*, IEEE Transactions on Circuit Theory, Vol. CT-19, No. 2, pp. 183-189, March 1972.

[6] D. S. Humpherys, *"The Analysis, Design and Synthesis of Electrical Filters"*, Prentice-Hall, 1970.

[7] V. W. Leung, L. E. Lawrence, P. S. Gudem, *"Digital-IF WCDMA Handset Transmitter IC in 0.25-μm SiGe BiCMOS"*, IEEE Journal of Solid State Circuits, Vol. 39, No. 12, pp. 2215-2225, December 2004.

One Approach to I/O Based Design of Digital Sliding Mode Control for Nonlinear Plants

Darko Mitić, Čedomir Milosavljević and Boban Veselić

Abstract - The paper deals with design and simulation of a new digital sliding mode controller whose synthesis is based on an input-output discrete-time nonlinear model of plant. The design procedure is explained through an illustrative example, while the validation of the proposed control algorithm is performed by digital simulation.

Keywords - Quasi-sliding mode, Chattering reduction.

I. Introduction

Sliding mode control systems belong to a class of nonlinear control systems, known as variable structure systems [1], which have been studied in the research community for almost fifth decades. This kind of control forces a system phase point to move along a predefined sliding hypersurface, so that a system gains good performances such as robustness to parameter variations and external disturbances, known in advance dynamics described by lower order equations etc. The modern implementation of sliding mode control, based on microcontrollers, assumes the discretization process of sliding mode control, causing the quasi-sliding motion [2] and undesirable chattering phenomenon in the $O(T)$ vicinity of a sliding hypersurface.

Generally speaking, the sliding mode control design methods could be divided into two groups: the techniques based on the state-space model representations, wherein the use of observer is mandatory, and the methods utilizing only the output measurements. The input-output (I/O) based design method of digital sliding mode controller for nonlinear systems is the subject of this paper. Two approaches are possible. The first one is based on the linearized model of nonlinear plant [3]. This method is superior over the conventional linear control techniques. The second one utilizes the I/O discrete-time nonlinear models of nonlinear plants [4]. The latter approach will be discussed in this paper.

The digital sliding mode control, proposed herein is the combination of the control algorithm given in [4] and the solution described in [5]. The result is the new control law which significantly suppresses the chattering phenomenon.

The paper is organized as follows. In Section II, the mathematical model of nonlinear plant is given and the basic definitions are introduced. The controller design procedure is described in Section III. The Illustrative example both with the digital simulation results are given in Section IV. The paper ends with concluding remarks and the list of cited references.

II. Mathematical Model of Nonlinear Plant

Let us consider the discrete-time nonlinear single-input-single-output (SISO) plant in the following form:

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$$y_{k+1} = f(y_k,...,y_{k-n}) + g(y_k,...,y_{k-n})u_k, \qquad (1)$$

where y_k is the plant output, u_k is the control input, n is the positive integer representing the plant order, $f(y_k,...,y_{k-n})$ and $g(y_k,...,y_{k-n})$ are smooth functions of past values of the plant output signal. Notice that the plant is linear with respect to the control input and that y_k stands for $y(kT)$ where T is a sampling period. For the sake of brevity, we will use the next notations $f_k = f(y_k,...,y_{k-n})$ and $g_k = g(y_k,...,y_{k-n})$ in further text. We also assume that the function g_k is strictly positive and bounded.

Suppose that there exists a model of the plant Eq. (1) where $\hat{f}_k = \hat{f}(y_k,...,y_{k-n})$ and $\hat{g}_k = \hat{g}(y_k,...,y_{k-n})$ are estimated functions of f_k and g_k, respectively. We define the modelling error as:

$$\begin{aligned}\varepsilon_k = {} & f_k(y_k,...,y_{k-n}) - \hat{f}(y_k,...,y_{k-n}) + \\ & + (g_k(y_k,...,y_{k-n}) - \hat{g}_k(y_k,...,y_{k-n}))u_k\end{aligned}, \qquad (2)$$

and assume that it is bounded and its limit E is known:

$$\max|\varepsilon_k| < \mathrm{E}, \quad \forall k. \qquad (3)$$

We suppose that the reference input signal r_{k+1} is known in advance as the output of the reference system defined as:

$$r_{k+1} = a_0 r_k + ... + a_n r_{k-n} + b_0 \rho_k + ... + b_m \rho_{k-m}, \qquad (4)$$

where $a_0,...,a_n$ and $b_0,...,b_n$ are the coefficients of the stable polynomials $A(z^{-1}) = a_0 + a_1 z^{-1} ... + a_n z^{-n}$ and $B(z^{-1}) = b_0 + b_1 z^{-1} + ... + b_m z^{-m}$, respectively, z^{-1} is the unit delay and ρ_k represents the input of reference system.

It is now possible to introduce the tracking error in the form of:

$$e_k = y_k - r_k. \qquad (5)$$

Using Eq. (2), Eq. (1) can be rewritten in the next manner:

$$\begin{aligned}y_{k+1} = {} & f_k + g_k u_k - (\hat{f}_k + \hat{g}_k u_k) + \hat{f}_k + \hat{g}_k u_k = \\ & = \varepsilon_{k+1} + \hat{f}_k + \hat{g}_k u_k.\end{aligned} \qquad (6)$$

The following section consider the design aspects of the novel digital sliding mode control.

III. DIGITAL SLIDING MODE CONTROL

The design goal is to find a digital sliding mode control providing the zero value of the so-called switching function defined as:

$$s_k = c_0 e_k + c_1 e_{k-1} + ... + c_n e_{k-n}, \quad (7)$$

where $c_0,...,c_n$ are the coefficients of the polynomial $C(z^{-1}) = c_0 + c_1 z^{-1} + ... + c_n z^{-n}$ with all zeros inside the unit disk. Once the system is in quasi-sliding mode i.e. $s_k = 0$ is reached, the tracking error e_k will converge towards zero.

In order to accomplish the design task, we propose the new digital sliding mode control algorithm:

$$u_k = -\frac{1}{c_0 \hat{g}_k}\left(\begin{array}{l} c_0(\hat{f}_k - r_{k+1}) + c_1 e_k + c_2 e_{k-1} + \\ + ... + c_n e_{k-n+1} + \dfrac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k) \end{array}\right). \quad (8)$$

Notice that the relay component of the control law Eq. (8) is filtered through the discrete-time integrator, so the chattering is significantly reduced in that way.

The substitution of Eq. (8) in Eq. (6) gives:

$$s_{k+1} = c_0 \varepsilon_{k+1} - \frac{\alpha T}{1-z^{-1}}\operatorname{sgn}(s_k), \quad (9)$$

and finally:

$$s_{k+1} - s_k = c_0(\varepsilon_{k+1} - \varepsilon_k) - \alpha T \operatorname{sgn}(s_k). \quad (10)$$

The question is now how to choose the parameter α to obtain the quasi-siding mode. The system is said to be in the quasi-sliding mode if the following three conditions of the s_k dynamics is satisfied:

a) Starting from any initial state, s_k moves towards the quasi-sliding surface $s_k = 0$ and crosses it in a finite time period;
b) Once the quasi-sliding surface $s_k = 0$ is reached, s_k changes its value around the surface forming the so-called *zigzag* motion;
c) The *zigzag* motion is stable and it occurs inside the predetermined vicinity of the quasi-sliding surface.

These three conditions of quasi-sliding mode existence can be expressed as:

$$s_k(s_{k+1} - s_k) < 0. \quad (11)$$

Proposition: The quasi-sliding mode exists in the system described by Eqs. (6) and (8) if α is selected according to the following inequality:

$$\alpha > \frac{1}{T}\Delta E, \quad (12)$$

where:

$$\Delta E > \max\left|c_0(\varepsilon_{k+1} - \varepsilon_k)\right|, \ \forall k. \quad (13)$$

Proof: If Eq. (3) is valid then there exists the finite ΔE satisfying Eq. (13) for each k. The multiplication of Eq. (10) with s_k yields:

$$s_k(s_{k+1} - s_k) = c_0(\varepsilon_{k+1} - \varepsilon_k)s_k - \alpha T\left|s_k\right|. \quad (14)$$

It is evident that if α is chosen according to Eqs. (12) and (13), the quasi-sliding existence condition given by the Eq. (11) will be satisfied. □

IV. ILLUSTRATIVE EXAMPLE WITH DIGITAL SIMULATION RESULTS

In order to verify the proposed digital sliding mode control algorithm, we perform the digital simulation on the inverted pendulum continuous-time model described by:

$$J\ddot{\theta}(t) + Mgh\sin(\theta(t)) = u(t), \quad (15)$$

where $\theta(t)$ is the angular position of inverted pendulum, $u(t)$ is the control input representing the torque applied to it, M is the load mass, J is the inertia moment, h is the suspension link length and g is the gravitational acceleration. The nominal and the perturbed values of the inverted pendulum parameters are given in Table I.

TABLE I
PARAMETERS OF INVERTED PENDULUM

Parameter	Nominal	Perturbed
M	1 kg	0.75 kg
J	0.25 kgm^2	0.31 kgm^2
h	0.5 m	0.5 m

In order to obtain the discrete-time model of nonlinear plant we will use the second Euler's method where:

$$\frac{d}{dt} \sim \frac{1-z^{-1}}{T} \quad (16)$$

and $\theta(t)$ is substituted by θ_{k+1}. For the sake of clarity, we will denote θ with y i.e. $y(t) = \theta(t)$ and $y_k = \theta_k$. The implementation of Eq. (16) in Eq. (15) yields the discrete-time representation of Eq. (15) in the form of Eq. (1):

$$\begin{aligned} y_{k+1} &= 2y_k - y_{k-1} - \frac{MghT^2}{J}\sin(y_{k+1}) + \frac{T^2}{J}u_k = \\ &= f_k + g_k u_k. \end{aligned} \quad (17)$$

As $\sin(y_{k+1})$ is not known because y_{k+1} is not available, for the realization of the control algorithm Eq. (8), we use the estimated functions $\hat{f}_k$ and $\hat{g}_k$:

$$\hat{f}_k = 2y_k - y_{k-1} - \frac{MghT^2}{J}\sin(y_k)$$
$$\hat{g}_k = \frac{T^2}{J} \tag{18}$$

The modelling error Eq. (2) is:

$$\varepsilon_k = -\frac{MghT^2}{J}(\sin(y_k) - \sin(y_{k-1})), \tag{19}$$

so that Eq. (3) is valid.

The simulation is performed in such way that the nonlinear plant, defined by Eq. (15), is simulated in continuous-time using 4th Runge-Kutte method with perturbed parameters from Table I. The proposed control algorithm is realized in discrete-time with zero-order hold circuit and the nominal values of plant. The parameters of controller are chosen as follows:

$$\alpha = 0.1$$
$$T = 0.1\,s \tag{20}$$
$$C(z^{-1}) = 1 - 1.3z^{-1} + 0.4225z^{-2}$$

The reference input signal is the step signal with the amplitude of 1 rad.

In Fig. 1 the response of the system output is presented. It is obvious that the proposed digital sliding mode controller enables good tracking of the reference input signal with the error given in Fig. 2. The control input signal u_k, shown in Fig. 3, is rather smooth what is the consequence of filtering the relay component $\mathrm{sgn}(s_k)$ through the discrete-time integrator. In Fig. 4, the switching function s_k is presented. The tracking precision depends on the accuracy of the switching function according to Eq. (7). In other words, when the system is in the quasi-sliding mode and the steady-state is reached, the tracking error is determined by the following equation:

$$e_\infty = \frac{s_\infty}{C(1)}. \tag{21}$$

We can see from the Fig. 5, where the enlarged switching function response is given, that the quasi-sliding mode really occurs in the region defined by $|s_k| < \alpha T = 0.01$. This automatically causes the corresponding tracking error according to Eq. (21), shown in Fig. 6.

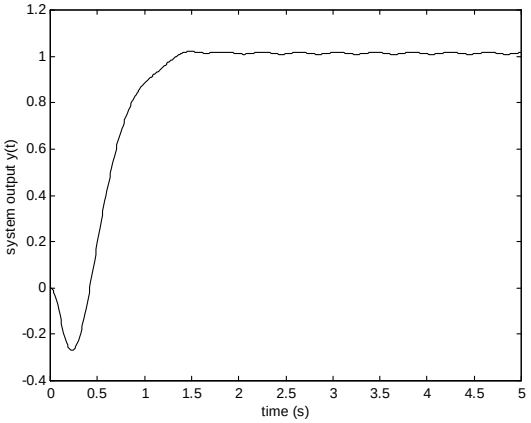

Fig. 1. The system output y_k response

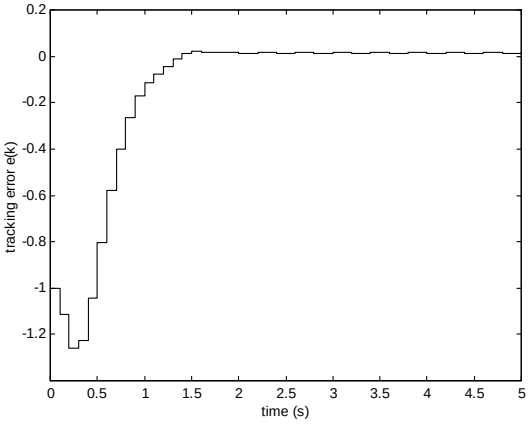

Fig. 2. The tracking error signal e_k

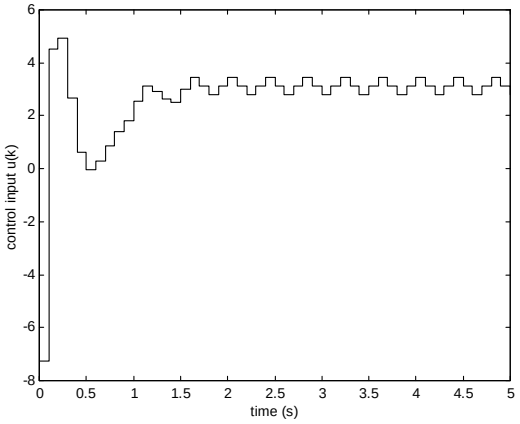

Fig. 3. The control input u_k

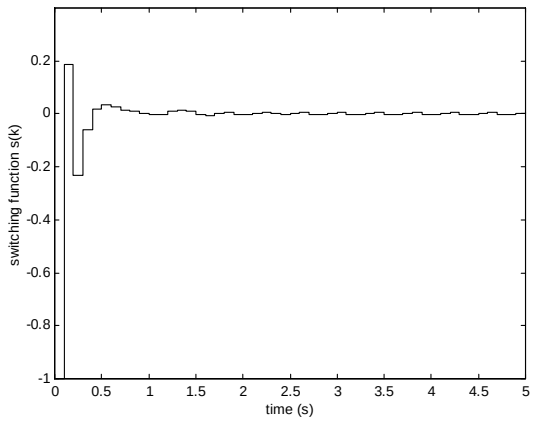

Fig. 4. The switching function s_k response

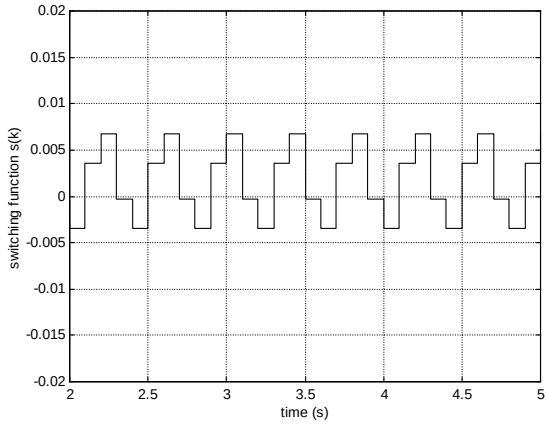

Fig. 5. The switching function s_k response (enlarged)

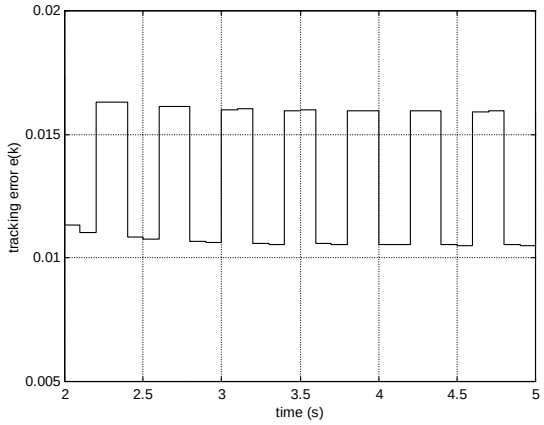

Fig. 6. The tracking error signal e_k (enlarged)

V. CONCLUSION

The novel digital sliding mode control for nonlinear plants is presented in this paper. The proposed control algorithm uses the input-output nonlinear discrete-time model for design purposes. Since the relay component of the control law is filtered through the discrete-time integrator, a significant chattering alleviation is achieved. The verification of the proposed approach is done by digital simulation.

REFERENCES

[1] Utkin V.I., *"Sliding Modes in Control and Optimization"*, Berlin, Springer-Verlag, 1992

[2] Milosavljević Č., "*General conditions for the existence of a quasi-sliding mode on the switching hyperplane in discrete variable structure systems"*, Automatic Remote Control, Vol. 46, 1985, pp. 307-314.

[3] Corradini M.L.,Orlando G., *"Discrete Variable Structure Control for Nonlinear Systems"*, Proceedings of 3rd European Control Conference, Rome, Italy,1995, pp. 1465-1470.

[4] Munoz D., Sbarbaro D., *"An Adaptive Sliding-Mode Controller for Discrete Nonlinear Systems"*, IEEE Transactions on Industrial Electronics, Vol. 47, No. 3, June 2000, pp. 574-581.

[5] Mitić D. Milosavljević Č., *"Sliding Mode Based Minimum Variance Control and Generalized Minimum Variance Controls with O(T2) and O(T3) Accuracy"*, Electrical Engineering (Archiv fur Elektrotechnik), Vol. 86, No. 4, July 2004, pp. 229-239.

Bandgap Voltage Reference in CMOS

Milan Savić and Vančo Litovski

Abstract - This paper presents an example of the CMOS bandgap voltage reference design. Proposed circuit is fabricated in CMOS 0.35μm. Temperature variations of the reference voltage are measured and the results are presented.

Keywords – Bandgap reference, CMOS

I. Introduction

Analog circuits incorporate voltage and current references extensively. Such references are dc quantities that exhibit little dependance on supply and process parameters and a well-defined dependance on the temperature.

As a part of the wider project, a bandgap voltage reference for supplying ADC is being designed. Temperature range of interest is -40 to 80 °C. Other requirements are: high PSRR and small chip area. Standard CMOS process is used (Alcatel Semiconductors CMOS 0.35 μm C035M-A 5M/2P/HR), where only vertical PNP bipolar transistor is available.

This paper is organized as follows. Section 2 discusses the concepts used in this design. Section 3 describes the proposed circuit. Circuit performance is presented in Section 4.

II. Design Objectives

The overall objective of designing a precision reference is to achieve high accuracy over all working conditions. Most important are: temperature variation, process variation and supply variation. Concepts of reducing the impact of those variations on reference voltage deviation, which were used in the proposed circuit, will be explained in the following.

The base-emiter voltage of bipolar transistor or, more generally, the forward bias voltage of a pn-junction diode exhibits negative temperature coefficient (TC). On the other hand, two bipolar transistors that operate at unequal current densities, exhibit difference between their base-emitter voltages that is directly proportional to the absolute temperature. Using these negative- and positive-TC voltages, a reference having a nominally zero temperature coefficient can be developed.

Well known simple PTAT (Proportional To Absolute Temperature) current generator topology is shown in Fig. 1. [1]. This circuit has a zero-current quiscent state. In order to avoid this state, a start-up cicuit is requiered. The output current of this circuit is very power supply voltage dependant. This can be reduced by using cascode current mirrors. Voltage difference between nodes X and Y is the most common source of inaccuracies. In order to avoid this, an operational amplifier can be used, with X and Y as inputs, as shown in Fig. 2. Here, PTAT the voltage, equal to $I_{\text{out}}R_2$, is added to the base-emitter voltage (negative-TC), providing voltage with nominally zero temperature coefficient.

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The output voltage equals:

$$V_{\text{ref}} = V_{\text{BE3}} + (R_2/R_1)\cdot V_{\text{T}} \cdot \ln n \qquad (1)$$

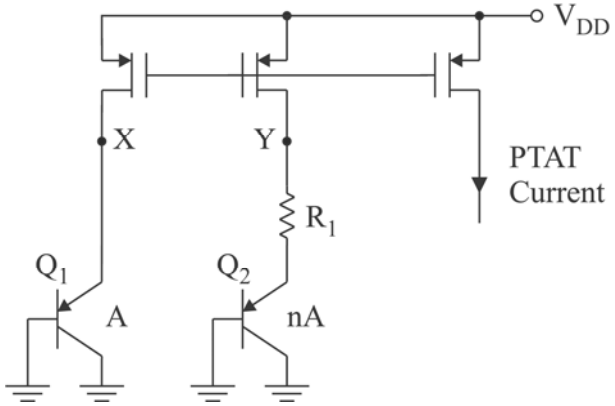

Fig. 1. Simple PTAT current source

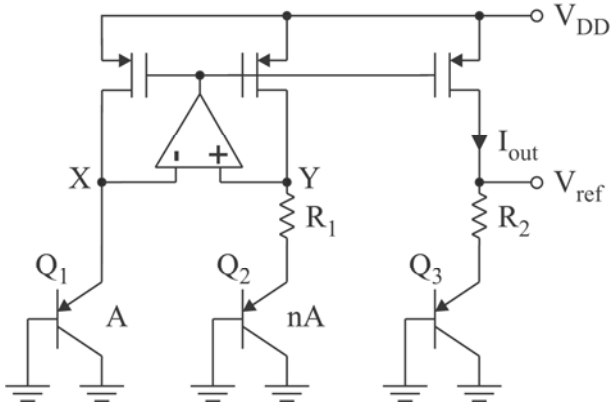

Fig. 2. Simple bandgap voltage reference

This reference is first-order voltage reference, because the PTAT cancels only the first-order term in the polynomial approximation that represents relationship between the diode voltage and temperature.

By adjusting the circuit elements, the value of the TC at room temperature can be set to zero. [1]

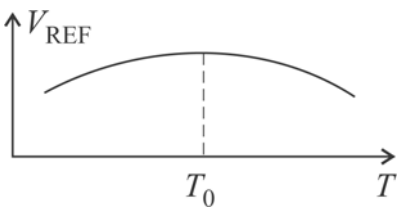

Fig. 3. Temperature dependence of a bandgap voltage

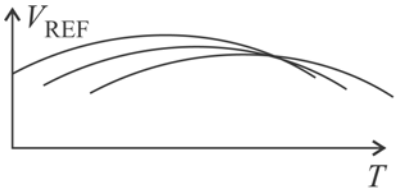

Fig. 4. Variation of the zero-TC temperature for different samples

Process variations have great impact on bandgap voltage deviation. Figure 4 presents the variation of the zero TC temperature for different samples (different process parameters). Trimming techniques offer the solution to this problem [2]. For the circuits with trimming network, PTAT current can be adjusted after fabrication. Voltage variations can be minimized by careful layout design. Namely, special attention should be paid on matching of the current mirror devices, resistors (R_1 and R_2 in Figure 2.) and BJTs.

Supply voltage variations, both dc and transient noise, result in reference voltage deviation. Line regulation performance refers to the steady-state voltage changes in the reference resulting from dc changes in the input supply voltage. The robustness and the stability of the circuit with respect to the power supply noise are defined as the power supply rejection (PSR). Though PSR refers to small-signal response, the general techniques used to improve line regulation will enhance PSR as well. [2]

III. Proposed Circuit

The design and layout considerations of the proposed circuit will be presented in this section.

A. Design

Proposed circuit is shown in Figure 5. Bandgap core is the same as the one presented in Figure 2. Startup circuitry is added to ensure that output voltage and regulated supply do not remain at ground when power is applied. On startup, MOS transistor MS5 forces current into the collector of the Q1. This ensures that the circuit avoids the zero-current state. While reaching the stable state of operation, the gate voltage of MS2 rises, and turns it on. As a result, gate voltage of MS4 decreases and turns off current through MS4, MS3 and MS5, driving the bandgap core into desired state of operation.

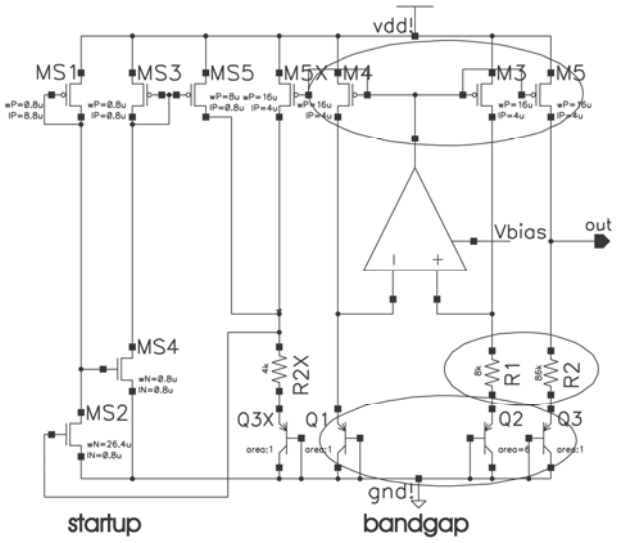

Fig. 5. Bandgap reference

Figure 6 presents the detailed circuitry of the operational amplifier used in the bandgap core.

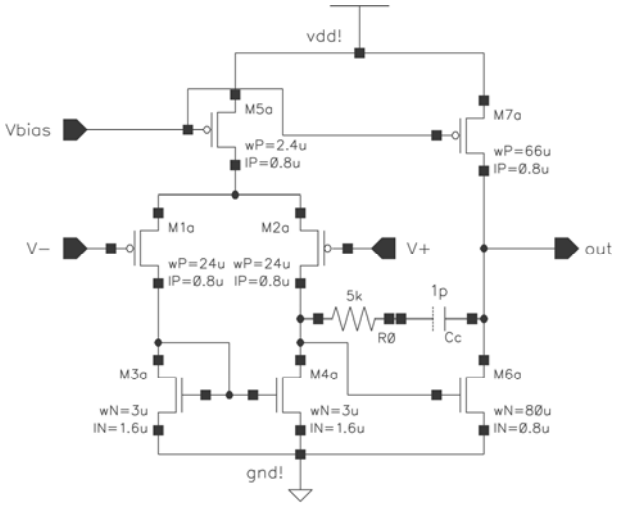

Fig. 6. Amplifier used in the regulated supply circuit

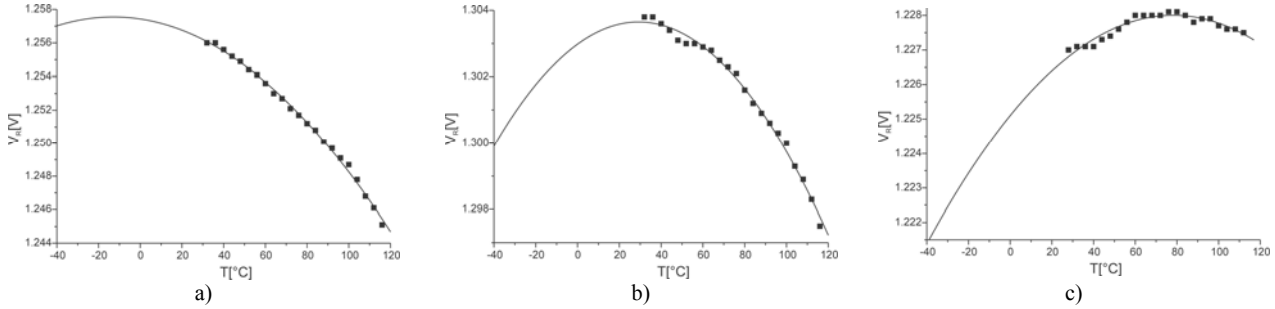

Fig. 7. Measurements on random samples.
Temperature coefficients are a) 44.7 ppm/°C b) 12.8 ppm/°C c) 41.5 ppm/°C
for the temperature range (-40 °C, 80 °C)

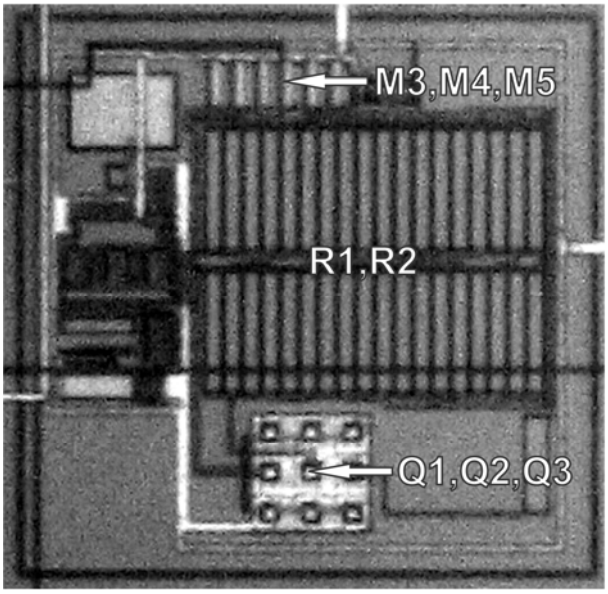

Fig. 8. Photomicrograph of the reference

B. Layout Considerations

Figure 8 presents the photomicrograph of the reference circuit. During layout design special attention was paid on matching. Namely, all the grouped circuit devices (see Fig. 5) should be closely matched in order to minimize the impact of process variations on the reference operation. Common centroid technique is applied for current mirror transistors, resistors and bipolar transistors, as shown in Figure 8. In order to minimize the impact of the substrate noise, the bandgap reference circuit is surrounded with ground ring. The reference power is supplied through separate pins, which minimizes the power noise.

IV. Circuit Performance

TABLE I
Performance Summary

Area	25214μm^2
Power	3.3mW
Supply	3.3 V

TABLE II
PSRR (Simulation)

Frequency	PSRR [dB]
DC	70
1 kHz	87
100 kHz	67

Figure 7 presents the measured results for three random samples. Reference voltage is measured for temperatures from 28°C to 120°C. In order to roughly assess the temperature coefficient for the temperature range of interest, i.e. -40°C to 80°C, measured results are fitted with second order polynomial curve.

It can be noted that measured samples exhibit temperature coefficient less than 50 ppm/°C. It can also be noted that nominal voltage variations are considerable.

Implementation of the trimming network would greatly reduce the additional temperature variation induced by the process variations. On the other hand, it would consume additional area and introduce more complex testing procedures. The variation of the nominal reference voltage can be circumvented with the calibration of the digital part of the system for which this bandgap is designed, so it does not present a problem.

And finally, the PSR performance simulations were performed. Table II gives the PSR variation with respect to frequency. The addition of the output off-chip 0.1 μF capacitor would greatly improve the PSR performance over higher frequencies.

IV. Conclusion

Proposed circuit fulfills the imposed requirements. Measured random samples exhibit the temperature coefficient less than 50 ppm/°C. DC power supply rejection is 70 dB according to performed simulations. Circuit occupies area of 25214 μm^2 and dissipates 3.3 mW with +3.3 V power supply. Measurements show the great impact of the process variations on the circuit performance. This can be reduced with implementation of the trimming network.

References

[1] Razavi, B., *"Design of Analog CMOS Integrated Circuits"*, McGraw-Hill, 2000.

[2] Rincon-Mora, G. A., *"Voltage References From Diodes to Precision High-Order Bandgap Circuits"*, Wiley, 2000.

[3] Brooks, T., Weatwick, A. L., *"A Low-Power Differential CMOS Bandgap Reference"*, ISSCC Dig. of Tech. Papers, pp. 248-249, Feb. 1994.

[4] Baker, R. J., Li, H. W., Boyce, D. E., *"CMOS Circuit Design, Layout and Simulation"*, New York, 1998.

[5] -, Cadence 2002 IC 4.46 Package Documentation.

[6] Litovski V., *"Projektovanje elektronskih kola: simulacija, optimizacija, testiranje, fizičko projektovanje"*, Nova Jugoslavija, Vranje, 2000. (in Serbian)

Verification of Digital System Test Patterns using a VHDL Simulator

Miljana Sokolović, Mark Zwolinski

Abstract - In this paper an approach for test pattern verification for a digital system-on-chip is proposed. It is based on digital system simulation using a standard VHDL simulator. The approach is verified for two arithmetic blocks which are parts of an integrated power-meter and represent large combinational digital systems.

Keywords – Testing, VHDL.

I. INTRODUCTION

Integrated Circuit (IC) fabrication consists of a series of different steps including photolithographic printing, etching, doping, implanting, masking and chemical vapour depositioning. After these steps are applied, a complete IC can be obtained. IC surfaces are exaggerated in diagrams in order to distinguish between different layers of oxide, polysilicon and metal. Conversely, in reality, they are not at all flat. Even with exaggerations, the diagrams represent an idealized approximation of actual fabricated circuit structures [1]. The actual circuit structures are not nearly as well defined as textbook diagrams would lead one to believe. Cross sections of actual integrated circuit reveal a variety of nonideal physical characteristics that are not entirely under the semiconductor manufacturer's control. Thus, no fabrication process can be perfect and free of defects.

Real digital integrated systems may have a variety of defects. By testing them, a manufacturer can easily separate good and bad ICs. The quality of the IC is improved by testing since defective devices are not shipped to market. IC testing is a very expensive activity because no additional value is obtained.

Testing is an activity that implies the comparison of the fault free (ff) circuit response with the one obtained from the observed circuit, CUT (Circuit Under Test). There are two general testing concepts: functional and structural testing. Verification that the circuit satisfies all required functions is referred to as functional testing. For combinational digital circuits this is a very uninteresting and time consuming process, because all possible combinations of input patterns must be applied to the circuit inputs in order to make sure that its function is correct. It is also very difficult to apply this to circuits with a large number of inputs.

On the other hand, structural testing is defect-oriented. Instead of checking if the circuit functions correctly, here the test searches for defects. The aim of such testing is to determine a test signal that will ensure that the responses of the ff circuit and the faulty one are different. The algorithm for test signal generation based on the structural testing concept is shown in Fig. 1.

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Prepare the list of the defects
For each defect from the list
{
Select the next defect from the list;
Generate the test for the selected defect;
For all other elements from the defects' list
{
Remove those (defects) that are covered with the generated test;
}
}

Fig. 1. The algorithm for test signal generation based on the structural testing concept

Generating a test signal that will cover every possible defect in the circuit is a very complex job, especially in an industrial environment. Thus, it is necessary to avoid having a list of all theoretically possible defects and create a list of defects that is both realistic and short.

Structural testing is impossible to perform at a high level of design abstraction. Thus the HDL description of the system must be loaded into the synthesis tool, then the synthesis must be performed, and after that the real netlist of the system with the actual gates and connections can be obtained.

This paper presents a VHDL-based approach for validation of the test patterns for large digital combinational systems. The approach assumes that the synthesis of the system has already been performed and that the post synthesis netlist is available.

The paper is organized as follows. In the first section faults and defect issues are discussed. Some basic principles of digital systems testing are given in the second section. After that the steps in the digital system design are listed and explained. In one of those steps, ff gates are replaced with faulty ones. Then the general approach of test pattern verification is given. The section after gives the principles of modelling faulty combinational gates. This approach is applied to two examples of large combinational arithmetical circuits which are parts of the power-meter IC. These examples and the obtained results are presented in the last section.

II. FAULTS IN DIGITAL CIRCUITS

Faults have physical causes, called defects. Defects often consist of missing or an extra material, or of an impurity. Such defects at the layout level of the chip are translated into electrical faults and then into logical faults, such that they can be tested with logical signals. A fault is a model of behaviour due to the defect or the abstract model of the defect.

Faults can be single and structural. Single faults are related to fan-out issues, i.e. stems and branches. On the other hand, structural faults can be interconnect faults and

component faults. Interconnect faults are stuck-at faults, bridging (short) and open (break) faults. Component (transistor) faults are divided into stuck-open and stuck-short faults.

In order to make the test pattern generation easier, some assumptions about faults and physical defects can be made [3]. Mapping of defects into electrical, and thereafter into logical faults is called fault modelling. The principle of fault modelling is to reduce the number of effects to be tested by considering how defects manifest themselves. About 50% of faults that appear during tests in manufacturing are static faults. They are modelled with a single stuck-at fault model. According to this model a fault at one node is represented as either stuck at high level, that is 1, or low voltage level, that is 0.

There are many advantages of this kind of modelling. It can represent many physical faults. It is independent of technology, as shown in Fig. 3. Multiple faults also appear in digital circuits. But their relative probability of appearing is much lower. Most test pattern generation is based on single stuck-at faults, because detecting single stuck-at faults also detects many other faults. This kind of modelling significantly reduces the test size to a reasonable value. For an n-net circuit it gives approximately 2n faults. This representation can also be used to model other digital circuit faults.

Examples of defects modelled by stuck-at faults are shown in Fig. 3.

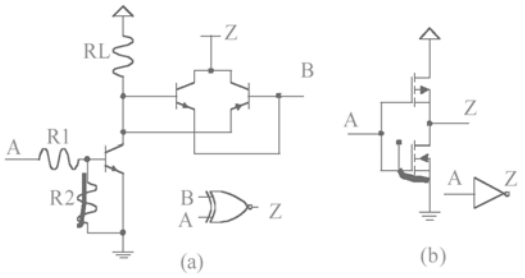

Fig. 3 Examples of static defects in logic gates; a) XOR BJT gate b) CMOS inverter

III. Principles of Digital Circuit Testing

The main aim here is to generate a test for a selected defect. This is the most important and the most difficult issue in the algorithm shown in Fig. 1 [2]. One test can be used for detecting a certain defect, only if it can guarantee observability and controllability.

Observability is the ability of the test to force the effect of the defect to at least one output of the circuit. Controllability, on the other hand, is the ability of the test to force a state at the defect node different to that caused by the defect.

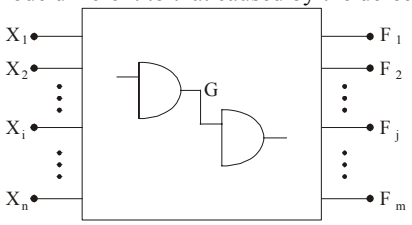

Fig. 4. The combinational circuit for the testing problem formulation

For the circuit shown in Fig. 4, n inputs are denoted with a vector $\mathbf{X}=[X_1, X_2, \ldots X_i, \ldots, X_n]$; m outputs are denoted with a vector $\mathbf{F}=[F_1, F_2, \ldots F_j, \ldots, F_m]$. Assume that it is necessary to create a test for the stuck-at fault at the node G, which is here denoted as G/s. The state at node G, can be expressed as the function of the input vector. The test must satisfy two requirements expressed by the following equations.

$$G(X) = \bar{s} \tag{1}$$

and,

$$F_j = (1, X) \oplus F_j(0, X) = 1. \tag{2}$$

These two equations present controllability and observability conditions. If at least one of these two equations is not satisfied, the defect is not testable in this way, but may be detected using some other approach (for example I_{DDQ}).

IV. Digital System Design

It is almost impossible to generate a structural test sequence for the VHDL behavioural description of a digital circuit. The description itself does not contain any information about the logic gates that will implement the design after synthesis. Because of that, in order to get the final testable post-synthesis netlist of the circuit, it is necessary to go through all digital circuit design steps. For this purpose the Cadence system was used here [3].

The design flow of an ASIC begins with simulation of the RTL (Register Transfer Level) description of the design in VHDL in order to verify the circuit's functionality. This simulation was performed in the NCSim simulator. Cadence PKS was used for logic synthesis, as well as for initial and final timing analysis. It takes a VHDL description of the design and appropriate technology libraries and generates a standard cell netlist. That netlist is imported into Silicon Ensemble to perform floorplanning, cell placement and routing. The clock tree is inserted by CTPKS, an integral part of Cadence PKS or by using a separate program, CTGen. The layout is completed within the Virtuoso layout editor. Back annotation can be performed for more accurate timing analysis based on the extracted parasitics from Silicon Ensemble.

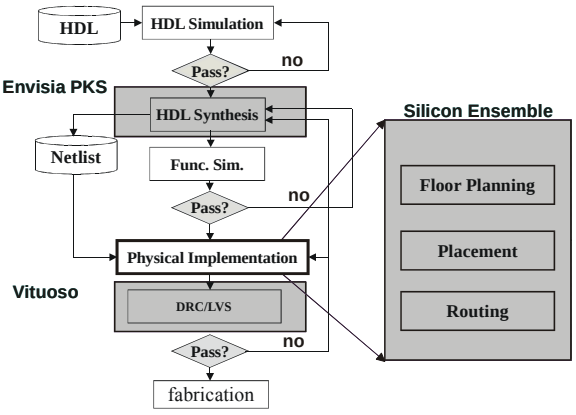

Fig. 5 Digital (ASIC) circuit design flow using Cadence

After these steps, a netlist of the circuit containing all actual library logic gates and their connections is available. For this netlist it is now reasonable to create a defect oriented test and to perform an estimation of the defect coverage as well as the generated test verification.

In this way two arithmetic blocks' netlists of interest were extracted. They were: a 24-bit combinational subtraction unit and a 48-bit addition-subtracting circuit.

V. The Approach of Test Pattern Verification

In order to perform test pattern verification it is necessary to have a post-synthesis netlist of the circuit, models of the faulty library elements used during the synthesis phase and the proposed test vectors. The aim of this verification is to determine the fault coverage of the proposed test sequence.

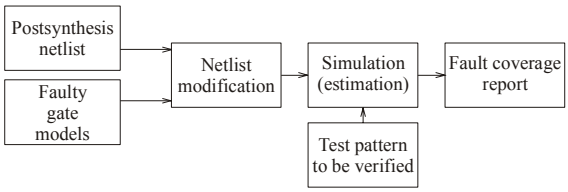

Fig. 6. The test pattern verification approach

The approach is shown in Fig. 6. First, the library logic gates used in the synthesis must be available in the VHDL netlist. Every logic gate must be modelled with all possible stuck-at defects. The modelling of the faulty gates will be explained later. The ff gates are then replaced in the netlist with the faulty ones. For a specified test sequences, the modified netlist is then simulated (using VHDL) for each of the defects specified in each logic gate. This simulation at the same time performs an estimation of the fault coverage. In this way we determine how many and which faults are left undetected with the proposed test sequence. After that an additional test can be generated and verified again in order to achieve 100% fault coverage.

VI. Modelling Faulty Library Logic Gates

Modelling of faulty gates here assumes the stuck-at faults models of the gates and devices are incorporated into their VHDL descriptions [4]. For testing the arithmetic circuits of interest, VHDL descriptions of faulty models for an inverter (inv), two input OR gate (OR2_fault), NXOR gate (EN_fault), and full adder (FA_fault), should be available. The 24-bit subtraction block and the 48-bit addition-subtraction circuit are shown in Fig. 7, while the modified library cells are shown in Fig. 8.

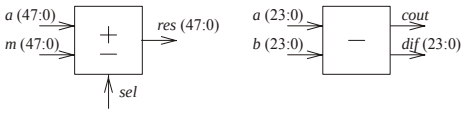

Fig. 7. Block diagrams of the observed combinational circuits a) addition-subtraction, b) subtraction

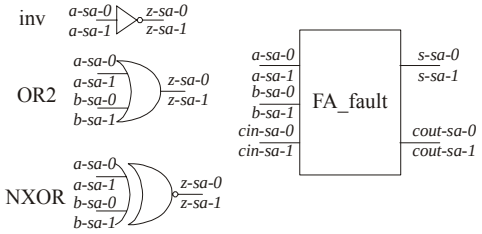

Fig. 8. Faulty logic gates

The model of each logic gate must contain the description of its behaviour for every possible stuck-at fault. Stuck-at faults are related to each gates' input or output. Fig. 9. gives the VHDL description of the NXOR logic gate. It is based on that in [4]. All other gates and circuits are similarly described

Now instead of the ff components from the library, these faulty model components are instantiated in the modified netlist. After this modification, the resulting circuits are simulated according to the testbench description given in [4]. In this VHDL testbench program, a file that contains the test pattern to be verified, is specified.

```
library IEEE;
use IEEE.std_logic_1164.all;
use work.fault_inject.all;
entity EN_fault is port (
            z: out STD_LOGIC;
            a: in STD_LOGIC;
            b: in STD_LOGIC);
end EN_fault;
architecture inject_fault of EN_fault is
begin
nn: process(a,b) is
variable z_sa1, z_sa0, a_sa0, a_sa1, b_sa0, b_sa1 : fault_ptr:=null;
begin
if z_sa1=null then
z_sa1:= new fault_model'(new string'(inject_fault'instance_name&"z_sa1"),
false,false,first_fault);
first_fault:=z_sa1;
.
.
.
end if;
if z_sa1.simulating then          z<='1'after 1ns;
elsif z_sa0.simulating then       z<='0'after 1ns;
elsif a_sa1.simulating then       z<= b after 1ns;
elsif a_sa0.simulating then       z<=not b after 1ns;
elsif b_sa1.simulating then       z<= a after 1ns;
elsif b_sa0.simulating then       z<=not a after 1ns;
else                              z<=not (a xor b)after 1ns;
end if;
end process nn;
end architecture inject_fault;
```

Fig. 9. VHDL model of the faulty NXOR logic gate

After running this simulation a file with the correct results is obtained as well as a file with a list of defects covered by the test pattern. At the end of this report file, the exact number of stack-at faults covered by the proposed test sequence is given.

TABLE I
OBTAINED SUBTRACTION RESULTS

A	B	Diff
000000H	000000H	000000H
FFFFFFH	FFFFFFH	000000H
FFFFFFH	000000H	000000H
000000H	FFFFFFH	000000H

It should be mentioned that for many other different combinational circuits, whose tests have been verified in this way, the most covering test patterns (always covers at least 90% of all stuck-at faults) are all zeros and all ones.

TABLE II
OBTAINED ADDING-SUBTRACTION RESULTS

A	M	sel	Diff
000000000000H	000000000000H	0	000000000000H
000000000000H	000000000000H	1	000000000000H
FFFFFFFFFFFFH	FFFFFFFFFFFFH	0	000000000000H
FFFFFFFFFFFFH	FFFFFFFFFFFFH	1	FFFFFFFFFFFEH

The file that gives the correct result (results.txt) of the subtraction is shown in Table I. Part of the obtained covering report (file faults.txt) is given in Fig. 10. Similar results are obtained for the addition-subtraction circuit. The results and fault coverage for this circuit are shown in Table II and in Fig. 11. It can be noted that 100% fault coverage is achieved for both examples.

```
:test(test):uut@oduzimacoff1_n24(netlist):
fad12_23@fa_fault(inject_fault)cin_sa1
Fault #1
Detected by input: 000000000000000000000000 111111111111111111111111
outputs: 100000000000000000000001
expected outputs: 000000000000000000000001 at  400 ns  900 ns
.
.
.
:test(test):uut@oduzimacoff1_n24(netlist):
i_18450@inv(inject_fault)z_sa1
Fault #287
Detected by input: 000000000000000000000000 111111111111111111111111
outputs: 100000000000000000000001
expected outputs: 000000000000000000000001 at  400 ns143900 ns
Undetected:
Fault cover:
287faults,  287detected
```

Fig. 10. Partial verification report for the subtraction circuit

```
:test(test):uut@oduzimacoff1_n24(netlist):
fad12_23@fa_fault(inject_fault)cin_sa1
Fault #1
Detected by input: 000000000000000000000000 111111111111111111111111
outputs: 100000000000000000000001
expected outputs: 000000000000000000000001 at  400 ns  900 ns
.
.
.
:test(test):uut@oduzimacoff1_n24(netlist):
i_18450@inv(inject_fault)z_sa1
Fault #287
Detected by input: 000000000000000000000000 111111111111111111111111
outputs: 100000000000000000000001
expected outputs: 000000000000000000000001 at  400 ns143900 ns
Undetected:
Fault cover:
287faults,  287detected
```

Fig. 11. Partial verification report for the adder-subtraction circuit

VII. Conclusion

A method for test pattern verification in combinational circuits is presented in this paper. It is based on VHDL simulations and is used and verified with examples of two arithmetic circuits of the integrated power-meter. Future work will extend the concept to sequential circuits.

References

[1] Burns, M., Roberts, G., "*An Introduction to Mixed-Signal IC Test and Measurement*", Oxford University Press, New York, 2001.

[2] Litovski, V., "*Electronic Circuit Design*", in Serbian, Nova Jugoslavija-Vranje, Niš, 2000.

[3] Dimitrijević, M., Jovanović, B., Anđelković, B., Sokolović, M., "*Experiences in Unisg Cadence – The Industry Standard for Electronic Circuit Design*", Proc. of the XLVII Conference of ETRAN, Herceg Novi, 2003, Vol. 1., pp. 31-34.

[4] Zwolinski, M., "*Digital System Design with VHDL*", Prentice Hall, UK, 2004.

VHDL-AMS Modeling and Compilation for Parallel Mixed-Mode Simulation

Bojan Anđelković, Marko Dimitrijević and Milunka Damnjanović

Abstract – In this paper a survey of recommended VHDL-AMS modeling practices for effective parallel simulation is given. Also, a need for extension of VHDL-AMS standard is considered in order to enable the designer to influence parallel simulation performance during the model development. Mixed-mode circuit partitioning algorithms that should be applied during the model compilation are presented.

Keywords – Parallel mixed-mode simulation, VHDL-AMS

I. Introduction

Today's high end integrated circuits may contain millions of transistors and becoming increasingly complex in the diversity of devices (embedded software, micro-electro-mechanical components). Having in mind the rapid growth of the electronic systems complexity and short time-to-market demands, the simulation has become time consuming and represents a bottleneck in the design flow. The modern simulation is based on system modeling in one of standard Hardware Description Languages (HDL), such as VHDL-AMS [1], which support an easy description of mixed-signal VLSI systems with various portions described at different abstraction levels. VHDL-AMS simulation is a compute intensive, particularly for large models. In order to accelerate the simulation process and reduce very long simulation runtimes of such HDL descriptions parallel simulation tools can be used [2]. Parallel simulation is based on splitting the circuit into several pieces and simulating them in parallel one piece per workstation. The potentially larger amount of the memory in workstation clusters will enable the execution of larger simulation models.

This paper contains some VHDL-AMS modeling recommendations necessary to achieve high-performance parallel simulation. Also, existing partitioning methods that should be performed during the VHDL-AMS model compilation are presented. A need for extension of VHDL-AMS in order to adapt it for the use in parallel simulations is considered.

A brief overview of VHDL-AMS modeling features is presented in Section II. Also, some modeling recommendations for the development of VHDL-AMS models for parallel simulations are given. Mixed-mode circuit partitioning techniques performed during the VHDL-AMS model compilation are discussed in Section III. Section IV summarizes the presented survey of parallel modelling recommendations and partitioning algorithms together with some future work directions.

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II. VHDL-AMS Modeling Features

A. VHDL-AMS Model Description

VHDL-AMS is an Analog and Mixed-Signal extension to the Very-High-Speed-Integrated-Circuits Hardware Description Language (VHDL). It is a combination of the base IEEE Std 1076-1993 (VHDL) standard and IEEE 1076.1-1999. (analog and mixed-signal extensions) [3]. VHDL-AMS is an internal name, widely used in the designers' community, for the combination of these standards.

VHDL-AMS provides behavioral and structural description of both discrete and continuous systems. Being a superset of VHDL it inherited all its advantages such as structural and functional decomposition, separate compilation, a powerful sequential notation, and the strong type system of a modern programming language. The discrete models are specified using component instantiations, concurrent signal assignment and the process statement. Modeling of continuous systems is based on the theory of Differential and Algebraic Equations (DAEs). DAE-based continuous systems can be modeled similar to discrete models at several hierarchical levels. A special notation for DAE's is introduced describing precisely what system of equations is implied at each simulation time. VHDL-AMS also has the ability to describe non-electrical physical phenomena. Mixed-discipline models with different domains such as electrical, physical, and thermal can be described and simulated in a single entity.

A structure of a VHDL-AMS model and an overview of the language elements and statements are given with the help of a simple RC circuit model with a pre charged capacitor shown in Fig. 1 [4].

For representing the unknown continuous variables in the system of DAEs, VHDL-AMS introduces a new class of objects, the *quantity* [5]. Quantities can also be declared as ports of the model (the points that can be connected to other models). Additional branch quantities are provided to support conservation semantics of the systems like electrical circuits. There are two kinds of branch quantities: across quantities representing effort like effects such as voltage or temperature, and through quantities for flow like effects such as current and fluid flow rate. In the RC circuit example, the branch quantities are capacitor and resistor voltage and current. They are declared with reference to two *terminals*. Terminals can be of different *natures* that represent distinct energy domains (electrical, thermal, etc.). Using of terminals as ports of the model enables constructing nodes on hierarchical descriptions when such model is instantiated.

```
-- Set initial value (pre charged capacitor)

LIBRARY DISCIPLINES;
LIBRARY IEEE;

USE DISCIPLINES.ELECTROMAGNETIC_SYSTEM.ALL;
USE IEEE.MATH_REAL.ALL;

ENTITY RC IS
END;

ARCHITECTURE behav OF RC IS
    TERMINAL n1,n2: ELECTRICAL;
    QUANTITY v_in ACROSS i_in THROUGH  n1 TO electrical_ground;
    QUANTITY u_r ACROSS i_r THROUGH n1 TO n2;
    QUANTITY u_c ACROSS i_c THROUGH n2 TO electrical_ground;
BEGIN


    BREAK  u_c => 0.5;       --initvalue

    v_in == 1.0;      --constant  voltage source
    i_r  == u_r  / 1000.0;      --resistor  equation
    i_c  == 1.0e-6 * u_c'dot;   --capacitor equation
END;
```

Fig. 1. VHDL-AMS model of an RC circuit

The system of DAEs can be described using *simultaneous statements*. These statements express the system behaviour by specifying relationships between quantities. The language supports two quantity attributes (*'dot* and *'integ*) to specify derivatives and integrations over time, respectively. VHDL-AMS also provides two special simultaneous statements, called *simultaneous if* and *simultaneous case*, to change the set of equations. These statements include conditional expressions and depending of their satisfaction appropriate set of equations is solved.

A special construct called the *break* statement is used to represent discontinuities in VHDL-AMS model descriptions. It specifies new initial conditions and the possible occurrence of a discontinuity. The model developer should provide the necessary break statements to notify the simulator of possible discontinuities. In the example, break statement is used to setup initial value for capacitor voltage.

Since DAE solvers use numerical algorithms to solve the equation systems, VHDL-AMS enables the designer to specify individual tolerances for quantities which must be satisfied by the simulator. It gives the designer an opportunity to trade between accuracy and simulation speed, as more accurate solutions require longer simulation runtimes.

VHDL-AMS is developed as a universal and tool independent language for modeling and documentation of both analog and digital devices and physical subsystems from other domains. That enables the designer to focus on the model equations without distraction of specific simulator internals. In that way they can create models with different abstraction levels that improve significantly simulation speed.

B. Modeling Recommendations for Parallel Simulation

A set of recommended VHDL-AMS modeling practices to help designers achieve effective parallel simulation is given in [6]. Performances of VHDL-AMS parallel mixed-mode simulation depend on hardware processing environment (number of processors, interconnecting network), VHDL-AMS compiling techniques, and VHDL-AMS models used for simulation. Some model features, such as model complexity, model abstraction and stimulus influence parallel simulation performance, but the designer cannot do anything to improve them. However, there are some modeling issues that can be under model developer's control. These modeling issues include simulation time resolution, number of processes, data types, and shared variables.

VHDL-AMS gives the designer an opportunity to develop models at many levels of abstraction. In sequential simulation executing on a single processor, less abstract models increase simulation time. However, when parallel simulation is used, increasing the number of details in a model can yield more units capable of executing concurrently. In that way, when more detailed models are used, it is possible to achieve parallel simulation speedup comparing to a uni-processor. When such models are developed for parallel simulation, it is necessary to enable de-coupling between model elements in order to improve simulation performance.

The use of physically-oriented delay or parasitic information (such as SDF and VITAL) during VHDL-AMS simulation decreases parallel simulation performance. These timing models distribute evaluations at a wider range of time instants in the simulation time domain and that decreases parallelism. Better performances can be achieved by reducing the precision of delay and other timing parameters in the model.

In order to improve parallel simulation performance, VHDL-AMS models should consist of more processes, tasks, or their equivalents than there are processors executing simulation.

The transmitting events between processors on a parallel computer influence the simulation performance more than when the communication is performed in the memory subsystem of single-processor architecture. Therefore, if it is necessary to transmit more than one scalar signal value at the same time between different processors (i.e. workstations on a computer cluster), parallel simulation performance can be improved by aggregating these scalars into a single composite event. Such aggregation can be automatically implemented during the VHDL-AMS compilation process, as described in [7], or the designer can implement such aggregation during the development of VHDL-AMS model source code.

Shared variables added in VHDL'93 standard can decrease parallel simulation efficiency, because they require communication between two or more processes in which they are used. Therefore, the model developer should avoid use of variables referenced by more than one process. If such variables must be used it is necessary to maximize the variable's locality to as few processes as possible.

Besides mentioned discrete-event modeling recommendations, there are also recommended continuous-domain modeling practices given in [6]. The parallel VHDL-AMS model developer can maximize simulation performance of analog and mixed-signal systems through appropriate use of circuit decomposition, tolerances and discontinuities.

In order to reduce communication latency during parallel simulation, large mixed-signal systems should be described as a collection of smaller continuous-domain models completely surrounded by discrete-event models.

As mentioned in the previous subsection, in VHDL-AMS quantity tolerances that must be satisfied during the equation system solving, can be specified. It is recommended to use broader tolerances, because in that way it is easier to divide the parallel solver among different cluster nodes by facilitating convergence of independent parts of the solution. However, broad tolerances give less accurate simulation results, so a compromise between parallel simulation performance and solution accuracy should be made.

Situations in which implicit or explicit value discontinuities occur in a quantity should be avoided. Use of VHDL-AMS ramp and slew quantity attributes reduces the impact of discontinuities on parallel simulation.

III. VHDL-AMS COMPILATION FOR PARALLEL SIMULATION

A. Parallel Mixed-Mode Simulation

A survey of parallel mixed-mode simulation algorithms and implementations is given in [2]. Mixed-mode designs are particularly convenient for parallel simulation, since they are by default partitioned into analog and digital parts that can be executed concurrently. Therefore, a parallel mixed-mode simulator consists of two distinct simulation kernels: continuous-time differential equation simulation kernel and discrete-event simulation kernel. In order to achieve parallel mixed-mode simulation, appropriate synchronization protocols [8] between these analog and digital simulation kernels are necessary.

Digital components in parallel discrete-event simulation are modeled as a collection of concurrently executing logical processes (LPs) that communicate via message passing. LPs can be assigned to different cluster nodes and distribute the simulation across the network of workstations.

The domain decomposition technique described in [9] is often used for parallelization of differential equation solvers.

B. Mixed-Mode-Circuit Partitioning

High-performance parallel simulation requires partitioning the simulation model into several parts in order to simulate one part per processor. Electronic circuits have natural clustering that can be used to achieve good partitioning results.

The partitioning methods are based on either parallelism in the simulation algorithm or in the circuit being simulated. Partitioning based on simulation algorithm is limited by the properties of specific algorithm used for simulation. The later method exploits the concurrency and parallelism in the circuit structure in order to minimize communication between cluster nodes and balance the nodes workload.

In parallel discrete-event simulation (PDES), the system under simulation is modeled as a collection of concurrently executing logical processes (LPs) that communicate via message passing. LPs then maybe assigned to different cluster nodes, thus distributing the simulation across the network of workstations.

Many of the partitioning algorithms for parallel logic simulation are based on a directed graph representation of the simulated circuit. In such representation the vertices of the graph denote logic components while edges represent signals. In [10] a multilevel approach to partitioning is proposed. It optimizes all factors for improving parallel logic simulation by decoupling them into separate phases.

The main objective in partitioning is to reduce the simulation time through equal load balance of processors and low communication overhead. Since, interconnecting signals between partitions cause time consuming communication, it is necessary to achieve a small number of signals connecting the partitions.

The partitioning should also provide equal workload for all slave nodes which enables optimal distribution of simulation effort. In order to estimate the workload, each circuit element can be assigned a weight according to its simulation complexity. One such partitioning method is COPART [11] implemented in TITAN parallel transistor level simulator. It reads the circuit description in SPICE and after partitioning a SPICE netlist for each partition is created, which is required for parallel simulation. In this method the structure of the circuit is mapped to an undirected graph, where the nodes represent the circuit elements and the edges are the signals connecting them. Appropriate weights for the nodes and the edges are assigned representing the simulation effort needed to simulate the element (i.e. the node in the graph). Signals connected to a lot of elements are widely distributed over the circuit and their cutting cannot be avoided during the partitioning. Therefore, such signals have lower weights meaning lower significance during the partitioning. The partitioning process is focused on signals connected to a few elements to avoid cutting them. Similar workload for each cluster node is achieved if the element weight sums are similar for all partitions. As the partition simulations are synchronized by the master process, a master circuit description with special references to the cut nets is also created.

Mixed-signal VHDL-AMS simulator SEAMS [12] exploits component-level partitioning and *analog island* modeling to completely partition the VHDL-AMS description at the entity-architecture level and simulate the partitioned system on a workstation cluster. SEAMS analyzes the VHDL-AMS model description and generates a set of characteristic expressions (CEs) from the simultaneous statements. CEs gover the behavior of the continuous part of the mixed-signal system. Partitioning of a VHDL-AMS model, implemented in SEAMS, is based on grouping and solving for the unknowns occurring in a connected set of CEs. The set of CEs consists of equations that are sufficient to determine the unknowns in the set. The criterion for grouping depends on the characteristics of the equations in the model. A single set of CEs is called *analog island*. The objective in partitioning is that no two analog islands may communicate during simulation. Break conditions and quantities are used for the communication between the discrete-event and the continuous processes.

As it can be seen, only partitioning algorithms which guarantee a minimum communication overhead may be able to provide good speed-up on workstation cluster. The mapping of LPs to workstations can be performed automatically based on some partitioning and load-balancing heuristics. However, automatically parallelized code generally cannot achieve good speed-up. Sometimes the model developer is in much better position to know the runtime characteristics of the processes and would want to manually perform partitioning and load-balancing. Therefore special parallel simulation languages, such as Parsec [13] have been developed. They allow user to influence parallel simulation performances during the model development. Parsec is a C-based PDES language that allows the model developer to specify the specific node on which an entity will be created by using an appropriate option during entity creation. It enables that model can be partitioned in such way that message communication between nodes is minimized, with balanced computation load. Also, the language has special constructs to specify communication between entities and control the execution of all processes [14]. Each entity will execute its own tasks, and if necessary, communicate

with one another by sending and receiving messages. One code example in Parsec is shown in Fig. 2 [14]. In this example the entity *worker* performs some tasks, then receives a *storeRequest* message from another entity, stores the message, and resumes working on another task.

Similar constructs can be added to VHDL-AMS in order to extend the standard language and allow the user flexibility to influence simulation performance during the model development. Desired features for PDES languages can be found in [14] and can be used as a basis in the development of VHDL-AMS extensions for parallel simulations.

```
entity worker {
  …
  doTask();
  receive (storeRequest msg) {
     storeMessage(msg);
  }
  doMoreTask();
}
```

Fig. 2. Parsec code example

IV. CONCLUSION

VHDL-AMS is a standard mixed-signal HDL that promises to play very important role in the specification and verification of mixed-signal systems. Since it is tool and vendor independent, it has advantages over other simulator specific parallel simulation languages. However, in order to use VHDL-AMS for parallel simulation some constructs and elements from parallel simulation languages should be added into VHDL-AMS. It would give the designers an opportunity to take advantage of standard HDL together with ability to have more control over parallel simulation performance during the model development. Also, the designer should follow presented modeling recommendations to achieve effective parallel simulation. During the compilation of VHDL-AMS models, appropriate partitioning techniques should be applied to minimize communication between cluster nodes and enable equal workload.

REFERENCES

[1] Christen, E., Bakalar, K., "*VHDL-AMS – A Hardware Description Language for Analog and Mixed-Signal Applications*", IEEE Trans. CAS, Vol. 46, No. 10, Oct., 1999., pp. 1263-1272.

[2] Savić, M., Anđelković, B., Litovski, V., "*Parallel Mixed-Mode Simulation – Preliminary Study*", Proc. of V Symposium on Industrial Electronics INDEL 2004, Nov., 2004, pp. 76-79

[3] IEEE Computer Society, "*IEEE Standard VHDL-AMS Language Reference Manual*", IEEE Computer Society, 1999.

[4] http://www.hamster-ams.com

[5] Ashenden, P., Peterson, G., Teegarden, D., "*The System Designer's Guide to VHDL-AMS*", Morgan Kaufmann Publishers, San Francisco, 2003.

[6] Peterson, G., Willis, J., "*High-Performance Hardware Description Language Simulation: Modelling Issues and Recommended Practices*", Trans. of The Society for Computer Simulation International, Vol. 16, No. 1, 1999., pp. 6-15.

[7] Willis, J., Siewiorek, D., "*Optimizing VHDL Compilation for Parallel Simulation*", IEEE Design & Test of Computers, Sep., 1992, pp.

[8] Frey, P., Radhakrishnan, R., "*Parallel Mixed-Technology Simulation*", Proc. of the 14th Workshop on Parallel and Distributed Simulation PADS'00, May, 2000, pp. 7-14.

[9] Fröhlich, N., Riess, B., Wever, U., Zheng, Q., "*A New Approach for Parallel Simulation of VLSI Circuits on a Transistor Level*", IEEE Trans. CAS, Vol. 45, No. 6, Jun, 1998, pp. 601-613

[10] Subramanian, S., Rao, D., Wilsey, P., "*Study of a Multilevel Approach to Partitioning for Parallel Logic Simulation*", 14th International Parallel and Distributed Processing Symposium, May, 2000, pp. 833-836

[11] Fröhlich, N., Riess, B., Wever, U., Zheng, Q., "*A New Partitioning Method for Parallel Simulation of VLSI Circuits on Transistor Level*", Proc. of Design, Automation and Test in Europe, 2000, pp. 679-684.

[12] Frey, P., Nellayappan, K., Shanmugasundaram, V., Mayiladuthurai, R., Chandrashekar, C., Carter, H., "*SEAMS: Simulation Environment for VHDL-AMS*", Proc. of the 1998 Winter Simulation Conference, Dec., 1998, pp. 539-546.

[13] Bagrodia, R., Meyer, R., Takai, M., Chen, Y., Zeng, X., Martin, J., Song, H., "*Parsec: A Parallel Simulation Environment for Complex Systems*", Computer, Vol. 31, No. 10, Oct., 1998, pp. 77-85

[14] Low, Y., Lim, C., Wentong, C., Huang, S., Hsu, W., Jain, S., Turner, S., "*Survey of Languages and Runtime Libraries for Parallel Discrete-Event Simulation*", Simulation, Vol. 72, No. 3, March, 1999, pp. 170-186

INSTRUCTION FOR AUTHORS

Name of the author/s, Affiliation/s

Abstract: *Short instruction for authors is presented in this paper. Works that are to be printed in the review "Electronics" should be typed according to this instruction.*
Keywords: *Review Electronics, Faculty of Electrical Engineering in Banjaluka, Instruction for authors.*

1. INTRODUCTION

In the review "Electronics", we publish the scientific and professional works from different fields of electronics in the broadest sense like: automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. In addition to the scientific and professional works, we present new products, new books, B. Sc., M. Sc. and Ph.D. theses.

In order to enable the unification of the technical arrangement of the works, to simplify the printing of the review "ELECTRONICS", we are giving this instruction for the authors of the works to be published in this professional paper.

2. TECHNICAL DETAILS

2.1. Submitting the papers

The works are to be delivered to the editor of the review by the E-mail (elektronika@etfbl.net) or on floppy (or CD) by post mail to the address of the Faculty of Electrical Engineering (Elektrotehnicki fakultet, Patre 5, 78000 Banja Luka, Republic of Srpska, Bosnia and Herzegovina).

2.2. Typing details

The work has to be typed on the paper A4 format, 8.27" width and 11.69" height (21.0x29.7 cm), upper margin of 1" (2.54 cm) and lower margin of 0,59" (1,5 cm), left and right margins of 1,57" (2 cm) and 0,39" (1cm) (mirrored margins). The header and footer are 0,5" (1.27cm) and 57" (2 cm). The work has to be written in English language. Our suggestion to the authors is to make their works on a PC using the word processor MS WORD 97/2000, and for the figures to use the graphic program CorelDraw, if the graphs are not going from the original programs, i.e., from the programs received (like MATLAB).

The title of the work shall be written on the first page, in bold and 12 pt. size. Also, on the first page, moved for one line spacing from title, the author's name together with the name of his institution shall be printed in the letter size (10pt, *Italic)*. The remaining parts of the manuscript shall be done in two columns with 0.5cm distance. The work shall be typed with line spacing 1 (Single) and size not less than 10 pt (like as this instruction). After the title of the work and the name of the author/s, a short content in English language follows, written in italics. The subtitles in the text shall be written in bold, capital letters of the size as in the text (not less than 10 pt.). Each work shall, at the beginning, comprise a subtitle INTRODUCTION, and, at the end, the subtitles CONCLUSION and BIBLIOGRAPHY / REFERENCES.

The operators and size marks that do not use numerical values, shall be written in common letters. The size marks that can use numerical values shall be written in italics. The equations shall be written in one column with right edge numeration. If the breaking of equations or figures is desired, those may be placed over both columns.

Illustrations (tables, figures, graphs etc.) may be wider than one column if necessary. Above a table there shall be a title, for instance: Table 2. *The experimental measuring results.* The same applies to figures and graphs but the accompanying text comes underneath the figure of graphs, for instance: Fig.3: *Equivalent circuit diagram...*

The work should not be finished at the beginning of a page. If the last manuscript page is not full, the columns on that page should be made even. Number of pages should not go over 6.

3. CONCLUSION

This short instruction is presented in order to enable the unification of technical arrangement of the works.

4. REFERENCES

At the end of work, the used literature shall be listed in order as used in the text. The literature in the text, shall be enclosed in square brackets, for instance: ...in [2] is shown ...

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