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Часопис "Електроника" у издању Електротехничког факултета у Бањој Луци ослобођен је плаћања пореза на промет на основу мишљења Министарства науке и културе Републике Српске, број 06-75/97 од 20. новембра 1997. године

PREFACE

Symposium INFOTEH®-JAHORINA is continuation of the International symposium JAHORINA that was held last time on April 1991.

The main organizer of the Symposium is the Faculty of Electrical Engineering East Sarajevo and the co-organizer is the Faculty of Electrical Engineering Banja Luka. The Symposium is supported by The Faculty of electrical engineering, Belgrade, Serbia and Montenegro, the Faculty of electronics, Niš, Serbia and Montenegro, the Faculty of technical sciences, Novi Sad, Serbia and Montenegro.

The goal of the Symposium is multidisciplinary survey of the actual state in the information technologies and their application in the industry plants control systems, the communication systems, the manufacturing technologies, power system, as well as in the other branches of interest for the successful development of our living environment.

During the first Symposium INFOTEH®-JAHORINA 2001, that was held on 12-14 March 2001 in the hotel Bistrica at Jahorina, 53 works have been presented, six companies presented their development and manufacturing programs in telecommunications, power electronics, power systems and process control systems. More than hundred participants took part in the Symposium working. Round table about potentials and possibilities of economic cooperation between Republic of Srpska and FR Yugoslavia has been held during the Symposium, regarding successful appearance at domestic and foreign market.

During the second Symposium INFOTEH®-JAHORINA 2002, that was held on 25-27 March 2002, 76 works have been presented, and five companies presented their development and manufacturing programs. More than hundred and thirty participants took part in Symposium working. Round table entitled "Reforms in high education – step forward to the European University" has been held during the Symposium.

The third Symposium INFOTEH®-JAHORINA 2003 was held on 24-26 March 2003. More than hundred and fifty participants took part in the Symposium working, coming from Serbia, Montenegro, United Kingdom and Republic of Srpska. At the Symposium 73 papers have been presented and nine student papers. Four companies presented their development and manufacturing programs. Round table entitled "New Technologies and Industrial Production Capabilities for small Countries in the Transition Process" has been held during the Symposium. All papers are presented in symposium proceedings, CD version.

The fourth Symposium INFOTEH®-JAHORINA 2005 was held on 23-25 March 2003 in the hotel Bistrica at Jahorina. The main topics of the Symposium were: Computer science application in control systems, Information-communication systems and technologies, Information system in manufacturing technologies, Information technologies in power systems, Information technologies in other branches of interest. More than hundred and seventy participants took part in the Symposium working, coming from Serbia, Montenegro, Republic of Srpska, Federation of Bosnia and Herzegovina, Croatia and Macedonia. At the Symposium two invited papers, eighty and three papers and three student's papers have been presented. Three companies presented their development and manufacturing programs. All papers are presented in symposium proceedings, CD version (ISBN-99938-624-2-8).

This issue of international journal “Electronics” includes the most interesting papers selected from the fourth Symposium INFOTEH®-JAHORINA 2005.

I would like to invite all readers of the “Electronics” journal to take active participation at the next Symposium INFOTEH®-JAHORINA. Updated information can be obtained from the Symposium web page: http://www.infoteh.rs.ba.

Professor Slobodan Milojković. Ph. D.
Chair, INFOTEH®-JAHORINA 2003 Programmee Committee

SHORT BIOGRAPHY OF GUEST EDITOR

Slobodan M. Milojković was born in Belgrade, Serbia and Montenegro on 26 June 1941. He received the B.Sc. and M.S.E.E. degrees from the University of Belgrade in 1963, 1975, respectively, and Ph.D. degree from the University of Sarajevo in 1978. In January 1964, he joined the Institute of Thermo Technique and Nuclear Technique, Energoinvest, Sarajevo, where he worked in modeling and numerical simulation in the various physical processes: nuclear technique, termo technique, electrical engineering, electrochemistry, electrothermal engineering, electromagnetic. In September 1964, he began academic career as an honorary lecturer in the Faculty of Electrical Engineering. In May 1970, he was an honorary docent, teaching courses in theoretical electrical engineering. In January 1981, he joined the Faculty of Electrical Engineering, University of Sarajevo, where he is presently Full Professor, teaching courses in theoretical electrical engineering. From October 1994 to April 1996, he worked as a Guest Professor at Technical University of Munich in High Voltage Institute. During that time, he was working on the development of the software modules for modeling, calculation and visualization of electromagnetic fields in high voltage equipment. The Asea Brown Boveri AG Research Center, Heidelberg, used those newly created modules in a software package POLOPT®. He led research projects supported by international organizations and commercial enterprises. His current research interest involves the computer-aided design of electromagnetic devices. Dr S. Milojković is one of the authors of monograph "Integral Methods for the Calculation of Electric Fields, for Application in High Voltage Engineering", Scientific Series of the International Bureau Research Center Juelich - Germany, 1992, ISBN 3-89336-084-0. He is also author of 6 books and over 10 scientific journal papers, 30 conference papers and 70 research projects. He was the supervisor of nearly 70 Diploma engineering thesis, 15 Master thesis and 4 Ph.D. thesis. Dr S. Milojković was awarded the Prize of the enterprise Energoinvest Sarajevo, the Gold medal of Technical Military Academy Rajlovac, the Gold diploma of the Faculty of electrical engineering Sarajevo, the Diploma of the Faculty of electrical engineering Tuzla, the Gold diploma of the University Sarajevo.

SYSTEM FOR SPACE AND FACILITIES PROTECTION CONTROL

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Abstract: *One practically realized system for space and facilities protection control is described in the paper. The system is realized using two types of 8-bit CMOS microcontrollers PCI 16F84A and PIC 12F629. Basis of the system are two units, main unit and remote control unit. Main unit is located at the entrance of space or facility that is protected. That unit realizes all operations connected with access authorization and opening or closing of entrance in space/facility. Remote control unit is portable and is used for identification at entrance in facility/space. That unit transmits code that main unit receives. Main unit checks the code and access permission and opens entrance or disables access in facility/space. The system can be used for protection of individual facilities or for protection of more facilities. By programming it can be obtained necessary level of complexity and security of protection. By interconnecting more main units and connecting with personal computer it can be realized information system for monitoring and control of protection of more facilities and spaces. Practical realization of main unit and remote control unit is described in the paper. Electrical schemes are given, way of functioning is described and parts of practically realized software are given for both units.*

Keywords: *Space and facilities protection, Microcontrollers, Main unit, Remote control unit, Access authorization and identification, Access code, Programming of level of complexity and security of protection, Information system for monitoring and control of access protection.*

1. INTRODUCTION

Protection, control and monitoring of access into spaces and facilities is very important and broad area where electronic devices and systems are used. Such devices and systems are mainly based on application of microprocessors and microcontrolers [1,2]. It enables obtaining very funcional but simple and cheap such systems and devices.

Application of microcontrolers for solving of practical problems is very simplified, speeden and cheapen process of electronic devices and systems design. Devices and systems based on microcontrolers are simpler in construction, have smaller number of components, and consecuently are more times cheaper and more reliable than similar devices and systems realised using other methods [1] .

One practically realized system for protection control of spaces and facilities where access is controlled is described here. The described system is realized using two types of 8-bit CMOS microcontrollers PIC 16F84A and PIC 12F629 from PIC Microchip family [3,4,6]. Basis of system are two devices, i.e. two units, main unit and remote control unit. The main unit is placed at entrance of facility/space where access is controlled. The remote control unit is portable. The system can be easily used for protection of individual facility/space or for protection of more facilities/spaces. By interconnection of more main units and their connection with personal computer it is possible to realize an information system for monitoring and control of protection of more facilities and spaces where access is controlled.

Practical realization of main unit and remote control unit is described in the paper. Their electrical schemes are given, way of functioning is described and parts of practically realized software for both units are given.

2. DESCRIPTION OF SYSTEM REALIZATION

Practically realized system that is described here is real example of specialized system realized using microcontrollers.

Basic requirements that were put before design of the system are:

- using the cheapest microcontrollers of PIC type,
- code for system control is entered or by keyboard or is emitted by remote control unit,
- communication beetwen system and user is performed by LCD type display,
- communication beetwen the remote control unit and the main unit is performed by infrared light,
- the main unit generates all needed signals for control of mechanism for open/close of entrance,
- code for open/close of entrance and the code length can be simplly changed,
- interruption of signal for control of mechanism for open/close is performed or after certain time or after action of final position switch,
- construction with minimal number of components to minimize cost of the system,
- independence of system on type of driving motor for mechanism for open/close of entrance,
- simple assembly of the system.

The system is completely realized according to given requirements. Minimal number of components is used and all complexity is transferred to software. Such concept allows that function and logic of the system can be almost completely changed without any change of system hardware.

The main unit is fixed device. It is placed at entrance of facility or space where access is controlled. Microcontroller PIC16F84A is used for the unit realization. It realizes all operations needed for check of access authorization and for opening or closing of entrance to facility/space. It also performs other functions, as is communication with user by LCD display used in main unit and generation of control signals needed for control and drive of mechanism that open/close entrance in facility/space. Possibilities and characteristics of the microcontroller are sufficient to realize all needed functions. External input and output elements for communication with user are added only. That are simple display of LCD type and keyboard with 10 keys. At the LCD display it is shown information about

facility or space where access is controlled, and information is the access enabled or disabled after attempt to open entrance. Also, data and other information during programming of the main unit are shown and controlled on the display. Function of keyboard is to enable using of system in situations when the remote control unit is failed or is losed. In that case it can be used keyboard. Also, keyboard is used during programming of the main unit.

The remote control unit is portable device. It has small dimensions and can be carried together with standard keys. It is used for identification during attempt to enter into facility/space. Main function is generation and emission of infrared light signal carrying code for control (opening/closing) of entrance into controlled facility/space. The main unit receives, decodes and checks the code and entrance permission, and opens entrance or prevents entry into facility/space. This remote control unit is realized using microcontroller PIC 12F629 whose low power consumption is ideal for portable devices with small dimensions supplied by batery. The power supply is realized by one standard comercial batery. In the remote control unit there are two keys that can have different functions depending on concrete program in microcontroller. One possibility is that one key activates emission of code for entrance opening, and second key activates emiting of code for entrance closing. Other possibility is that each key activates emitting of different codes for control of one of two main units.

The system is basically simple and cheap. It can be easily used for protection of single facility or for protection of more facilities. By programming it can be easily obtained needed level of complexity and security of protection. For facilities and spaces that do not require high level of protection it can be easily programmed needed code. The code will be emitted by remote control unit, received and decoded by main unit. The main unit will open or close entrance into protected facility/space. For facilities/spaces where very high level of complexity and security of access protection is required, in programs of main unit and remote control unit it can be programmed generators of pseudo random numbers for code generation. Then, each activation of remote control unit generates different code that is received by main unit and is compared with expected code. In this way it is minimized possibility for unauthorized discovery of code and for unauthorized access to facility or space. Also, for different users (different remote control units) it is possible to introduce different codes and lead record about moment and time of access of users.

If more main units and personal computer are interconnected, than it is possible to form information system for control of protection of more facilities and spaces where access is controlled. Such information system can define different levels of authorization of access for users and facilities/spaces, monitor and lead record about accesses to facilities/spaces by users, dynamically change access authorizations and levels of authorization, giving such higher and more flexible level of protection, monitoring and control of protection of facilities and spaces.

Next developing tools where used during development of the system:

- **MPLAB IDE** – complete development environment that the company Microchip has developed to ease writing programs for its microcontrollers [3,6]. It consists of editor, simulator, debuger, linker, support for programmators.
- **PICEASY** – developing system for PIC microcontrollers [7]. It consists of developing board that is connected and used with PC computer, and for control is used PICFLASH software.
- **PROTEL DXP** – developing tool for drawing of electric schemes and for design of printed circuit boards [5]. It is intended for development of electronic devices, their simulation and producing of complete documentation.

3. MAIN UNIT

The main unit is basic unit in the system. It is realized using microcontroller PIC 16F84A [3,7]. The microcontroller comprises more additional components and more I/O pins what makes it good choice for realization of such simpler devices. Basic characteristics of the microcontroller are: set of 35 instructions, 1024x14 bit of flash type program memory, 68x8 bit of RAM type data memory, 64x8 bit of EEPROM type data memory, 13 I/O lines, 8-bit timer, 4 interrupt sources, possibility of protection bit programming, saving of energy using sleep mode. Here in practical realization it is used standard quartz crystal with working frequency of 4MHz.

The main system unit performs next functions:

- communication of the system with user by LCD display,
- read the key combination entered by user and check is it corect code,
- receive and decode signal sent by remote control unit and chack is the received code corect,
- for corect code it generates control signals for mechanism that performs opening/closing of entrance,
- in mode of waiting for code it shows a message on the display (for example adress, name of ovner, name of company, time and date, etc.).

Electric scheme of the main unit is shown in Fig.1. All functions of main unit are implemented by microcontroller. All I/O pins are used and some of them have double function. So, the microcontroller is maximally used. Minimal number of other components is used and the most of functions are implemented by software. So, minimal cost is achieved. It can be seen from the electrical scheme that, besides the microcontroller, in this unit are also used: keyboard, diode for keyboard lightening, one line LCD display, quartz crystal, additional keys, diodes, resistors, capacitors.

One of functions of microcontroller in the unit is reading keyboard with 4x3 keys using scan method. Two additional keys are not shown in the scheme since they are switches of final position and are phisically placed at entrance of facility/space. Also, the microcontroller generates all needed signals for control of mechanism that drives door/gate at the entrance of facility/space.

Complete program for the main unit is practically developed, tested and written into microcontroller. The program is realized modularly. Besides the main program, there are also procedures for processing of interrupt requests.

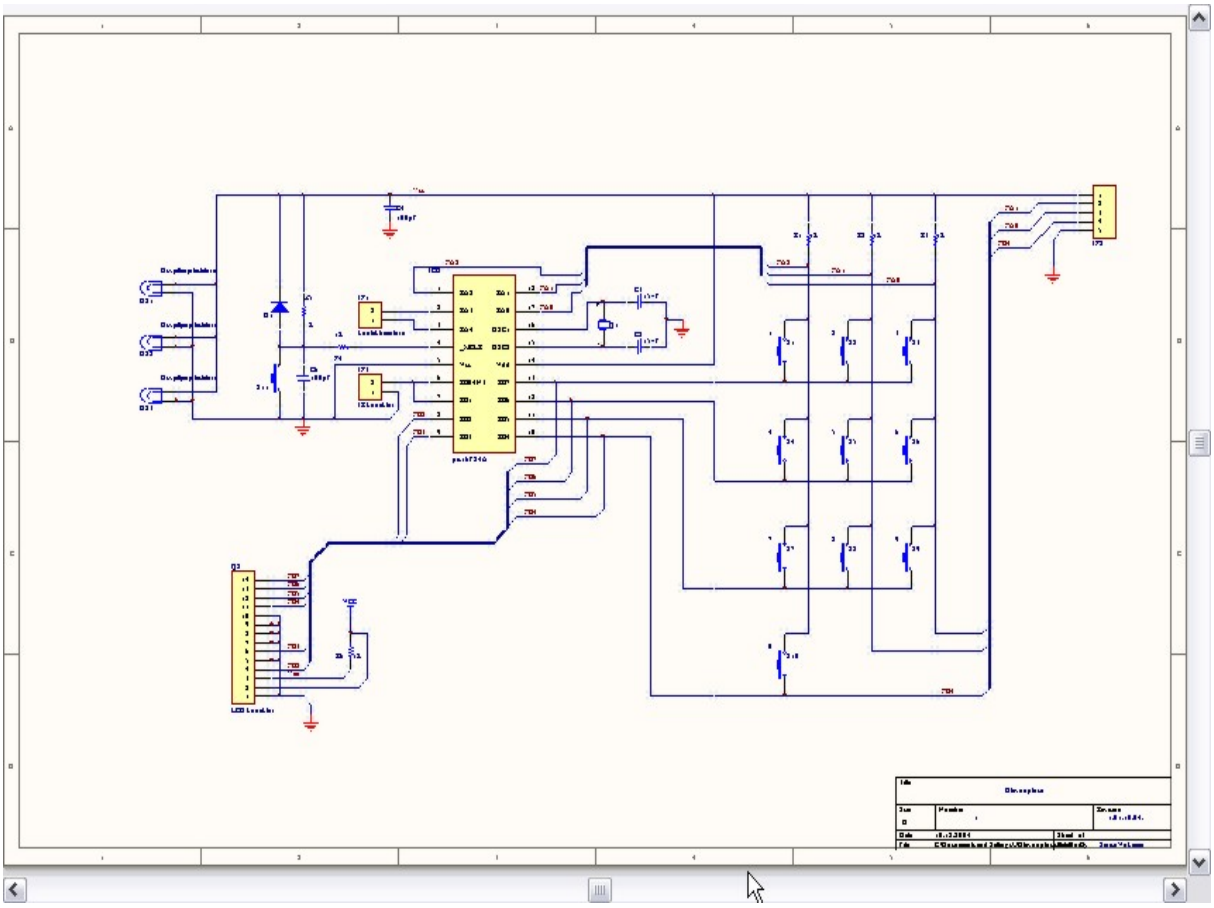

Fig. 1: *Electrical scheme of main unit.*

One part of main unit program is given in the next part of the text.

```
;*********************************************
;Filename: Main unit
;Date:16.03.2004.
;Notes: Program for main unit
;*********************************************
 list  p=16f84A
 #include <p16f84a.inc>
 #include <LCD.H>
  __CONFIG  _CP_OFF &_WDT_OFF &_PWRTE_ON
&_XT_OSC
;Definition of temporary registers
DelayCount       equ   0x10
DelayCountLow    equ   0x12
DelayCountHi     equ   0x14
AtemptCounter    equ   0x16
Numbers          equ   0x18
COD_TEMP         equ   0x28
OPEN             equ   0x40
TEMP_COD1        equ   0x30
TEMP_COD2        equ   0x32
TEMP_COD3        equ   0x34
TEMP_COD4        equ   0x36
PCL_TEMP         equ   0x38
COD1      equ     0x20
COD2      equ     0x22
COD3      equ     0x24
COD4      equ     0x26
;            *START OF PROGRAM*
org   0x00
GOTO Start
org   0x04; Interrupt program is performed  from this
instruction
GOTO  Interrupt
;Configuration of the microcontroller
 page0
 clrf   PORTA
 clrf   PORTB
 page1
 movlw   0x03
 movwf   TRISB
 movlw   0x07
 movwf   TRISA
 page0
 bsf    INTCON,GIE
 bsf    INTCON,INTE
```

```
  bcf    STATUS,Z
  clrf   PORTB
  clrf   TEMP_W
  clrf   OPEN
  call   Init
;Main program
Main
      movwf  TEMP_W
      call   Table
      andlw  0xFF
      btfsc  STATUS,Z
      GOTO   Loop
call   Send_Char
L1   movf   TEMP_W,W
      addlw  1
      GOTO   Main
Loop   goto  Loop
```

4. REMOTE CONTROL UNIT

Remote control unit has relativelly simple function. Its main task is to generate and emitt code that the main unit has to recognise as a signal for entrance opening or closing.

The remote control unit really is a modern key. Each of thise units have identical hardware structure but emitts different unique code that can open/close only one system/entrance. The unit is implemented by microcontroller PIC 12F629 [3,7]. This microcontroller is one of the simplest microcontrollers from this family. It is 8-bit microcontroller with flash type program memory. It is implemented in CMOS technology and energy consumption is very small making it very siutable for portable batery supplied devices. Main characteristics of the microcontroller are: set of 35 instructions, 1024x14 bit flash type program memory, 68x8 bit RAM type data memory, 128x8 bit EEPROM type data memory, 6 I/O lines, analog comparator, two timers, possibility for protection bit programming, saving of energy using sleep mode.

Main requirements for remote control unit are:

- simple writing, generating and changing of code, but prohibition of its reading,
- code emitting by infrared light,
- generating at least one code for system control,
- miniature dimensions and minimal energy consumption.

Given requirements are completly fullfiled using microcontroller PIC 12F629. This microcontroller has low price, small dimensions and low energy consumprion and is one of the best solutions for simple remote control units. Electric scheme of the remote control unit is given in Fig.2.

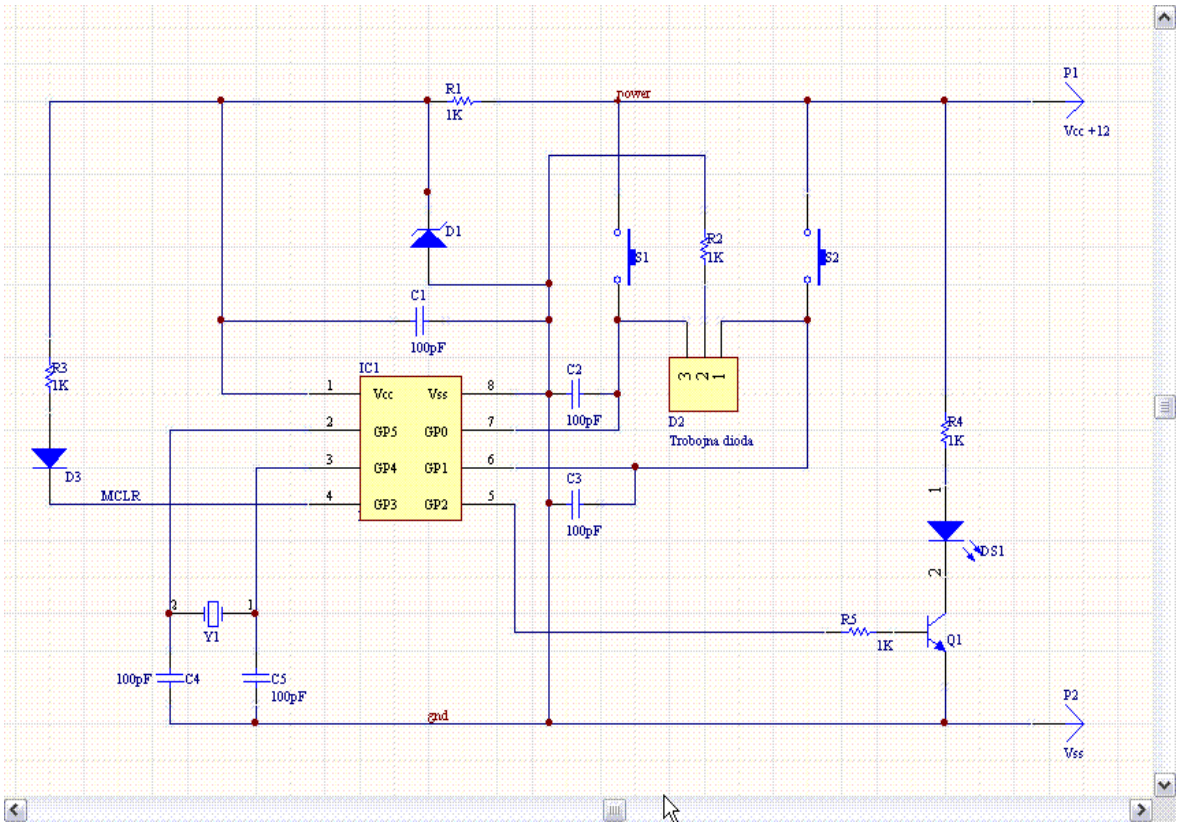

Fig. 2: *Electrical scheme of remote control unit.*

Complete program for the remote control unit is practically developed, tested and written into microcontroller.

One part of remote control unit program is given in the next part of the text.

```
;*********************************************
;Filename: Remote control unit
;Date:18.05.2004.
;Notes: Program for remote control unit
;*********************************************
 LIST P=PIC12f629, R=HEX
INCLUDE p12f629.inc
INCLUDE kod1.pas          ; include file with code
__CONFIG _ExtRC_OSC & _WDT_OFF & _CP_OFF &
_MCLRE_OFF
IRLED       equ   2       ; Infrared LED
Count       equ   0x07
DelayCount    equ   0x08
DelayCountLow equ   0x09
DelayCountHi  equ   0x0a
;----- Start -----
      org 0x00
      btfsc STATUS,GPWUF
      goto Transmit
      clrf GPIO
      movlw   b'00000000';Enable weak pull-up on GP0 and
GP1
      option              ;and wake up on pin change
      movlw   b'00111011' ; Set GP2 as output and other are
inputs
      tris GPIO
      goto _Sleep
; Procedure for time delay
       Delay
       movwf DelayCount
       DelayStart:
      decfsz DelayCount,F
      goto DelayStart
      retlw 0x00
   LongDelay
      movwf DelayCountHi
      clrf DelayCountLow
   DelayLoop:
      nop
      incfsz DelayCountLow,F
      goto DelayLoop
      decfsz DelayCountHi,F
      goto DelayLoop
      retlw 0x00
  Transmit:
      comf GPIO,W             ;read and invert GPIO
      andlw b'00000011'
      btfsc STATUS,Z          ; check is key pressed
      goto _Sleep             ; if not go to sleep
      movlw 0x1e
      call LongDelay          ;wait for 30 ms
      comf GPIO,W             ;read and invert GPIO again
      andlw b'00000011'
      btfsc STATUS,Z          ;is key still pressed
      goto _Sleep             ;if not go to sleep
```

5. CONCLUSIONS

Practically realized and described system is cheap and simple. For implementation are used cheap standard microcontrollers adapted to requirements of each unit of the system. So, it is enabled usage of minimal number of additional elements, decreased dimension and decreased energy consumption. Functions of units are implemented by software. That enables simple change and adaptation of function to concrete need.

Hardware solutions of the system units are very universal for such applications. By softwate it can be very simple defined needed complexity and needed level of protection by implementing appropriate algorithm.

This system can be used for protection control for different spaces and facilities. That can be facilities/spaces from ones where is not needed higher protection level than only controlled and easened access (for example court yards, garages, parkings, etc.) to ones where high level of access protection and control have to be assured (for example business offices, warehouses, production plants, specially controlled facilities and spaces, etc.).

By interconnection of more main units and personal computer it is possible to realize information system with very large flexibility for protection, monitoring and control of access for more facilities/spaces.

By programming of system units it is possible to simply obtain needed level of complexity and security of protection, depending of importance and level of protection that have to be achieved for certain facilities and spaces.

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DETECTION OF UNEXPECTED EVENTS IN THE PROCESS INDUSTRY USING FUZZY MODELS

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Abstract: *The paper describes detection of unexpected events in the industry plant using fuzzy models of the selected process variables. The real-time detection of the unexpected events is based on the one of two inbuilt detection mechanisms depending on existing or not existing corresponding measured data. It is based on calculation of the real-time deviation of characteristic parameters - measured and estimated. The system is developed and verified on the tunnel kiln in the ceramic industry. A large process database for training of the Takagi-Sugeno fuzzy estimation models is used. The result of usage these high precision detection and estimation models is the higher quality control process and decrease of the waste products.*

1. INTRODUCTION

The growth of industrial production causes an increase in energy consumption, which is reflected in more severe operation of large energy production and distribution systems. The staff of the dispatching centers is faced with increasingly high demands concerning the reliability and security of providing the required energy consumption. For that reason, intensive research is being conducted in order to find new, faster and more accurate computer methods for implementation of high-level, supervisory control functions, such as fault diagnosis or monitoring. Traditional, algorithmic approaches use methods of filtering and estimation [1]. Expert systems are also one of the approaches, but an extensive heuristic knowledge base is required for their operation. However, in cases when the information on the system state is incomplete or mathematical model of the processes is ill-defined, methods of machine learning are much more suitable [2]. The artificial neural networks (ANNs) represent the learning technique that is capable of acquiring and storing new 'process knowledge' on the basis of representative training samples regarding system behavior in different operating conditions [2]. Recently, this approach was frequently applied in developing the high-level supervisory control functions. The models have superseded rule-based techniques is one of the premier research directions for intelligent systems diagnosis. A model is an approximate representation of the actual system being diagnosed. Model-based diagnosis involves using the model to predict faults using observation and information from the real device or system. One advanced approach in process modeling is fuzzy logic[3]. Fuzzy logic provides mechanisms to represent and manipulate linguistic concepts. It deals with approximates rather then exact measurements and it is based on fuzzy set theory [4,5].

This paper presents the results of the research conducted in order to apply the fuzzy models in designing the state estimator, as well as fault detection, as the basic functions of the supervisory control system. State estimator is used for detection of unexpected events like sensor breakdown or system transition from one state to another.

The next section of the paper describes the Takagi-Sugeno modeling. The third section gives the general overview of the procedure for detection of unexpected events. The forth section gives the experimental results of the fault detection procedures applied on tunnel kiln.

2. TAKAGI-SUGENO FUZZY MODELING

Fuzzy models are expected to be characterized with: (1) an accurate and fast procedure for calculation of the desired quantity; (2) a general and flexible procedure, applicable to a wide class of very diverse problems. Fuzzy model generation based on learning by examples approach is achieved during the structure identification and model parameter identification step [6]. In cases when the input quantities are known, structure identification step reduces to determination of the required number of rules and determination of the conditional part of the rule. The required number of rules can be determined using cluster validity measures, or cluster removal and/or merging techniques. Determination of the conditional part of the rule necessitates defining of the fuzzy sets of input variables. This can be done using grid-type space partitioning and fuzzy clustering methods. Structural identification is a more difficult task, which is usually executed off-line.

Takagi-Sugeno fuzzy models are used for modeling the system according to established relations between the relevant parameters of the system [5,7]. These relations are presented in form of if-then rules. Therefore, every relation is defined with appropriate conditional and consequence part. Consequence can be interpreted like an action that will be taken, if conditional part of the rule is satisfied. Takagi-Sugeno (TS) fuzzy model belong to category of models, which are formed using measured data of the system. After data driven training of fuzzy model, adequate set of fuzzy rules is created. Each fuzzy rule contains input-output variables described in domain of the fuzzy sets. Fuzzy set is especial kind of set in which every element is characterized with appropriate degree of qualification for fuzzy set – real number from interval [0,1]. For every fuzzy set, one if-then rule is formed. Every system can be observed like universal system that is described with *n* input and one output variable.

The final goal of fuzzy modeling of systems is defining approximate functional dependence between established input and output of system: $y = f(x_1, x_2, ..., x_n)$.

On the base of functional dependency, determined like this, it is possible to estimate the behavior of system output for given values on system input.

Basic idea of TS fuzzy model is in fact that system of any complexity is a combination of intercourse related sub models. If every of K regions correspond to a sub model, then the system behavior of these regions could be described with simple functional dependency. If these dependencies are linear and if every sub model has one fuzzy rule, than TS fuzzy model could be described with K rules with following:

$$R_i: \text{If } x_1 \text{ is } A_{i1} \text{ and } x_2 \text{ is } A_{i2} \text{ and ... and } x_n \text{ is } A_{in}$$
$$\text{then } y_i = a_i x + b_i, \qquad i = 1,2,3...,K$$

where R_i is i^{th} rule, $x_1, x_2, ..., x_n$ are inputs, $A_{i1}, A_{i2}, ..., A_{in}$ are fuzzy sets assigned to corresponding

inputs, y_i is output value of i^{th} *rule*, a_i and b_i are parameters of consequence function. Final output of TS fuzzy model for x_k input sample is:

$$\hat{y}_k = \frac{\sum_{i=1}^{K}[\beta_i(\mathbf{x}_k)\, y_i(\mathbf{x}_k)]}{\sum_{i=1}^{K}\beta_i(\mathbf{x}_k)}\ ,\ k = 1,2,3,\ ...,\ N.$$

where β_i is activation level of i^{th} rule.

3. DETECTION OF UNEXPECTED EVENTS

Algorithm for detection of the unexpected events calculates error between estimated and measured process data and generates information in realtime system. The real-time detection of the unexpected events is based on the one of two build detection mechanisms depending on existing or not existing corresponding measured data. Both cases are explained in more details in text as follows.

3.1. Event detection when measured value is not present

Detection is based on calculating the deviation between estimated value and mean value of the process variable that have been tracked. Mean value of process variable is calculated on the basis of data from the process history. If we assume process variable y and set of its known values as $y_1, y_2 ... y_n$, then mean value m and standard deviation s of process variable y are:

$$m = \frac{1}{n}\sum_{i=1}^{n} yi \qquad (1)$$

$$s = \sqrt{D(y)}\ , \qquad (2)$$

where $D(y)$ is variance of process variable y.

Depending on data calculated for detection purpose two limits are defined in order to determine ranges for errors:

$$l1 = 3 \cdot s \qquad (3)$$

$$l2 = 5 \cdot s \qquad (4)$$

Errors are detected according to the conditions as follows:

$$m - l1 < y' < m + l1 \qquad (5)$$

$$m - l2 \le y' \le m - l1 \qquad (6)$$

$$m + l1 \le y' \le m + l2 \qquad (7)$$

$$y' > m + l2 \qquad (8)$$

$$y' < m - l2 \qquad (9)$$

In case that value is inside range defined by (5) estimated value is acceptable and no information are generated. In case that estimated value is inside range defined with (6) or (7) worning information are generated. In case that value is in range defined with (8) or (9), an alarm is generated.

3.2. Event detection when measured value is present

Second way of event detection is based on calculating deviation between estimated value and mean value of the error (m'). The error is calculated as difference between the measured value (y_i) and estimated value (y_i') of model output:

$$m' = \frac{1}{n}\sum_{i=1}^{n} |\, y_i - y_i' \,| \qquad (10)$$

$$s' = \sqrt{D(|\, y - y' \,|)} \qquad (11)$$

On the base of data calculated for detection purpose, two limits are defined in order to determine ranges for errors:

$$th1 = 3\, s' \qquad (12)$$

$$th2 = 5\, s' \qquad (13)$$

Errors are detected according to the conditions as follows:

$$0 \le |y - y| < m' + th1 \qquad (14)$$

$$m' + th1 \le |Y - Y| \le m + th2 \qquad (15)$$

$$m' + th2 < |Y - Y'| \qquad (16)$$

In case that value is in range defined in (14) estimated value is acceptable and no information is generated. In case that error is in range defined with (15) or (16), another value is calculated:

$$v = |y - y'| / th1 \qquad (17)$$

Value V is then sumarised in last twenty time instances like it is shown in (18) to determine a sort of an accumulation:

$$a = \sum_{i=n-20}^{n} v_i \qquad (18)$$

If accumulation of error is greater then defined threshold and repeat consecutive, the warning will be generated.

4. RESULTS AND COMMENTS

Detection algoritam has been tested in realtime system. It was a control system of the tunnel kiln. A tunnel kiln is used for baking of roof tiles heated along tunnel kiln at different temperatures. The carriages loaded with roof tiles passes through the tunnel in a discontinuous manner, since they are pushed through the tunnel periodically and kept at certain positions for predefined time intervals. The tunnel kiln is subdivided into a couple of various temperature zones. Heating zones are supplied with groups of burners operated on natural gas and circulating hot gasses, while cooling zones are equipped with a large number of openings for pumping out the hot air, as well as circulating cold air. Control of burner groups and pumps is accomplished using a number of programmable logical controllers (PLCs). The data regarding the measured temperatures are transmitted from all the PLCs, using communication lines, to the monitoring computer. Reliability of the control loops is impaired by frequent malfunctioning of the temperature sensors. Early detection of the temperature sensor failure would enable significant savings in material and energy. High accuracy of such an algorithm enables early detection of the temperature sensor failure and/or substitution of the actual temperature measurement with a temperature estimate.

The most representative temperature is used for graphical review of calculated error and in the most representative intervals of time – that are periods of disagreement between estimated and measured process data, when error is the highest. A period like this is shown on figure 1, the lower line represents an estimated and the upper one measured process data. A central part of the diagram shows that estimated value does not meat measured value when it is not in usual regime.

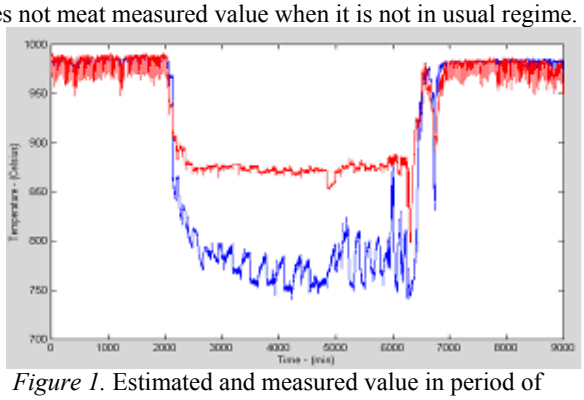

Figure 1. Estimated and measured value in period of disagreement.

On figure 2 it is shown error between these two values calculated in the same time period as in figure 1. and information that are generated.

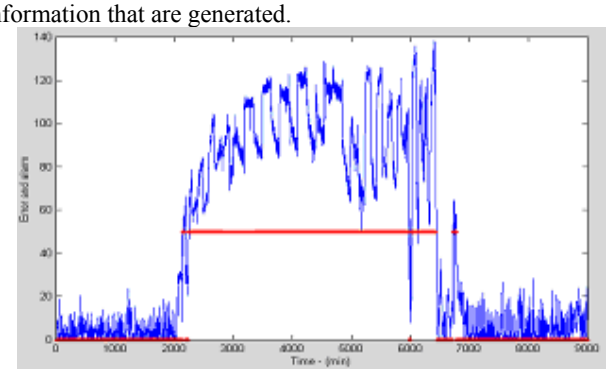

Figure 2 Absolute error and generated alarm information.

As it is explained above, alarms are generated on the base of error between estimated and measured process data and absolute error is then standardized (17) and accumulated (18). On figure 2. curved line represents absolute error and a horizontal line presents alarm information generated. As it is shown alarm information are generated only in region where error is higher then given threshold.

Accumulated value, given with (18) is then compared with threshold determined beforehand and if the accumulated value is greather then threshold, information to user is generated.

On figure 3. it is shown that alarm information (horizontal line) is constantly generated when accumulation *a* (smaller curved line) was above threshold (30 in this case). In order to get a better look on the moment when alarm information started to be generated, appropriate time period is shown on figure 4. It is shown, more clearly, that alarm information did not appear until accumulation of the error was under the threshold. When accumulated value for the first time was above the threshold the alarm information was generated (time sample 2150) on figure 4. In the moment when accumulated error drops below the threshold again (time sample 2180), the alarm information is stopped till the moment when accumulated value is above again (time sample 2250).

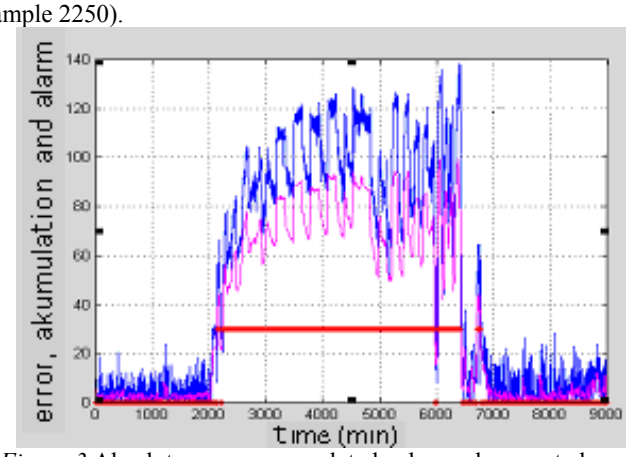

Figure 3 Absolute error, accumulated value and generated alarm information

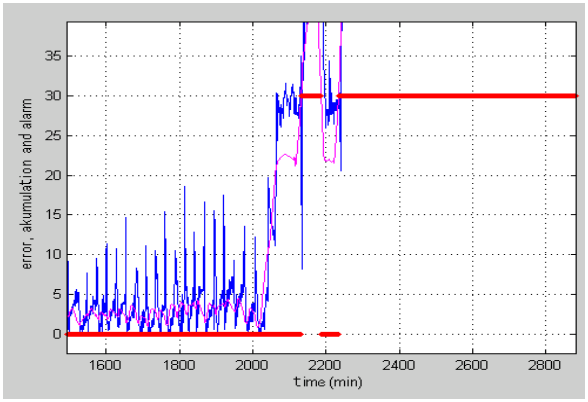

Figure 4 Moment when alarm information started

5. CONCLUSION

Using the system for detection of unexpected events based on temperature estimation in tunnel kiln, an early discovery of faulty sensors is accomplished. This also means the reduction of production waste, which appear as a consequence of wrong information from measuring point.

This enables industrial control systems to have less qualified personnel occupied with the work that usually consists of graphic analysing archived process data and discovering faulty sensors according to free estimation.

Beside that, because of very high accuracy of estimated process data dedicated control group can lead the process on the base of replacing measured data with estimated values, while faulty sensors are being replacing or repairing.

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ANALYSIS OF THE"END-TO-END" QoS ARCHITECTURE IN 3G/4G MOBILE NETWORKS

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Abstract: *The research in 3G/4G mobile telecommunication networks is directed toward an "all-IP" transmission to mobile end-users. There is the great variety of applications (from simple web-searching to high-bandwidth multimedia applications) and it is necessary to provide the integral "end-to-end" QoS architecture. This paper gives the overview of the "Moby Dick" architecture, which is currently in experimental phase.*

Keywords: *"End-to-end" QoS architecture, 3G/4G mobile telecommunication networks.*

1. INTRODUCTION

The research activities in the third/fourth generation (3G/4G) mobile telecommunication network are focused primarily on the "all-IP" transmission to the end-user. Since there is the great variety of applications which these networks should support (e.g. Web-browsing, broadband multimedia applications etc.) it is necessary to provide the appropriate Quality of Service (QoS), especially in the network parts based on IP transmission [1,2,3,4].

During the past few years, international standardization bodies have been intensified their activities in finding the appropriate QoS architectures. Two architectures are of special importance for implementation in 3G/4G mobile networks: Integrated Services (IntServ) and Differentiated Services (DiffServ) architectures. The IntServ approach is based on "end-to-end" resource reservation and "per-flow" basis, while DiffServ approach provides group traffic flow managing on "per-hop" basis with the appropriate network access control.

Both architectures apply techniques for CAC (Connection Admission Control) and algorithms for service differentiation and packet prioritization.

The "all-IP" QoS implementation will be probably based on the adequate DiffServ architecture. But for the 3G QoS provisioning it is necessary to analyze CoS (Class of Service) which support detailed parameter identification for different service types.

The fixed network QoS support is available based on appropriate mechanisms and protocols, which have found their role in network structure. But, on the other side, the overall QoS provisioning in 3G/4G mobile networks is still in experimental phase.

In addition to the fact that fixed QoS characteristics should be enabled on network level, the special problem is handover between access routers, frequent changing of IP addresses, traffic congestion, high probability of bit error rate, changeable traffic characteristic and mobile user resource distribution that increases QoS provisioning mechanism and protocol complexity. It is not an easy task to maintain the same QoS level for mobile equipment in access network as well as the transparency connection maintenance. But, if the guaranteed QoS level is not achieved, the network will not be able to support different services.

The protocol architecture in the 3G/4G mobile networks is very complex, due to the different access technologies applied. When analyzing the QoS in these networks, the starting point should be its realization as an "end-to-end" concept. This means that mobile terminals should communicate using different access technologies, different QoS parameters (bandwidth, priorities, latency, jitter, losses) as well as different available resources.

From the network operator point of view, it is necessary to verify access levels and user authorization issues, and to define the criteria needed for appropriate resource planning and billing. These functions are implemented in AAAC (Authorization, Authentication, Accounting and Charging) component of the QoS architecture.

Taking all this into account it could be concluded that for the successful implementation of user requirements in 3G/4G mobile networks, it is necessary to define the overall "end-to-end" QoS architecture.

The rest of the paper deals with the main elements of the "end-to-end" QoS architecture proposed in the "Moby Dick" project which implementation is in progress [5].

2. THE "MOBY DICK" QOS ARCHITECTURE

The main goal of the "Moby Dick" project is to provide "end-to-end" QoS definition, implementation and evaluation in mobile networks based on IPv6 protocol, which is able to support heterogeneous access technologies: WCDMA (UMTS – Universal Mobile Telecommunications System), Wireless LAN (802.11b) and Ethernet.

The basic requirements for this architecture are:

- Unified "all-IPv6" architecture for Internet access (WCDMA, WLAN and Ethernet);
- Support for seamless handover across heterogeneous access networks;
- Development and implementation of AAAC (Authorization, Authentication, Accounting and Charging) mechanism;
- Definition of mobility-enabled "end-to-end" QoS architecture;
- Integration of Mobility, QoS and AAAC mechanisms.

The QoS architecture is based on DiffServ approach, and the main elements of the architecture are (Fig.1):

- MT – Mobile Terminal;
- AN – Access Network (Ethernet, WCDMA or 802.11b);
- AR – Access Router;
- QoS Broker – high-level entity responsible for QoS management and overall user admission;
- AAAC entity – high-level entity responsible for keeping the user profile, for authenticate, authorize, and account the user for charging the user for its network resources usage;

This architecture provides user mobility (both with horizontal and vertical handover) based on Mobile IP

procedures, with QoS capabilities based on DiffServ procedures and AAAC mechanisms.

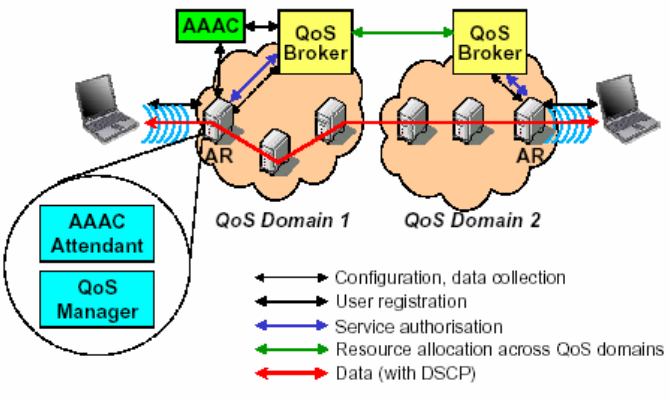

Fig.1: *Moby Dick QoS architecture.*

Different parts of the network architecture, responsible for mobility management functions, QoS and security, are connected in a unified part by the above-mentioned entities. The software components, responsible for the QoS delivery process, are integrated at different levels of the protocols stack, and are located in three network entities: the *Mobile Terminal*, the *Access Router* and the *QoS Broker*.

2.1. Mobile terminal (MT)

The *NCP* (Networking Control Panel) resides on the highest level of MT protocol stack and sends requirements for AAAC registration. There is adjusted version of IPv6 protocol stack for Linux (MIPL) on the network level, which supports QoS fast handover and DSCP (Differentiated Services Code Point) mechanism of packet marking that provides filtering of IPv6, ICMPv6 and header transport protocols (TCP, UDP) in accordance to the customer requirements. The *MTNM* (Mobile Terminal Network Manager) module is placed between IP layer and data layer and is responsible for handover function realization. The *RCF* (Radio Convergence Function) module is responsible for the channel data control functions, transmitting and receiving IP packets, in accordance with IP QoS requirements.

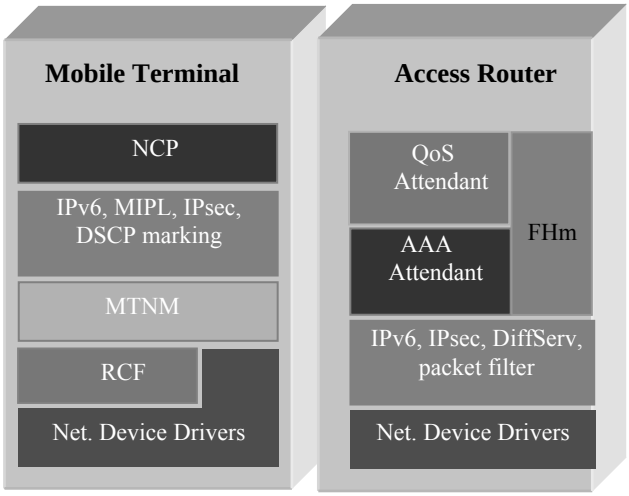

Fig.2: *QoS components in mobile terminals and access router.*

2.2. Access Router (AR)

The Access Router performs functions typical for a DiffServ Edge Router: traffic management, traffic shaping and policing, PHB (Per Hop Behaviour) mechanisms etc. The *QoS Attendant* located in the AR module makes decision concerning the access management, priority and PHB. The AR performs traffic monitoring from the access interfaces to the core interfaces, collects some parameters of the packets and establishes the interaction with the QoS Broker.

In this architecture, the AR also performs a role in the Fast Handover (FH) procedures. With the *Fast Handover module* (FHm), the old AR notifies the QoS Broker of the preparation of a FH to a new AR. The AR also informs the QoS Broker of the load of its queues so the QoS Broker may reconfigure them.

2.3. QoS broker

The aim of the QoS Broker is to provide resources and admission control, and to configure all access network components, according to a set of conditions given by administration entities. In order to provide the user requirements, the QoS Broker interacts with AAAC system during the phase of user registration. After user registration, AAAC system sends data about user profile, and than QoS broker performs SAC (Service Admission Control) for each service which the user requires.

The OoS Broker is a complex entity responsible for different functions in the heterogeneous environment (Fig.3). In the core of this entity exists the *QoSB Engine* that performs all key algorithms for QoS management, and the realization of these algorithms is based on data obtained by the *Virtual Router Module (VRM).* The VRM provides unique interface for *QoSB engine* and maps management commands into adequate network commands for each AR. It has a database that keeps information about routers, vendors, models, and communication formats. The QoS Broker provides several additional interfaces: *AAAC Interface* which receives user information from *AAAC Server,* and *QoS Broker Interface* for information exchange with other QoS Broker. *The Mobility Interface* performs QoS management during the handover.

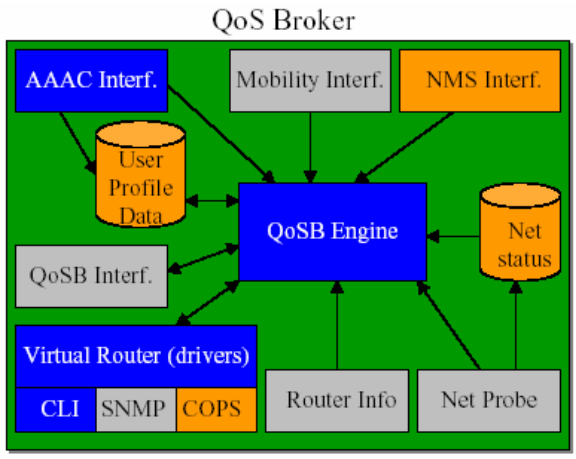

Fig.3: The *QoS Broker architecture.*

The management and monitoring functions are performed by three main functions: *NetProbe* performs network status monitoring and collected information is inserted in a database (*Net Status*); *RuterInfo* module collects information about particular router; *NMS Interface* allows the NMS (Network Management System) entity to define the network resources that can be used by QoS Broker.

2.4. The Radio Resource Management

When a request for a new service appears, the IP DSCP code of the first packet received by the AR is mapped onto one of the Radio QoS classes and the request to the QoS Mapping component has been sent.

Parameters such as bandwidth, latency, packet losses etc. must be converted into a specific number of time slots, transport formats and convolution codes. Packet differentiation requires marking them with a DSCP. The network operator assigns to each DSCP a certain level of QoS.

For example, the real time service S1 is mapped into UMTS conversational QoS class (Table 1). This step is performed after the service initiation: the finite set of radio parameters, according to previously dedicated resources and specific cell radio configuration, is calculated. The relative priority has been assigned to each service class: '1' denotes the highest priority, '4' the lowest, and '0' means 'no priority'.

"Service parameters" indicate the typical service parameters used for the configuration of the Access Router, while "service description" indicates typical services to be used with these network services.

Table 1. *Service classes and parameters.*

Service		Relative Priority	Service parameters	Description
Name	Class			
S1	EF	1	Peak BW: 32kb/s	Real time services
S2	AF41	2	Unspecified Signaling	IP Signaling
S3	AF21	3	CIR: 256 kb/s	Priority data transfer
S4	AF1	4	Three drop precedences (kb/s): AF11 – 64 AF12 – 128 AF13 - 256	streaming, ftp
S5	BE	0	Peak bit rate: 32 kb/s	Best Effort
S6	BE	0	Peak bit rate: 64 kb/s	Best Effort
S7	BE	0	Peak bit rate: 256 kb/s	Best Effort

Figure 4 shows the Mobile Terminal and Access Router components involved in the managing of WCDMA radio resources. The IP QoS Control procedures, based on DiffServ codepoints, are directly mapped onto the physical layer.

The RRC (Radio Resource Control) entity computes the changes of the radio parameters to provide a proper operation of the Radio Interface Protocols: PDCP, RLC, MAC and PHY. The mapping table in the RRC provides a set of UMTS parameters such as BER, delay, etc., according to the requested Radio QoS class.

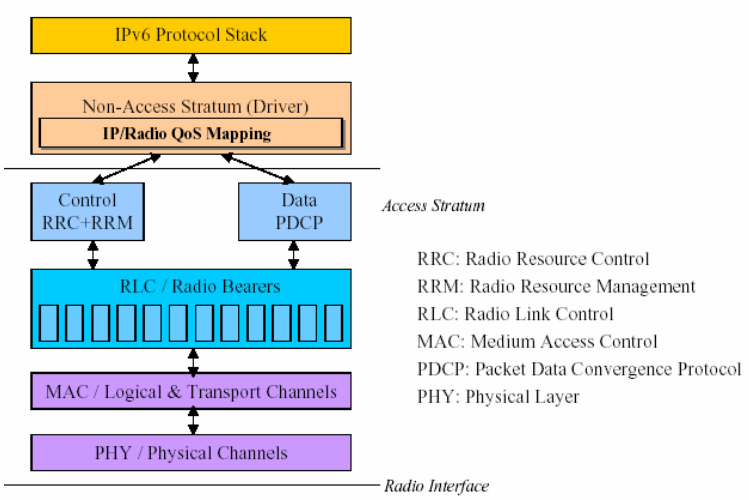

Fig.4: *Layered WCDMA architecture (Radio QoS).*

The final testing of the QoS Broker functions is performed by simulation, Fig.5.

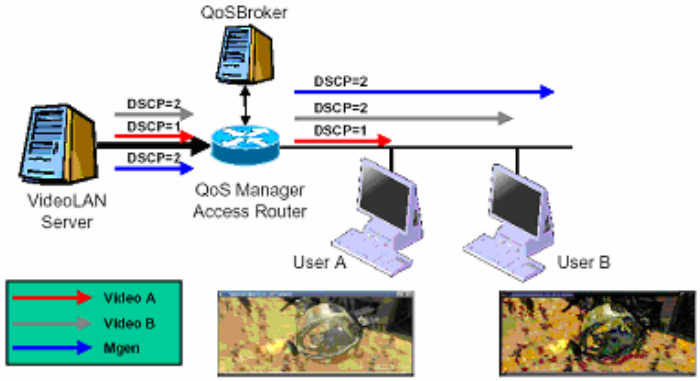

Fig.5. Simulation of QoS Broker functions.

In this example, the video application (generated by video server) with two video streams is chosen for the simulation, and each of them has different QoS DSCP. One of streams shares resources with the background traffic flow (Mgen application). In this case, User A receives higher quality video signal in comparison to signal received by user B.

3. CONCLUSION

The "end-to-end" QoS provisioning in 3G/4G mobile networks is very complex task, taking into account a number of different activities: resource reservation, SLA (Service Level Agreement) mechanisms, billing, network management etc. The most important activities are:

- Identification of specific problems of mobility and radio access impacts on the provision of "end-to-end" QoS.

- Selection of requirements on external networks that might be needed to enable QoS.
- Selection of mechanisms within the access network to operate.
- Adaptation of QoS concepts for the fixed Internet to the mobile wireless environment.

The realization of all these activities is necessary in order to provide a unified QoS architecture with guarantees concerning the user requirements in heterogeneous access networks and different mobility scenarios.

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CHAOTIC CSK AND DCSK SYSTEMS PERFORMANCES WITH MAXIMUM LIKELIHOOD DETECTION

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Abstract – *Nonlinear dynamic based systems that are generated using chaotic sequences are analyzed in this paper. Special attention is given to CSK (Chaos Shift Keying) and DCSK (Differential Chaos Shift Keying) system performances evaluation for maximum likelihood detection using Viterbi algorithm. Originally results, obtained by computer simulation are compared with analytical and simulation results for CSK and DCSK systems with correlation detector. Also, comparation with classical telecommunications systems is given, and problem of chaotic sequences synchronization and orthogonallity are considered.*

Keywords – *chaotic systems*, *Chaos Shift Keying, Differential Chaos Shift Keying, maximum likelihood detection, symbolic dynamics.*

1. INTRODUCTION

Chaotic signals are wideband, irregular, apperiodical and uncorrelated signals. It is based on complex waveforms, unsuitable for long-term prediction, but generated using deterministic mechanism. These signals are inherently immune for interference, multipath propagation and characterized by low probability of interception. Therefore, chaotic signals applications vary from cryptography to spectrum spreading in CDMA systems. Important characteristics of these systems are based on fast decrease of correlation function side lobes.

Systems based on non-linear dynamics, where signal is generated according to chaotic sequence, are considered in this paper. Performances of CSK (Chaos Shift Keying) and DCSK (Differential Chaos Shift Keying) with maximum likelihood detection are analyzed.

Original results, obtained by Monte Carlo simulation are compared with previously derived analytical results. These results are compared with classical communication system performances. Synchronization problem is analyzed and possibility of proposed schemes application in multipath environment is considered.

2. GENERATION OF CHAOTICAL SECUENCES

Parameter that provides a quantitative measure of the degree of stochasticity for a trajectory is Liapunov exponent. It is defined as an average long term growth rate for the semi-axis in the ellipsoid that was our starting point and it can be expressed as

$$\lambda\left(x[0]\right) = \lim_{N\to\infty} \frac{1}{N} \sum_{i=0}^{N} \ln\left|f'\left(x[i]\right)\right| \qquad (1)$$

A chaotic signal is any signal where above expression is greater than zero.

There is a lot of different maps that can be used in the chaotic systems – Bernoulli shift, tent mapping, logistic mapping, tailed shift etc. Bernoulli shift represents one-dimensional mapping defined on interval [0,1]. In this case, principle of random sequence generation can be described by

$$x_{k+1} = \mathrm{mod}(2x_k, 1) \qquad (2)$$

Result signal takes all possible values between zero and one. It can be shown [1] that result signal is uncorrelated for the delays greater that zero. Unlike standard PN sequences, chaotic signal is uncorrelated and its spectrum perfectly matches to ideal random signal spectrum.

Modulated signal can be formed according to eq. (3). As elements of the sequence x_k can take any value from set [0,1] it is clear that the modulated signal can take any point on the unite circle

$$y_k = \exp(j\pi x_k) \qquad (3)$$

3. TIPICAL CHATIC MODULATION SHEMES

As it was already shown, it is possible to realize a kind of phase modulation (similar to PSK [2]) based on the generated chaotic sequence. Direct result of such approach is CSK, where two chaotic generators in receiver are synchronized with corresponding generators in transmitter. Structure of CSK transceiver is presented in Fig. 1.

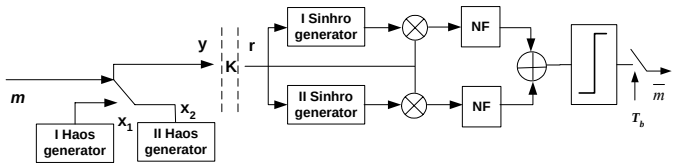

Fig. 1: CSK transceiver.

If signal x_1 is transmitted, upper correlator will recognize it and produce correlated copy. The other, unsynchronized, system produce less correlated signal on the output. These signals are subtracted from each other and result signal goes to the limiter, where detection is performed.

Basic problem of CSK system is complex synchronization. The ideal synchronization is practically impossible because of lack of periodicity. On the other hand, for Bernoulli shift it stands $y_{k+1} = y_k^2$. Therefore, for received signal it can be written

$$r_{k+1} = y_{k+1} + \eta_{k+1} = y_k^2 + \eta_{k+1} = (r_k - \eta_k)^2 + \eta_{k+1} \approx r_k^2 \qquad (4)$$

This synchronization principle satisfies in practical conditions but it is not ideal (because of the noise η_k influence). Compared with the referent BPSK system, the system performances are significantly worsened. As well as in classical communication systems, synchronization problem can be retrieved combining a differential coding in transmitter and incoherent detection in receiver.

For the case of chaotic systems, solution is found in DCSK modulation, described by eq. (5), and transceiver structure is presented in Fig. 2.

$$y(t)=\begin{cases} x(t), & kT_b \le t < \dfrac{2k+1}{2}T_b \\ x\left(t-\dfrac{T_b}{2}\right), & \dfrac{2k+1}{2}T_b \le t < (k+1)T_b,\ m(t)=m_1 \\ -x\left(t-\dfrac{T_b}{2}\right), & \dfrac{2k+1}{2}T_b \le t < (k+1)T_b,\ m(t)=m_2 \end{cases} \quad (5)$$

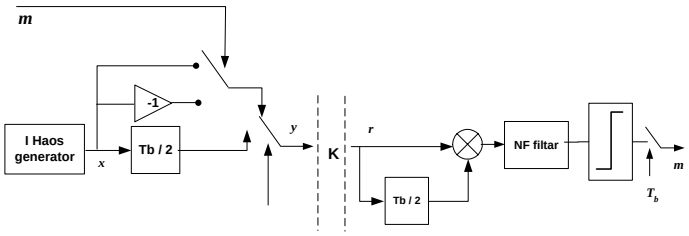

Fig. 2: DCSK transceiver.

In DCSK, for each symbol period, a portion of the chaotic waveform (the reference signal) is transmitted followed by its inverted or non-inverted copy (the information-bearing signal), depending on the information bit. At the receiver, the information is extracted by means of the differentially coherent demodulation, which is performed by correlating the information-bearing part of the signal with the reference.

The chaotic signals are well suited for spread-spectrum communications. For such a system, for the duration of one bit in sequence $m_1(t)$, there are L symbols from chaotic generator. Therefore, value L is important factor for CDMA chaotic system evaluation.

Approximate expressions for the bit error probability of CSK and DCSK systems are known [1]. This approximation is considered to be highly accurate for large L.

$$BER_{CSK}=\frac{1}{2}erfc\left(\sqrt{\frac{1}{5\dfrac{N_0}{E_b}+6L\left(\dfrac{N_0}{E_b}\right)+2L^2\left(\dfrac{N_0}{E_b}\right)^3}}\right) \quad (6)$$

$$BER_{DCSK}=\frac{1}{2}erfc\left(\sqrt{\frac{1}{4\dfrac{N_0}{E_b}+4L\left(\dfrac{N_0}{E_b}\right)^2}}\right) \quad (7)$$

Performances of CSK and DCSK with correlation detector are estimated using Monte Carlo simulation. Simulation results correspond excellently with analytical expressions for large L. It is clear that these systems performances are inferior to BPSK for the value of 4-5 dB.

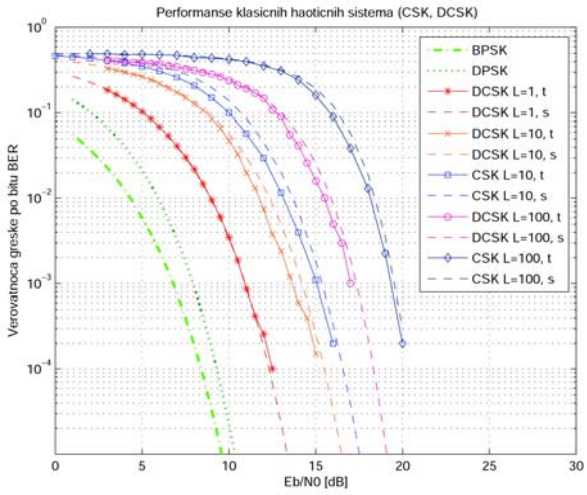

Fig 3: Performances of CSK and DCSK systems with correlation detector.

4. SIMBOLIC DYNAMICS

In this case, continual trajectories are represented by discrete symbols [3]. Range of possible values are divided into the subsets, as it is presented in Fig. 4 The message symbol m_1 selects the map, which calculates the state at time instant k+1. Maps that correspond to m_1=0 and m_1=1 are represented by blue and red color, respectively.

Every subset corresponds to some state of pseudo-chaotic (PC) generator, while output is given by (8) where b_j can take values 0 or 1, and $x \in [0,1]$.

$$x = 0.b_1b_2b_3\ldots \equiv \sum_{j=1}^{\infty} 2^{-j} b_j \quad (8)$$

Applying successive iteration over x, pseudo-chaotic signal with limited number of levels is created [4]. We can assume that input of generator is equal to zero if input symbol values are located in left subinterval and vice versa.

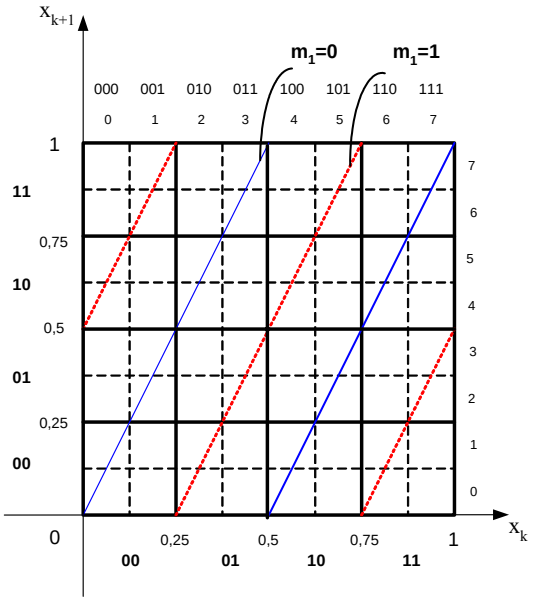

Fig 4: Maps and 8-state space partition, pseudo-chaotic CSK.

This way, Bernoulli shift is approximated using *M*-bit shift register and D/A converter. In Fig. 5. and Fig. 6., structure of the pseudo-chaotic generator and the corresponding trellis diagram for message 01 are presented respectively.

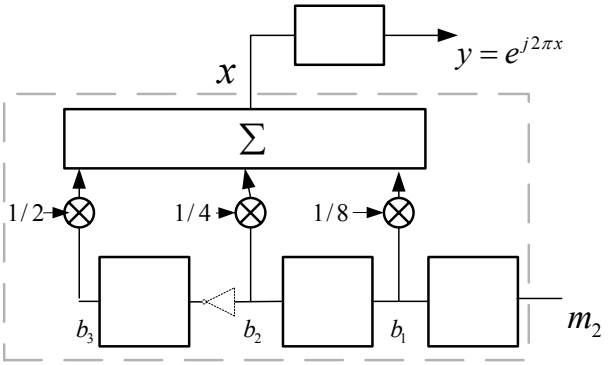

Fig. 5: Pseudo-chaotic generator structure, four states, eight possible levels on the output, CSK.

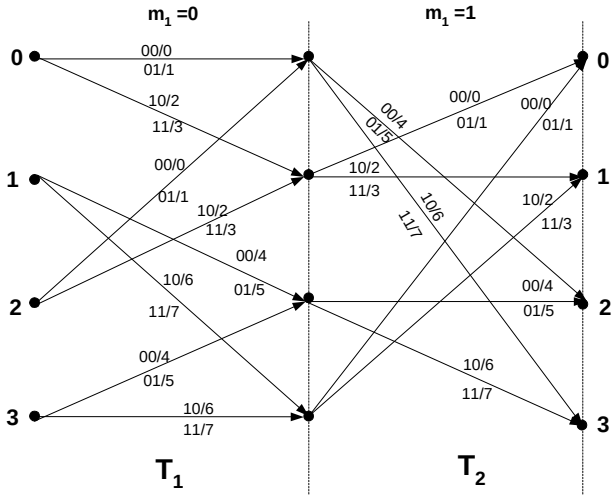

Fig. 6: Trellis structure for four states and eight possible levels on the output, CSK.

5. CSK SD

The basic idea behind the SD-CSK scheme is to replace the chaos generator, presented in the CSK scheme in Fig. 1, with a pseudo-chaotic encoder. We denoted with $m_1(k)$ the binary stream to be modulated according to the original CSK scheme. On the other hand, the input sequence $m_2(k)$ is used to generate the pseudo-chaotic carrier (this sequence "feed" PC generator).

Every PC generator transform sequence m_2(k) into the pseudochaotic signal using Bernoulli shift while sequence $m_1(k)$ perform tasting of information into the CSK signal (Fig. 7). Generators on the transmitter side differ in existence/ non-existence of inverter, represented by the dashed line in Fig. 5. That way, signals on the output of the corresponding generators are always antipodal. In this paper, special case of CSK where L=1 is considered. Ono pseudo-chaotic iterant is generated per one information bit. It is assumed that sequences $m_1(k)$ and $m_2(k)$ has the same bit rate. If sequence $m_2(k)$ has a bit rate that is L times greater than in $m_1(k)$, the spreading factor is equal L.

Transmitted signal is normalized to unit amplitude and it is represented by

$$s_k = \left[\cos(\varphi_k), \sin(\varphi_k)\right], \quad \varphi_k = 2\pi x_k \tag{9}$$

Corresponding space-signal representation is shown in Fig. 8. Obtained PC signal can be decoded using Viterbi algorithm [5] operated on the trellis with different number of the states. This is direct result of the symbolic dynamics approach. Number of levels is $N=2^M$, and received PC signal can be processed using Viterbi decoder with S=2, 4, 8,...., N states.

In this paper, metric is calculated according to known received signal $r=(r_1, r_2)$ and possible transmitted signals $s_k = (s_{k1}, s_{k2}),\ k = 1,...,S$:

$$d_k = \sqrt{(r_1 - s_{k1})^2 + (r_2 - s_{k2})^2} \tag{10}$$

The performances of CSK systems, based on symbolic dynamics, are estimated using Monte Carlo simulation. Information bit sequences with length N=50000 are considered. The simulation results are presented in Fig. 9. If number of states is greater or equal to 8 and number of output levels is N=S, performances does not depend on number of the states.

However, because of the limited number of output levels (8, 16 or 32), this signal does not "look like" enough to the chaotic signal. Therefore, it is convenient to increase number of the output levels. Simulation results show system performances degradation, especially for small number of decoder states. Even for S=16 performances degradation is small. For the case of S=32, it is practically unnoticeable. By using Viterbi decoder with $32=2^5$ states and $N=128=2^7$ receive signal levels, PC signal with properties similar to the chaotic signal can be synthesized. Furthermore, decoding of this signal is rather simple.

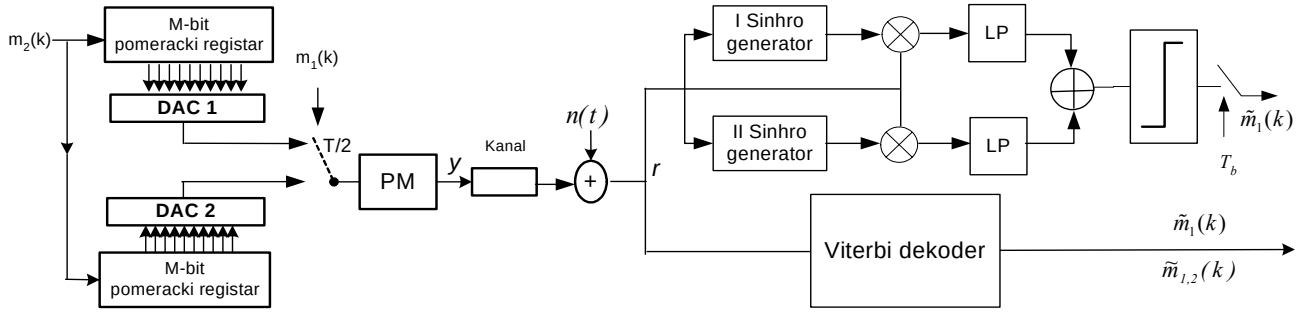

Fig. 7: Blok šema SD-CSK.

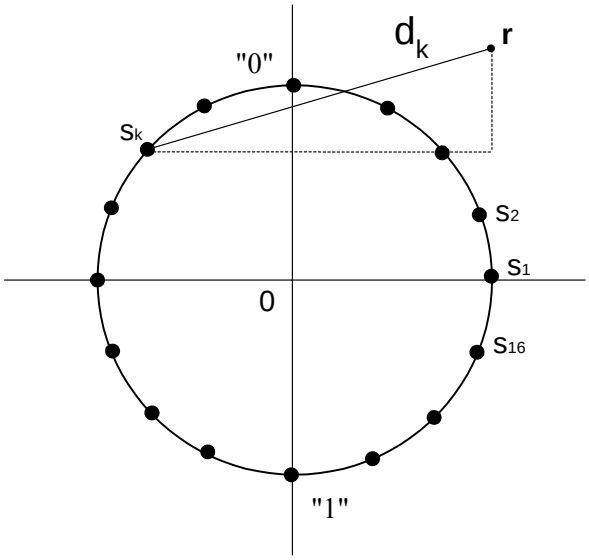

Fig. 8: Constellation diagram for SD-CSK and metrics in decoding process, N=16.

It is interesting to consider what happen if generator in the transmitter create PC signal with great N, and receiver does not have information about number of signal levels. Decoding is then performed according to a less set of possible symbols s_k.

For this case and Viterbi decoder with 16 states and 16 assumed signal levels, simulation results are presented in Fig. 10. If real number of levels of the received signal is greater, performances are similar, but BER floor appear. For greater difference of levels, floor level is noticed for BER=10^{-2}. If assumed number of level is somewhat greater (32, 64, ...), floor will be lower and decoding is more successful. However, this situation is never desirable. Therefore, for reliable communication, number of signal levels in transmitter and receiver has to be matched.

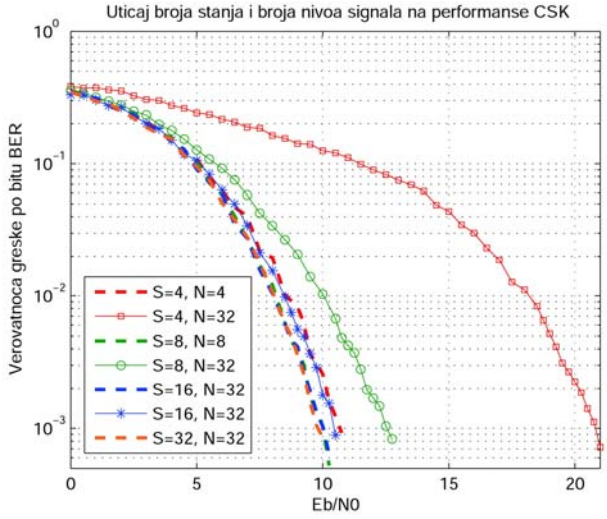

Fig. 9: Effect of number of states and number of output levels on CSK system performances.

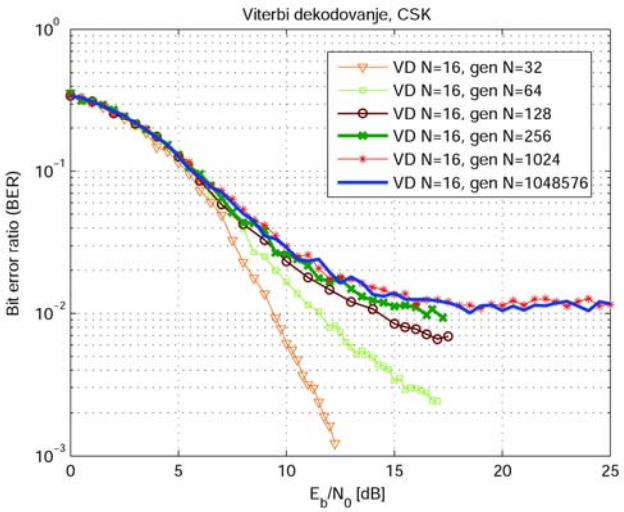

Fig. 10: Effect number of levels mismatch in transmitter and receiver.

6. COMPLETE DECODING

Observing Fig. 7, it can be noticed that two binary sequences, $m_1(k)$ and $m_2(k)$, exist on the system input. It is assumed that $m_1(k)$ bring information and only assumption for $m_2(k)$ is equal probability of symbols "0" and "1". If information sequence is already scrambled, the part of information can be transmitted using sequence $m_2(k)$. Then, information sequence can be demultiplexed to $m_1(k)$ and $m_2(k)$.

In this case, Viterbi decoder is optimal and designed for decoding of both sequences, that is not possible by using correlating receiver. This approach is referred to as complete decoding and simulation results show that gain of about 3 dB can be achieved, as it is presented in Fig. 11. This is expected as one CSK symbol brings two information bits.

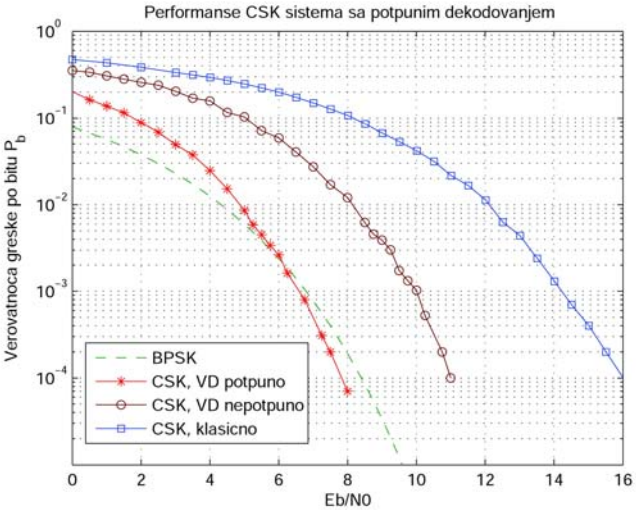

Fig. 11: Performances of CSK system with complete decoding.

Although we assumed that mapping is based on Bernoulli shift, it does not have to be optimal in general case. Furthermore, if system with symbolic dynamics is analyzed, search for optimal mapping types deteriorate to appropriate choice of PC generator coefficients. For Bernoulli shift mapping, optimal coefficients are (1/2, 1/4, 1/8). For the case of S=N=8, this combination results with maximal free distance and coding gain [6]

$$G = 10\log_{10}\frac{d_{free}}{d_0} = 10\log_{10}\frac{2}{\sqrt{2-\sqrt{2}}} = 4.17dB \qquad (11)$$

7. MULTIPATH INFLUENCE

In wireless channel, there is a fading (usually Rayleigh distributed) besides the white Gaussian noise. Signal is transmitted over several propagation paths (multipath environment). Preliminary researches in the area of the chaotic systems with correlation receivers [7] show that chaotic sequences for spectrum spreading are usually uncorrelated. Also, compared with the classical communication systems, capacity increasing is 10-12%.

On the other hand, it is known that DPSK is inherently convenient for using in the systems with multipath propagation. Therefore, similar properties can be expected from DCSK [8], [9]. In the case when DCSK combine with maximum likelihood decoding principle, further improvement of characteristics can be expected.

In further research, performances of the system with several users will be analyzed in details. Also, greater values of spreading factor and more realistic channel models will be considered.

8. CONCLUSION

In this paper, basic principles for the chaotic signal generating have been presented. Also, for the case of CSK and DCSK modulation, possibilities of the transmitter and the receiver generation have been considered. Using simulation approach, known analytical results for the bit error probability in receiver with correlation detector have been verified.

Special attention is given to design of receiver that works on the maximal likelihood principle. Pseudo-chaotic coder structure and system performances for different number of states and output levels have been considered. Incompatibility effect of output level number and assumed level number in the receiver has been analyzed. Complete decoding principle has been specially considered.

Developed simulation model represents a tool appropriate for system analyze in the case of CDMA multipath environment, which represents subject of further research.

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INFLUENCE ANALYSIS OF NON-ACTIVE POWER COMPENSATION ON POWER QUALITY

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Abstract: *This paper presents a new method of non-active power compensation under non-sinusoidal conditions. As non-active power filtering has influence on harmonic distortion, the effect of compensation on power quality is considered. The effect of compensation on power quality for a diversity of load currents is successfully tested using computer simulated tests.*

Keywords: *Non-active power compensation*, *harmonic distortion, power quality.*

1. INTRODUCTION

For electrical circuits with sinusoidal voltages and currents, concepts such as active power, reactive power, apparent power and power factor are well defined. Reactive power represents the measure of oscillating energy flow between the load and source. A great number of electric loads draw from the system not only active power but also reactive power which is necessary to establish the electric and magnetic fields. Those loads, which apparent power consists of active and reactive power, have power factor (cos φ) less than one. The load needs for reactive power can be accomplished by procuring it by synchronous generators but this is not convenient because of the reactive power transmission reduces line transmission capability. Low power factor also causes the voltage drops and additional energy losses in the transmission system. Therefore, the reactive power is mostly produced by the sources located near to loads. In such a way, reactive power compensation e.g. power factor improvement is performed. The most common devices used for reactive power compensation are capacitors. Questions regarding the capacitor location and type and the value of compensating capacitance should be considered.

For the electrical circuits with non-sinusoidal voltages and currents, there is no universally adopted definition of reactive power, apparent power and power factor. The problem is more complex because the oscillating energy flow can not be distinguished from the non-active power caused by the harmonic distortion, so the term non-active power is introduced instead of reactive power. Many definitions have been formulated to characterize non-active power for electrical systems with non-sinusoidal voltages and currents [1-11]. The problems with suggested definitions occur when the compensation circuit should be designed.

Distortions of the voltage and current waveforms occur if the system contains generator of non-sinusoidal voltage, non-linear or time-variant devices. The complex-periodic functions of the distorted voltage and current can be expressed as sums of sinusoidal functions, which angular frequencies are in arithmetic progression. The voltage and current distortions are specially expressed in the presence of magnetic circuits reached the saturation and non-linear impedances (induction furnaces, transformer reached the saturation, arc furnaces). Semiconductor devices also produce harmonics (diode bridges, uninterruptible power supply devices, static converters). The high level of harmonics has unpleasant effect on power system. Therefore, measuring and compensation of harmonics is of great importance [12-14].

This paper presents a method of optimal non-active power compensation of three phase load under non-sinusoidal condition. The harmonic distortions of load current before and after the non-active power compensation are considered, too. In such a way, two important values needed for power quality evaluation are taken into account: the power factor of the load and the factor of harmonic distortion of the line currents (THD factor).

2. NON-ACTIVE POWER COMPENSATION UNDER NON-SINUSOIDAL CONDITION

For a three-phase four-wire system, the instantaneous phase voltages and the line currents can be expressed as instantaneous three-dimensional vectors:

$$\mathbf{u}(t) = \begin{bmatrix} u_a(t) & u_b(t) & u_c(t) \end{bmatrix}^T \quad (1)$$

$$\mathbf{i}(t) = \begin{bmatrix} i_a(t) & i_b(t) & i_c(t) \end{bmatrix}^T \quad (2)$$

The instantaneous voltages and currents are assumed to be periodic quantities:

$$u_j(t) = \sum_{k=1}^{n_j} \sqrt{2} U_{jk} \cos(k\omega t + \theta_{jk}) \,, \; j = a,b,c \quad (3)$$

$$i_j(t) = \sum_{k=1}^{m_j} \sqrt{2} I_{jk} \cos(k\omega t + \psi_{jk}) \,, \; j = a,b,c \quad (4)$$

where U_{jk} is the magnitude of the k-th voltage harmonic of phase angle θ_{jk}, I_{jk} is the magnitude of the k-th current harmonic of phase angle ψ_{jk}, n_j is the highest order of the voltage harmonics, m_j is the highest order of the current harmonics and ω is the angular velocity (equal to $2\pi f$, f being the basic frequency).

The instantaneous active power of a three-phase circuit can be obtained as inner product of the previous two vectors:

$$p(t) = \mathbf{u}(t)^T \, \mathbf{i}(t) \quad (5)$$

and represents the sum of instantaneous powers of the individual phases:

$$p(t) = p_a(t) + p_b(t) + p_c(t) \quad (6)$$

The active power P is time average of the instantaneous power over one period of the instantaneous power $p(t)$:

$$P = \frac{1}{T}\int_0^T p(t)dt \tag{7}$$

The instantaneous power of each phase can be split up into active power components $p_{j\mathrm{p}}$ (j=a,b,c) and oscillating non-active power components $p_{j\mathrm{q}}$ (j=a,b,c),

$$p_j(t) = p_{j\mathrm{p}}(t) + p_{j\mathrm{q}}(t)\ ,\ j = a,b,c \tag{8}$$

in such a way that active components yield constant average power equal to active power P and oscillating non-active components yield average power equal to zero in each phase. The non-active power components are useless power component and should be eliminated, e.g. compensated.

The energy wasted during power transmission has a close relation to the effective value of the current in the line supplying a load. Therefore, the problem of power decomposition and non-active power minimization can be resolved through the minimization of the rms value of the current in the line supplying the load [15,16]:

$$J_1 = \int_0^T f(i(t))dt = \frac{1}{T}\int_0^T \left(i_a^2(t) + i_b^2(t) + i_c^2(t)\right)dt \to \min \tag{9}$$

observing the constraint

$$\int_0^T g(i(t),u(t))dt = \frac{1}{T}\int_0^T \left(\sum_{j=a,b,c} u_j(t)\,i_j(t)\right)dt = P \tag{10}$$

which represents the condition that the active power of the line supplying the load can not be changed. Functional J_1 has the extreme value if functions $i(t)$ and $u(t)$ satisfy the following equation:

$$\frac{\partial f}{\partial i_j} - \mu\frac{\partial g}{\partial i_j} = 0\ ,\ \mu \in R\ ,\ \ j = a,b,c \tag{11}$$

By solving the previous equations the required line currents of minimal effective values are obtained:

$$i_{j\min}(t) = \frac{P}{U_a^2 + U_b^2 + U_c^2}u_j(t)\ ,\ j = a,b,c \tag{12}$$

where U_a, U_b and U_c are the effective values of the phase voltages.

The physical interpretation of expression (12) is that the line currents have to be in phase with the source voltages in order to minimize the effective values of line currents under the constraint of unchanged active power. Expression (12) represents Fryze's definition of instantaneous active currents for three-phase systems.

The amount of active power in the total power (the load power factor) can be expressed as follows:

$$PF = \frac{\sqrt{J_{1\min}}}{\sqrt{I_a^2 + I_b^2 + I_c^2}} = \frac{P}{\sqrt{U_a^2 + U_b^2 + U_c^2}\ \sqrt{I_a^2 + I_b^2 + I_c^2}} \tag{13}$$

The instantaneous active and non-active power components of each phase are:

$$p_{j\mathrm{p}}(t) = u_j(t)\,i_{j\min}(t)\ ,\ j = a,b,c \tag{14}$$

$$p_{j\mathrm{q}}(t) = p_j(t) - p_{j\mathrm{p}}(t)\ ,\ j = a,b,c \tag{15}$$

The instantaneous power for a three-phase system is obtained by summing active and non-active components of each phase:

$$p(t) = p_{\mathrm{p}}(t) + p_{\mathrm{q}}(t) \tag{16}$$

Theoretically, the compensation of non-active power components under non-sinusoidal condition is possible, but for practical implementation a very complex compensator is required because of the complex non-active power waveforms. A shunt compensator of the useless power configured as in Fig. becomes a generator of the non-active power. After the compensation the power factor will be PF'=1.

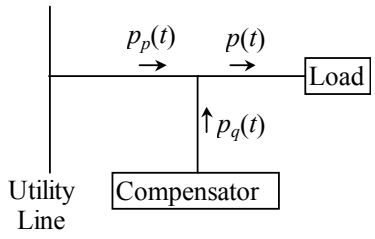

Fig. 1. *The non-active power compensation*

Question how a real compensator can be constructed should be considered. In order to find the optimal compensating capacitances for a three-phase system, e.g. the compensating capacitances which provide the best current reduction, the following criterion can be established:

$$J_2 = \frac{1}{T}\int_0^T \sum_{j=a,b,c}\left(C_j\frac{du_j(t)}{dt} + i_j(t)\right)^2 dt \to \min \tag{17}$$

Functional J_2 has the extreme value if the following condition is satisfied:

$$\frac{\partial J_2}{\partial C_j} = \frac{2}{T}\int_0^T \frac{du_j(t)}{dt}\left(C_j\frac{du_j(t)}{dt} + i_j(t)\right)dt = 0\ ,\ j = a,b,c \tag{18}$$

Solving the previous equation, the optimal compensating capacitances are obtained:

$$C_{j\,\mathrm{opt}} = -\frac{\frac{1}{T}\int_0^T \frac{du_j(t)}{dt}i_j(t)dt}{\frac{1}{T}\int_0^T \left(\frac{du_j(t)}{dt}\right)^2 dt} = \frac{\sum_{k=1}^{\min(n_j,m_j)} k\omega U_{jk}\,I_{jk}\sin(\theta_{jk} - \psi_{jk})}{\sum_{k=1}^{n_j} k^2\omega^2 U_{jk}^2}$$
$$j = a,b,c \tag{19}$$

The factor which defines the amount of active power in the total power (the power factor) after the compensation is:

$$PF' = \frac{\sqrt{J_{1\min}}}{\sqrt{J_{2\min}}} \tag{20}$$

3. INFLUENCE OF THE COMPENSATION ON CURRENT DISTORTION

The presence of harmonics in current causes the overload which can be expressed by using the effective value of complex-periodic current. The contents of harmonics in the load current can be determined by using THD factor:

$$THD_j = \sqrt{\sum_{k=2}^{m_j} I_{jk}^2} \Big/ \sqrt{\sum_{k=1}^{m_j} I_{jk}^2}\ ,\ j = a,b,c \quad (21)$$

The THD factor can be expressed in the time domain, as follows:

$$THD_j = \sqrt{1 - \frac{2\left(\left(\frac{1}{T}\int_0^T i_j(t)\cos(\omega t)dt\right)^2 + \left(\frac{1}{T}\int_0^T i_j(t)\sin(\omega t)dt\right)^2\right)}{\frac{1}{T}\int_0^T i_j^2(t)dt}}$$

$$j = a,b,c \quad (22)$$

Non-active power compensation can increase the harmonic contents of the line currents. The presence of harmonics is unpleasant because they cause problems by overloading and overheating capacitors used for non-active power compensation and by causing their aging. The harmonic components also cause problems because they flow through electrical network. The problem is more severe when the condition for parallel resonance between the network and the capacitor is fulfilled.

By comparing the power factor before and after the reactive compensation, the influence of compensation on power quality can be considered. A compromise between allowed line current harmonic distortion and required load power factor should be made.

4. SIMULATION RESULTS

A case study of a three-phase system with sinusoidal and balanced source voltages and distorted and unbalanced load currents is considered. The load currents are assumed to contain 10% of all odd harmonics up to the seventh order (Fig. 2). The line currents obtained after the compensation of whole non-active power and after the compensation by using the capacitors of optimal capacitances ($C_{a\text{opt}}$=0.0029 p.u., $C_{b\text{opt}}$=0.0013 p.u. i $C_{c\text{opt}}$=0.0025 p.u.) are presented in Fig. 3.

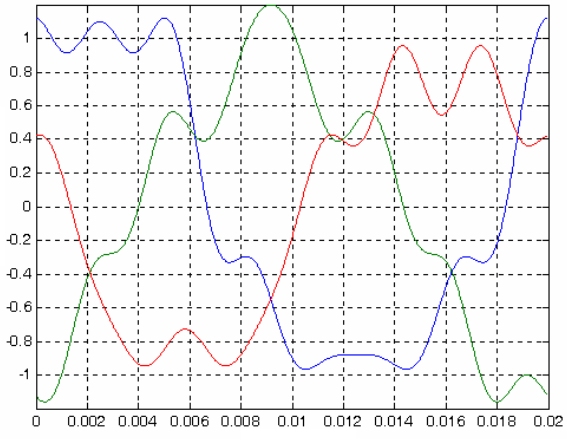

Fig. 2: *Three-phase load currents*

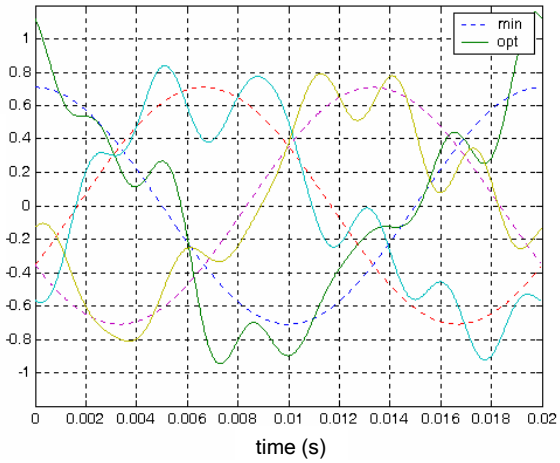

Fig. 3: *The line currents obtained after the compensation of whole non-active power and after the compensation by using the capacitors of optimal capacitances*

The load power factor and the factors which define power quality before the compensation are presented in Table 1. The load power factor and the factors which define power quality after the compensation of whole non-active power and after the compensation by using the capacitors of optimal capacitances are presented in Tables 2 and Tables 3.

Table 1: *The power factor of non-compensated load and the factors which define power quality*

	phase a	*phase b*	*phase c*
I	0.8008	0.7280	0.6625
THD	0.2379	0.2379	0.2379
PF	0.6848		

Table 2: *The load power factor and the factors which define power quality after the compensation of whole non-active power*

	phase a	*phase b*	*phase c*
I	0.5017	0.5017	0.5017
THD	0	0	0
PF'	1		

Table 3: *The load power factor and the factors which define power quality after the compensation by using the capacitors of optimal capacitances*

	phase a	*phase b*	*phase c*
I	0.5827	0.5301	0.4802
THD	0.3269	0.3267	0.3282
PF'	0.9418		

A case study where the source voltages and the load currents are distorted and unbalanced is then considered. The load currents are the same as in the previous example. The source voltages contain harmonics which are found in a real power system: third (1.5%), fifth (3.5%), and seventh (1%)

harmonic (Fig. 4). The line currents obtained after the compensation of whole non-active power and after the compensation by using the capacitors of optimal capacitances are presented in Fig. 5.

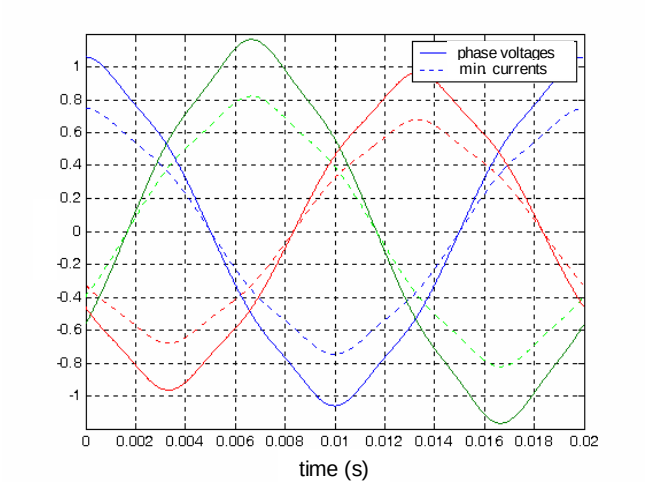

Fig. 4: *Three-phase source voltages and the line currents obtained after the compensation of whole non-active power*

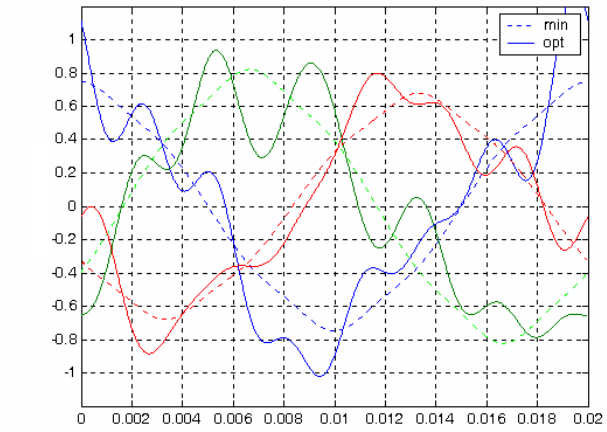

Fig. 5: *The line currents obtained after the compensation of whole non-active power and after the compensation by using the capacitors of optimal capacitances*

The load power factor and the factors which define power quality before the compensation are the same as in the previous example (Table 1). The load power factor and the factors which define power quality after the compensation of whole non-active power and after the compensation by using the capacitors of optimal capacitances are presented in Tables 4 and 5.

Table 4: *The load power factor and the factors which define power quality after compensation of whole non-active power*

	phase a	*phase b*	*phase c*
I	0.4985	0.5484	0.4536
THD	0.0393	0.0393	0.0393
PF'	1		

Table 5: *The load power factor and the factors which define power quality after the compensation by using the capacitors of optimal capacitances*

	phase a	*phase b*	*phase c*
I	0.5913	0.5417	0.4796
THD	0.3621	0.3676	0.3237
PF'	0.9300		

It can be noticed from the previous two examples that the total non-active power compensation includes the compensation of harmonic distortion of the line currents. Non-active power compensation using reactive compensators improves the load power factor but also increases the harmonic contents of the line currents.

5. CONCLUSION

This paper presents a new method of non-active power compensation under non-sinusoidal voltages and currents. The influence analysis of non-active power compensation on power quality has been considered. The total non-active power compensation includes the compensation of those harmonics in the line currents which originated from the line currents. The non-active power compensation using reactive compensators improves the load power factor but also increases harmonic contents of the line currents. When the source voltages are also distorted, the harmonic contents in the line currents are additionally increased. Therefore, a compromise between allowed line current harmonic distortion and required load power factor should be made.

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TESTING AND DIAGNOSTICS OF ADC FOR AN INTEGRATED POWER METER

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Abstract: *Modern power-meters are based on digital processing of instantaneous signals values. ADCs are very important parts of such systems. Their significance requires special attention during the design process. Testing and diagnostics techniques for the ADC implemented in the integrated power-meter are described in this paper. The prototype is designed as ASIC and realized in 035μm CMOS technology. In addition to the implemented DFT, DFD and BIST solutions, it was necessary to develop an efficient and inexpensive test set-up, that enabled high-quality performance measurements in the laboratory environment, avoiding the use of expensive industry testers.*

Keywords: *Testing, Diagnostics, ADC.*

1. INTRODUCTION

ADCs are common mixed-signal components in complex mixed-signal designs, since they form the interface between the real world and the world of digital logic. Comprehensive testing of ADCs is expensive, because there is wide variety of ADC designs that require different techniques and equipment to test them. It is a process that drives up the cost of integrated circuits without adding any new functionality. Testing cannot change the quality of the individual ICs; it can only measure the quality if it already exists. However, semiconductor companies would not spend money to test products if the testing process did not add value [1].

Testing may create a serious limitation for high-volume commercial applications due to the testing difficulties inherent to microsystem under test. Accessibility, controllability, and observability must be insured since encapsulated, miniaturized, integrated microsystem has only a few additional output connections. Besides, in order to determine the cause of malfunction, it is important to have good diagnostic possibilities. Some internal nodes must be made accessible. Therefore, a major problem is controlling the set-up of test conditions and the observation of test responses of a device under test (DUT).

Functional multidisciplinarity is major obstacle because different parts of a mixed signal microsystem, such as analog or digital signal processing parts, require completely different approaches to testing. Developing a set-up for test assumes that a DUT usually needs to be brought into defined state before testing starts. This is inherently difficult for systems where special environmental conditions are required.

Interference of signals is another issue of mixed-signal testing. In a highly integrated microsystem, the various subsystems are in immediate proximity and therefore can influence each other, i.e. the heat dissipation of a digital signal processor (DSP) may influence analog circuitry.

We intend here to present ADC testing theory, DFT techniques, and measurements that are related to a practically implemented converter. Special attention will be paid to the testing of a sigma-delta ADC. Some hints related to possible approach to diagnostics will be given.

The paper is organized as follows. In the second section DFT specifications for ADC based on sigma-delta modulator is described briefly. The subsequent section deals with the test set-up structure. It was necessary to develop additional hardware as well as a software to control data acquisition card. Diagnostic aspect of ADC testing is highlighted briefly in the fourth section. ADC testing strategy will be explained in the fifth chapter. Afterward, test set-up and corresponding testing procedure will be described in two subsequent sections. The last section presents test results of the ADC implemented within the integrated power meter.

2. DFT SPECIFICATIONS FOR ADC

Generally, sigma-delta analog-to-digital converters (ΣΔ ADC) use a crude ADC combined with a noise-shaping process to produce an oversampling pulse density modulated data stream. This data stream is then digitally filtered and decimated to produce high-resolution ADC samples. ΣΔ ADC are typically used to digitize continuous signals in sampled channels [2].

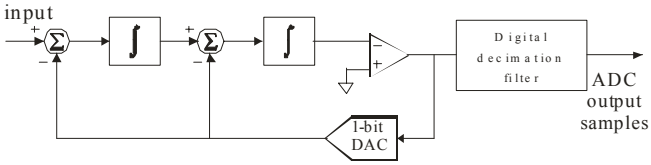

Fig.1: Second order sigma-delta ADC

Architecture of the ADC embedded into the integrated power meter [3] is shown in figure 1. It consists of a sigma-delta modulator and a decimation filter. The ΣΔ modulator coarsely quantizes the input at a high rate, trading accuracy in the analog circuitry for speed. The quantization noise is effectively pushed out of the desired band into higher frequencies providing, a higher resolution after filtering and decimation. The dynamic range of the modulator depends on the oversampling ratio (OSR) [2]. Increasing the order results in more complexity, while increasing the OSR requires faster op-amp settling.

The second block of a ΣΔ ADC is a decimation filter. Its function is to remove all out-of-band signals and noise, and to reduce the sampling rate by M [2]. For the integrated power meter M=128 [3]. By averaging M values of the coarsely quantized sigma-delta output, the filter gives a high-resolution output (21 bit) at the low rate of 4,096 kHz.

According to the given converter's mixed structure, it is necessary to develop some DFT techniques for its testing. The concept of an ADC DFT is shown in figure 2 [3]. It can be noticed that this concept offers observing and analyzing

both analog and digital signals. Analog signals at the output of each integrator stage are differential and using an analog multiplexer they can be selectively observed at output pins. Output of the sigma-delta modulator is digital. This signal is available at one bidirectional pin of the chip. It must be acquired in real time with the oversampling frequency of 524.288 kHz. The test set-up must satisfy this demand. These digital signals are fed into decimation filter that follow. In case that sigma-delta modulator does not operate, there is an additional pin that controls the direction of this data flow. By setting this bit, digital input data for the decimator stage can be brought into from the external circuitry using the same pin.

Each decimator contains 4 stages. Two of them are Sinc filters which perform decimation by the factor 8 and 4 respectively, and the other two stages are FIR filters which also perform decimation by factor 2 each and reduce the out-of-band noise. At the output of the decimator resolution of the digital input signal is increased from 1 to 21 bit while the sampling rate is decreased 128 times. Finally, the output signal is stored as 24-bits wide digital word 4096 times in a second in the output register. This register can be accessed using three wire serial communication port (SCP) [4] at rate of 400 kHz.

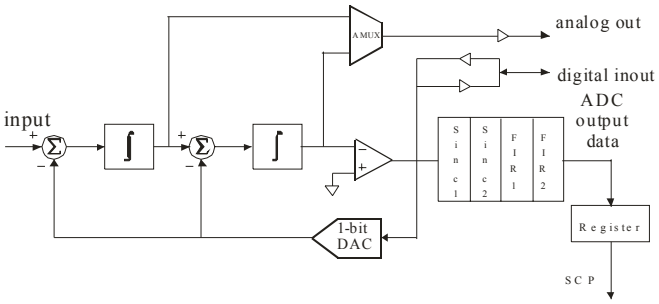

Fig.2: DFT for the ADC

In addition, the voltage reference [5] and the clock signal are left as the output pins for testing purposes. This clock signal is necessary for synchronization during the real-time acquisition.

3. ADC TESTING

Typical ADC tests are: ADC code edge measurement, DC tests, transfer curve tests, and dynamic ADC tests. Each one of them will be explained now [1].

3.1. ADC Code Edge Measurement

The aim of this test is to find the input voltage threshold between two successive ADC codes that causes an output code change. To measure ADC intrinsic parameters such as integral nonlinearity (INL) and differential nonlinearity (DNL), which will be explained later, an ADC transfer curve must be derived. Two well-known methods for this are *center code testing* and *edge code testing* [1]. Code centers are defined as the midpoint between the code edges. This is shown in figure 3.

One should note that the code centers fall very nearly on a straight line, while the code edges show much less linear behavior. The center code testing should be avoided because it produces an artificial low DNL value.

There are several different ways to search for the code edges. The most obvious method to find the edge is a step search method where one simply adjusts the input voltage of the ADC up or down until the output codes are evenly divided between the first code and the second code. To achieve repeatable results, one needs to collect about 50 to 100 samples from the ADC in order to provide statistically significant number of conversions. This method can be very time consuming for high resolution ADCs and is not a production-worthy solution.

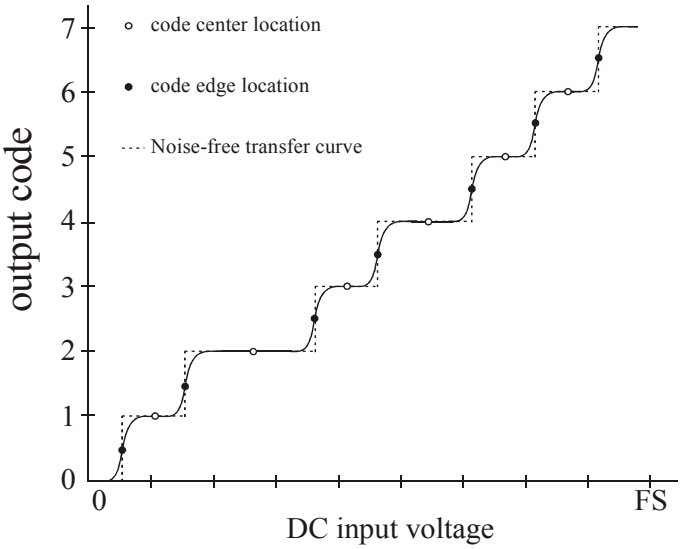

Fig.3: Code edges and code centers

The next technique for edge search is a servo method. This is actually a fast hardware version of the step search. By using this hardware, the output codes from ADC are compared against a value programmed in the search value register. If the ADC output is greater than or equal to the expected value, the integrator ramps downward. If it is less than the expected value, the integrator ramps upward.

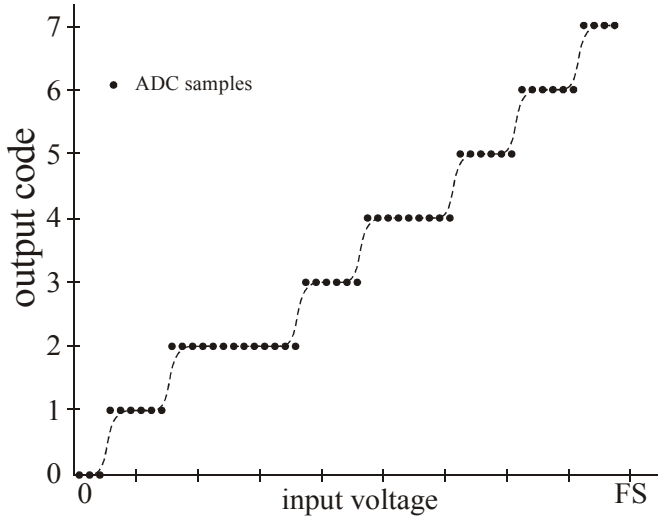

Fig.4: ADC samples from linear ramp histogram test

The most common production testing technique is the histogram method. It can be the linear ramp method or the sinusoidal method. The simplest way to perform a histogram test is to apply a rising or falling linear ramp to the input of the ADC and collect samples from the ADC at constant sampling rate. The ADC samples are captured while the input ramp slowly moves from one end of the ADC conversion range to the other. This is shown in figure 4. Now the number of occurrences of each code is plotted as a histogram. Ideally, each code should be hit the same number of times, but this would only be true for perfectly linear ADC. The

histogram shows which codes are hit more often, indicating that they are wider codes. After obtaining the histogram, a code edge transfer curve must be derived using a simple mathematical equation that sums the code widths.

To compensate for the poor linearity of the ramp generators, the alternative: sinusoidal histogram method can be performed. It is easier to produce a pure sinusoidal waveform than to produce a perfectly linear ramp. This method also allows testing in more dynamic, real-world situation, since ramps are varying very slowly. By using a sinusoidal signal instead of a ramp, one would expect to get more code hits at the upper and lower codes than at the center of the ADC transfer curve, even when testing a perfect ADC. This is shown in figure 5.a. This can be compensated by using an uneven distribution of voltages inherent to sinusoidal waveforms, shown in figure 5.b. The effects of the nonuniform voltage distribution can be removed after normalization.

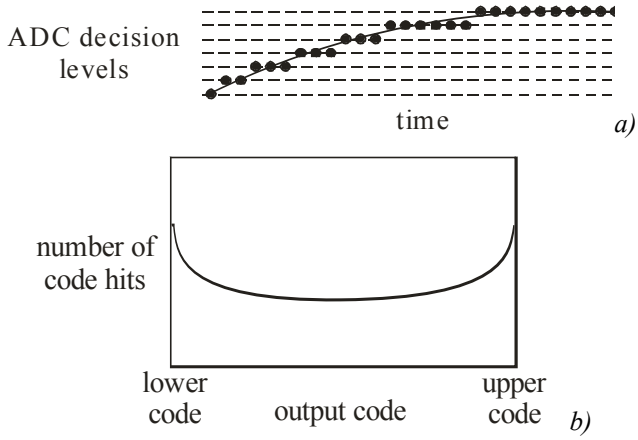

Fig.5: a) ADC samples from sinusoidal histogram test; b) Sinusoidal histogram for an ideal ADC

3.2. DC Tests and Transfer Curve Tests

DC Tests and Transfer Curve Tests comprise:

- DC Gain
- DC offset,
- INL,
- DNL,
- monotonicity and
- missing codes tests.

Once the ideal transfer curve has been established, DC gain and offset can be measured. The gain and offset are measured by calculating the slope and offset of the best-fit line. Sometimes, offset is defined simply as the offset of the first code edge from its ideal position while the gain is defined as the ratio of the actual voltage range divided by the ideal voltage range [6].

DNL is the difference between each analog increment step and the calculated device LSB increment.

INL is the worst-case variation in any of the code boundaries with respect to an ideal straight line drawn through the endpoints. It is also sometimes defined in comparison to a "best fit" straight line. These two parameters are shown in figure 6 [7].

In order to obtain DNL and INL one has to determine LSB step. Device LSB step is calculated by dividing the total span of the ADC by the number of corresponding analog input transition steps, or code transitions.

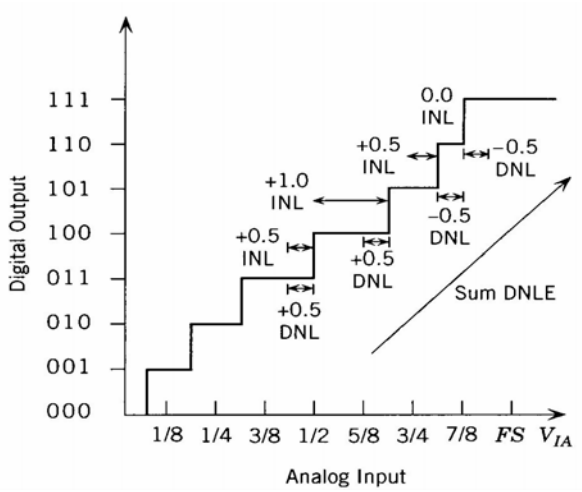

Fig.6: DNL and INL of an ADC

ADC can be nonmonotonic when one or more of its code widths is negative. However, this failure mechanism is quite rare. Nevertheless, ADC can appear to be nonmonotonic when its input is changing rapidly. ADCs are not tested for monotonicity with a slowly changing input. Monotonicity errors show up as signal-to-noise ratio failures and as a sparkling.

The code whose voltage width is zero is recognized as a missing code. This means that the missing code can never be hit, regardless of the ADC's input voltage. A missing code appears as a missing step on an ADC transfer curve. Although a true missing code is one that has zero width, missing codes are often defined as any code having a code width smaller than some specified value.

3.3. Dynamic ADC Tests

Dynamic ADC parameters are:

- maximum sampling frequency,
- maximum conversion time, and
- minimum recovery time.

Maximum conversion time is the maximum amount of time it takes an ADC to produce a digital output after a stabile input signal is asserted. The ADC is guaranteed to produce a valid output within the maximum conversion time.

It should be mentioned that an ADC's maximum sampling frequency is simply the inverse of the maximum conversion time. Some ADCs require a minimum recovery time, which is the minimum amount of time the system must wait before asserting the next input signal level to be converted. This definition also changes the maximal sampling frequency as the inverse of the maximum conversion and minimum recovery time sum.

Typically, aperture jitter is guaranteed by acceptable signal-to-noise ratio (SNR) performance. It introduces noise in a digitized signal. This test must be performed in very high-frequencies ADCs.

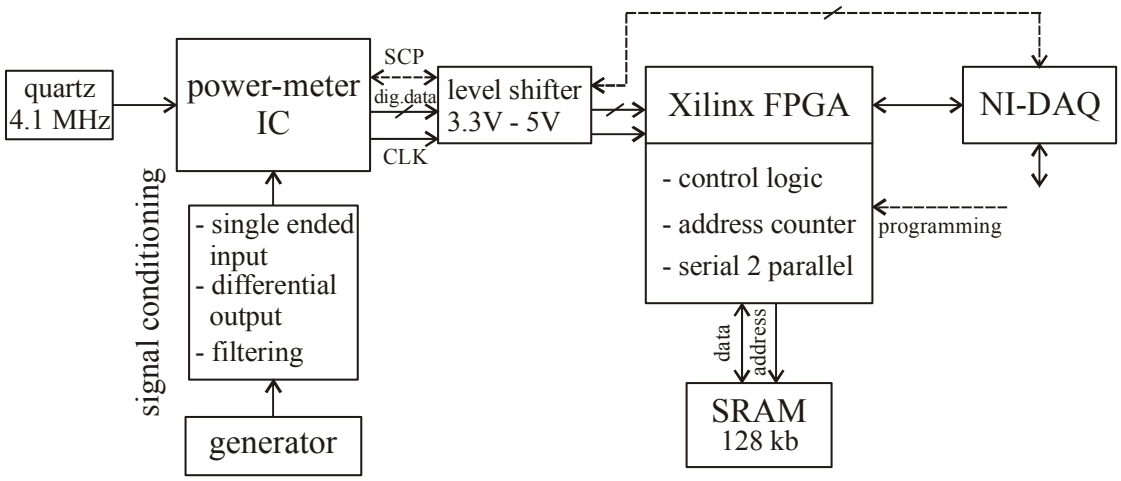

Fig.7: ADC test set-up

Sparkling is the next occurrence to be tested. This is a phenomenon that happens most often in high-speed converters. It is the tendency for an ADC to occasionally produce a conversion with an offset larger than the expected value. The sparkling shows up in time-domain as an abrupt variation from the expected values. Though, sparkling is specified as a maximum acceptable deviation from the expected conversion result. For example, one might find in an ADC datasheet that sparkling is specified as less than 2 LSBs. This means that a casual discrepancy greater than 2 LSBs never occurs. Since it is a random digital failure process, sparkling often produces intermittent test results.

ADC sparkling tests are often added to a test program as a quick sanity check, making use of samples collected for one of the required parametric tests.

Considering all tests listed and an existing architecture of the ADC, it is very important to establish the significance of tests to be performed. Tests such as INL and DNL are not well suited for sigma-delta converters. Instead, channel tests like gain, offset, signal-to-noise ratio, idle channel noise, etc., are commonly specified. Additionally, ΣΔ ADCs may produce self-tones when their inputs are set to certain DC levels. Self-tones appear as spikes in the frequency spectrum of an ADC output. Unfortunately, self-tones do not occur at predictable frequencies. This makes worst-case self-tone testing very difficult.

ADC resolution puts a new scope into testing. When the resolution exceeds 12 or 13 bits, it becomes very expensive to perform transfer curve test such as INL and DNL because of the large number of code edges that must be measured. Fortunately, transmission parameters such as frequency response signal to distortion ratio and idle channel tests are much less time-consuming to measure. It is also impractical to test self-tones at every possible DC input level. Self-tones should at least be tested with the analog input tied to ground. When characterization indicates that a particular ADC design is not prone to self-tones generation, then this test is often eliminated in production [1].

A limited budget also limits the list of tests that can be performed in the laboratory environment. By performing further industry testing, a complete view of the correct ADC design can be carried out.

4. ADC DIAGNOSTIC

Another important issue in ADC testing arises when a fault is detected. Actually the main designer's task is to determine the cause of the malfunction and to remove it by redesign. This is especially important during the prototyping phase. The problem is very complex because different types of soft (parametric) and hard (catastrophic) faults in analog part are likely to exhibit similar behavior.

Technical diagnostics is one of the most attractive research subjects today. Modern, powerful concepts allow for new breakthroughs to be done in this area. One of these concepts is application of artificial neural networks (ANNs) for the purpose of fault detection.

Such an application is shown on an example of analog nonlinear dynamic electronic circuit with no restriction to the number and type of faults [8]. An integrated CMOS operational amplifier was used as a case study of implementation.

The concept is based on fault dictionary creation and application of ANN as both: the system for data compression that memorizes the table representing the fault dictionary, and the mapping machine that looks-up the table to find the most probable fault-code. Exhaustive list of soft and hard faults is easily modeled and isolated, such as open-circuited faults, short-circuited faults, faulty values for every transistor channel length, and for every channel width.

This approach is very promising since it allows mixing domains, which can be extremely useful to establish methods for diagnostics in mixed signal circuits, in order to cover faults in both analog and digital part of the circuit.

5. TEST SET-UP STRUCTURE

According to the DFT techniques applied during sigma-delta ADC design, and to available acquisition hardware, original test set-ups for two kinds of data acquiring were developed.

One test set-up was developed for collecting high frequency small resolution digital data at the output of the sigma-delta modulator in real-time. This test set-up is shown in figure 7 [9]. It consists of a signal conditioning block, memory block, control block, level shifter and acquisition hardware.

The control logic block is implemented on FPGA Xilinx XC4003E [10]. It is designed to generate control and address signals during the real-time data loading from the

sigma-delta modulator into the memory block (128kb SRAM) in one direction, and the corresponding hand-shake protocol needed to transfer data from RAM to the PC using NI-DAQ PC-DIO-96-PnP acquisition card [11].

In addition, this set-up includes quartz oscillator, microswitches, level-shifting circuits that adjust the logic level between different blocks of the set-up and sine-wave generator.

The same test set-up was rearranged for acquiring digital data at the output of the ADC (dashed lines). These data have low data-rate as well as high resolution. They are available at the output of the chip and are approachable only through two SCP (serial communication port) pins.

Since both test set-ups use the PC for storing data, it was necessary to develop software that enables communication between embedded protocols of different parts of the testing systems.

6. TEST PROCEDURES

Developed test set-ups are capable to provide:

- DC and transfer curve tests: gain, offset, linearity, monotonicity,
- Tests in frequency domain: idle channel tests and SNR measurement.

DC and transfer curve tests require set-up that enables reading digital data stored in one register of the chip. During the testing, the ADC is differentially fed with a very slow linear ramp (5 Hz at most). Data from the register are stored in the PC where they can be further analyzed. After adjusting the input voltage range of the ramp, and after applying it to the input of the ADC, digital values at the output of the converter are read as well as the absolute time of reading, which corresponds to the instantaneous voltage level at the input.

The high resolution of 24 output bits obstructed INL and DNL measurement. Obtained ADC transfer curve does not show edge or level but gain and offset can be calculated.

Frequency domain tests are convenient to determine parameters of ADCs based on sigma-delta modulator [9]. These tests require higher frequencies and lower resolution.

During this test it is important to collect digital data from the output of the sigma-delta modulator. ADC is stimulated with differential sinewave (50Hz) signal with amplitude of up to 250 mVpp. The single bit output of sigma-delta ADC is observable through an external bidirectional port.

SRAM stores the output data for real time period of one second. Afterward the data are transferred from SRAM block into the PC for further analysis.

This set-up can deal with different clock frequencies (up to 50MHz) and different signal waveforms. It is easy to upgrade with additional SRAM cells in order to increase the amount of collected digital data.

Due to implemented DFT techniques, this set-up enables observing voltage levels at the output of each integrator stage in the time domain using oscilloscope.

7. TEST RESULTS

Figure 8, shows obtained transfer curve. It gives a clue about the monotonicity, gain, and offset of the ADC. The statistics of this graphic are shown in figure 9. The input voltage varies from -250mV to 250mV, while the output is signed 24-bit digital word. It should be noted that full scale input voltage range does not drive the output into saturation. Figure 8 represents transfer curve without gain and offset correction that can be provided by the DSP part of the power meter.

The obtained results indicate that within the required input voltage range (from -125mV to +125mV), ADC gain has a value of 1.18, while offset is 8.66% of the full scale.

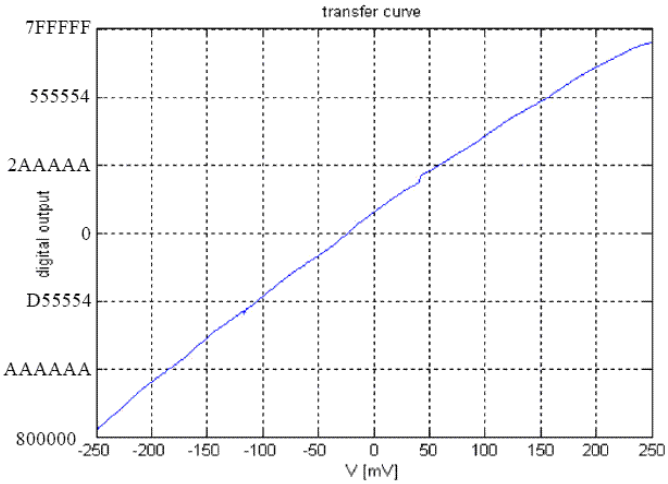

Fig.8: Test results of a transfer curve ADC testing

	X		Y	
min	-250		-405.5	
max	250		391.4	
mean	0.7738		27.67	
median	-3.054		36.6	
std	145.8		237.1	
range	500		796.8	

Fig.9: Statistics of the obtained ADC transfer curve

Figures 10 and 11 show results of obtained power spectra. The output spectrum of the idle channel (no input signal) obtained applying FFT over the acquired output of the second order modulator channel is shown in Fig. 10. The output spectrum of the modulator supplied with a sinewave of 50Hz and amplitude of 125mVpp is shown in Fig. 11.

Comparing these spectra one concludes that spurious tones are imported with the input signal. Using previous results (Fig. 10 and Fig. 11) one can extract essential ADC parameters such as SNR and SFDR. Besides, conclusions can be made about the noise shaping function.

For the obtained spectra the following sigma-delta modulator parameters may be predicted:

- SFDR is -52dB, in bandwidth up to 2kHz
- SNR is -70dB in bandwidth up to 2kHz
- noise shaping slope is 40dB/decade.

ADC's are rather demanding from the system diagnostics point. Defects are hard to detect, i.e. locate unless it is hard. In this case diagnostics comes down to the detection of faulty blocks within A/D chain. Within our laboratory there are research efforts in solving this problem using artificial neural networks [8].

Therefore, by analyzing the signals available in this chain, shown in Fig. 2, faulty blocks can be detected. Accordingly, fault detection in the first integrator stage can be performed by analyzing its output signals. These signals should be symmetric, thus, any asymmetry would indicate fault in the integrator stage. These faults could include badly matched switched capacitors, wrong modulator coefficients or faults in operational amplifier. Similar discussion could be applied for the second integrator stage.

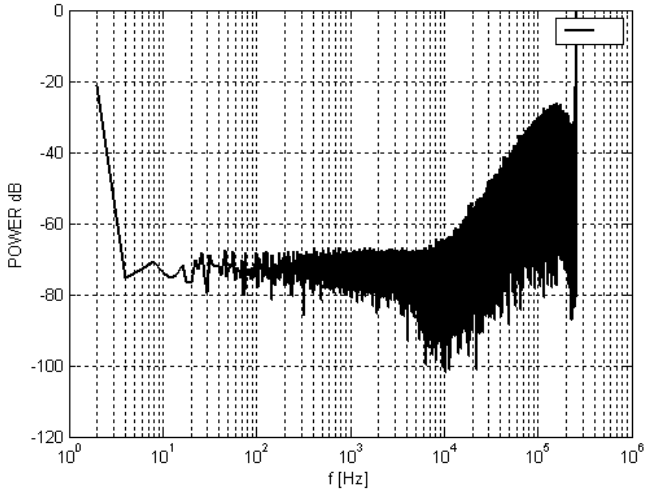

Fig.10: Power spectrum of ADC output during idle testing condition

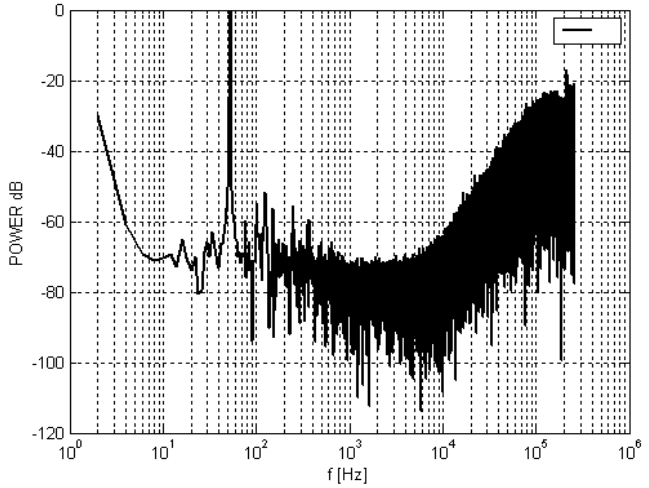

Fig.11: Power spectrum of ADC output stimulated with a sinewave of 50Hz and 125mVpp.

Integrator outputs are fed into quantizer, and then into flip-flop. These signals are digital and, thus, can be connected to the digital IO pin, enabling the acquisition and FFT analysis. Faulty FFT of these signals would imply faults in the quantizer or the flip-flop circuits.

Within digital filters, signal frequency is reduced and the resolution is increased. Digital output signals can be used for fault detection in the filter block.

Output of the bandgap circuit is connected to the output pin, enabling the fault detection of the bandgap circuit. In case of the bandgap malfunction, external referent voltage can be feed into the chip.

8. CONCLUSION

ADC testing theory, DFT technique and practical measurements are presented in this paper. A special attention is paid to testing of ΣΔ ADC. All levels of tests are performed in the laboratory environment and a further industry testing is planned, as well. ADC testing required the development of the test set-up that contains hardware and software solutions. The implemented testing methods are very simple and offer functional oriented testing for a very low cost and give a good base for diagnostics as well.

ACKNOWLEDGEMENT

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REGULATION AND TRACKING IN DIGITAL SYSTEMS WITH CROSS-COUPLING CONTROL

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Abstract: *In the previous papers of the authors the novel structure of two distant speed-controlled or positioning servodrives with cross-coupling control has been proposed. The structure enables synchronous motion of the servomechanisms. The suggested cross-coupling control is based upon the idea of simulating effects that appear in a virtual mechanical link between the shafts of drives. In this paper, a novel approach to design a cross-coupled regulator of nonlinear contour tracking is proposed. The tracking and regulation problem can be united by introducing the reference input into the regulator. Results of analytical design are verified by computer simulation runs of an elliptic contour tracking example.*

Keywords: *Tracking systems, Regulators, Digital control, Coupling coefficients, Observers.*

1. INTRODUCTION

In many engineering applications (biaxial control of machine tools, cross-coupling motion controller for mobile robots, biaxial computer control for manufacturing systems, automatic guidance system of self-controlled vehicles, for example), the speed or angular positions of shafts of two distant electromechanical drives are to be controlled simultaneously. The control must enable the desired transient responses and zero steady-state values of position and speed error signals. To match these requirements, different control structures have been proposed and tested. The original structures of cross-coupling speed and position control based on the application of the concept of electrical shaft are proposed in the papers [1] and [2], respectively. Namely, the cross-coupling control is accomplished by a digital simulation of stiffness and friction of a virtual twisting mechanical connection between the output shafts of the drives.

In [3]-[12], results of the research of authors and their cooperators during the period lasting many years were directed towards the improvement of the controlling structure of cross-coupling motion. In the research, the DC and induction motors have been used. The particular attention has been paid to the development of methods enabling sufficiently accurate observation of the system state variables in the presence of constant or slow varying external load torque disturbances acting on the motor shaft.

Fig. 1 illustrates the controlling structure of a positioning servosystem with cross-coupling control, suggested in paper [5]. Angular positions $\theta_1(t)$ and $\theta_2(t)$ of two distant electrical drives represent controlled variables. In the steady-state, angular positions of drive shafts are to be the same and equal to the common reference θ_{ref}. The system is subjected to three kind of disturbances: set point $\theta_{ref}(t)$, initial angular displacement $\Delta\theta(0) = \theta_1(0) - \theta_2(0)$ and load torques $T_{L1}(t)$ and $T_{L2}(t)$ acting on first and second drive, respectively.

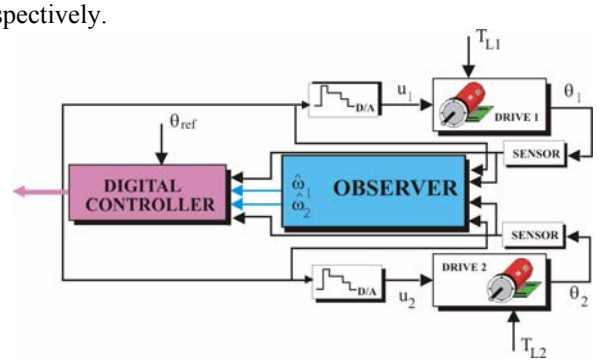


Fig.1: *Block diagram of a servosystem with cross-coupling control*

In Fig. 2, the structure of digital controller is shown in details. The angle positions of the cross-coupled servos are controlled by the common position controller (PI structure, for example). The cross-coupling mechanism comprises two elements: (i) Coupling channels that simulate the viscous friction and stiffness of a virtual mechanical shaft coupling the servos; (ii) Digital PI controller that eliminates the difference between the steady-state values of angular positions of the servos. Such kind of cross-coupling control based on the digital simulation of torques of a virtual mechanical link between the shafts of servomechanisms, represents the main feature of the suggested structure.

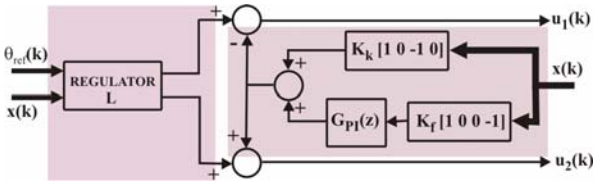


Fig.2: *Digital controller structure in a positioning servosystem with cross-coupling control*

The use of observer included into the scheme of cross-coupling control system is illustrated in Fig. 1. The observer processes the torque commands and the quantized signals from the position transducers and enables the correct estimation of shaft speed signals in the presence of the constant or slow varying load torque disturbances.

The efficiency of synchronization of two drives and other advantages of the developed cross-coupling control based upon the application of the conventional digital PID controllers were given in the previous papers. The most important features and steady-states behaviour of the proposed system have been analyzed in details. Also, the

suitable procedures for setting of controller parameters with respect to the desired system continuous-time responses are given.

In this paper, the synthesis of controlling structure for coordinated contuor motion in a two-axis system is shown. By designing an additional dynamics, the contour tracking is reduced to the problem of controlling the system with two cross-coupled electrical drives. Advantages of the suggested structure and results of outlined method of control parameter tuning are verified by simulation runs.

2. REGULATION AND TRACKING IN CONTROL TASKS

Recall, the solution of the regulation problem means that the state variables of the system will remain close to their equilibrium value (e.g. zero) in the presence of external disturbances. The state feedback is a simple but powerful technique for solving the regulation problem, even in the case of unstable systems. Another important class of problems are met in tracking requirements wherein the system output should be close or equal to system reference signal. Note that the tracking problem reduces to a regulation problem in the case of the zero reference signal. In general, the tracking and regulation problems are unified by introducing the so called concept of zero-input state trajectories.

The design procedure is based on models of the control plant with transfer function $G_0(s)$, disturbance $w(t)$, and reference input $r(t)$. For the sake of clarity, it is convenient to introduce the realization sets as follows:

$$\mathsf{S}_0 \overset{\text{def}}{=} \left\{ (\mathbf{A},\mathbf{b},\mathbf{d}) : G_0(s) = \mathbf{d}\left(s\mathbf{I}-\mathbf{A}\right)^{-1}\mathbf{b} \right\}, \tag{1}$$

$$\mathsf{S}_{0d} \overset{\text{def}}{=} \left\{ (\mathbf{E},\mathbf{f},\mathbf{d}) : G_{0d}(s) = \mathbf{d}\left(z\mathbf{I}-\mathbf{E}\right)^{-1}\mathbf{f} \right\}, \tag{2}$$

$$\mathsf{S}_w \overset{\text{def}}{=} \left\{ (\mathbf{A}_w,\mathbf{0},\mathbf{d}_w) : W(s) = N_w(s)/D_w(s) \right\}, \tag{3}$$

$$\mathsf{S}_r \overset{\text{def}}{=} \left\{ (\mathbf{A}_r,\mathbf{0},\mathbf{d}_r) : R(s) = N_r(s)/D_r(s) \right\} . \tag{4}$$

Note that discrete-time model (2) represents zero-order hold (ZOH) equivalent model for the plant (1).

THEOREM 1. Let $(\mathbf{E},\mathbf{f},\mathbf{d})$ be the zero-order hold equivalent of the complete controllable and observable plant. Let $r(k)$ be the reference input having z-transform $R(z) = N_r(z)/D_r(z)$. Let the zeros of $D_r(z)$ be $z_i, i = 1,\dots,p$. If these zeros (counting multiplicities) are also eigenvalues of $\mathbf{E}$, then $r(k)$ can be tracked with zero steady-state error by the regulator structure without additional dynamics.

If the conditions of the theorem are not satisfied, an additional dynamics must be included into the tracking system, in order to achieve the system robustness with respect to persistent disturbances and model uncertainties. Namely, if $z_1,\dots,z_m$ are poles of $R(z)$ but not eigenvalues of $\mathbf{E}$, from these zeros an additional dynamics system $z^m/\delta(z)$ should be formed with

$$\delta(z) = z^m + \delta_1 z^{m-1} + \cdots + \delta_m \ . \tag{5}$$

The cascade combination of the additional dynamics and the ZOH equivalent of the plant gives an augmented design plant that satisfies the exact tracking property of the previous theorem. Consequently, the regulator designed for the augmented plant, should achieve tracking of the reference input with zero steady-state error. In the case of stable closed-loop system, this property does not depend on the model uncertainties. This approach is based on the "robust servomechanism paradigm", and the well known "internal model principle" [13].

Let λ_w and λ_r be sets with the eigenvalues of the matrices $\mathbf{A}_w$ and $\mathbf{A}_r$, respectively. Thus,

$$\Lambda_w = \left\{ \left(\lambda_{w_1}, m_{w_1}\right), \left(\lambda_{w_2}, m_{w_2}\right), \dots \right\} \tag{6}$$

and

$$\Lambda_r = \left\{ \left(\lambda_{r_1}, m_{r_1}\right), \left(\lambda_{r_2}, m_{r_2}\right), \dots \right\}, \tag{7}$$

where λ_{w_i} and λ_{r_i} are the eigenvalues of $\mathbf{A}_w$ and $\mathbf{A}_r$ with multiplicities m_{w_i} and m_{r_i}, respectively. Let Λ be the union of the sets λ_w and λ_r. The common eigenvalue appears in λ_w and λ_r is included only once with the higher multiplicity in Λ. For example, in the case of tracking of a sinusoidal input with radial frequency ω_r and rejection of step disturbance, the sets become

$$\Lambda_r = \left\{ (j\omega_r, 1), (-j\omega_r, 1) \right\}, \ \Lambda_w = \left\{ (0,1) \right\}$$

$$\Rightarrow \quad \Lambda = \left\{ (0,1), (j\omega_r, 1), (-j\omega_r, 1) \right\} \ . \tag{8}$$

If one wants to track step input and to reject a sinusoidal disturbance, the set Λ should be define in the same manner.

3. DESIGN OF TRACKING SYSTEM

In the previous section it is indicated that the additional dynamics, implemented as part of the compensator, must include both the poles of the reference trajectory and poles of disturbances that are to be tracked and rejected, respectively. The following design procedure given for single-input, single-output plants is a discrete-time version of one given and proved in literature [13], [14]. Note, that a multivariable version of the tracking algorithm can be developed, too.

The design procedure is based on the state-space models for the plant (1)-(2), disturbances (3), reference input (4), and measurement, that is assumed to be a combination of plant state variables $\mathbf{x}(t)$ and possible disturbances $w(t)$ as follows

$$y_m(t) = \mathbf{c}_m\mathbf{x}(t) + f_m w(t) \ . \tag{9}$$

Fig. 3 shows the digital tracking system under consideration. The system is designed by using state feedback, and observer in the case when some state variables are immeasurable. The feedforward gain g may improve the transient response of the system, but cannot affect the stability of the system because it does not change the closed-

loop pole spectrum. By results of several simulation runs, the appropriate value of g can be selected.

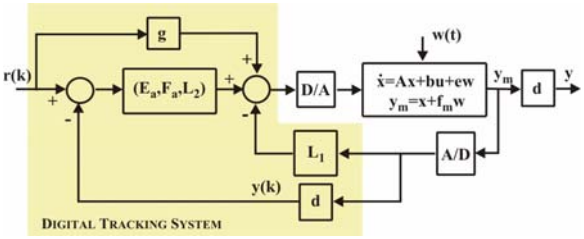


Fig.3: *A digital tracking system with full-state feedback*

Table 1. *Design procedure of a digital tracking system for a plant having ZOH digital equivalent given by realization set* (2).

1° Calculate the necessary additional dynamics which must contain the poles of the reference input signal and the disturbance. The digital model of additional dynamics is defined as

$$\mathsf{S}_{\mathsf{a}} \overset{\text{def}}{=} \left\{ \left(\mathbf{E}_{\mathsf{a}}, \mathbf{f}_{\mathsf{a}}, \mathbf{d}_{\mathsf{a}}, 1 \right) : G_{\mathsf{a}}(z) = z^s / \delta(z) \right\}, \tag{10}$$

where

$$\delta(z) = \prod_i \left(z - \mathrm{e}^{\lambda_i T} \right)^{m_i} \overset{\text{def}}{=} z^s + \delta_1 z^{s-1} + \cdots + \delta_s , \tag{11}$$

and $\lambda_{\mathsf{i}} \in \Lambda$ are eigenvalues with multiplicity m_{i}. The total number of eigenvalues is $s \overset{\text{def}}{=} \sum m_{\mathsf{i}}$ .The state-space model is given in observable canonical form, where

$$\mathbf{E}_{\mathsf{a}} = \begin{bmatrix} -\delta_1 & 1 & 0 & \dots & 0 \\ -\delta_2 & 0 & 1 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -\delta_{s-1} & 0 & 0 & \dots & 1 \\ -\delta_s & 0 & 0 & \dots & 0 \end{bmatrix}, \qquad \mathbf{f}_{\mathsf{a}} = \begin{bmatrix} -\delta_1 \\ -\delta_2 \\ \vdots \\ -\delta_{s-1} \\ -\delta_s \end{bmatrix}$$

$$\mathbf{d}_{\mathsf{a}} = \begin{bmatrix} 1 & 0 & \dots & 0 \end{bmatrix} . \tag{12}$$

2° Calculate the $(n+s)\times 1$ feedback vector $\mathbf{L}$ for the designed model which comprises the additional dynamics $\left(\mathbf{E}_{\mathsf{a}}, \mathbf{f}_{\mathsf{a}}, \mathbf{d}_{\mathsf{a}}, 1 \right)$ in cascade with the ZOH equivalence model of the plant $\left(\mathbf{E}, \mathbf{f}, \mathbf{d} \right)$. In the state-space representation

$$\mathbf{x}_{\mathsf{d}}(k) = \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{x}_{\mathsf{a}}(k) \end{bmatrix}, \tag{13}$$

the matrices of the designed model are

$$\mathbf{E}_{\mathsf{d}} = \begin{bmatrix} \mathbf{E} & \mathbf{0} \\ \mathbf{f}_{\mathsf{a}}\mathbf{d} & \mathbf{E}_{\mathsf{a}} \end{bmatrix}, \ \mathbf{f}_{\mathsf{d}} = \begin{bmatrix} \mathbf{f} \\ \mathbf{0} \end{bmatrix}. \tag{14}$$

Regulator gain vector $\mathbf{L}$ can be partitioned as

$$\mathbf{L} = \left[\underbrace{\mathbf{L}_1}_{n\times 1} \;\vdots\; \underbrace{\mathbf{L}_2}_{s\times 1} \right] . \tag{15}$$

3° Implement the additional dynamics as a part of the serial compensator in a way shown in Fig. 3. Introduce the experimentally adjusted feedforward gain g .

In step **2°** of above procedure, gain vector $\mathbf{L}$ may be calculated in different ways.

By applying Ackerman's formula, one obtains

$$\mathbf{L} = \begin{bmatrix} 0 & \dots & 1 \end{bmatrix}^{\mathrm{T}} \mathbf{W}_{\mathbf{C}}^{-1} \, p(\mathbf{E}) \ , \tag{16}$$

where $\mathbf{W}_{\mathbf{C}}$ is the controllability matrix of the digital plant model given by the triple $\left(\mathbf{E}, \mathbf{f}, \mathbf{d} \right)$, while

$$p(\mathbf{E}) = \mathbf{E}^n + p_1 \mathbf{E}^{n-1} + \ldots + p_n \mathbf{I} \tag{17}$$

represents the matrix characteristic polynomial of the closed-loop system.

Gain vector $\mathbf{L}$ of controller may be calculated using formula

$$\mathbf{L} = \left[\left(p_1 - a_1 \right) \ \left(p_2 - a_2 \right) \ \dots \ \left(p_n - a_n \right) \right]^{\mathrm{T}} \bar{\mathbf{W}}_{\mathbf{C}} \mathbf{W}_{\mathbf{C}}^{-1} \ , \tag{18}$$

where $\det(z\mathbf{I} - \mathbf{E}) = z^n + a_1 z^{n-1} + \ldots + a_n$ is the characteristic polynomial of the digital plant model. Unlike of $\mathbf{W}_{\mathbf{C}}$, $\bar{\mathbf{W}}_{\mathbf{C}}$ is the controllability matrix of digital plant model transformed into the controllable canonical form.

Numerical Example.

In the example, the type-1 servo is considered in which the dc armature-controlled motor having transfer function

$$G_0(s) = \frac{K_T K_m}{s(T_m s + 1)} \ , \tag{19}$$

is used. The motor parameters are: electrical driving torque constant $K_T = 1\ \mathrm{N{\cdot}m/A}$, electromechanical gain factor $K_m = 4$ and mechanical time constant $T_m = 0.2\ s$. The sampling period $T = 0.1\ \mathrm{s}$ is adopted. The control system is desired to track the reference signal in the presence of disturbance. Suppose that one wants, during the time interval $0 \le t < 40$, to track the unit pulse train having period of $40\ \mathrm{s}$, and then the sinusoidal signal $r(t) = 2\sin(0.2\pi t)$. In the same time, the plant is subjected by sinusoidal load torque disturbance

$$T_{\mathrm{L}}(t) = 5\sin(0.2\pi t)\,\mathrm{h}(t-35)\ \mathrm{N{\cdot}m} .$$

The plant input and output are shown in Fig. 4.

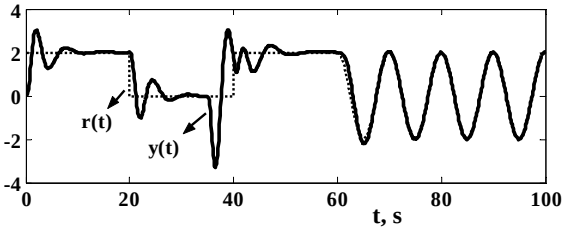
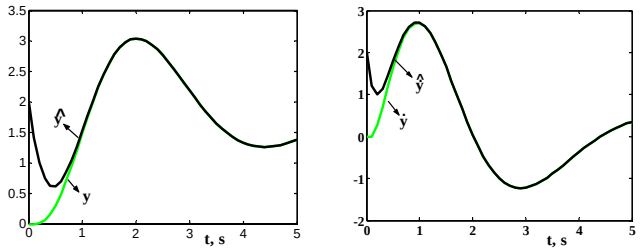


Fig.4: *The plant input and output for the tracking system shown in* Fig. 3.

In order to accomplish the previous digital control, the observer, that estimate some or all of the plant state variables from input/output measurements, must be designed. Traces in Fig. 5 illustrate the ability of identity observer to estimate the

speed and angular position of the drive shaft in the absence of load torque disturbance.



(a) (b)

Fig.5: State variables of the plant (19) and their estimates obtained by identity observer before the presence of load torque

4. PARAMETER SETTING IN DIGITALLY CONTROLLED TRACKING SYSTEM WITH CROSS-COUPLING MOTION

In [2]-[5], it is shown that, in the case of drives with identical characteristics, the pole spectrum of the considered cross-coupled system (Fig. 1) is decoupled. The spectrum consists of two pole pairs that can be placed separately. Consequently, cross-coupling control parameters (K_f, K_s) and parameters of digital position regulator (control vector $\mathbf{L}$ in Fig. 2) can be set independently. The parameters of digital regulator in the structure of Fig. 6 can be tuned using the procedure given in Table 1.

If the reference input and disturbance don't satisfy the supposed models (3) and (4), the tracking may not be perfect. However, the tracking will be achieved despite of both disturbances and model inaccuracies, as long as the closed-loop system with the actual plant remains stable. It is already shown in [2]-[7] and [9] how to choose the values of cross-coupling parameters (K_f and K_s) belonging to the determined stable region of (K_s, K_f) - plane.

In majority of cross-coupling control system, characteristics of coupled drives are not identical but very close to each other. In such a case, the mentioned pole pars in the procedure of control parameter adjusting are weakly coupled.

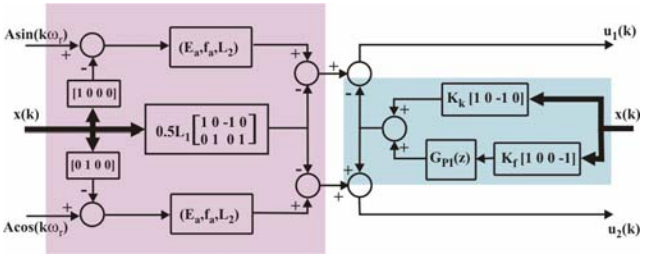


Fig.6: *Digital controller structure in a tracking system with cross-coupling control.*

5. ILLUSTRATIVE EXAMPLE OF A TRACKING SYSTEM

To illustrate the procedure of independent setting of controller parameters within the proposed structure, the example of two coupled servomechanisms having completelly different characteristics is considered (see [3]-[4]). The first and second system control plants are characterized by parameters $T_{m1} = 0.2$ s, $K_{T1} = 1$, $K_{m1} = 4$ and $T_{m2} = 0.4$ s, $K_{T2} = 1.6$, $K_{m2} = 5$, respectively. Note that the characteristics of coupled drives are quite different. The sampling period $T = 0.1$ s was adopted. Reference input signals are defined by the tracking contour described in the form of parametric equations. For example, in the case of an elliptic contour, the applied reference signals are:

$\theta_{\text{refl}}(t) = A_1 \sin(\omega_r t)$ and $\theta_{\text{ref2}}(t) = A_2 \cos(\omega_r t)$, with $A_1 = 1$, $A_2 = 5$ and $\omega_r = 2\pi f_r$, $f_r = 0.1$ Hz.

To achieve a desired speed of response and settling time of $T_s = 5$ s, we choose closed-loop pole locations in accordance with the step response of the prototype system based on the Bessel polynomials [15]. Using the outlined procedure given in Table 1, the design model (13)-(14) is a fourth-order system. Using the roots of a normalized fourth-order Bessel polynomial, scaled by $1/T_s = 0.2$ and mapped into the z-plane, one obtains

$$z_{1,2} = 0.9172 \pm \text{j}0.1017 \text{ and } z_{3,4} = 0.8948 \pm \text{j}0.0296.$$

The feedback vector that places the poles of the closed-loop designed model at these locations is calculated as

$$\mathbf{L} = \underbrace{[0.359004 \quad -0.0330308}_{\mathbf{L}_1} \mid \underbrace{0.025072 \quad 0.0250629]}_{\mathbf{L}_2} \qquad (20)$$

Recall, the control vector $\mathbf{L}$ in (20) is determined on the based of first plant characteristics. Note that the decoupled system (that is for $K_f = K_s = 0$) is unstable. With $K_s = 0.4$ and $K_f = 0.04$, the drives are fairly coupled.

Figs. 7 illustrate the system ability of successful tracking the elliptic contour.

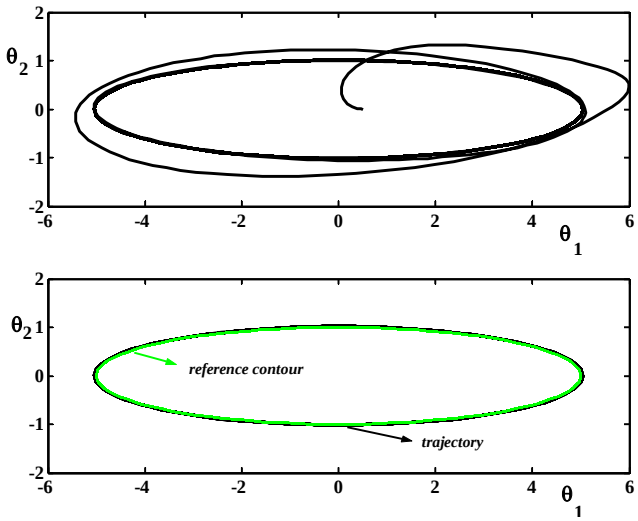


Fig.7: *Tracking as result of cross-coupling control in time* $0 \le t \le 300$ *s ; Reference contour and trajectory in time* $200\ s \le t \le 300\ s$.

In order to verify the effectiveness of the proposed cross-coupling control structure, the system is subjected by constant load torque disturbance $T_{L2}(t) = 10\,\text{h}(t-50)$ N·m. Responses in Fig. 8 visualize the tracking ability of the cross-

coupled system in the presence of a constant load torque disturbance.

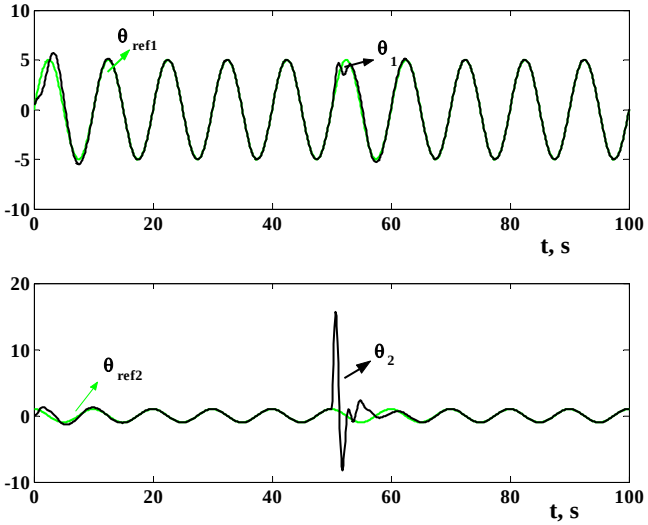


Fig.8: *Responses of the cross-coupled system in the presence of load torque disturbance* $T_{L2}(t)$.

6. CONCLUSION

The results of outlined structural synthesis, analytical design, and simulation have demonstrated the efficiency of proposed structure in tracking a nonlinear trajectory by two positioning servodrives with cross-coupling control. Since the certain portions of controlling mechanisms are decoupled or weakly coupled, the control parameters may be tuned by using a relatively simple procedure that can be applied in both the similar and quite different servodrives.

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HIGH PRECISION SYNC PULSES SEPARATION FROM A VIDEO SIGNAL

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Abstract: *This paper presents a method for a high precision separation of sync pulses from a video signal. The method almost completely eliminates the influence of both power supply low frequency interference and distortions of video signal caused by imperfections of TV tuner and IF amplifier on precision of the sync pulses separation from a video signal. Frequency standard - line frequency, which is used for the synchronization of a local quartz oscillator, is separated from composite sync pulses. Experimental results have shown that jitter (i.e. standard deviation) of the line frequency obtained by this method is of the order of a tenth of a ns up to 1 ns, as well as that precision and reliability are significantly better compared to the LM1881N syncseparator in chip.*

Keywords: *Video signal, Sync pulses separation, Line frequency, Interference, Jitter.*

1. INTRODUCTION

The TV system is very convenient for the dissemination of standard time and frequency signals because of its wide bandwidth and stable propagation characteristics, and also because of the fact that a relatively small capital investment in the existing TV network is required. The standard signals were inserted in the 19-th and 332-rd line of the video signal's vertical retrace interval in the specific Synchronized Active TV System, realized in the TV Beograd [1]. However, if dissemination of the time signal is not necessary, then the TV system, proposed in [2], by which the frequency standard only can be disseminated to the interested users, may be realized simpler and cheaper. The main feature lies in the fact that the synchronizing pulses generator in the TV studio is externally synchronized by an atomic frequency standard. Therefore, all characteristic frequencies of the PAL TV format preserve excellent long-term frequency stability of the atomic frequency standard (it may be either cesium or rubidium frequency standard, but the most cost-effective is the GPS reference receiver HP58503A). Any suitable signal, which is an integral part of the TV format, may be used at the receiving side as the frequency standard for the synchronization of the local quartz oscillator in order to calibrate the oscillator under test. Either the TV line frequency (15625Hz) or color subcarrier (4.43361875MHz) may be used for that purpose. However, the TV line frequency as a received frequency standard has significant advantages over the color subcarrier: simpler extraction from the video signal; PLL for synchronization of the local oscillator is also simpler.

The main problems are reliable and precise separation of the sync pulses (full name is Composite Synchronizing Pulses, CSP in further text) from the video signal, and then the separation of the TV line frequency from the CSP. The interferences which may appear, and which may completely disable the separation of the CSP from the video signal, will be firstly described in this paper, and then the method for the separation of the CSP, which eliminates almost completely the influence of the interferences on the CSP separation precision from the video signal, will be presented [3,4].

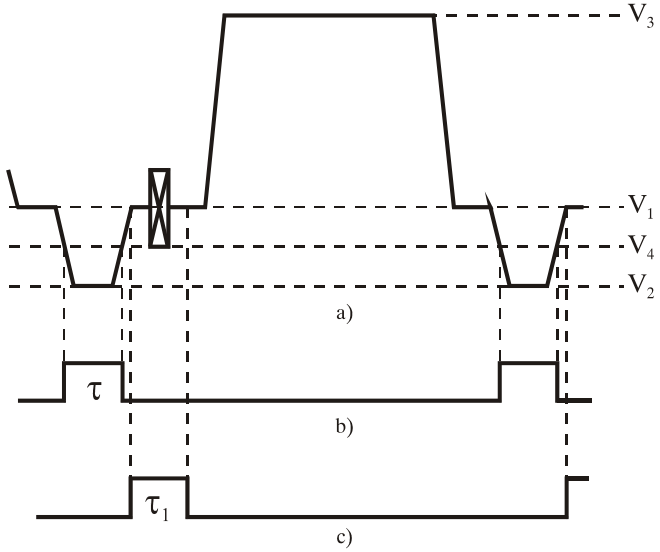

Fig. 1. a) *Characteristic voltage levels in one line of videosignal, b) Inverted CSP,c) Control signal for the clamping circuit*

2. DISTORTIONS AND INTERFERENCES OF THE RECEIVED VIDEO SIGNAL

In order to clarify the method by which the CSP are extracted, the characteristic voltage levels in one line of the video signal are shown in Fig.1.a). V_1 is the blanking level (the "black" level), V_2 is the sync pulses level, whereas the V_3 is the "white" level. It may be concluded from the Fig.1.a) that the CSP can be simply extracted by the voltage comparator. The video signal is applied to one input of the voltage comparator, whereas the reference voltage for the comparation V_4 is applied to the other input. V4 should be set to half of the sync pulses amplitude, i.e. $V_4=(V_1+V_2)/2$, which produces the inverted CSP (duration of which is τ = 4.7μs), shown in Fig.1.b).

However, such a simple method of the separation cannot be used because the characteristic voltage levels of the video signal, obtained from the TV tuners and IF amplifiers, are not constant but varying which causes the undesired operation of the voltage comparator. Using oscilloscope, the following interferences are detected in the video signal:

1). Due to a difference of potentials between the pole which carries the TV antenna (the real "earth" potential) and the protective lead – the "grounding" of the power supply electric installation (in three-phase electric installations, the protective lead is usually connected to the "neutral" lead, the potential of which depends on the load asymmetry between the phases), the interference signal from the power supply (50Hz) is formed, which may amount up to 2Vpp, and is directly superimposed to the video signal. This is the dominant interference, and it may even be greater than the total video signal amplitude.

2). The circuit for separation of the CSP is always used with some additional equipment (for example the digital counter, oscilloscope, vector-voltmeter, etc.) which are all "grounded". Since it is almost impossible to ground all instruments in "one point", and knowing that coaxial cables

which interconnect these instruments make "loops", and additional interference due to power supply (50Hz) is also generated. This interference is not large and usually amounts up to several tens of mVpp.

3). The delayed automatic gain control, with the time constant of the order of ms, is applied in the TV tuner – IF amplifier combination. Because of that, there is a small variation of the video signal amplitude (and of the sync pulses amplitude, as well) which is of the order of up to several percents of the total video signal amplitude.

4). At IF amplifiers, the supression of the audio carrier from the video signal is usually perfomed by a parallel LC resonant circuit tuned for 5.5MHz, to which the signal is fed through a serial resistor. The parallel resonant circuit itself is also loaded by a resistor. Because of the capacitor influence, variations of the characteristic video signal D.C. levels within a TV field are introduced, depending on the TV lines' content within a TV field. In addition to that, the slow changes of the video signal's D.C. levels also appear, which depend on the slow picture brightness changes. These variations usually amount up to several percents of the total video signal amplitude.

The type 1) interferences, which are dominant, can be eliminated by coupling both the antenna coaxial cable shield and the internal lead through a capacitor, whereas the type 2) – 4) interferences can not be eliminated from the video signal in this way. For instance, amplitude of the video signal obtained from the TV tuner and IF amplifier may range from 1Vpp to 2.7Vpp, depending of the manufacturer. The sum of the interferences of types 2) – 4) may cause variations of the V_1 and V_2 levels of up to couple of hundred mVpp, which is much less than for type 1) but still does not allow the correct separation of the CSP by the voltage comparator.

3. METHOD FOR PRECISE SEPARATION OF THE CSP FROM THE VIDEO SIGNAL

High precision and reliability of the CSP separation can only be achieved if all types of interferences, which may appear in the video signal, are eliminated or compensated to the greatest possible extent. Block diagram of the method for the precise CSP separation from the video signal is shown in Fig.2 [3,4]. The first step is the D.C. restoration of the received video signal.

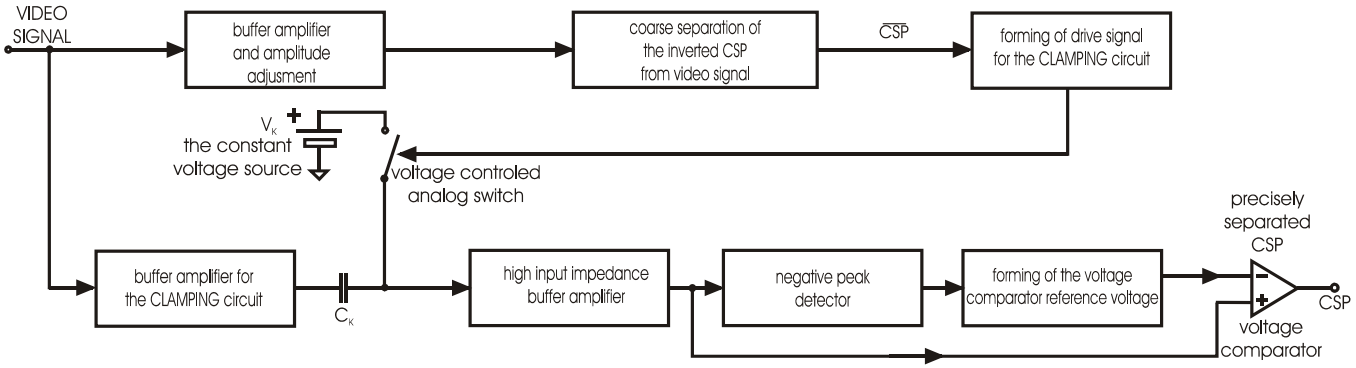

Fig.2: *Block diagram of the method for precise separation of the composite synchronizing pulses from the video signal*

The fast clamping circuit is used for the D.C. restoration in the block diagram of the Fig.2. The video signal is firstly applied to the clamping circuit buffer amplifier, and then to the high input impedance buffer amplifier through a C_K capacitor. The fast clamping, which is in fact performed by setting some convenient part of the video signal to the constant voltage level V_K, is realized by the voltage controled analog switch. From the Fig.1.a) it may be concluded that either the V_2 level or V_1 level can be used for the clamping. However, the clamping must be performed at the black level V_1 in order to avoid possible sync pulses distortions.

The analog switch control must be very reliable in order to obtain the non-distorted video signal with correctly restored characteristic levels. In the upper part of the Fig.2, after the buffer amplifier, the video signal amplitude is adjusted to the value which assures the reliable operation of the inverted CSP coarse separation circuit, Fig.1.b). The negative going edge of the inverted CSP drives the circuit (non-retrigger monostable multivibrator) in which the signal that controls the clamping circuit (i.e. the analog switch) is formed. It is the τ_1 pulse which closes the analog switch, Fig.1.c). The characteristic composite synchronizing pulses' sequence within the vertical retrace interval limits the duration of the τ_1 pulse to the value not greater than 4.3μs.

The analog switch closes with the appearance of the τ_1 pulse, the color subcarrier is short-circuited, and V_K level appears at the high input impedance buffer amplifier output. During τ_1, C_K is charged rapidly through a small switch resistance. The switch opens after the τ_1 pulse is finished, and C_K can be discharged by a very small (negligable) extent until another τ_1 pulse appears. The video signal is transferred to the high input impedance buffer amplifier output through C_K. The D.C. restored video signal is obtained at the high input impedance buffer amplifier output, with the black level V_1 clamped at the constant value V_K, whereas other characteristic levels are automatically corrected from their initial values. The type 1), 2), and 4) interferences are eliminated in this way. However, the sync pulses level V_2 is usually not constant but varies within the TV field due to the type 3) interference, and in some cases also due to the parasitic video signal amplitude modulation by the large type 1) interference. These residual variations are usually not greater than several percents of the video signal amplitude.

The D.C. restored video signal is then applied to the negative peak detector in order to compensate the V_2 level variations' influence on the CSP separation precision, as well. The negative peak detector output is in fact the envelope of the varying sync pulses level V_2 within the TV field. Based on the negative peak detector output signal and the known constant value of V_K, the reference voltage for the voltage comparation V_4 is formed and applied to one voltage comparator input. The D.C. restored video signal is applied to the other voltage comparator input. The V_4 level is adjusted to be at the half of the sync pulses amplitude, Fig.1.a).

However, its value is not constant within the TV field because it follows the D.C. restored video signal V_2 level variations (i.e. it follows the sync pulses amplitude variations). Finally, the preciselly separated CSP are obtained at the voltage comparator output. The influences of all low frequency interferences and the video signal's amplitude variations on the CSP separation precision are eliminated to the greatest possible extent by the described method.

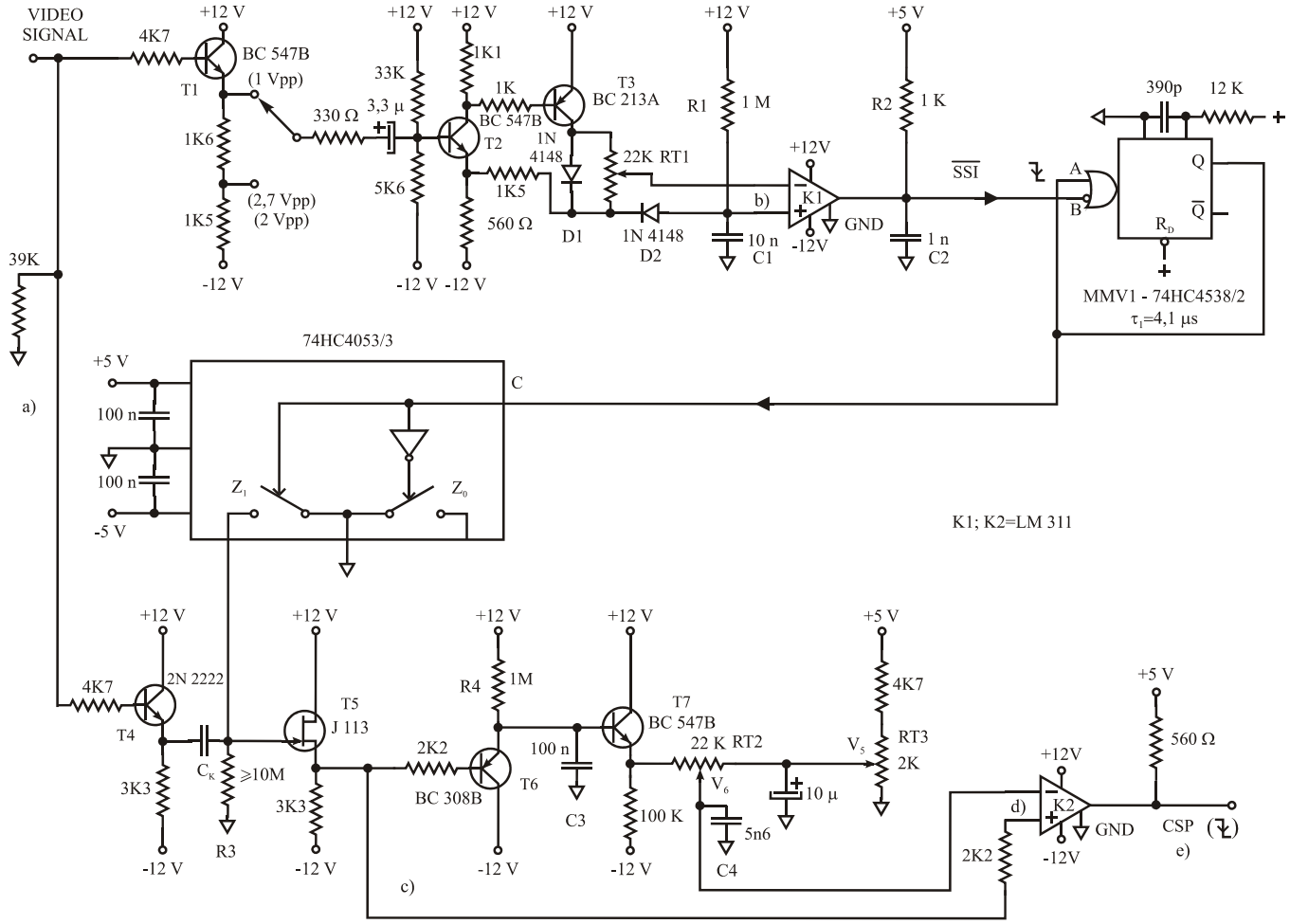

Fig.3: *Detailed schematic diagram of the circuit for the precise CSP separation from the video signa*

The circuit for precise CSP separation from the video signal, based on the block diagram of the Fig.2, is realized and its detailed schematic diagram is shown in Fig.3. The electric ground potential is chosen for the clamping level V_K because it is the simplest and most reliable solution. The most important waveforms which illustrate the operation of the Fig.3 circuit, recorded by the HP 54200A digital oscilloscope, are shown in Fig.4.

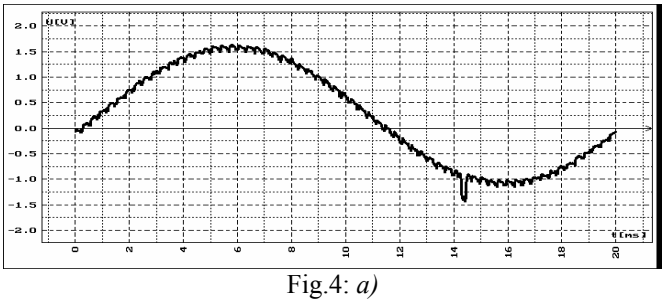

Fig.4: *a)*

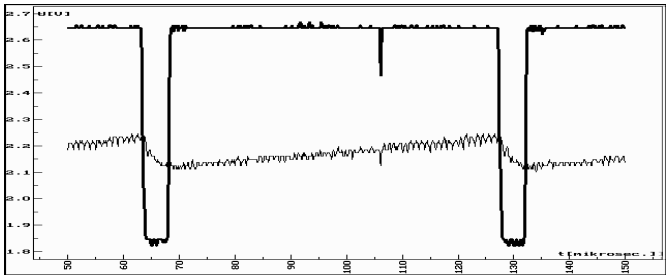

Fig.4: *b)*

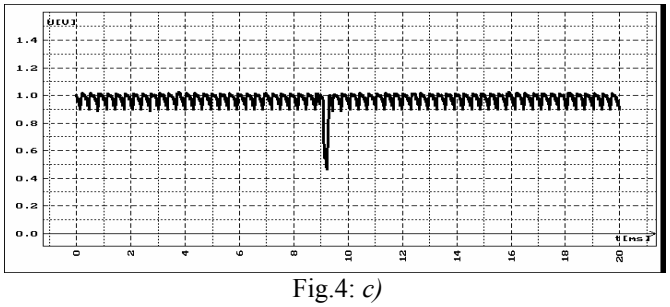

Fig.4: *c)*

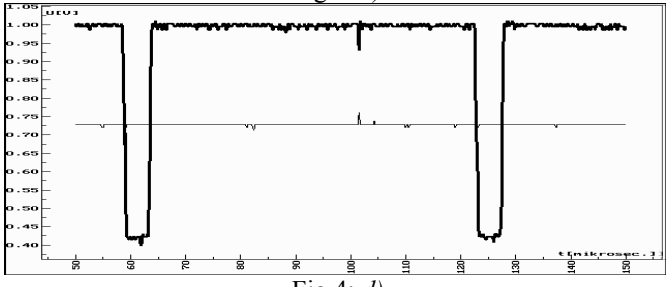

Fig.4: *d)*

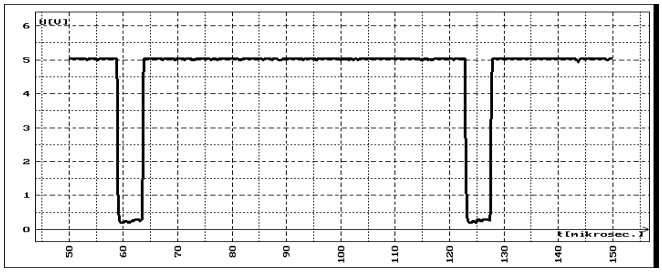

Fig.4: *e)*

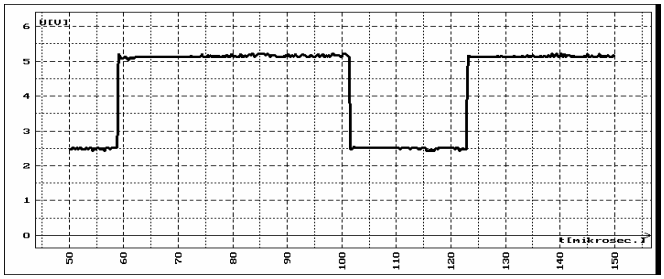

Fig.4: *f)*

Fig.4: *The most important waveforms which illustrate the Fig.3 circuit operation*

The black picture video signal (V_1-V_2=0.6V_{PP}; V_3-V_1=0) is summed with the 2.8V_{PP} sine wave interference (50Hz), and then applied to the Fig.3 circuit input. The sum of the video signal and the sine wave interference is shown in Fig.4.a) for the duration of 20ms, i.e. for the duration of one TV field. The low resolution of the HP 54200A does not allow individual sync pulses to be seen, but the vertical retrace interval can be clearly observed. The input signals for the voltage comparator K1, used for the inverted CSP coarse separation, are shown in Fig.4.b) for the duration of 100μs (approximately 1.5 TV line). Using oscilloscope, the 22KΩ trimmer resistor (RT1), placed in the collector circuit of the T3 transistor, should be adjusted so that the voltage comparator K1 input signals are positioned relative to each other as in the Fig.4.b). The D.C. restored video signal, obtained at the source of the T5 N-FET, is shown in the Fig.4.c). The input signals for the voltage comparator K2, which is used for the precise CSP separation, are shown in Fig.4.d). For the Fig.3 circuit optimal operation, it is necessary to adjust the 2KΩ trimmer resistor so that the V_5 voltage equals the V_1 level of the D.C. restored video signal. The D.C. voltage shift for N-FET source-follower, when the source voltage is greater than the input (i.e. gate) voltage by approximately the pinch-off voltage ($U_{GS(OFF)}$), is compensated in this way. After that, the V_6 voltage is adjusted to the half of the D.C. restored video signal sync pulses' amplitude (i.e. to the V_4 level of the Fig.1.a) by the 22KΩ trimmer resistor. The precisely separated CSP, obtained at the K2 output, are show in Fig.4.e).

4. EXPERIMENTAL RESULTS

The method for testing of the Fig.3 circuit is shown in the Fig.5. The composite video signal obtained from the TEK 1411 sync pulses generator is used for the measurements in order to avoid the influence of both the phase fluctuations

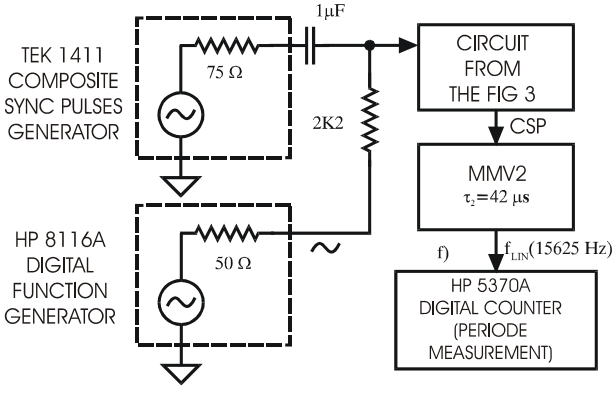

Fig.5: *The method for testing of the Fig.3 circuit*

originating along the microwave links and the TV tuner local oscillator instabilities, which are always present at the real TV signal reception. The 50Hz sine wave interference obtained from the HP 8116A digital function generator is superimposed to the video signal obtained from the TEK 1411. The negative going edge of the separated CSP is reference, and it carries the information about the TV line frequency f_{LIN}. The simplest and most reliable way to separate f_{LIN} from the CSP is to utilize the NON-RETRIGGER monostable multivibrator MMV2 which is triggered by the negative going edge of the separated CSP. The monostable's quasistable state should last about 40-50μs [2,3,4]. Because of that, both the equalizing pulses and the vertical pulses located in the middle of a TV line are prevented from causing the undesired MMV2 triggering. The TV line frequency is obtained at the MMV2 output. Either positive going edge of the Q output or negative going edge of the inverted Q output must be used for the measurements since they are obtained after passing through a couple of the internal logic gates, so that the quasistable state duration variations, due to both the passive components (R, C) values or the internal logic gates' trigger threshold variations, do not affect them. The MMV2 time constant is approximately 42μs, and the line frequency signal is obtained at its output, Fig.4.f). The line period of 64μs is measured by the HP 5370A digital counter which is capable of performing the statistical computation of the measurement results. In this way, the line period jitter (i.e. the standard deviation) is obtained for 10^4 individual measuremnt results.

The jitter (i.e. 1σ standard deviation) of the TEK 1411 H-DRIVE output, the period of which is 64μs, is measured first. The H-DRIVE output jitter is σ_0=0.55ns, which is in fact the TEK 1411 composite video signal generation precision, and therefore the lowest possible line period jitter [4]. After that, the line period jitter of the precisely separated CSP is measured for video signal obtained from the TEK 1411, Fig.5, but with the sine wave interference generator disconnected. The jitter is measured for TEK 1411 operating in both the "A.C. BOUNCE" mode and the "BLACK BURST" mode. The generated composite video signal picture brightness changes abruptly from zero brightness (black picture) to maximum brightness (white picture) in the "A.C. BOUNCE" mode, with the brightness change frequency of about 1Hz. Since the TEK 1411 is capacitor-coupled, and with the total video signal amplitude of 2V_{PP}, the abrupt changes of approximately 1V for all video signal levels are introduced at the precise CSP separation circuit input. The picture brightness is constant and equal to zero in the "BLACK BURST" mode. It was determined for many groups of measurement results that the line period jitter

is practically the same for both "A.C. BOUNCE" and "BLACK BURST" mode, and that the increase of jitter is mostly in the range of 0-0.13ns compared to the initiale value of σ_0=0.55ns. Finally, the precise CSP separation circuit is tested for the 50Hz sine wave interference influence, Fig.5. The sine wave interference amplitude is varyed in the range from $0.5V_{PP}$ to $5V_{PP}$. The measurement results which represent the jitter increase due to the sine wave interference for the "A.C. BOUNCE" mode of the TEK 1411 (the most difficult operation conditions for the CSP separator) are given in the Table 1, whereas the Table 2 represents the jitter increase due to the sine wave interference for the "BLACK BURST" mode.

Table 1. *Influence of the 50Hz sine wave interference amplitude on the line period jitter increase for the "A.C. BOUNCE" mode of TEK 1411*

Amplitude (Vpp)	0,5	1	2	3	5
σ(ns)	0,80 to 0,96	0,86 to 1,12	0,92 to 1,16	0,95 to 1,28	1,08 to 1,46

Table 2. *Influence of the 50Hz sine wave interference amplitude on the line period jitter increase for the "BLACK BURST" mode of TEK 1411*

Amplitude (Vpp)	0,5	1	2	3	5
σ(ns)	0 to 0,23	0,13 to 0,33	0, 23 to 0,41	0,33 to 0,73	0,61 to 1,04

The measurement results given so far are obtained using "ideal" video signal, generated by TEK 1411, and they represent the metrological capabilities of the precise CSP separation circuit itself. The real video signal obtained from a TV receiver is always of lower quality, with the phase fluctuations, which cause the additional line periode jitter increase [4]. For the RTS TV signal in VHF band, the line period jitter ranged from 10-15ns (usually 12ns), whereas the line period jitter ranged 3-8ns (usually 5-6ns) for the RTS TV signal in UHF band.

5. LM1881N – UNIVERSAL SYNC SEPARATOR IN CHIP

The specific integrated circuits which perform the CSP separation from the video signal, with a few external passive components, are commercially available for a long time. We made experiments with the LM1881N sync separator in chip, manufactured by National Semiconductor. LM1881N is convenient to be powered by +5V because outputs will then have TTL levels, with the maximum input signal amplitude limited at $3V_{PP}$. The manufacturer's recommendations in choosing the external passive components' values were observed. LM1881N has several outputs, the most important is the separated CSP output. Testing of the LM1881N is done in exactly the same way as for the precise CSP separation circuit of Fig.3, i.e. according to the block diagram of Fig.5.

The best results were obtained with the "A.C. BOUNCE" mode disabled, and with the sine wave interference generator disconnected. The line period jitter ranged from 1.4-2ns, usually 1.5-1.6ns. The 50Hz interference generator is then reconected, the CSP output of the LM1881N (pin 1) is being monitored on an oscilloscope, with the digital counter still measuring the jitter. It was determined that LM1881N operated worse for the $2V_{PP}$ video signal amplitude than for the $1V_{PP}$ video signal amplitude. By monitoring signal on the oscilloscope, it was noticed that errors in the LM1881N operation were frequent, and that significant parts of the CSP sequence within the TV field (the TV field frequency is also 50Hz) were lost. For the $1V_{PP}$ video signal amplitude, LM1881N operates well for the 50Hz sine wave interference amplitude not greater than 0.3-$0.35V_{PP}$. The jitter is then approximately 5.6ns. Finally, LM1881N is tested for the worst case, with TEK 1411 in the "A.C. BOUNCE" mode, and with $0.25V_{PP}$ 50Hz sine wave interference superimposed to the $1V_{PP}$ video signal amlitude. The jitter ranged from 5.6-6ns. However, errors in the LM1881N operation were frequent.

6. CONCLUSION

This paper presents the method for precise CSP separation from the video signal. The influences of both the low frequency interference and the abrupt picture brightness changes on the CSP separation precision are eliminated to the greatest possible extent by this method. The experimental results indicate that the line period jitter is of the order of 1ns even for the interferences with the amplitude several times greater than the total video signal amplitude. On the other hand, sinc separators in chip are very sensitive to both the abrupt picture brightness changes and the superimposed low frequency sine wave interference. Because of that, they cannot be applied if high reliability, metrological accuracy and precision are required.

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CARDIO CLINIC INFORMATION SYSTEM REALIZATION

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Abstract: *Medical information systems (MIS) bring relevant improvements in every aspect of medical healthcare. The main reasons for MIS development are advantages in quality of health services, clinical costs reduction and making medical data representation more suitable for scientific and educational use. At the same time, data access must be protected enough to avoid misusage. This paper presents the results of the research and implementing internal clinic MIS in Cardio clinic of the Clinical Center of Niš. A global strategy for implementing MISs as modular and Web-oriented systems is presented too.*

Keywords: *Medical information system (MIS), Cardio clinic, Electronic Patient Record (EPR).*

1. INFORMATICS' INFRASTRUCTURE - BASIC FOR THE FUNCTION OF INFORMATION SYSTEM

Medical information systems, in general, are different in some functions, depending on what type of clinic they are created for. However, a great number of functions are the same and they are building the unique base. This paper presents the vision and the description of the medical information system intended to be used at the Clinic for cardiovascular diseases, which, with certain changes, can be adapted simply and very quickly to work in any other specialized clinique, health center or clinic center. For successful functioning and exploitation of applications for one medical information system, first of all it's necessary to complete certain hardware and software systems, which need to carry out necessary informatics infrastructure for its functioning. They are:

- realization of intranet network,
- installation of appropriate operating systems on servers and working stations,
- DBMS installation and data base creation,
- realization of network-security and anti-mallware software subsystems.

The topology of local network depends on location and arrangement of buildings and working places. In this kind of realization the most common topology of a network is 'star', with a number of hierarchy levels. The first level of hierarchy in network represents the connection between the main switch and other switches on the second level. Second level of network refers to connection between LANs of some buildings, more exactly from their main switches to the work stations or the next level of switches or hubs. Because the network is installed in hospital buildings it has to be resistant to interactions with electrical medical instruments. In certain areas SFTP cable needs to be used because of possibility of signal interference and disturbance appearance where other sensitive equipment exists(coronary unit, X-ray department and etc.). It's also very significant to provide internet connection, so the web capability can be used completely.

Because, cardiology clinic information system applications are realized as an independent platform, choice of the operating system should not be a big problem. Intraclinic information system basic applications are developed in Borland Delphi 7 as CLX applications, which means that they both should properly work under Windows and Linux operating systems. The advantage of the CLX application is that the same program code can be compiled under Windows (Delphi) and under Linux (Kylix) environments without significant changes. As a result, heedlessly of the environment, executive files are received with equivalent functions [2].

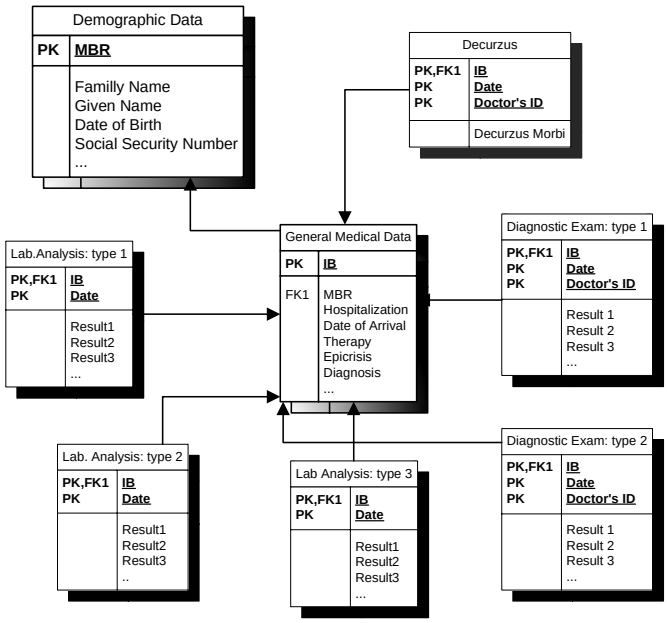

Figure 1.1 *EPR - basic structure*

The database is, still, the heart of the system and demands for its correct functioning are the most critical. Database is created so it can fully support predicted EPR model (Electronic Patient Record) with its basic structure given on Figure 1.1. In the perspective, information system will be facing large quantities of data, so installation of the some robust and reliable DBMS is necessary. The Interbase 6 database system, witch usually comes with standard Delphi distribution is used for testing purposes. The mentioned Interbase DBMS is used for the system testing, but in the near future it would be changed with more progressive object oriented InterSystems Caché, or some more robust relational DBMS like DB2 or Oracle.

Standard username/password login system is suggested method of user authentication. For passwords, as for some sensitive data, it's predicted irreversible md5 and sha1. In the perspective user authentication could be improved using smart cards, bar code readers and different biometric sensors. Also, confidentiality of information on computer systems can be achieved in the appropriate level by building access control mechanisms on the base of operating systems security solutions.

In some cases, the additional level of protection from an unauthorized access can be achieved by using the firewall, too. Usually, firewall is not one machine, but a combination of routers, network segment and host computer. Typically, firewall consists of the traffic filtering router and a proxy server.

Finally, it is necessary to provide continuous and stabile functioning of complete system, including both hardware and software subsystems.

2. IMPLEMENTATION ASPECT

As it was mentioned in the previous part, internal clinic information system is programmed in Delphi7/Kylix3 environment as cross platform CLX application, while the complete modeling and design is done by using Model Maker, UML case tool especially developed for Delphi. In the application realization different design patterns such as singleton, facade, abstract factory and double-checked locking are used.

The System foundation is electronic patient record (EPR, figure 1.1) which is realized according to all standards issued by the European Union regarding privacy of personal data and rights for their distribution. The problem of unique patient identification is resolved according to the recommendation of eEurope 2002 [4] using the combination of patient unique ID number and unique clinic identification. This identification method is significant because it permits undisturbed patient reception in cases when patient personal id number is unknown (loss of the personal documents in some emergency cases).

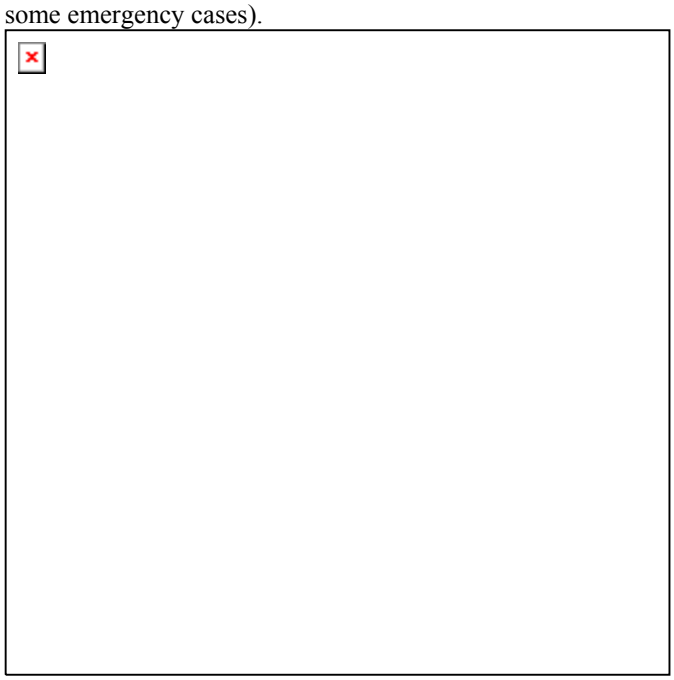

Figure 2.1 *Basic class structures TMISForm*

The object-oriented design is used in order to achieve more efficient development, implementation and later usage. First of all, all forms that can be opened inside the system have the same appearance and the same behavior. Class TMISForm, which is derived from TForm (figure 2.1), allows creating objects with adjustable visual elements. The connection to master-data set which is used in the forms that provide standard interface for different analyzes, diagnostics and examinations, is customizable too.

Class TMedicalAnalysisForm (figure 2.2) provides realization of specific forms that support inserting, editing and deleting of medical data. This class is derived from TMISForm, and with the inherited attributes and methods, it also possesses resources needed for manipulation with slave data supplier. Signature identification and language constants supplier which appear on a form as a label are also provided by the instance of TMedicalAnalysisForm class. Examples of these forms will be given in the next part of the paper.

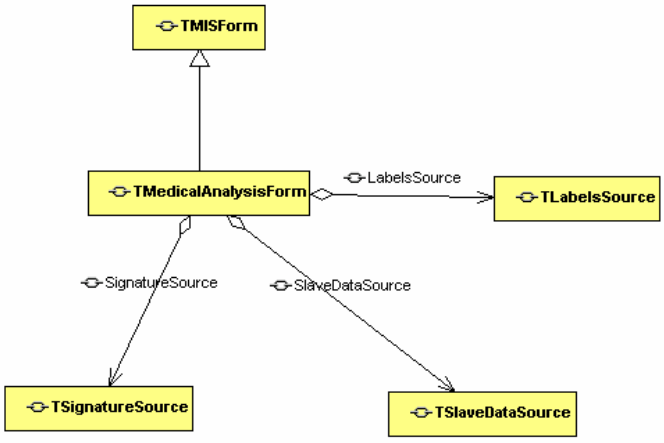

Figure 2.2 *Structure of TMedicalAnalysisForm class*

3. REALIZED FUNCTIONS REVIEW

Basic functions, required by the project, which this MIS had to provide, can be divided into following groups:

- History of disease and medical documentation management,
- financial and supply management support,
- scheduling and keeping up with diagnostic reports,
- forming different kind of reports, according to needs of clinic staff.

Figure 3.1 shows the diagram of basic functionalities which are connected to the process of medical documentation managing, together with their mutual connections and conditions.

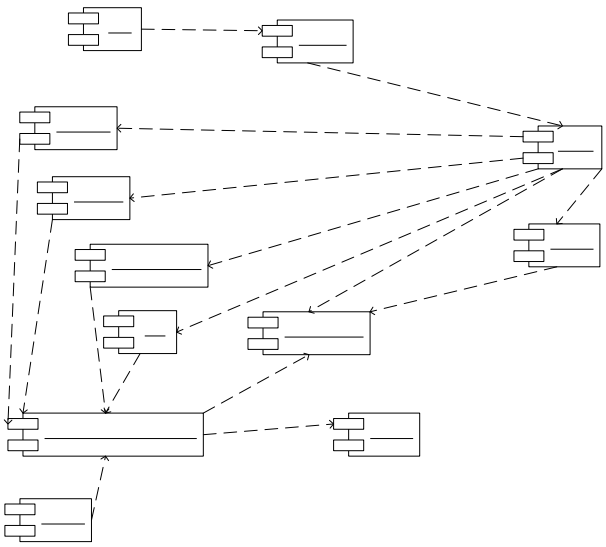

Figure 3.1 *Diagram of basic functional entireties of intraclinic IS*

On figure 3.1 you can also see following groups of the functionalities: Admittance evaluation, disease tracking (which is divided into CTM, Daily condition report, laboratory analysis and diagnostics), patient's condition evaluation and discharge. Admittance evaluation is done in several stages by entering basic data (demographic and social security data), opening history of disease and entering basic

sociomedical data (allergy data, vaccination, previous illness, and also taking the family and socioeconomic anamnesis).

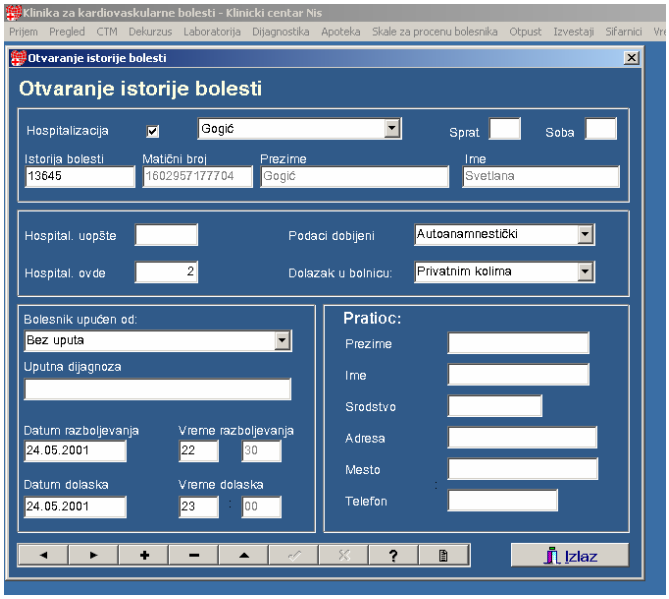

Figure 3.2 *Reception - opening illness history*

On the figure 3.2 you can see illness history opening form. As mentioned above, tracking process is divided into four large groups that contain total sum of 35 different forms who's jobs are to process appropriate daily condition report, examination, lab results and diagnostics.

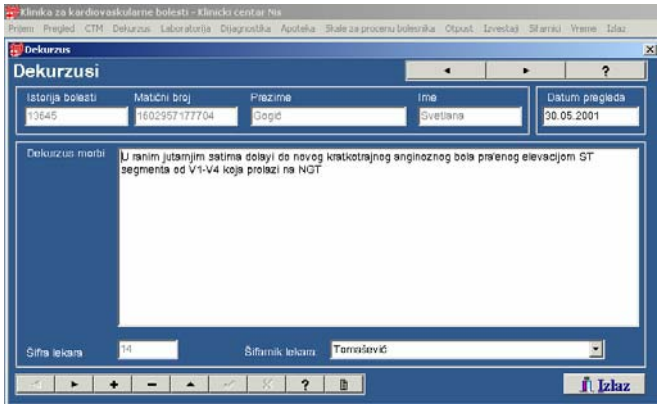

Figure 3.3 *Daily condition report*

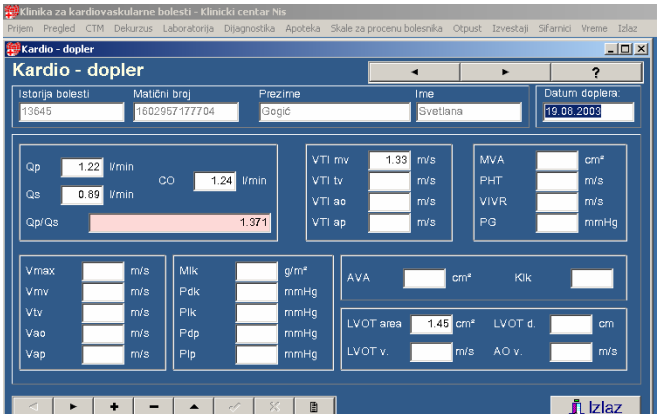

Figure 3.4 *Cardio - Doppler, as an example for diagnostics*

Figures 3.3 and 3.4 present view on Daily condition report and Cardio - Doppler diagnostic, as a view on characteristic master - detail form.

Support for discharge process, as well as generation of different kinds of reports is also realized. Illness history form which sends data into discharge list, according to reception data and daily condition report is given on figure 3.5.

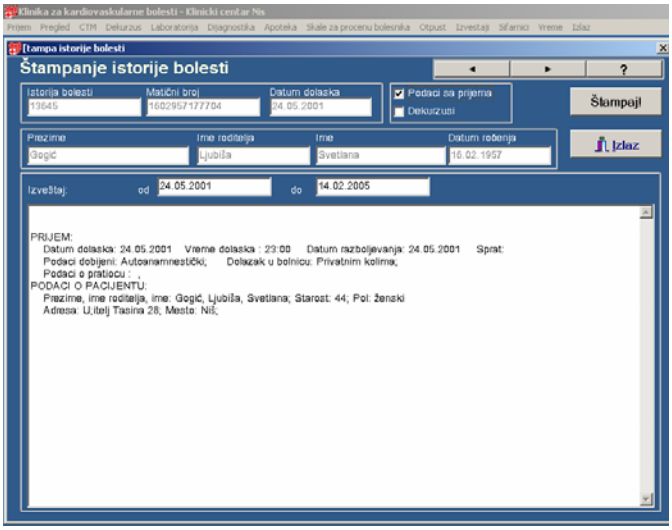

Figure 3.5 *History of disease printing form*

Considering illness history, all of the forms are created based on this model, and all of them have the titles with certain color and font; labels are also uniform as well as page frames and elements placement on the form. That adjustment is inherited from TMISForm class. Those parameters are adjusted on one place and after that they are forwarded on to each of the forms. Thanks to this way of the interface changing, adapting it to any other user is very simple and efficient.

Different standardized nomenclatures, such as 10th international illness classification [5], as well as domestic law norms were considered during the application realization. A medical personnel is able to add and closely determine diagnosis, by its type. Because applications enable tracking of more then one type of diagnosis (differential, current or discharge) this option gives wide opportunity for science and research work.

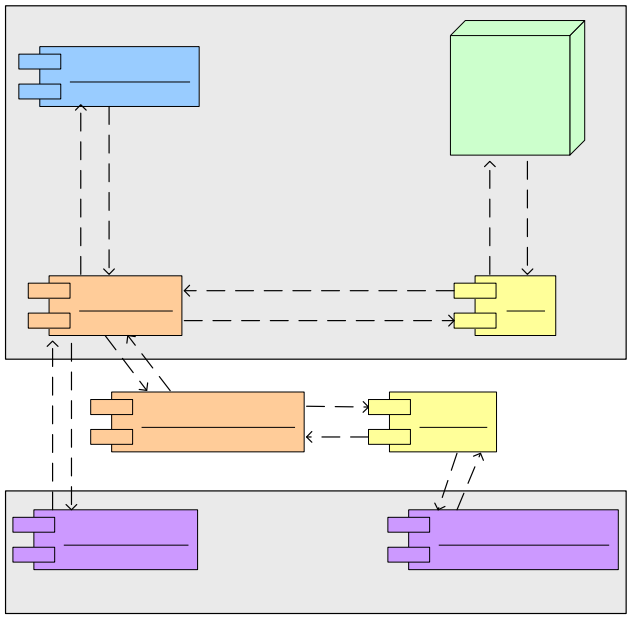

Figure 3.6 *System for scheduling and tracking examinations basic structure*

Scheduling and tracking system is expected to work as a part of already existing medical information system;

therefore it depends on its basic infrastructure (Figure 3.6). Realization of different reports that are created in the process of tracking examinations is achieved by using specialized component Rave 5, which is shipped with Delphi 7 installation. Forms can be generated also in the form that's convenient for further processing by the cases from the Microsoft Office XP® package.

The largest problem which scheduling application needs to solve is instant reservation of the first available term for the specific medical examination. Regarding the type of examination this term availability has different kinds of complexity issues, specifically material resources which are necessary for examination completion. The application provides users with various solutions:

- providing and finding convenient alternative terms for the wanted type of examination,
- scheduling number of examinations in the terms that are most convenient for the patient,
- forming daily, weekly, monthly and annual reports for scheduled examinations,
- automatic rescheduling in a case of sudden cancellation,
- users opportunity to solely define time and duration of all types of examinations.

Very important segment of this application is also conflict resolving which may appear during the examination scheduling. Specifically, the ways to neutralize overlaps in scheduled terms during the process of rescheduling. Dialog for examination scheduling, with available terms is given on Figure 3.7.

ReportER - application is meant to be a tool for reports generation, targeted on MD's science and research work. It serves as an addition to the basic information system and provides staff with filtration and search tools.

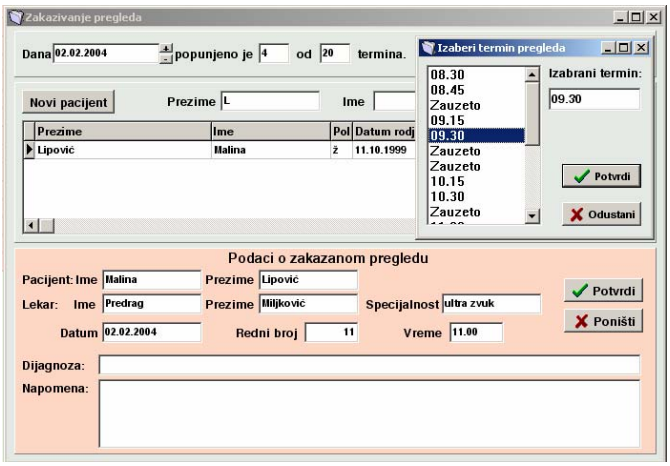

Figure 3.7 *Examination scheduling dialog*

Application main window (Figure 3.8) consists of tree (TTreeView instance class) made of inserted profile paragraphs (on the left), from the field list that provides instant active tree paragraph (TListView, up right) and Query Editor (down right). By adding the field from the list field in ListBox Editor and combining them with logical operators and parentheses you create a query. Formed query is forwarded, to Query Parse, by clicking on "Prosledi". Modules that are engaged on profile manipulation (Profile Manager and Profile Loader) are started by clicking on appropriate paragraphs in a pop-up menu. ReportER enables expanding of created queries by including several additional options:

- Patients geographic arrangement (by regions, community, place of settlement)
- Both, sexual and general structure by each paragraph of the query
- Patients arrangement by age
- Determining the percentage part of selected patients in the total number of patients, as well as the number of patients determined by categories
- Determining the average value, deviation and other standard statistic functions for every query element
- Enables option that allows users with appropriate privileges to print the list of patients.

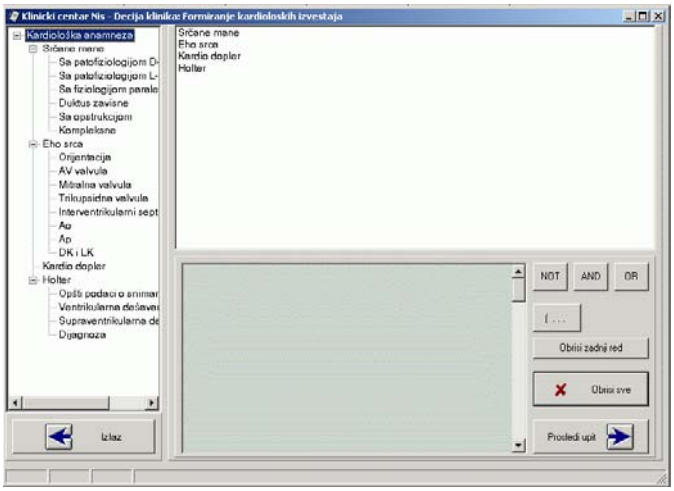

Figure 3.8 *Main window of ReportER application*

4. ADVANTAGES OF PRESENTED SOLUTION

Cardiology clinic information system, as a complete software solution provides support for:

- Basic (medical) activity,
- Attached business processes,
- Promotion of market position for the appointed medical institution, and
- More efficient education, science and research work.

The benefits of using this kind of information system are numerous, like:

- Increased efficiency of medical treatment by reducing the usual time needed,
- Greater level of resource exploitation (capacity, equipment, personnel) based on planning and scheduling,
- Business lead by expense control management and normative for medical services and price obtained by this,
- Greater insight in given medical services,
- More efficient control of stocks (drugs and other health care material),
- Systematic and simple work planning,
- Increased quality of medical and nonmedical work,
- More efficient and complete conduct of health care protection program,
- Instant information about the state of active processes,
- High-quality elements for science- research work.

This MIS was created in a way that it can follow all the phases of patient's medical treatment in a best possible manner: from admittance, examination, illness tracking, taking down all kinds of diagnostic analysis, creating medical documentation and down to a discharge. Except that intraclinic information system for Cardiology clinic is created in a way that it can provide:

- Connection between health care treatment and business system of the medical institution,
- Supports work and data by the time and the place of origin,
- Harmonization with law and other regulations,
- Connectivity with other systems,
- Reliable system work and efficient data protection,
- Simple and easy use of all system elements.

At the present time, created information system is in the phase of finale testing in appropriate medical institutions, with the expected beginning of its use in next couple of months.

5. CONCLUSION

Cardiology clinic, as a part of KC Niš, is marked with highly specialized medical activity. Using the information system, clinic can significlly increase it's business efficiency. The basic aspects of work advancement in Cardiology clinic can be seen in increased quality of offered medical services, better functioning of health care institutions and creation of better conditions for more efficient education and science-research work in the area of medicine which relies on existing data bases worldwide.

The use of information technologies in the department of health care is necessary for creation of more quality support for work and decision making processes. Medical information systems are not used only for collecting and processing the information, they are used as a powerful management systems witch provide the institution with timely and accurate pointers about quality of given medical treatment and resources available.

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COMMUNICATION PERFORMANCES OF POWER-LINE CHANNEL

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Nataša Gospić, University of Belgrade

Abstract: *The Power utility sector in Bosnia and Herzegovina is undergoing through process of structural reform. Following the examples from countries that already finished such reforms, Electricity Companies in Bosnia and Herzegovina explore their own capabilities for providing telecom services on liberalized telecom market. They investigate characteristics of power line as access medium, particularly for delivering broadband services to costumers. The paper describes fundamental characteristics of PLC system and power line channel with review of the main problems that the PLC technology faces. The paper, also, describes the modulation scheme (OFDM) used for PLC transmission.*

Keywords: *PLC, bandwidth, attenuation, noise, radiation, OFDM.*

1. INTRODUCTION

Recent research and development with communication networks area have addressed possibilities of using electricity supply networks as communication medium for applications in access networks (Local Loop Access Medium) e.g., for providing Internet, telephone and data services. Results obtained in researches of power line as communication channel recognized that sufficient bandwidth and signal-to-noise ratio (SNR) for providing such type of services is available. Due to differences between power distribution networks and conventional communication networks, specific solutions and signal transmission techniques are needed. This paper discussed properties of power line channel working on frequencies between 1 and 30 MHz.

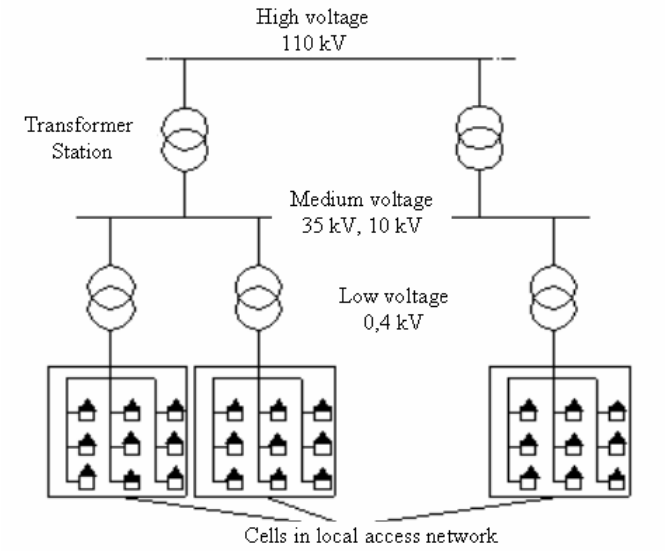

Figure 1: *Topology of the power distribution network in B&H*

In Europe, power distribution network is typically divided on three segments: high voltage, medium voltage and low voltage level (Figure 1). This paper deals with low voltage segment of distributive network as most interesting one for application in access networks and providing traditional telecom services to the end-users, as well as with solutions for use of home electrical installations as communication network inside the premise. Star/tree topology of the network with transformer stations as base stations, reminds on cell structure of cell-type radio networks. Due to the fact that power lines are shared medium, multiple access is used in PLC systems.

2. ELEMENTS OF PLC SYSTEM

Communication channel is physical path between transmitter and receiver. Figure 2 presents digital communication system using power line as medium for communication. Due to topology of low voltage power network there are a number of channels in PLC system, each one with its own characteristics and quality.

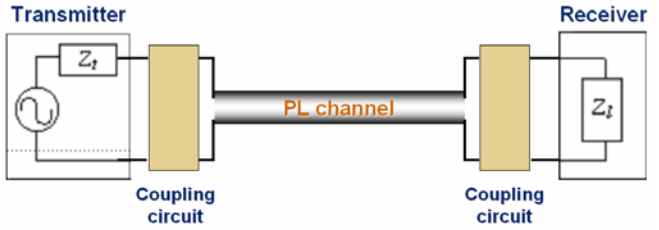

Figure 2: *Block diagram of the digital PLC system*

Output impedance of transmitter (Z_t) and input impedance of receiver (Z_l) are important parameters of communication system. For connection of transmitter and receiver to power line coupling circuits are used. Coupling circuit has two functions: to prevent that 50 Hz waveform enters into communication equipment, and to ensure that the received/transmitted signal is within the frequency band used for communication. In this way, dynamic range of receiver is increased and prevention that transmitter produced noise interfere signal on the communication channel is provided. Transfer function of broadband coupling circuit is presented in Figure 3. [1]

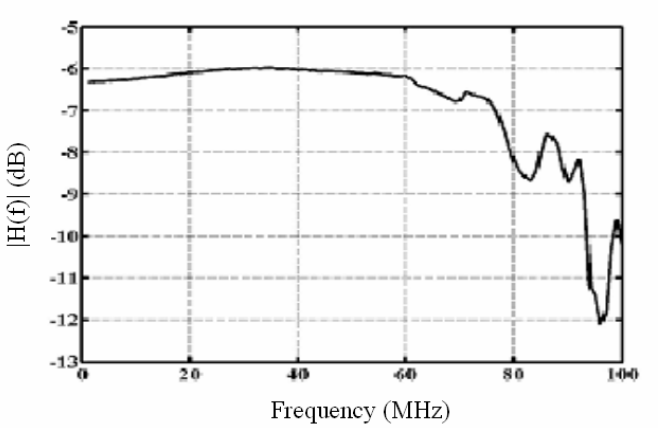

Figure 3:*Transfer function of the broadband coupling circuit [1]*

3. PROPERTIES OF COMMUNICATION CHANNEL

3.1. AVAILABLE BANDWIDTH

Frequency band available for PLC communication is not limited by physical characteristics of power line. However, regulatory authorities limit available frequency spectrum for PLC in order to prevent interference with other users of HF spectrum and their electronic equipment. European standard - CENELEC (EN 50065-1), from 1991, allow frequency spectrum 3kHz - 148,5kHz for PLC communication, see [2]. This spectrum is divided on five sub-bands:

- 3-9 kHz for electricity companies needs
- 9-95 kHz (A band) for electricity companies needs
- 95-125 kHz (B band) for users needs
- 125-140 kHz (C band) for users needs, CSMA protocol
- 140-148,5 kHz (D band) for users needs

CENELEC limits amplitude of signal in A-band to 5V maximum (0,75V - 5V, depend on modulation type). Signal amplitudes in B, C, and D-band are limited to 0,63V. Such regulation puts strong restrictions on services that can be realized using this technology. For high-rate applications wider bandwidth is needed, because bandwidth is proportional to bit rate. New generations of PLC systems (Broadband over Power Lines – BPL systems) utilizes frequencies between 1,6MHz and 30MHz, which means considerably increased bandwidth and enables use of power lines for broadband applications. Big problem is interference with other communication systems that already use stated part of frequency spectrum (radio-diffusion, amateur radio, aircraft navigation, etc.) [3].

3.2. EMISION OF SIGNAL

During HF signal transmission over power line, electromagnetic radiation around the conductor occurs. Intensity of radiation depends on output power of BPL transmitter. Due to that, power line acts as huge antenna with some gain and a complex multi-lobed radiation pattern. Electric field level measured on certain distance from conductor increases with frequency. For example, field level measured for 10MHz signal is several tenths of decibels higher than for 100kHz signal [4]. Because of frequency band used in broadband BPL communication, it is very important that signal emitted from power lines does not interfere with signals from other communication systems. That can be achieved by limiting maximum signal power level on the transmitter side. This problem is exactly what makes regulatory restrictions regarding use of mentioned frequency bandwidth in new generation of BPL systems. For underground power cables signal emission is relatively low, but for overhead power lines and home electric installations it has considerable contribution in interference with other electronic equipment.

3.3. IMPEDANCE MISSMATCHES

This problem seems to be solved (for example, use of 50 Ω cable and 50 Ω transmitter/receiver) for conventional communications. However, power distribution network is unmatched and a change of impedance depends on time, location and various loads connected to the power line, and its value have a range from several mΩ to several KΩ. There are two basic impacts of impedance mismatching on performances of communication system. First, if channel is not closed with its characteristic impedance, signal power on received side is attenuated. Second is related to the reflection which occurs when there are a number of connecting points on the specific path (power line), as well as when there are splices between cables with different characteristics, and each of them could change the impedance. As result of reflection beside original signal it will be a number of replicas, received in different time intervals. This multipath effect causes frequency selective fading and intersymbol interference, which have a considerable influence on performance of communication system.

3.4. ATTENUATION

During propagation between transmitter and receiver signal is exposed to attenuation, which is different on different frequencies. Attenuation is result of changing loads on the network and, in great extent, is varying over time. Further on, attenuation increases with distance between transmitter and receiver and with higher signal frequencies (Figure 4) [5].

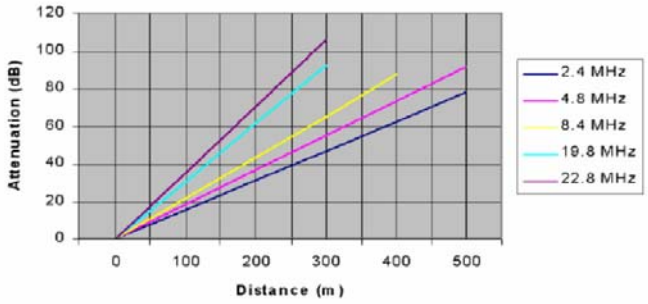

Figure 4: *Attenuation as function of distance between transmitter and receiver [5]*

All those cause wide dynamic range of attenuation (up to 100dB). To improve SNR on the receiver side in order to achieve good quality of detection, automatic regulated amplification and repeaters are needed. They sustain necessary power level and accuracy of the signal. For signal transmission over MV and LV networks, repeaters must be used for distances over 300 meters.

Figure 5 presents measurement results of attenuation level for the In-Home BPL system, which utilize home electric installations as communication channel, see [6]. Measurements are made for random pairs of electric sockets, in a number of objects. Generally, inside frequency band from 1MHz up to 30MHz, attenuation can be tolerable. Still, on different frequencies in period of time, maximum attenuation can be up to 80 dB.

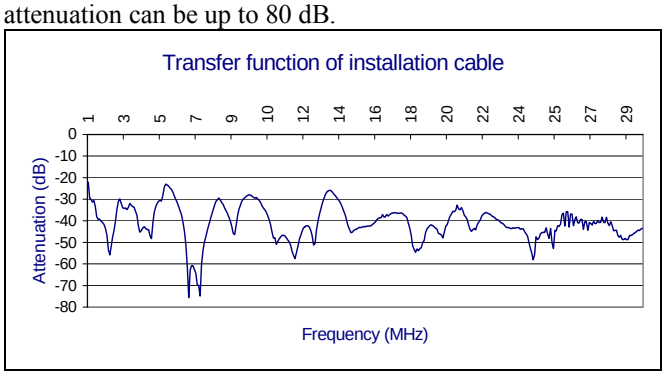

Figure 5 : *Attenuation on power line link between pair of electric outlets inside the premise [6]*

Random nature of these negative peaks on attenuation characteristic makes selection of “perfect” BPL

modulation technique very difficult task. Narrowband modulation with one carrier is based on the assumption that nulls will not overlap the carriers, or on utilization of equalizer to surpass the variations of channel properties over time. As reliable transmission technique in BPL systems, Orthogonal Frequency Division Multiplexing (OFDM) modulation is in use. More about OFDM modulation is presented in section 5.

3.5. NOISE ON COMMUNICATION CHANNEL

Signal-to-noise ratio is a key parameter in performances calculation of any communication system. This parameter refers to quality of communication, and can be defined as ratio of level of received signal and noise level. The greater is SNR the communication is better.

Noise statistic in BPL systems is quite different then Gaussian white noise model and has large variations over short periods of time. Additive noise in power line environment can be characterized as summation of following components: colored background noise; narrowband noise; periodic impulsive noise, synchronous with main frequency (50Hz); periodic impulsive noise, asynchronous with main frequency (50Hz); and asynchronous impulsive noise, see [7].

These noise sources have its own characteristics in time and frequency domains. The easiest way to present SNR for power line is using amplitude-frequency diagram presented in Figure 6. This diagram presents maximum noise level as function of frequency, measured on specific test location [6]. Maximum noise level is defined as noise level that is not threat for communication signal in specific period of time, but not on continuous basis. Average noise level is for 20db to 30dB lower than maximum measured level.

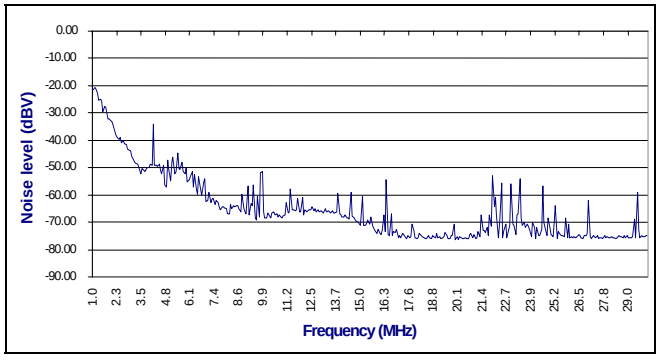

Figure 6: *Maximum noise level measured on one of test locations [6]*

In order to decrease impact of noise on signal transmission, different techniques can be employed, starting with various coding procedures with possibility of error correction up to frequency diversity. It must be remark that there is no universal solution for overcome this problem. For example, spread spectrum techniques provide good results for narrowband noise but, on the other hand, it cannot deal with white background noise.

4. MODEL OF PLC CHANNEL

In sections above, pereformances with negative impact on properties of power line communication channel, are presented:

- Unmatched impedance on the transmitter,
- Channel attenuation,
- Noise,
- Unmatched impedance on the receiver.

Figure 7 presents the Model of PLC Channel considering properties listed above. All of them, except noise, are presented as time dependent linear filters, each of them with specific frequency response. Noise is presented as random additive influence.

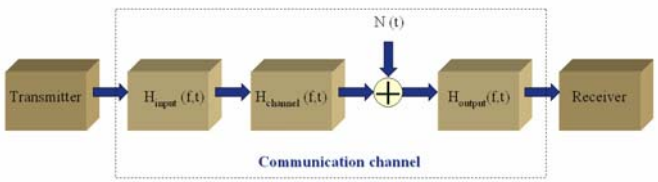

Figure 7: *Model of the PLC channel*

In spite of its simple form, this model contains whole set of variables that must be considered in design of communication system and its performances.

Channel parameters can be defined by measurement. Figure 8 presents results of measurement (left-side diagram) and simulation (right-side diagram) for four paths of power line link with length of 150 meters. Adequate parameters are presented in Table 1. [8]

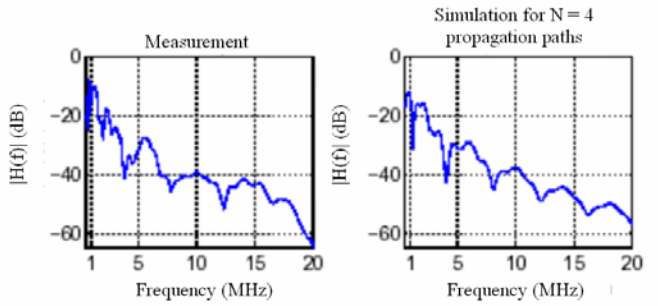

Figure 8: *Results of measurement and simulation for PLC link with length of 150 m [8]*

Table 1. *Model parameters [8]*

Link	1	2	3	4
Delay (μs)	1,0	1,25	1,76	2,64
Length (m)	150	188	264	397
Weighting factor g_i	0,4	-0,4	-0,8	-1,5
k=0,5	a_0=0		a_1=8 10^{-6}	

5. MODULATION TECHNIQUES IN PLC SYSTEMS

According to the fact that power lines are not primarily designed for transmission of broadband telecommunication signals, there are considerable impairments on power line channel. Every switching on and switching of the consumers on the power network or devices in households means changing loads (impedance) of the network. This makes adaptation of communication channel very difficult. As it is mentioned, this processes results with strong interference and frequency selective fading. Also, a multipath effect occurs. For solving these problems and achieving higher bit rates, modulation technique must be carefully chosen. Frequency Shift Keying (FSK), Orthogonal Frequency Division Multiplexing (OFDM), or Code-Division Multiple Access (CDMA) is commonly used.

5.1. OFDM MODULATION

Because of its resistance on multipath effect and excellent spectral efficiency, OFDM finds its application in modern telecommunication systems as well as in high-speed PLC systems (BPL). Most of the communication systems use one carrier for transmission of data signals. Advantage of system with multiple carriers is in method of generating and emitting signals. The basic idea of OFDM is to divide data flow in N parallel flows, each one transmitting by its own sub-carrier. Sub-carriers are mutually orthogonal in such way that there is adequate frequency spacing between them. Maximum of one sub-carrier is harmonized with nulls of all other sub-carriers. In this way spectral overlapping is allowed and considerably better spectral efficiency is achieved (Figure 9) [9].

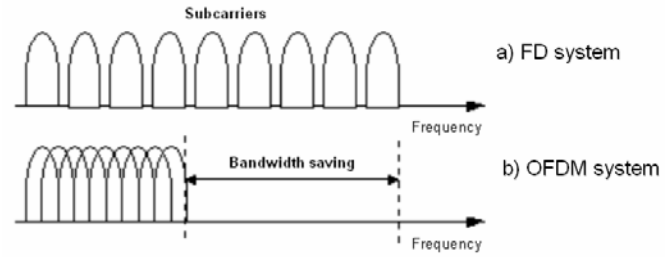

Figure 9: *Comparison: a) FD system and b) OFDM system [9]*

Sub-carriers are modulated using one of the techniques for narrowband modulation such as Binary Phase Shift Keying (BFSK) or Quadrature Amplitude Modulation (QAM). Each of sub-carriers is modulated by separate symbol and then, all of them are frequency multiplexed (OFDM). To achieve hardware simplicity of BPL modem, digital processing and properties of FFT (Fast Fourier Transformation) are used. Data signals are transformed in time domain using IFFT (Inverse FFT) at the transmitter, and after transmission reverse process is applied at the receiver side using FFT. [10] Overall number of sub-carriers is equivalent to a number of IFFT/FFT points. (Figure 10)

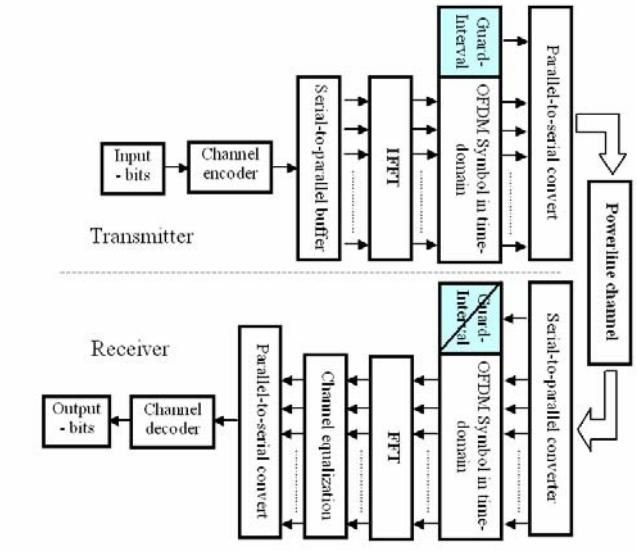

Figure 10: *Model of OFDM system*

Generation of symbols begin by mapping a sequence of information bits into sequence of symbols, using chosen type of modulation in basic band. Symbol time is extended N times, and each of sub-carriers is modulated by specific symbol. Modulation of sub-carriers at the transmitter is performed using IFFT, while demodulation at the receiver is performed using FFT. These algorithms enable realization of OFDM system with great number of sub-carriers but small complexity of the system. After modulation is carried out, the result is OFDM symbol.

Intersymbol interference (ISI) caused by multipath effect is also a problem. Narrowband systems are frequently exposed to multipath effect. For example, 10Mbps BPSK symbol is just 100ns length. With delay of 1μs, which is typical delay for power line, up to 10 symbols can interfere with received signal. On the other hand, signal is correctly received if the symbol, being demodulated in the receiver, has much longer duration then delay paths. OFDM utilizes these principles against multipath propagation.

Equivalent 10Mbps OFDM symbol, with 100 sub-carriers, is 10μs of duration. This, with use of cyclic prefix which is practically copy of the last several microseconds of the signal, can solve the problem of delay, even if it is greater than average. Cyclic prefix is inserted at the beginning of OFDM symbol to absorb interference and makes system resistant on multipath propagation on the channel. At the receiver, reverse process of the transmitter demodulates OFDM signal. First, cyclic prefix is removed from time domain signal, and than demodulation of each of sub-carriers is performed using FFT. After equalization parallel-to-serial conversion is performed and each symbol is demodulated.

Another advantage of OFDM modulation is possibility of tone allocation (turn on and turn off sub-carriers). It results in transmitting of signals just in a part of transfer function spectrum that can sustain required BER (Bit Error Rate) for a specific application. Figure 11 illustrates how tone allocation for power line is performed [6]. During pre-adaptation phase (establishing the link) all sub-carriers are emitted and transmitted, so transmitter and receiver can harmonize ton-allocation pattern for specific link. No data are modulated into sub-carriers for tones that are below SNR threshold. Resulting tone map, that used for signals transmission is presented below in Figure 11 (Adapted Frequency Domain).

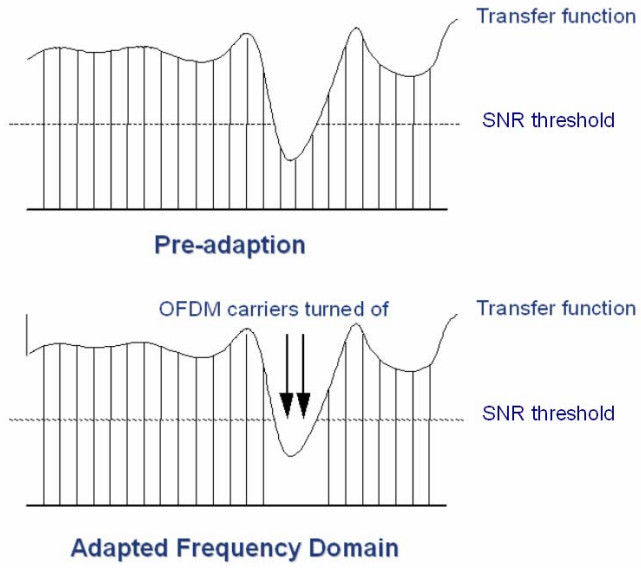

Figure 11: *Tone allocation [6]*

In the above case, tone allocation is performed to harmonize the transmitted spectrum with the amplitude of transfer function. The principle is equally useful for avoiding in-band continuous wave jammers (example is amateur radio signals) in used part of frequency spectrum. The narrowband noise can be with considerable higher amplitude then OFDM signal. Sub-carriers overlapped by such noise are simply turned off to improve BER. Bit rate can be optimized for every communication channel because OFDM has built-in spectral analyzer.

Finally, tone allocation represents an important regulatory advantage. Frequency could be masked to meet current and future international regulations concerning power line communication.

6. CONCLUSION

Since 1950, power lines have been used as communication paths for transmission of telecommunication signals for power companies internal needs (remote meter reading, load and tariff management, etc.) Due to the poor demands regarding bit rates, frequency bandwidth, signal level, etc., use of power lines for low bit rate data communication is already standardized and regulated. For past 15 years, a number of researches are been made regarding use of power lines for broadband communication. Results indicates that, beside the fact that power line is refer as not enough good communication medium due to its attenuation, noise, etc., new technologies overcame weaknesses and transform power line into reliably medium for communication.

After restructuring of Electricity Sector in Bosnia and Herzegovina, power distribution companies will diversified its services and, besides delivering electricity to the consumers, tends to enter the liberalized telecommunication market. According to that, trial fields investigations have to be initiated for use of PLC technology as solution for access communication networks.

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EMSIM 1.1. – PROGRAM FOR SIMULATION OF INDUCTION MOTOR STARTING

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Abstract – *In the paper program EMSIM 1.1, developed on the Power Engineering Departement of the Faculty of Electrical Engineering in Banjaluka, is described. Program is assigned for simulation of starting process of induction motor. Program is used for teaching purposes on the Department for Power Engineering. Accuracy and ease of use are achieved by combining Matlab simulation with an graphical user interface made in Visual Basic.*

1. INTRODUCTION

There are numerous professional programs related to power engineering: programs for system planning, power flow analysis, system optimization, modeling, supervising, machine projecting etc. Beside them, there is a lot of educational programs designed for teaching and training power engineering students and professionals. The purpose of educational software is to help understanding the principles of power system operation and the basics of energy conversion, as well as to illustrate symmetric components or harmonics etc.

Students at the Faculty of Electrical Engineering in Banjaluka are trained to use programs for professional purposes, but while learning, they use educational software as help. There is a lot of illustrative software like in /2, 3, 4/ which can be easily found on internet and download as freeware or shareware software. Those programs can't always be used as granted, because usually there are no details about mathematical models on which programs are based, and usually those programs can't be modified or configured to a specific purpose.

Since 2000 Departement for Power Engineering at the Faculty of Electrical Engineering in Banjaluka started to develop a new software package for purpose of training student. This package is called *EMSIM* and its basic purpose is to illustrate the principles of electrical machines operation and output characteristics. Program package is designed as easy to use, illustrative and based on detailed machine models. At present, part of the program regarded to simulation of induction machine starting process is finished. This program is called *EMSIM 1.1.*

2. *EMSIM 1.1.* – REQUIRED CHARACTERISTICS

Required characteristics for *EMSIM 1.1* program were:

- program had to be based on detailed mathematical model of induction machine written in form of state-space model. Differential equations had to been solved by proper numerical method. Three representative kinds of motor load had to be included: as constant, lineary and parabolic function of speed;
- Program had to have *user-friendly* interface, and developed as any other *Windows* application. With this, *easy-to-use* of program by the students who had no expirience with electricall machines simulation would been achieved;
- All the results had to be represented as plots, and printing and saving of results had to be obtained.

To achieve required characteristics, program is developed in two parts. Induction motor model is made as state-space model as usually formed by the theory of electrical machine modeling. Differential equations are solved by *Matlab's Runge-Kutta* numerical method with changable simulation step. Second part of program, *Windows* application-like interface is written in *Visual Basic*-u 6.0. Connection between these to parts of program is made by using *Active X* controlls in the background /6/.

Using the program is simple and intuitive. All parameters can be inserted, changed, saved, and results can be printed as like in any other Windows program. Detailed machine model which is solved by *Matlab* routines ensures enough accuracy.

Regarded to adopted program concept, any other transient process in induction machine, or any other machine transient analysis (like synchronous or DC) routines can be added as extra modules. By this, program can be easily upgraded.

3. INDUCTION MACHINE MATHEMATICAL MODEL

Three-phase induction motor model is developed as in /7/ by usinge standard methods from electrical machines theory. Model is written in state-space form in stationary reference frame. Accuracy of this model is adequate for almost all purposes /7/.

$$\underline{u}_s = R_s \underline{i}_s + \frac{d\underline{\Psi}_s}{dt}, \tag{1}$$

$$0 = R_r \underline{i}_r + \frac{d\underline{\Psi}_r}{dt} - j\omega\underline{\Psi}_r, \tag{2}$$

$$\underline{\Psi}_s = L_s \underline{i}_s + M \underline{i}_r, \tag{3}$$

$$\underline{\Psi}_r = L_r \underline{i}_r + M \underline{i}_s, \tag{4}$$

$$m_e = \frac{3P}{2}\left(\underline{\Psi}_s \times \underline{i}_s\right), \tag{5}$$

where $\underline{u}_{s,r} = u_{\alpha,r} + ju_{\beta,r}$, $\underline{i}_{s,r} = i_{\alpha,r} + ji_{\beta,r}$, $\underline{\Psi}_{s,r} = \Psi_{\alpha,r} + j\Psi_{\beta,r}$ are voltage, current and flux vectors, ω_m is mechanical speed, $\omega = P\omega_m$ electrical speed, P, number of pole pairs, L_S, L_r i M are stator , rotor and mutual inductances, and m_e is motor torque.

Mechanical subsystem is modeled by Newton equation:

$$J\frac{d\omega}{dt} = m_e - m_{opt}, \tag{6}$$

where J is inertia, and load torque m_{opt} can be given as function with constant, linear and parabolic part:

$$m_{opt} = m_{const} + k_1\omega_m + k_2\omega_m^2. \tag{7}$$

Transformation of terminal quantities from original (phase) domain to transformed domaien is obtained by Clark's transformation matrix /7/.

3. PROGRAM STRUCTURE

Program structure is shown on Fig. 1. Main program module is written in *Visual Basic*, and subprogram for numerical solving of mathematical model (1-7), called asinh1.m, is written in *Matlab*. Motor and load parameters, as well as simulation step size, can be typed directly, or loaded from file in the main module. When the simulation is started, parameters are saved in par.m file, and than *Matlab* is started

via *Active X* controls. *Matlab* than loads the parameters, starts the file asinh1.m. After the simulation is over, the results are saved in file simout.dat. All these processes are run in the background. The results can be shown as plots, using *Matlab's* drawing engine, also controlled by the *Active X* controls. All data transfer, error controll and communication between main module and *Matlab* are done by *Active X* controls. *Active X* controlls are written in *C++* language.

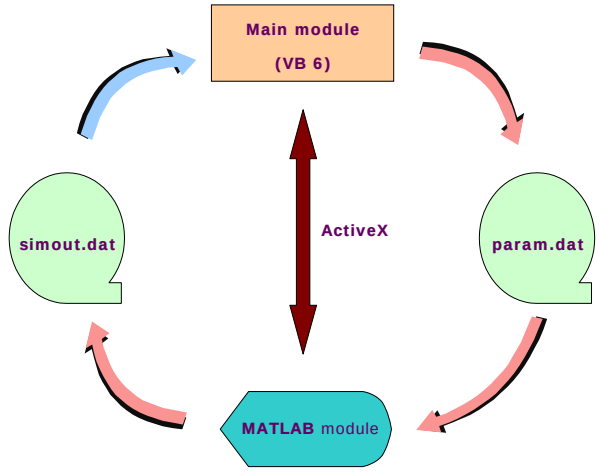

Fig1*: Program Structure*

4. PROGRAM INSTALLATION

Program is delivered on two floppy disks and is installed like standard *Windows* application. Software requirements are *Windows 9x* or *Windows XP* and installed *Matlab 5.2* or newer verison. There are two versions of *EMSIM 1.1* due to different *Active X* controls for *Windows 9x* and *Windows NT* (this information must be submitted before purchasing). Hardware requirements are *Pentium II* on 300 MHz, with 64 MB RAM and 4 MB free on hard disk.

After the installation, *EMSIM* icon will appear on *Desktop* as in the *Start Meny*. Installation process takes usually few minutes.

5. USING THE PROGRAM

EMSIM 1.1. can be started via *Start Meny*, or by double click on the icon on *Desktop*. Main screen is shown on Fig. 2.

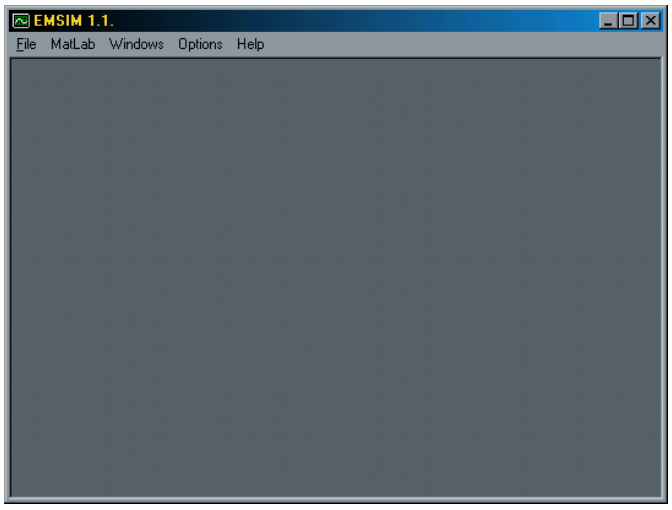

Fig. 2: *EMSIM 1.1. Main Screen*

Description of commands:

FILE – has options: creating a new simulation file (NEW), opening the existing simulation file (OPEN), saving (SAVE), printing the parameters (PRINT) and exit (EXIT);

MATLAB – with options for starting the simulation (START) and drawing the results (GRAPH);

WINDOW – choosing the active window;

OPTIONS – available only on versions for *Windows 9x* and *Matlab 5.1.* Before the first run, it is necessary to define the path to *MATLAB BIN* directory where simout.dat and param.dat files are to be placed.;

HELP – help, written in *Help Scribble*.

By choosing the option FILE/OPEN an existing parameter file can be opened (in *EMSIM* format *.pib), and the parameters can be changed. This window is shown on Fig. 3.

Terminal voltages are inserted as effective voltages per phase, and all the motor parameters are the parameters from equivalent circuit. Load torque (7) can have all three parts, or just one or two of them.

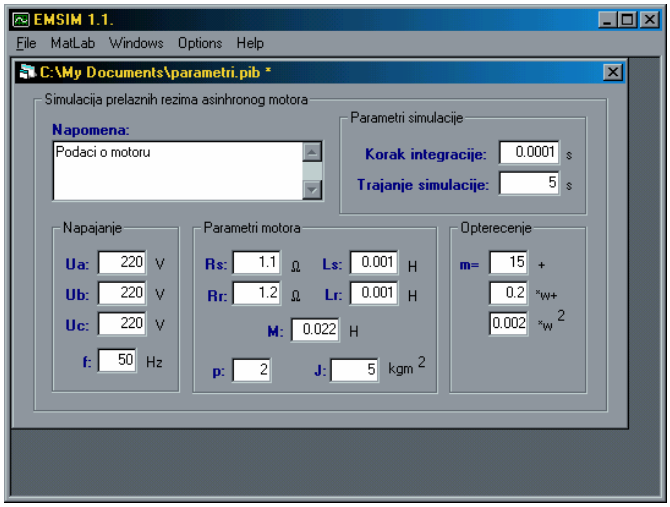

Fig. 3*: Parametar Entry Window*

After the simulation parameters are set, simulation can be started by option MATLAB/START. Simulation time depends of version of *Matlab*, step size and computer processor power. Program starts *Matlab* in the background (what can be seen on *System Tray*), but the user can not interrupt the simulation.

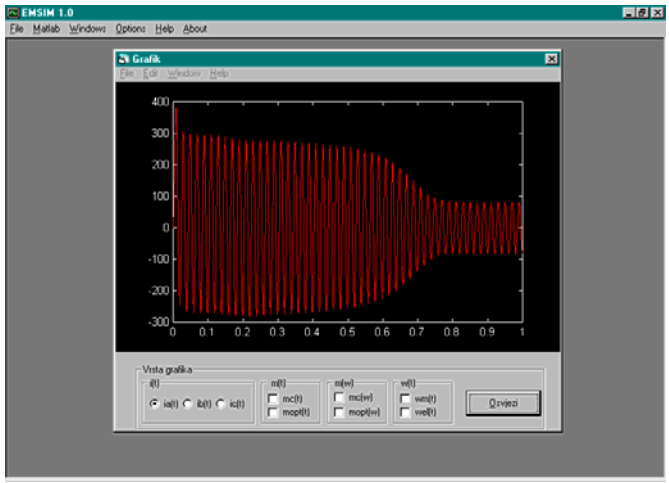

Fig. 4.: *Simulation Results (Phase Current)*

It can be noticed that simulation is finished faster than if the model is started directly in *Matlab*. After the simulation is over, program sends message "Simulation is done", and graphs can be plotted.

By choosing the option MATLAB/GRAFIK graph window will open. If the simulation parameters are changed in the meanwhile, then the program displays the message that the simulation must be restarted before the graphs are shown. On Fig. 4. plot window is shown. It has options for saving and printing the results. *EMSIM 1.1* can show phase currents/time, motor torque/time or torque/speed, and mechanical and electrical speed/time.

After choosing the value (current, torque or speed), button "Refresh" must be pressed. In newer version of software this will be obtained automatically. On Fig. 5. torque/time plot is shown (parameters are changed from Fig. 2). Torque/speed and speed/time plots are shown on Fig 6/7.

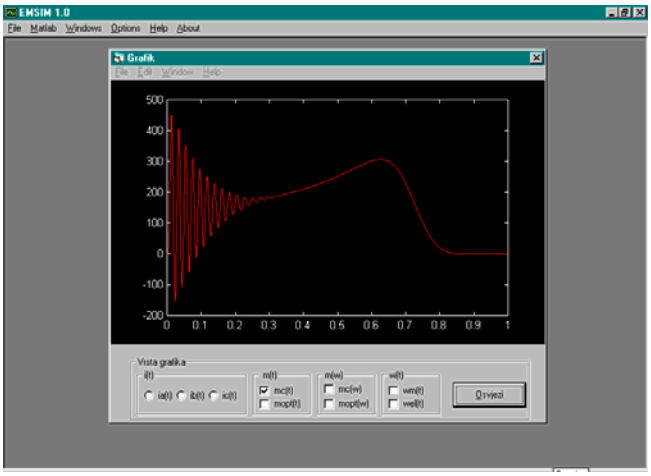

Fig. 5. Torque/time plot

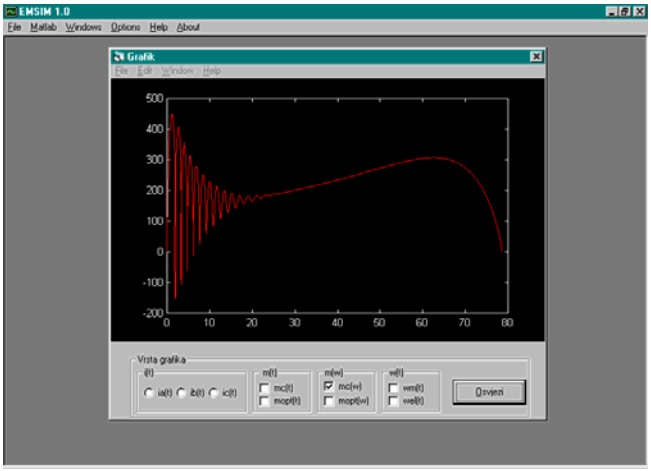

Fig 6. *Torque/speed plot*

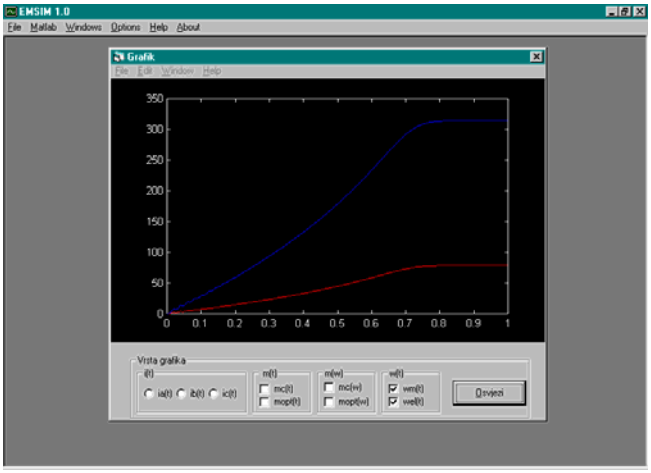

Fig 7. *Mechanical speed/time and electrical speed/time plots*

On Fig 8 motor and load torque characteristics are plot together. Operating point (torque/speed) can be found on intersection these two characteristics.

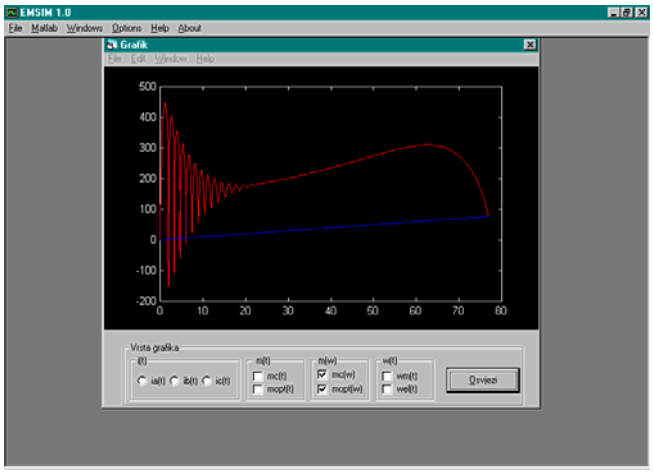

Fig 8: *Motor and Load Torque*

Help window is shown on Fig. 9.

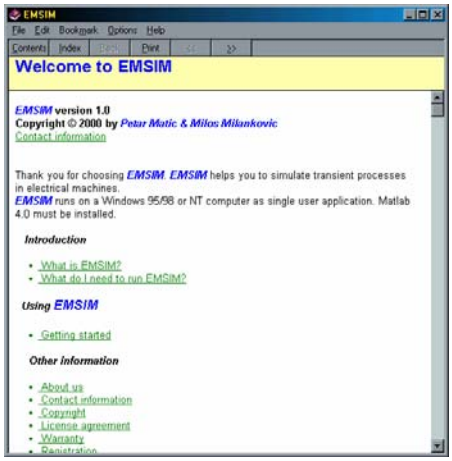

Fig. 9. *HELP Window*

6. CONCLUSION

In this paper development and use of a simple educational program is presented. This program has good accuracy, user friendly interface, and scalability for analysis of different electrical machine types and operating regimes / transient processes.

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UML-BUSINESS-PROFILE-BASED BUSINESS MODEL OF VISA ISSUING SYSTEM

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Abstract: *In this paper, one business modeling approach, based on the UML business profile, is presented. According to the UML business profile, business model consists of the business use case model and business object model. Business use case model is the external view of business domain and it represents the specification of business use cases, business actors and their relationships, shown by business use case diagrams and documented by high level activity diagrams. Business object model as an internal view of business domain shows business use case realizations and we propose use of sequence diagrams and business class diagrams based on detailed activity diagrams. Based on described methodology, the business model of migration system in BH has been developed. In this paper, some parts of the business model of the visa issuing subsystem are given to illustrate described methodology.*

Keywords: *UML business profile, Business modeling, Business use case model, Business object model.*

1. INTRODUCTION

Public administration institutions are complex systems that offer wide spectra of services to the external customers. They are characterized by appropriate organization structure and adequate business processes performed to fulfil customer's needs as a main goal. A business process is assumed as a specific series of spatio-temporal dependent activities, which has own begin and end, as well as clearly defined goal, inputs and outputs [1]. An organization structure represents a mutually related human and other material resources that are necessary for sucessful business process realization. A totality of custmers, organization structure and business processes is usually called business domain.

Business modeling represents the discipline that deals with business domain modeling. A business model is defined as an abstraction of the business domain parts and their relationships. A complete business model usually depicts business domain from different perspectives and its result of different aspect of analysis [1]. Each view is presented by one or more diagrams. Usually we consider four aspects of analysis [2]: concept (the highest abstraction level view of domain, where the problems and the goal architecture is described), structure (organization structure of business system), processes (business activities) and behavior (interactions between the resources – workers and objects).

The newer, use-case-driven, iterative and incremental based approaches to information system (IS) development process [3,4], such as RUP (*Rational Unified Process*), take the business modeling as the first phase in the IS development because the business model provides identification of the most suitable IS architecture for the particular business domain.

The main goal that should be achieved during the business modeling is the identification of all business processes and included activities, as well as process initiators and actors, process goals and results, nececssary resources (human, material and nonmaterial), process rules and constraints, present level of process automation, worker's responsibilities, alternate activity posibilities, ways for process improvement and eficiency augmenting, etc.

2. BUSINESS MODELING BASED ON UML BUSINESS PROFILE

2.1. UML business profile

Unified Modeling Language (UML) is the language for visual modeling of software systems [5-7]. It became the leading modeling language implemented in many CASE tools, and today it's the industrial standard for software modeling. Since business modeling is the first phase in IS development process and UML is the standard language for software modeling, extension and use of UML for business modeling is natural and logical, because during the whole cycle of IS development, from business modeling to software implementation and transition in business domain, the harmonized notation will be used and transition from business models to system UML models will be easier. Currently, there is no standard approach for business modeling based on UML. There are several different approaches: based on the standard UML [8], based on UML extensions [1], and finally, based on the UML business profile [2,9]. In practice, UML business profile is used more and more.

Talking about the profile, we talk about a defined set of standard language extensions that is built in UML and specialized for modeling in a particular domain. There are several different UML profiles. One of them is intended for the business modeling. UML business profile [5] specializes some base classes of the standard UML by introduction of business domain specific classes (Table 1), like business use case, business use case model, business object model, organization unit, work unit, business actor, worker, case worker, etc.

Table 1: Specialized classes for business domain.

Base class	Specialized class
Model	UseCaseModel, ObjectModel
Package	UseCaseSystem, UseCasePackage
Subsystem	OrganizationUnit, WorkUnit, ObjectSystem
Class	Worker, CaseWorker, InternalWorker, Entity
Association	Communicate, Subscribe

Some authors consider business model as a unique model [1], but according to UML business profile, business model consists of two models: business use case model and business object model (Fig. 1).

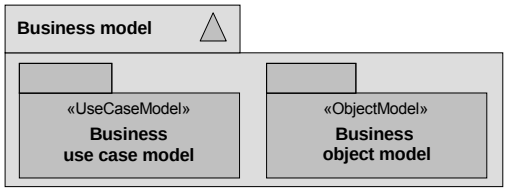

Fig. 1. Business model defined by UML business profile.

2.2. Business Use Case Model

A business use case model (BUCM) represents an outside view of the business system and describes the business system and its relationships with the external systems through the business use cases. We consider that business use case (BUC) is the business process, or some concrete function in the business system offered to the external systems. Those exterior systems are called business actors. BUC is the sequence of actions, performed by workers in a business system and by them the business system makes some concrete and recognizable value. BUCM contains descriptions of business actors and BUCs, and their interactions too. That is represented by BUC diagrams. BUCM includes the appropriate realization description of identified BUCs. BUC realization is documented by textual description and graphical presentation [9].

Textual description considers specifications of characteristics and activities of a particular process and it's a good base for non-functional requirements capturing in the next phase of system development.

For graphical presentation the activity diagrams or sequence diagrams could be used [10]. The process nature (exactly defined sequence of actions) and similarity with traditional notations prefer to use activity diagrams. It is recommended to use high-level activity diagrams [9], where only the main activities (macro activities), are shown without many details like responsibilities of workers and used objects. Additionally, swimlanes can be introduced to present activity distribution among the organization units or workgroups (recommended in complex business systems).

2.3. Business Object Model

A business object model (BOM) represents an inside view of a business system and in the completeness shows the process, procedures, business worker's behavior, used resources - business objects, and their relationships, that goals can be realized and expected results achieved. BOM usually includes detailed activity diagrams, some interaction diagrams and object diagrams [9]. A complete process description in the business model is shown by detailed activity diagrams – high level activity diagrams completed by workers' responsibilities, used objects and object flows. Responsibility areas of involved workers are emphasized by swimlanes. All activities, objects and object-flows connected to a particular worker are shown in the same lane, so we have as many swimlanes as workers who are involved in concrete BUC realization. In a more general case, we have not only workers, but workgroups and organization units as well.

An activity diagram is procedurally oriented and it is not appropriate for object-oriented (OO) IS development process, so BOM also includes some of OO interaction diagrams like: collaboration diagram or sequence diagram [11]. A collaboration diagram is suitable to focus on structural component of the process, but it isn't recommended in complex processes because of small or insufficient visibility. A sequence diagram offers possibilities to focus on temporal component of the process, and it is very close to an activity diagram, so it is recommended to use in BOM.

In order to have easier class modeling in the next analysis and design phases of IS development, BOM includes business object diagram or business class diagram also, which shows the static structure and relationships between objects. Thus, a business class diagram can be used to show the organization structure of business systems. BOM can include state charts too, especially in the case of more complicated transformations of business objects during the use case realizations.

2.4. Modeling Approach

UML as the standard modeling language, prescribes notation and semantics, but doesn't prescribe a modeling process. Several approaches are proposed [2,9]. The process described in this paper consists of the next phases (Fig. 2):

1. BUC specification by BUC diagram,
2. textual description of BUC realization,
3. graphical presentation of BUC realization by high level activity diagram,
4. detailed description of realization by detailed activity diagram,
5. OO interaction by sequence diagram, and
6. business class diagram.

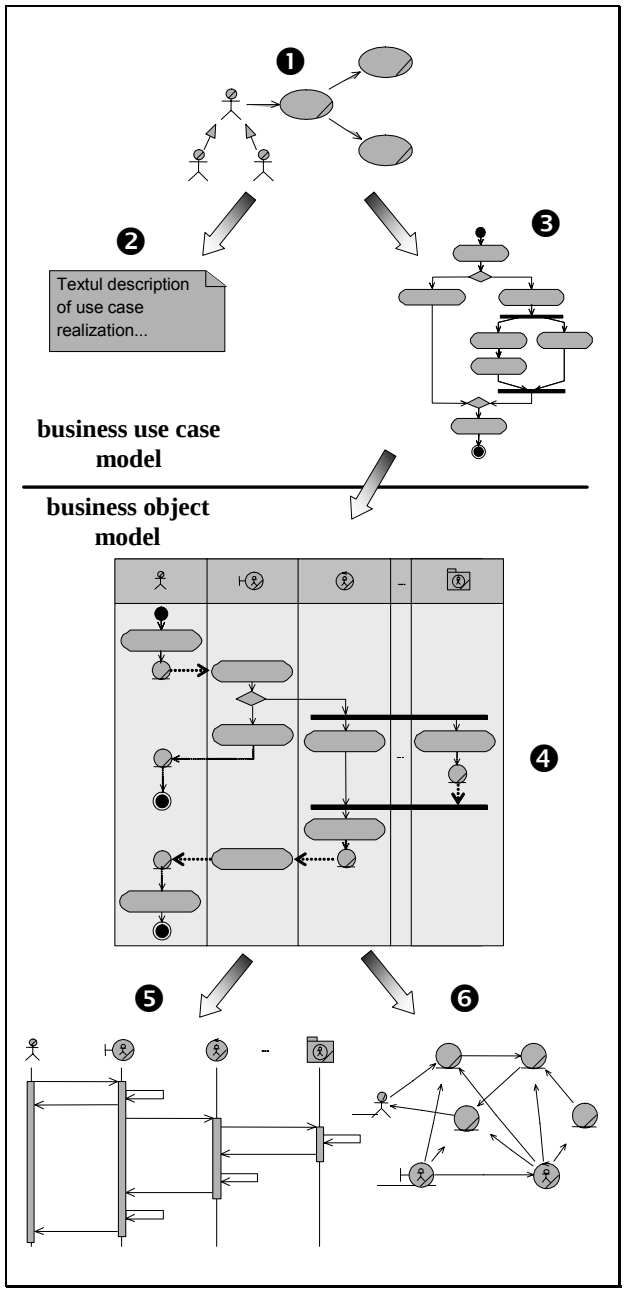

Fig. 2. Business modeling approach based on UML profile.

3. BUSINESS MODEL OF VISA ISSUING SYSTEM

Previously described approach is applied for business modeling of visa issuing subsystem in the framework of system for foreigner's migration evidence in B&H. In this paper only some parts of the visa issuing subsystem are presented as an illustration of the applied approach.

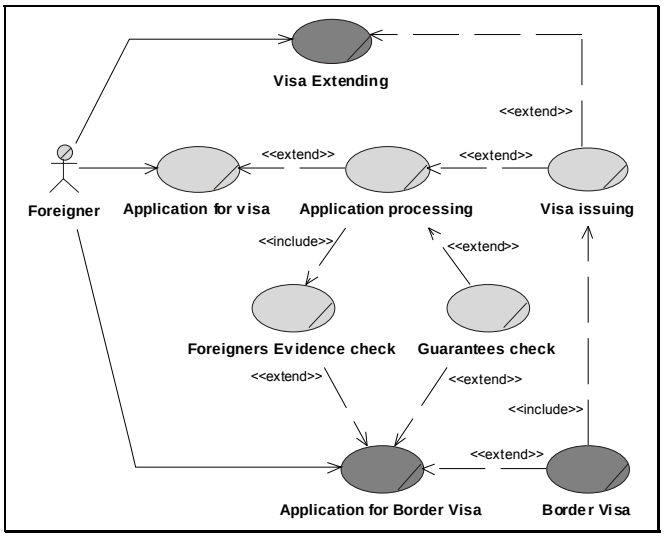

Fig. 3. BUC diagram of visa issuing subsystem for BUCs directly initiated by foreigner.

Fig. 3 shows the part of BUC diagram of visa issuing subsystem, which represents the BUCs that are directly initiated by business actor (foreigner) by submitting appropriate visa application. Besides those BUCs, there is another BUCs group that aren't directly initiated by foreigner, but initiated by some responsible government bodies or institutions. There is also another one BUCs group related to manipulations of visa stickers. These two groups of BUCs are also very important, but they aren't presented here.

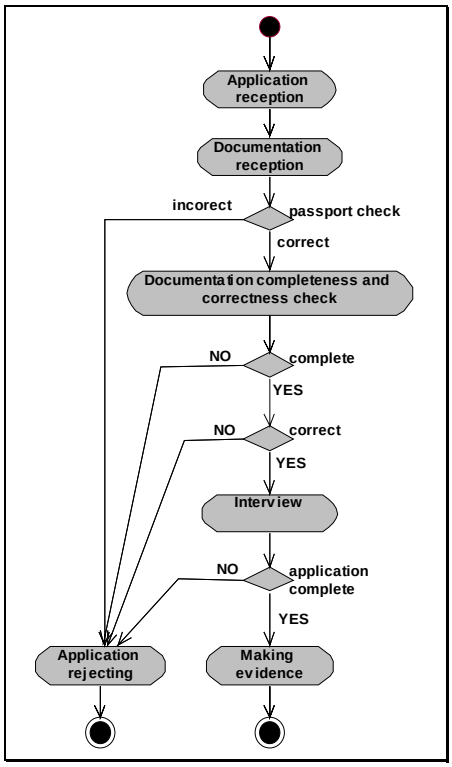

Fig. 4. Macroactivity diagram of BUC: Application for visa.

According to described apprach, all identified BUCs are documented by textual description and graphicaly depicted by macroactivity diagrams. Because of some objective reasons, only basic BUCs are shortly documented. Submitting visa application in Diplomatic and Consular Missions (DCM) abraod is the most usual way of application for visa. Fig. 4 shows the microactity diagram for this BUC. All business activities are performed by responsible person in DCM (case worker). From the IS point of view, the most interesting activity is the last business activity related to the recording of visa application in appropriate evidence, because only complete and valid applications should be recorded in a database. Observed BUC can be finished either by rejecting of visa application if the passport isn't valid or if attached documentation is uncomplete or invalid, either by application acceptance if everything is complete and valid. In the case of application acceptance, observed BUC will be extended by BUC Application Processing.

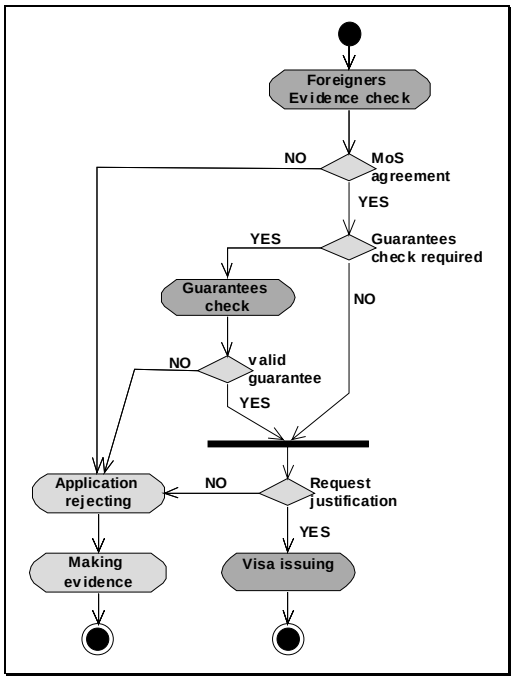

Fig. 5. Macroactivity diagram of BUC: Application Processing.

The **BUC: Application Processing** extends BUC: Submitting Visa Application in the case of valid and complete visa application. This BUC starts by the foreigner's status check in the Foreigner's Evidence which is performed by Ministry of Security (MoS). This macroactivity is excluded in this model as the separate **BUC: Foreigner's Evidence Check**. After that, in DCM, where visa application is submitted, justification of visa application is performed. That justification can include guarantees check which is separated in new one **BUC: Guarantee Check**. One possible end of this BUC could be rejecting of visa application if there is no MoS agreement or if request for visa isn't justified. In this case, rejecting should be recorded in a database. Another possible end is visa issuing if request is justified, so this BUC can be extended by BUC: Visa Issuing. As Fig. 3 depicts, BUC: Visa Issuing can also extend **BUC: Visa Extending** as well as **BUC: Border Visa** includes BUC: Visa Issuing.

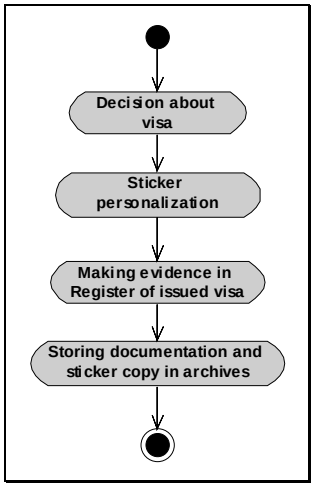

Fig. 6. Macroactivity diagram of BUC: Visa issuing.

According to described apprach, detailed activity diagrams are realized based on macroactivity diagrams, and after that sequence diagrams as well as business class diagrams. Related to some objective reasons and lack of space, detailed activity diagrams and sequence diagrams aren't presented in this paper. For each BUC particular business class diagram is performed and all those class diagrams are combined in one integrated business class diagram of visa issuing subsystem, which is shown by Fig. 7.

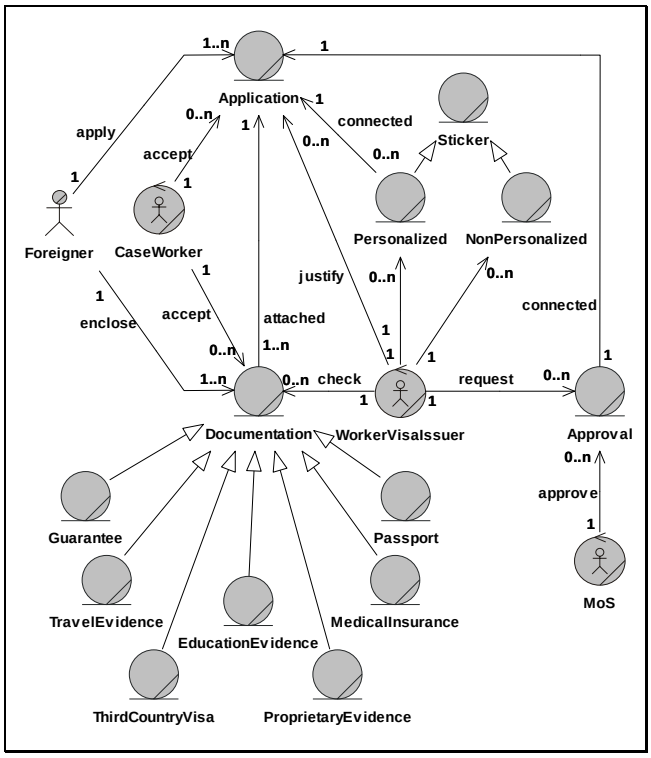

Fig. 7. Business class diagram of visa issuing subsystem.

4. CONCLUSION

Although primarily intended for visual modeling of software systems, thanks to the business profile, UML can be successfully used for business modeling, because very rich notation and semantics cover needs of all business domain analysis' aspects. UML based business modeling has the special importance as a base for IS development. Then, notations for business modeling and system modeling are harmonized, and the concepts used offer easy transfer of the business models into the system UML models.

In this paper, one business modeling approach, based on the UML business profile and founded on business use cases, is presented. According to the UML business profile, business model consists of the business use case model and business object model. Business use case model as an external view of business domain contains the specification of business use cases, business actors and their relationships, which is shown by business use case diagrams and documented by high level activity diagrams. Business object model as an internal view of business domain shows business use case realizations by sequence diagrams and business class diagrams based on detailed activity diagrams. Described approach can be used for business modeling of large-scale business systems, such as industry and government institutions. Based on described methodology, the business model of migration system in BH has been developed. In this paper, some parts of the business model of the visa issuing subsystem are given to illustrate described approach.

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ДОЂИТЕ ДА СЕ ДОГОВОРИМО!

INSTRUCTION FOR AUTHORS

Name of the author/s, Affiliation/s

Abstract: *Short instruction for authors is presented in this paper. Works that are to be printed in the review "Electronics" should be typed according to this instruction.*
Keywords: *Review Electronics, Faculty of Electrical Engineering in Banjaluka, Instruction for authors.*

1. INTRODUCTION

In the review "Electronics", we publish the scientific and professional works from different fields of electronics in the broadest sense like: automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. In addition to the scientific and professional works, we present new products, new books, B. Sc., M. Sc. and Ph.D. theses.

In order to enable the unification of the technical arrangement of the works, to simplify the printing of the review "ELECTRONICS", we are giving this instruction for the authors of the works to be published in this professional paper.

2. TECHNICAL DETAILS

2.1. Submitting the papers

The works are to be delivered to the editor of the review by the E-mail (elektronika@etfbl.net) or on floppy (or CD) by post mail to the address of the Faculty of Electrical Engineering (Elektrotehnicki fakultet, Patre 5, 78000 Banja Luka, Republic of Srpska, Bosnia and Herzegovina).

2.2. Typing details

The work has to be typed on the paper A4 format, 8.27" width and 11.69" height (21.0x29.7 cm), upper margin of 1" (2.54 cm) and lower margin of 0,59" (1,5 cm), left and right margins of 1,57" (2 cm) and 0,39" (1cm) (mirrored margins). The header and footer are 0,5" (1.27cm) and 57" (2 cm). The work has to be written in English language. Our suggestion to the authors is to make their works on a PC using the word processor MS WORD 97/2000, and for the figures to use the graphic program CorelDraw, if the graphs are not going from the original programs, i.e., from the programs received (like MATLAB).

The title of the work shall be written on the first page, in bold and 12 pt. size. Also, on the first page, moved for one line spacing from title, the author's name together with the name of his institution shall be printed in the letter size (10pt, *Italic)*. The remaining parts of the manuscript shall be done in two columns with 0.5cm distance. The work shall be typed with line spacing 1 (Single) and size not less than 10 pt (like as this instruction). After the title of the work and the name of the author/s, a short content in English language follows, written in italics. The subtitles in the text shall be written in bold, capital letters of the size as in the text (not less than 10 pt.). Each work shall, at the beginning, comprise a subtitle INTRODUCTION, and, at the end, the subtitles CONCLUSION and BIBLIOGRAPHY / REFERENCES.

The operators and size marks that do not use numerical values, shall be written in common letters. The size marks that can use numerical values shall be written in italics. The equations shall be written in one column with right edge numeration. If the breaking of equations or figures is desired, those may be placed over both columns.

Illustrations (tables, figures, graphs etc.) may be wider than one column if necessary. Above a table there shall be a title, for instance: Table 2. *The experimental measuring results.* The same applies to figures and graphs but the accompanying text comes underneath the figure of graphs, for instance: Fig.3: *Equivalent circuit diagram...*

The work should not be finished at the beginning of a page. If the last manuscript page is not full, the columns on that page should be made even. Number of pages should not go over 6.

3. CONCLUSION

This short instruction is presented in order to enable the unification of technical arrangement of the works.

4. REFERENCES

At the end of work, the used literature shall be listed in order as used in the text. The literature in the text, shall be enclosed in square brackets, for instance: ...in [2] is shown ...

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