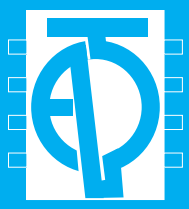

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Часопис "Електроника" у издању Електротехничког факултета у Бањој Луци ослобођен је плаћања пореза на промет на основу мишљења Министарства науке и културе Републике Српске, број 06-75/97 од 20. новембра 1997. године.

PREFACE

The 13th International Symposium on **Power Electronics – Ee 2005** (**Energetska elektronika – Ee 2005)** was held in Novi Sad from November 2 - 4, 2005. It was co-organized by Power Electronic Society (Serbia & Montenegro) sited in Novi Sad, Faculty of Technical Sciences from Novi Sad, Institute "Nikola Tesla" from Belgrade and Novi Sad Fair. Ministry of Science and Environmental Protection of Republic of Serbia, Provincial Secretariat for Science and Technological Development of AP Vojvodina, Serbian Academy of Science and Art (SANU), IEEE Serbia & Montenegro Section and Engineering Chamber of Serbia sponsored it.

Symposium on Power Electronics, widely known as Ee, is now in its fourth decade. This significant event shows constant interest of researchers, university professors, engineers, manufacturers, students and other experts in the field of Power Electronics. This time the main topic included power electronics switches, power electronics converters, electrical machines, electric drives, control & measurement in power engineering, power electronics in communications, electric power quality and renewable energy sources.

The Ee 2005 International Symposium presented the papers from various institutions of 17 countries (Austria, Bosnia & Herzegovina, Bulgaria, P.R. China, Czech Republic, France, Germany, India, Poland, Republic of Macedonia, Romania, Serbia & Montenegro, Spain, Switzerland, Turkey, United Kingdom, USA) and gathered more then 150 participants. Alongside, a tutorial and 6 student papers were also in the program. All papers were published as abstracts in *"Book of abstracts"* and as full papers in electronic form on CD-ROM *"Ee 2005"*. Besides the Proceedings of the Ee2005, the CD ROM contains presentations of the organizers and commercial sponsors, facts about Power Electronics Society, as well as complete bibliography from all symposiums on Power Electronics (1973-2005).

Due to restricted space, the selection of the papers in front of you is only one of several possible to represent the 13th Symposium on Power Electronics – Ee 2005. We would like to emphasize our thanks to the authors who have accepted our request for prompt respond and fast adaptation of the papers to journal requirements. More details about the symposium can be found at Internet address: www.ftn.ns.ac.yu/dee.

Besides the technical part of the Symposium, a student competitions: for the best hardware-software solution - *"Hardware & Software 2005"* were held for the first time. 4 student teams of 5 members from the universities of Banja Luka, Niš and Novog Sada competed in solving the problem of remote control of canal water ways in Vojvodina. The jury, consisting of eminent scientists, evaluated and rewarded the best solutions. The first prize was split between Novi Sad I and Niš teams, while the 3rd and the 4th were given to the Banja Luka and Novi Sad II teams. (http://www.ftn.ns.ac.yu/dee/hs-ns/eng/result-e.html)

We would also like to invite all readers of the »Electronics« journal to take active participation, submit their contribution and attend the next **14th International Symposium on Power Electronics – Ee 2007**, which will be organized in NOVI SAD, SERBIA & MONTENEGRO in **October/November, 2007** (www.ftn.ns.ac.yu/dee).

Guest Editors:

Prof. Dr. Vladimir Katić
Prof. Dr. Vladan Vučković

BIOGRAPHIES OF GUEST EDITORS

Prof. Dr. Vladimir A. Katić was born in Novi Sad, Serbia & Montenegro in 1954. He received B.Sc. degree from University of Novi Sad in 1978, and M.Sc. and Ph.D. degrees from University of Belgrade in 1981 and 1991, respectively, all in electrical engineering. From 1978 he is with Institute for Power, Electronics & Communication Engineering of the Faculty of Technical Sciences, University of Novi Sad, where he is currently Professor and Head of Power Electronics and Converters Group.

From 1993 to 1998 he was the Director of the Institute of Power, Electronics and Telecommunication Engineering and from 1998 - now the Vice-Dean of the Faculty of Technical Sciences of University of Novi Sad.

The main fields of scientific and research interest of Prof. Katić are power quality, power electronics converters, renewable energy sources and standardization in electrical engineering.

He is the author of several books: "Electric Power Quality - Harmonics" (2002), “Power Electronics – Laboratory Practice” (2000), "Power Electronics - Worked Problems" (1998), and the editor of the book "Modern Aspects of Power Engineering" (1995).

He is the author or co-author of more than 250 scientific papers published in international and national monographs, journals or conferences proceedings. He is also reviewer, member of international programme committees and session chairman of many international or national journals and conferences.

He is also the Vice Chair of IEEE Yugoslavia Section, Chairman of the IEEE Joint Chapter on Industrial Electronics/Power Electronics/Industry Application Soc. and Senior Member of IEEE. He is president of the Power Electronic Society (Serbia & Montenegro), observer Member at CIGRE SC36 (Paris), Member of International and National Committees of CIGRE and National Committees of CIRED and ETRAN.

Vladan Vučković, born 1928 in Kragujevac (Serbia, Yugoslavia), holds a Ph.D. degree from University of Belgrade, Department of Electrical Engineering (1964). Now retired, he was full professor at the University of Belgrade (Faculty of Electrical Engineering), at the University of Novi Sad (Faculty of Technical Sciences) and at the University of Niš (Electronic Faculty). During his 40-years university career he has established and taught numerous fundamental courses, as for example, Magnetic Amplifiers, Transient Phenomena in Electrical Machines, Power Electronics, Theory of Electrical Machines, Electrical Drives, Control of Electrical Drives, Microcomputers in Power Electronics.

Parallel to this assignment, he was about 30 years Manager of Control Department in Electrical Engineering Institute "Nikola Tesla" in Belgrade, where he and his team have developed a series of different devices in the field of power electronics, electrical drives and analog and digital automatic control.

He has published over 80 scientific papers and articles in national and international professional publications and conference proceedings, as well as two monographs ("Generalized Theory of Electrical Machines" and "Electrical Drives").

MODULAR HIGH POWER HIGHLY STABILISED MAGNET POWER SUPPLIES FOR PARTICLE ACCELERATORS AND SYNCHROTRONS

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Abstract: *The aim of this paper is to present a power electronics building blocks (PEBB) concept for high power magnet (superconducting or classical) power supplies for physics research institutions such as nuclear accelerators and synchrotron sources. A PEBB system described in this paper is based on [13kA, 18V] high frequency Zero-Voltage/Zero-Current switching (ZVZCS) converters built by Transtechnik for Large Hadron Collider (LHC) Machine at CERN. After a basic system description, interconnection and parallel operation of the basic system in order to increase the output current/voltage will be presented.*

Key Words: ***Accelerators, Synchrotrons, Pulsed Power Supplies, Superconducting Magnets, Soft-Switching Converters.***

1. INTRODUCTION

Superconducting or classical magnet power supplies (PSU) for physics research institutions such as nuclear accelerators and synchrotron sources usually demand a very high level of performance from the power converters, the most important being:

- DC stability and accuracy (ppm area),
- Dynamic response (ideal profile tracking),
- High efficiency,
- Wide operating current range (1% to 100%)
- Electro Magnetic Compatibility (EMC),
- Ease of replacement,
- System redundancy (n+1 based).

To meet these requirements, modular (PEBB based) IGBT converters with soft-switching techniques are used as the state of the art. In addition, a modular approach increases fault tolerance and decreases the overall system cost.

A PEBB system described in this paper is based on [13kA, 18V] and high frequency Zero-Voltage/Zero-Current switching converters built by Transtechnik for Large Hadron Collider Machine at CERN. The chosen sub-converter topology is described in three parts - Part 1: Circuit-breaker and contactor together with a soft-start circuit, input rectifier on the AC mains with a damped LC passive filter. Part 2: Full-bridge soft switching inverter. Part 3: High frequency transformers, rectifier stage and 4th order L-C output filter.

Such PSUs are intended to supply the basic types of magnets, both superconducting and warm resistive ones, such as:

- Dipoles for beam bending and steering
- Quadrupoles for beam focusing
- Sextupoles and higher order magnets for the beam correction, chromaticity control etc.

After design, control and operation description of a highly stabilised PSU, an analysis of converter adaptation for different pulsed voltages/currents will be presented. Interconnection and parallel operation of the basic system in order to increase the output current/voltage will be discussed.

2. BASIC BUILDING BLOCK FOR HIGHLY STABILISED MAGNET SUPPLIES

The basic sub-converter for the [3.25kA, 18V] converter is split in three modules i.e. “building blocks inside a building block” (Figure 1):

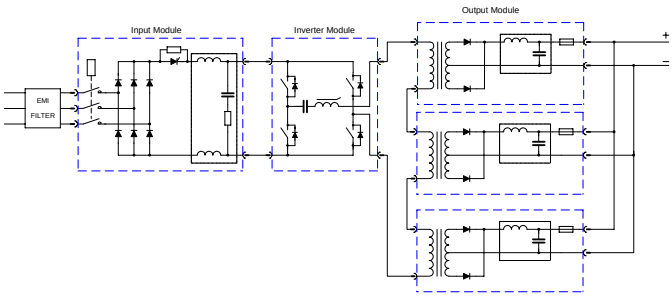

Figure. 1. *Basic building block: sub-converter for highly stabilized supplies*

- Input Module: a power contactor on the AC mains (3x400V, 50Hz), a diode rectifier with a damped L-C passive filter (70Hz)
- Inverter Module: Full-Bridge Zero Voltage Zero Current Switching Phase Shift inverter (FB-ZVZCS-PS) at 25kHz
- Output Module: high frequency transformers, rectifier stage and output filter. To fulfill the weight constraint, the module 3 is physically split in three modules of 1.1kA.

2.1 Input module:

The 3-phase mains voltage is rectified and filtered in the input module. An input contactor disconnects the complete sub-converter from the mains if there is no demand for power or in the case of a severe fault. The input module is equipped with a pre-charge circuit to limit the inrush current at the power-up. EMI Filter is provided at the modules input.

2.2 ZVZCS Inverter module:

The filtered DC-link voltage from the input module feeds the inverter running at 25 kHz. This stage employs a switch-mode inverter (ZVZCS = **Z**ero **V**oltage / **Z**ero **C**urrent **S**witching). The control of the power semiconductors (IGBTs) is done by introducing a phase-shift between the two legs of the bridge, instead of turning off the diagonally opposite switches in the bridge simultaneously as for a classical PWM. This phase-shift determines the output power whereas the switching

frequency is fixed to 25 kHz. The needed energy to achieve soft-commutation conditions for the switching of the leading leg (ZVS) comes from the series inductance, the leakage inductance and the output filter inductance. This means that the energy stored is large enough to charge and discharge the parallel switch capacitances (parasitic and snubbers) and the parasitic capacitances of the transformer. To regulate the output voltage / current with high precision from 1% to 100% and over a wide load range, a modified phase-shifting principle is applied, as shown in Fig. 2. By using a DC blocking capacitor and a saturable inductance, the primary current is reset during the freewheeling period, which provides ZCS conditions for the lagging-leg switches.

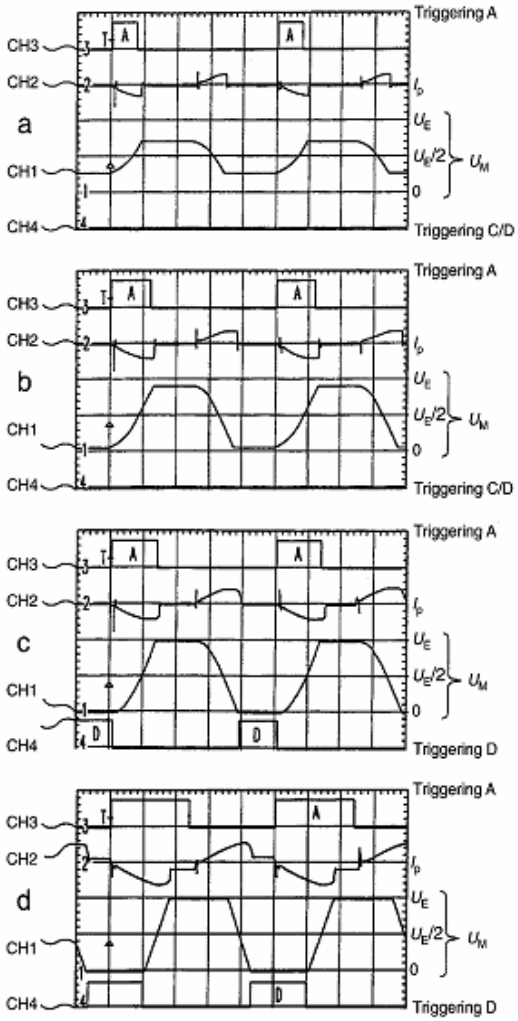

Figure 2. *ZVZCS Module in different modes: a) almost idle, b) low load, c) medium load, d) full load. U_M=DC-link mid-point voltage (100V/div), I_P=primary current (100A/div)*

2.3 Output module

- High frequency transformers and Schottky diodes:

To achieve the required output parameters (1100A, 18V) within one module (Figure 1), a special transformer with ferrite core UU93 and thin copper foil windings has been developed. The secondary is separated into 3 sections, each of them feeds a centre-tapped rectifier with 2 Schottky diode modules to handle the current with 20% safety margin. Considering the skin and proximity effects, the foils are wound in such a special way to enable the appropriate current sharing, that is - the current in each section and also in the Schottky diodes is almost identical. Furthermore, the series / parallel connection of the split modules guarantees a good current sharing between them.

- Passive filter:

To achieve the required output ripple of only 10mVpp at peak output current a quadruple stage output filter was implemented. The filter stages consist of iron powder cores and electrolytic capacitors with very low ESR and high reliability.

- Fuse and power connections:

A fuse is used to protect the output module against serious damage in case of a diode failure. All the output modules can be exchanged easily by pulling the units out via the special drawer system. A system of multiple single-pole high-current connectors is used for quick plug-in/plug-out to carry the high currents.

3. BASIC BUILDING BLOCK FOR PULSED MAGNET SUPPLIES

The system architecture for pulsed power supplies is similar to the one presented in paragraph 2, with a difference that two- or four-quadrant operation is required. This requirement leads to elimination of HF galvanic isolation and introduces (if required) a LF one. In addition, considering the pulse profile and magnet's duty cycle, it is not necessary and often not possible (because of the limited energy gradient through the equivalent supply inductance) for the input circuit to manage the complete power range. It is thus designed to handle the average power, while the power peaks are drawn from the DC-Link which at the same time provides the energy storage and the filtering function. Depending on (average power)/(peak power) ratio, peak power duration and magnet duty cycle, different energy storage methods can be used: electrolytic capacitors, batteries and super capacitors. Inverter or 2-quadrant chopper must be designed to handle the full load power.

Fig. 3. shows bipolar pulsed PSU with 4-quadrant chopper module designed for the steering dipole or trim quadrupole type magnets, while the figure 4. illustrates an energy recovery pulsed PSU with 2-quadrant chopper module for the kicker type magnets.

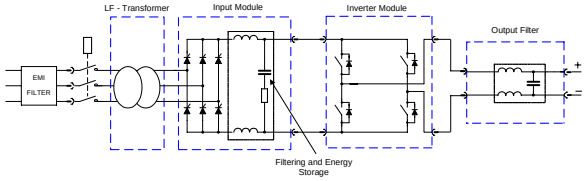

Figure 3. *Bipolar pulsed PSU with inverter / 4-quadrant chopper module*

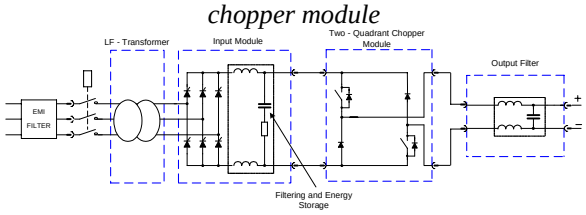

Figure 4. *Energy recovery pulsed PSU with 2-quadrant chopper module*

4. CONTROL OF CONVERTERS

To achieve the required high DC precision and stability, a triple cascaded control system have been implemented (Figure 5):

- a fast current loop at the sub-converter level (ZVZCS-inverter current control), having the task of attenuating the 6-pulse DC-link (300Hz) ripple, eliminating mains disturbances and of conversion of voltage-source to current-source converter for the purpose of sub-converters paralleling. The required bandwidth is 8 kHz
- a global voltage loop to control a global voltage source composed of (n+1) sub-converters with a required bandwidth of 700 Hz. Separate electronics handles the regulation of the whole converter and provides the reference and other control signals for all the sub-converters.
- a high precision current loop to control the magnet current with demanded high precision with a bandwidth of 1 Hz. A high precision current transducer, usually a Direct-Current Current-Transformer (DCCT), measures the output current of the power converters. With the Transtechnik converters for LHC, a CERN developed RST current control algorithm was used.

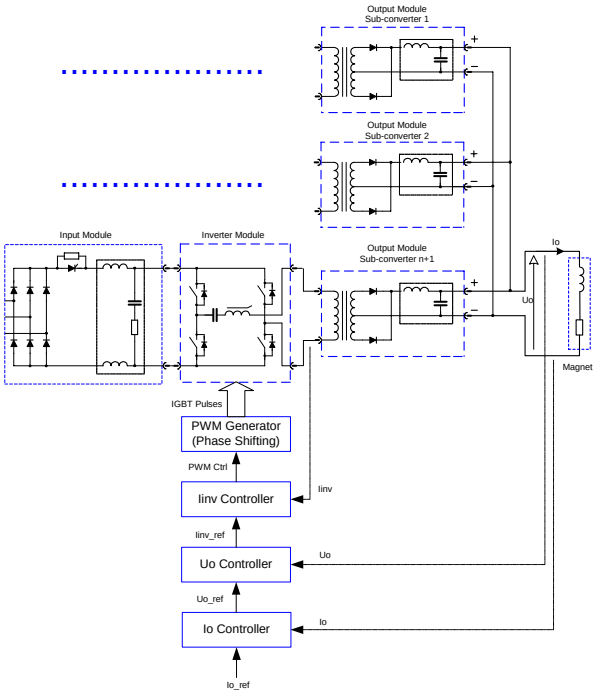

Figure 5. *Control structure*

Fig 6. shows an experimental frequency response of the fast current loop at sub-converter level, where:

Area [1], I_{REF} = 1.62500kA + 162.5A x sin (wt)
Area [2], I_{REF} = 4.71250kA + 162.5A x sin (wt)
Area [3], I_{REF} = 12,1875kA + 81.25A x sin (wt)

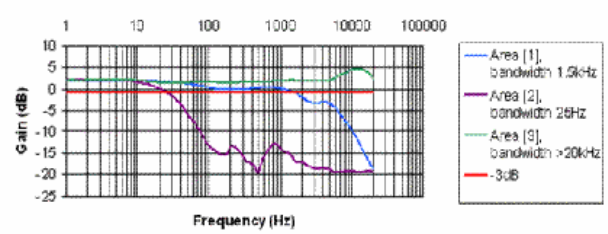

Figure 6. *Fast current loop frequency response*

Fig. 7 shows an experimental frequency response of the magnet voltage loop, where:

Area [1], U_{REF} = 0.540V + 0.18V x sin (wt)
Area [2], U_{REF} = 1.026V + 0.18V x sin (wt)
Area [3], U_{REF} = 2.700V + 0.18V x sin (wt)

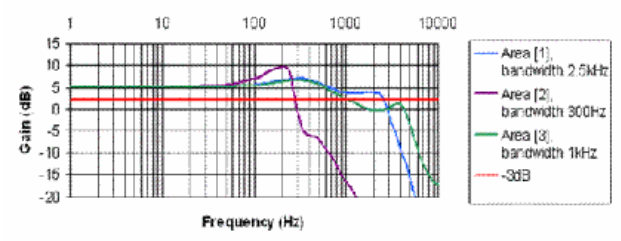

Figure 7. *Output voltage loop frequency response*

5. PARALLEL OPERATION/REDUNDANCY

The PEBB converter system has been designed in such way that several sub-converters can work in parallel. The voltage inverter topology used in the design means that the sub-converters are inherently voltage sources. In order to make the paralleling possible, a fast current loop, as discussed in paragraph 4, transforms the sub-converters into a controlled current sources.

For reasons of redundancy and availability, the converter has been designed to use one extra sub-converter in relation to the necessary power, as shown in Fig. 8. Fig. 9 shows the [13kA, 18V] converter (234kW nominal power) which make use of 5 [3.25kA, 18V] sub-converters with total available power 292.5kW. Fig. 10 shows the [20,5kA, 18V] converter (369kW nominal power) which make use of 7 [3.25kA, 18V] sub-converters with total power 430.5kW.

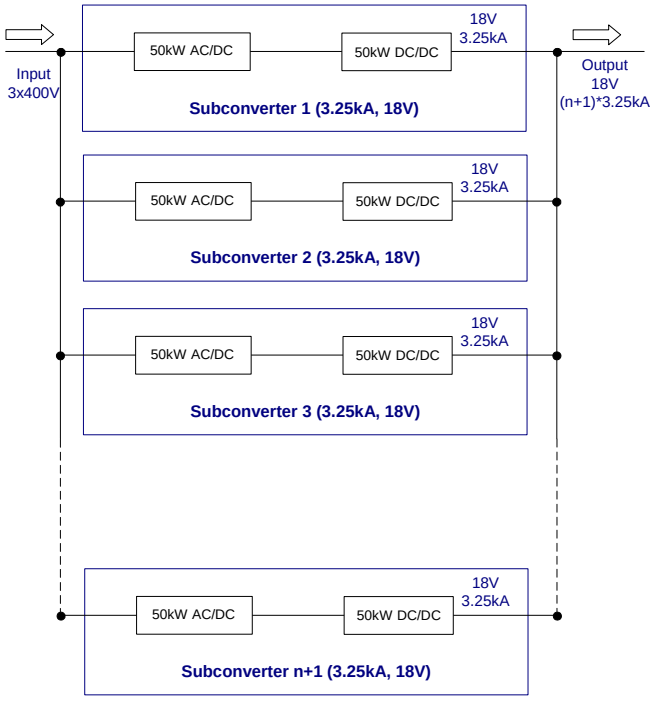

Figure 8. *n+1 redundancy concept*

Figure 9. *[13kA, 18V] converter*

Figure 10. *[20,5kA, 18V] converter*

The sub-converters are capable of being started independently and working alone. Under normal conditions, all the sub-converters are working in parallel with n/(n+1) capacity. If one of the sub-converters fails, the current reference for remaining sub-converters will increase, so that the current and voltage of the magnet do not change, as shown in Fig. 11. This feature is very important for the research institutions since the failure of one sub-converter does not lead to failure of the experiment in progress.

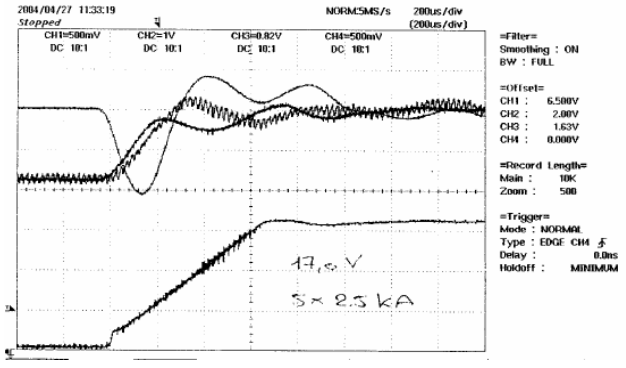

Figure 11. *Magnet voltage and sub-converter current when one sub-converter fails (time trace 200μs/div)*

With a simple inverter-transformer adaptation, it is possible to achieve a different voltage levels at the sub-converter output with the same PEBB design, provided the sub-converter power stays within the 58.5kW range. With the Transtechnik latest design the sub-converter power will be pushed to the 66kW, enabling larger power density.

6. PERFORMANCE

In addition to the features explained in the previous section, further converter performance can be summarised as:

- Current operating range from 1% to 100% of the 13kA/20.5kA maximum current with soft-commutation throughout the range (Figure 12, 13). The soft-commutation enables the use of only one inverter module per sub-converter.
- Measured efficiency is above 90% at full power.
- Output voltage ripple is less than 10 mV p-p in the 0 - 150 kHz frequency band, 2 mV r.m.s. for frequencies > 150 kHz and 1 mV r.m.s. for frequencies > 500 kHz (IEC 478-3-C for conducted EMI) (Figure 14).

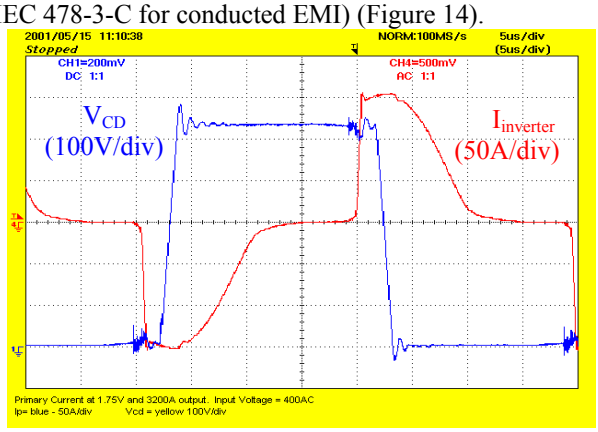

Figure 12. *Inverter current with high output current (3200A) and low voltage (1.75V)*

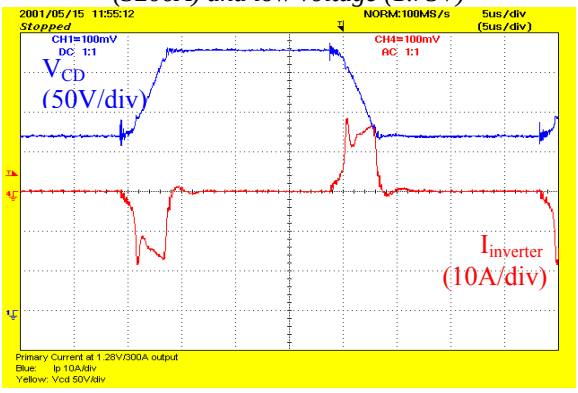

Figure 13. *Inverter current at low output power (300A, 1.3V)*

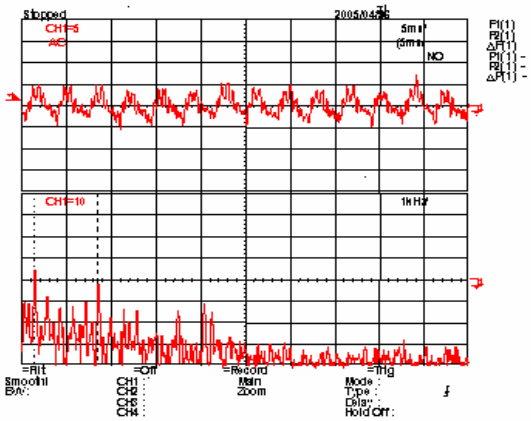

Figure 14. *Output voltage ripple and its frequency spectrum at full power*

7. CONCLUSION

A power electronics building blocks concept for high power magnet power supplies was presented in the paper. After design, control and operation description of a highly stabilised PSU, an analysis of converter adaptation for pulsed applications was presented. Interconnection and parallel operation of the basic system in order to increase the output current were discussed as well as the necessary steps to increase/decrease the output voltage.

It was shown that the PEBB concept enables the use of standardised sub-converters for the whole range of applications. Compared to classical "a specific supply for a specific magnet" design, the most important advantages of such concept are:

- Ease of replacement,
- System redundancy
- Fault tolerance
- Shorter stuff training time
- Reduction of the overall system cost

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RECENT PROGRESS IN MOTION CONTROL SYSTEMS AND ITS IMPACT ON POWER ELECTRONICS

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Abstract: *Power converters in motion control systems are accountable for converting the electric energy obtained from the primary source and adjusting the frequency and the amplitude of the output voltages and currents. The output quantities are suited according to the needs of the electric servo motor. At present, electric drives in general absorb two thirds of all the electric energy produced in an industrial country. Recent progress in motion control systems requires new power electronics technologies, solutions and components. The growth of high performance drives depends on the investments in new production sites. Recent trends of replacing production sites to countries where the labour cost is lower calls for a more advanced motion control systems, requiring less maintenance and skilled workers. The elements of motion control systems, and in particular the power electronic units became commodity products, their cost becoming one of the main issues. At the same time, the energy efficiency, a higher peak-to-rated power ratio, the energy quality and the regenerative braking imposed new standards to power converter topologies and solutions. This article outlines the impact of recent trends in motion control systems on the power converter topologies used in electric drives. Both high volume, low performance applications and the cutting edge applications are pointed out, including as well the insight into most recent power electronics products and solutions, offered by leading PE manufacturers.*

Key Words: ***Electric drives, power conversion, electric machines, motion control***

1. INTRODUCTION

Significant share of the power electronics devices gets used in electric servo drives, applied in motion control systems, industrial robots and general automation. At present, electric drives in general absorb two thirds of all the electric energy produced in an industrial country. Recent progress in motion control systems requires new power electronics technologies, solutions and components.

Over several past decades, electric drives have been replacing fluid power actuators and IC machines in both high performance and general purpose applications, the growth of electric drives application being determined by the current level of technology. High reliability, long lifetime, relatively low maintenance and short startup times of electric drives are in consort with their ecological compatibility: low emission of pollutants. The quality of electric drives is extended by a high efficiency, low no-load losses, high overload capability, fast dynamic response, the possibility of recuperation, and immediate readiness for the full-featured operation after the drive startup. Electric drives are available in a wide range of rated speeds, torques and power, they allow for a continuous speed regulation, reversal capability, and they easily adapt to different environment conditions such as the explosive atmosphere or clean room requirements. Unlike the IC engines, electric motors provide for a ripple-free, continuous torque and secure a smooth drive operation.

During the past two decades, the evolution of powerful digital microcontrollers allowed for a full-digital control of the electromechanical conversion processes taking place in an electrical drives. The process automation made significant progress in the fifties, thanks to the introduction of numerical control (NC). Although not flexible and fully programmable, NC systems replaced relays and mechanical timers common on the factory floor in the first half of the century. As the first reliable and commercially available microcontrollers were made in the sixties, they were advantageously used for the purpose of a flexible control of electric drives in production machines. As from then, the hydraulic and pneumatic actuators gradually disappear and give space to DC and AC electric motors. Among the first applications of variable speed frequency controlled AC drives were pumps, fans and compressors, where the speed regulation feature eliminated mechanical damping of the fluid flow and reduced the associated power losses and turbulence. For their increased reliability, low maintenance, and better characteristics, the frequency controlled induction motors gradually replaced DC drives in many of their traditional fields of application. Further technological improvements made the frequency controlled AC drives the cheapest actuators ever. Compact digital controllers emulate the functions traditionally implemented in the analog form and allow also the execution of nonlinear and complex functions that could not have been completed by analog circuitry (ANN, nonlinear estimators, spectrum estimation and others). Highly evolved observers of the drive states allow reduction of the number of sensors. The drives with minimum number of sensors and the shaft sensorless drives are more robust and reliable than their sensored counterparts. The lack of sensors and associated cables makes the drive cheaper and the installation simpler and faster. In the development phase are the advanced parallel control structures such as the direct and incremental torque control that make the use of a large numerical throughput to implement a non-cascade control concept thereupon augmenting the response speed and overall drive dynamic performance.

The growth of high performance drives depends on the investments in new production sites. Recent trends of replacing production sites to countries where the labour cost is lower, calls for more advanced motion control systems, requiring less maintenance and skilled workers. The elements of motion control systems, and in particular the power electronic units became commodity products, their cost becoming one of the main issues. At the same time, the energy efficiency, a higher peak-to-rated power ratio, the energy quality and the regenerative braking imposed new standards to power converter topologies and solutions.

The article discusses the problems and future trends in each group of electric drives. Particular attention is paid to the motion control algorithms and to the developments in the power conversion control. Specific influence of an ever increased number crunching capability of modern digital controllers on the drive controller structures is probed deeply. Performance enhancements of semiconductor power switches are outlined and their influence on the drive converter topology and characteristics is briefly analyzed. Finally, the needs and the possibilities are outlined for a digitally controlled drive to assume versatile adaptation and self -commissioning features, reducing in such a way the need for the operator interventions in both the installation and regular operation phases.

2. POWER CONVERTERS IN CONTEMPORARY MOTION CONTROL SYSTEMS

Traditional approach in designing production automata, used during most of the 20th century, included following steps:

- Decision on basic motion needs, based upon the set of desired operations, tools, materials and production technology
- Decision on the transmission technology and couplings
- Preliminary estimates on the tooling and electric actuators
- Design and prototyping of the robot mechanics
- Preliminary testing with provisional electric actuators (in most cases, parallel runs are made with several competitive drive&controls suppliers).
- Detecting the most critical compliance problem, the problems of mismatched motor-load-controls, insufficient bandwidth and precision, and similar).
- Correcting the design, in general, by adding components and modules, and specifying the key elements having a higher grade and cost than planned.
- Considering power electronic devices, the robot performance problems are often resolved by specifying higher peak and RMS currents than planned.

In brief, mechanical, electric and control designs did not overlap. As a consequence, the total weight of the production machine moving parts was higher, increasing the cost, reducing the energy efficiency and impairing the overall performance. Due to reasons well known, contemporary production machines are expected to have a competitive cost, and to achieve as short as possible cycle time. The later implies an elevated bandwidth and precision, bringing up the issue of transmission elements to a critical level. In many cases, the usage of linear motors is a must. All of the performance criteria listed is highly dependent on the total weight of the moving parts. Therefore, there is a pressing need to reduce the weight of the moving parts, and this is possible through the contemporaneous design, organized through a synergic link between mechanic, electric and information technologies.

The structure of an intelligent motion control system applied in industry includes:

- Communication link of the production cell with the production site host computer.
- Hardware and software resources for the high-level interpretation and optimization.
- Diagnostic and supervision on the technology level.
- Diagnostic, protection and supervision on the motion control level
- Coordination, profiling, cinematic calculations, interpolation.
- Single-axis micro-interpolation, torque, speed and position control

Traditional design approach is illustrated in Fig. 1.

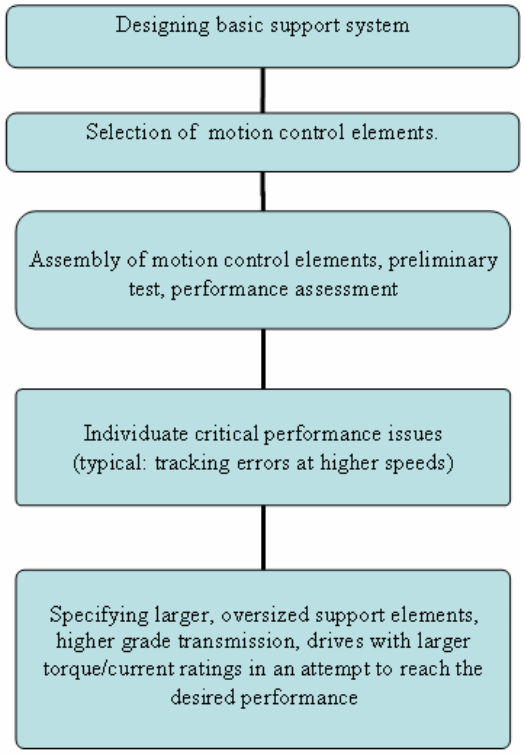

Fig. 1: *Traditional design approach*

As a consequence, the peak and RMS current ratings of servo motors is generally above the essential minimum. This in turn leads to an increased cost and size of power converter active components. At the same time, the power conversion losses are increased, and the problem of thermal management adds to the system size and cost. In Fig. 2, recently adopted design procedure is given, organized through a synergic link between mechanic, electric and information technologies.

Concurrent design of electrical, mechanical and control subsystems requires an extensive use of computer simulations. In particular, mechanical supports, transmission and transducers have to be simulated by using real-time finite-element packages, taking into account the form and the grade of materials. At the same time, standard transducers and transmission elements, normally obtained from third parties, have to be accompanied with the necessary models, facilitating such simulation. In a way, the procedure of simulating the dynamic behavior of the prototype robot resembles simulation of electric circuits in Pspice, with Pspice models of individual components being supplied from the supplier in a standardized form.

Real –time simulation of industrial robots is not fully automated yet, and it requires a great deal of on-site programming, relating to the current needs to relate, interface and integrate the available software packages, focused on narrower application fields such as the electrical (power electronics, motors), mechanical and control domains. On an average, proper simulation allows an accurate performance prediction (Comau). In subsequent drive selection, a saving of up to 50% is possible in terms of the peak/RMS current and torque ratings.

Further reduction of the drive ratings is obtained by scrutinizing the load torque prediction. The available computer tools allow for a more precise calculation of several load torque components for each individual motor, based on the motion profile, the ambient conditions and the temperature range, the cycle times, production processes, the quality of materials involved and characteristics of the MCS elements used. It is possible to identify and sum the following torque components:

- Load torque related to gravity
- Viscous friction
- Resistive torques related to tools and work materials, including cutting resistance, drilling, punching, and similar
- Static/dry friction forces and torques
- Torque disturbances coming from transmission and other elements.
- Inter-axis coupling related to the MCS dynamics.
- Inertial torques (acceleration, deceleration)

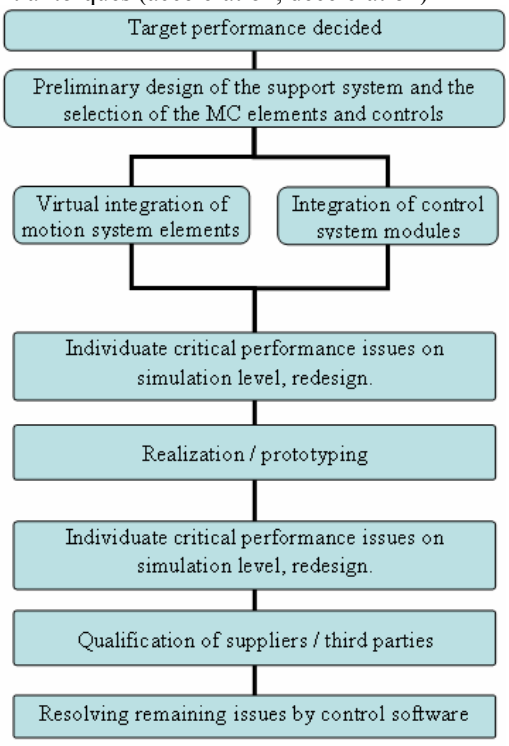

Fig. 2: *Contemporary design of the MCS*

Finally, in a cost optimized design, the rated torques and currents of servo motors involved are reduced to a necessary minimum. On the other hand, the needs to increase the productivity and reduce the cycle times lead to elevated acceleration torques. As a consequence, the peak torque/current values tend to increase, while preserving or reducing the rated RMS values. Therefore, the power converters are required to withstand higher short-term overloads, while their passive components and cooling systems can be designed to much lower average values. Considering the cost and weight structure of power converters, the power semiconductors and sensors are going to prevail while the passive components tend to shrink. When specifying thermal management elements and heatsinks, their thermal capacity becomes more important than the thermal resistance.

3. EXTENDED LIFETIME REQUIREMENTS

Reduced availability of trained servicemen at oversees production sites requires an extended operating life of all the power electronics components and systems. Besides, considering the use and practice related to spare parts, the average storage life has to be extended as well. Major issue in this regard is related to power electrolytic capacitors. Their lifetime is limited essentially by the process of loosing the electrolyte and drying out. Their aging is highly accelerated at elevated temperatures and at increased RMS current ratings. While other passive and active components tend to shrink, the electrolytic capacitors increase their relative part in the converters size and cost. A strenuous effort is made to achieve power converter designs free from electrolytic capacitors, relying on next generation metalized polypropylene and other capacitor technologies.

Electrolytic capacitors do limit the storage life as well. In cases where a new part has never been connected to power for years, and used to be stored instead, it would have to be re-formed before use. Otherwise, in cases when the unit comprising such a capacitor is directly connected to the rated voltage, the electrolytic capacitor would exhibit a very low resistance (i.e. a short), causing a fatal failure. An effort is made to prolong the storage life of power capacitors (Panasonic, Nichicon).

In some cases, it is necessary to provide a backup power supply for auxiliary circuits, capable of keeping the control circuitry and processors active during the powerdown intervals. lead-acid or nickel-cadmium batteries are frequently used to suit such needs. Whenever an extended lifetime is needed, super-capacitors are used. Still immature in technology, the super-capacitors are available for low rated voltages only (2-3V).

4. REGENERATIVE BRAKING

Multiple servo drives have their acceleration/deceleration phases spaced in time, according to the multiaxis motion profile. The intermediate circuits of relevant power converters (i.e. the DC-bus) are in most cases paralleled, to allow for the exchange of the energy between the accelerating and braking motors. Though, as the acceleration/braking phases may not overlap, the system occasionally has an excess of energy in the intermediate circuit. Traditionally, Dynamic Braking Resistor (DBR) circuit is used, equipped with an active power switch. Whenever an excessive voltage in the intermediate circuit is detected, the active power switch (T7 in Fig. 3) is turned on and the energy is dissipated in resistor R, eventually turning into heat.

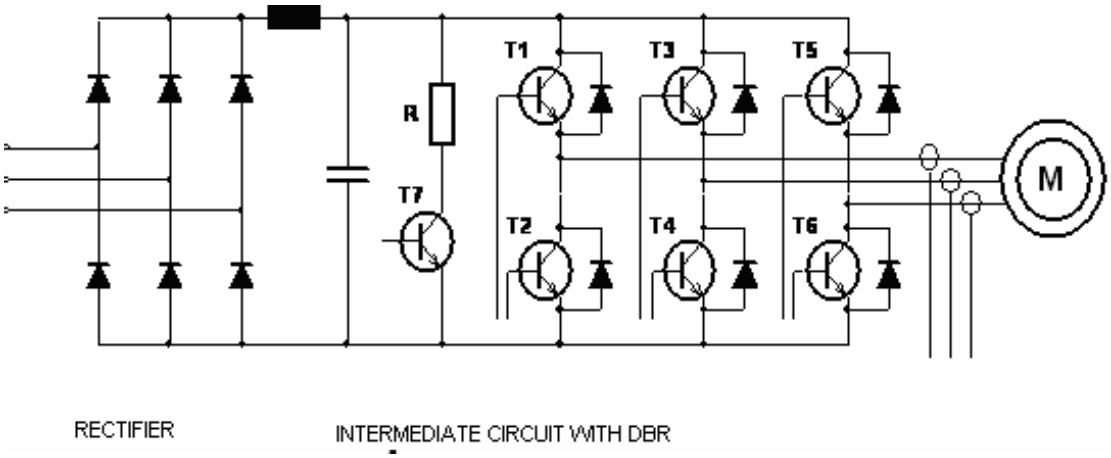

Fig. 3. *Dynamic braking resistor (R) and an active power switch (T7) in DC-link circuit*

In some applications, thermal management is critical, and the additional heat cannot be handled. In other cases, safety issues prevent the use of a braking resistor. Namely, due to elevated surface temperatures of the resistors, dust deposits in textile and similar industries can be set to fire. Therefore, it is of interest to manufacture and deploy regenerative front-end converters (see Fig. 4).

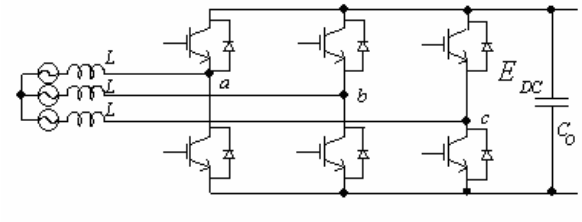

Fig. 4: *Regenerative front-end converter*

5. FREE-WHEELING PROTECTION

Complex mechanical structure of a production machine can be damaged in case of collisions or the lack of control. In case of an interruption of the main power supply, the accelerated masses may proceed moving by inertia, and eventually crash, damaging the tools, moulds, or make other damage. As a precaution, the servo motors are frequently equipped with brakes. The motor brakes can be used as a safety measure. Though, their braking action is not controllable, and they cannot make the system stop along a predefined trajectory. Rather abrupt, the use of mechanical brakes should be avoided whenever possible.

When the powerdown event happens with the system masses running, their kinetic energy can be used as the energy source. Controlled braking is possible with the servo motors operating as generators, and with the kinetic energy being fed back into the intermediate circuit through the power converter / inverter. As long as the control section is properly supplied, the system can be driven down to a full stop, running along any predefined trajectory, hence avoiding any collision or other mechanical threat. In order to provide continued auxiliary power supply, the SMPS module should have the possibility to use the DC-bus (intermediate) voltage in all cases when the mains voltage is too low.

6. LOW COST ELECTRIC DRIVES IN TEXTILE INDUSTRY

Textile machines generally feed or use hundreds of threads (500-1000). Traditional textile machines make use of a single controllable electric drive, with hundreds of thread-feeders coupled to the main drive by means of belts or frictional couplings. This prevented tension control of individual threads. Nowadays, there is a pressing need to use low power (50-100W) controlled induction motor drives for each of the thread-feeders. With a total power of 50 – 100 kW, textile machines power management require novel power electronics solutions. Due to an extraordinary high number of individual drives, the textile machine requires low cost, robust and reliable electric drives with slow, but reliable communication channels. Having the cost reduction as the primary goal, significant research resources are assigned to development of simple converter topologies, new types of electric motors and algorithms for the sensorless speed control.

Among other requirements, electric drives in textile machines are expected to be environmentally friendly; low thermal, acoustic and electromagnetic emissions are forced by government regulations and international standards. The level of the electromagnetic interference strongly depends on the power section layout and might be improved by the introduction of newly developed power switches with spatially distributed lifetime control (CAL). At the same time, the cost reduction of the power switches would give a strong incentive to a more frequent use of electronic controlled drives in textile machine applications.

Power semiconductors are used within the drive converter for accurate control of the energy flow between the power source (i.e. the mains) and the motor. They have extremely short response times and low dissipation. The dramatic developments in IC technology, particularly during the last ten years, have made possible the design of modern, self-protected components, with simple, “low loss” drive characteristics, wide dynamic control range, switching power levels up to the megawatt range, and a direct interface to microelectronic systems.

Fig. 5: *The Intelligent Power Module with integrated power devices and control electronics. IRAMS device interfaces directly to 3.3V and 5V processors.*

In Figs. 5 and 6, IRAMS intelligent power module is presented. It houses almost all of the power electronics and control electronics required to supply and control an induction motor. Device is made by IR, and it interfaces directly to most DSP and RISC controllers. It is of interest to compare the component cost of an inverter made with the IPM and the cost of the equivalent inverter build by using traditional components. The rated power of 1HP was taken as the design example. The intelligent 3-phase module comprises 6 IGBT power switches with associated power diodes, the internal gate drivers and the thermistor. Using the data of Table I, one calculates the total component price as equal to USD 15.095. Traditional bridge converter requires six IGBTs, six fast diodes, one thermistor and three IGBT drivers (one per leg). From Table I the total component cost is USD 14.6313. The comparison shows that the converter with the IPM is, in terms of the component cost, insignificantly more expensive (USD 0.4637 or 3.17%). However, it is obvious that the reduction in the manufacturing cost is more than likely to offset this component price difference. Discrete design requires individual handling, assembly, cooling, fixing and soldering for each of the semiconductor power switches.

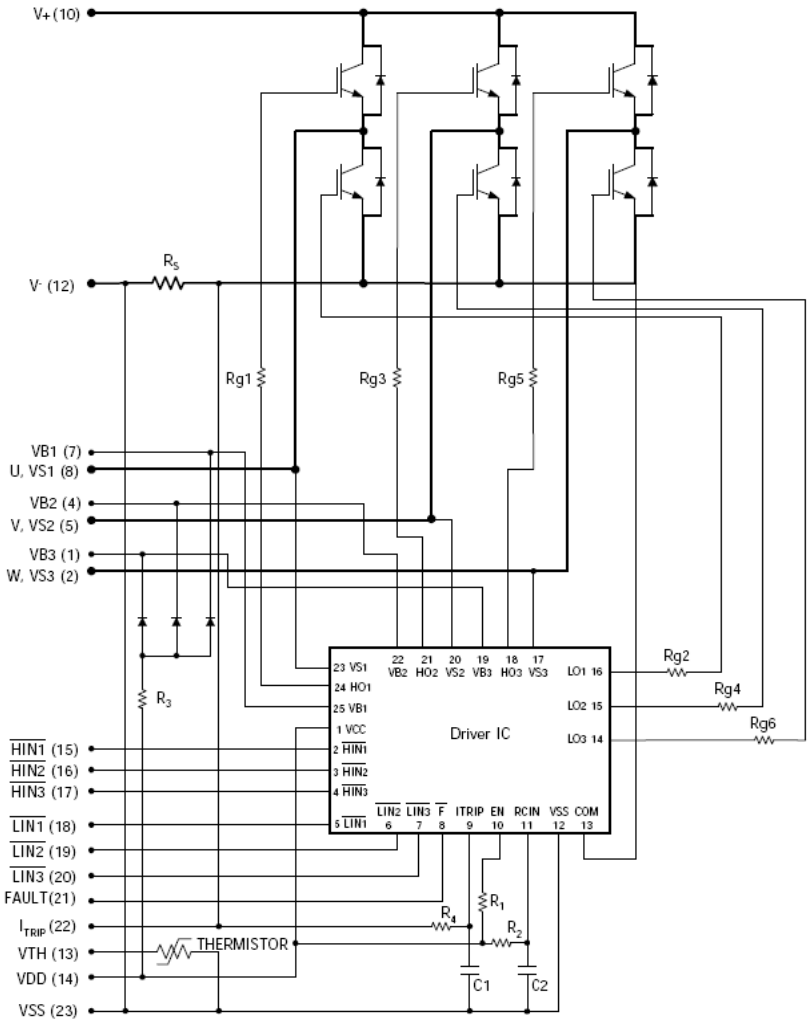

Fig. 6: *Internal schematics of IRAMS Intelligent Power Module.*

TABLE I. COMPONENT PRICES FOR 1HP INVERTER
(reference: www.Digikey.com).

Description	Code	Quantity	Unit price (USD)
3-phase IGBT VSI 6-pack module; integrated drivers & thermistor	IRAMS06UP60A-ND	1,000	10.625
IGBT with anti-parallel diode	IRG4BC10UD	10,000	1.2
Thermistor	KTY135, SOT-23	1,000	0.417
IGBT (no diode)	IRG4BC10U, IRG4BC10U-ND	10,000	0.98305
Fast diode	RS3JB-13	3,000	0.351
Driver, one IGBT pair	IR210STR	2,500	2.07

Commonly adopted way of supplying 500-1000 inverters within a textile machine is the use of a 3-phase transformer with 3x400V 50Hz delta-connected primary winding, and with star-connected secondary winding having 3 x 220V 50 Hz between the terminals. The inverters are having topology given in Fig. 7. Being single-phase load, the inverters are wired to 3x220V 50Hz supply alternatively, in an attempt to equalize average loading of individual phases.

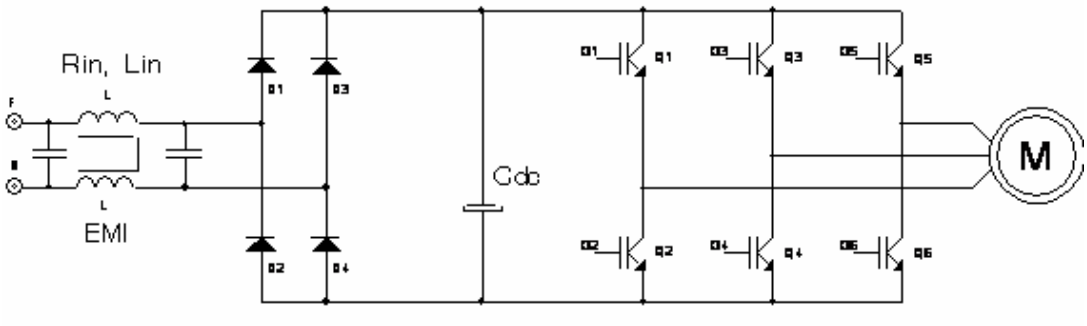

Fig. 7: *Single-phase supplied inverter with the 3-phase output.*

With a diode rectifier at the front end, the converter in Fig. 7 draws a non-sinusoidal, distorted current from the 50Hz mains. The input current waveform is given in Fig. 8. Considering a low rated power of the drive (50-100W in textile machines), the line current distortion caused by a single inverter is not significant. The problem arises from the fact that there are 500-1000 units within each textile machine, having a total rated power of roughly 100 kVA. At this point, low frequency harmonics produced by a passive frond-end converter cannot be tolerated. Harmonic limits for Class A and Class D equipment, according to EN 61000-3-2 is given in Fig. 9. These cannot be met with a passive front-end and P_{nom}>1 HP. Therefore, the power converters such as the one in Fig. 7 should be equipped with active power factor corrector.

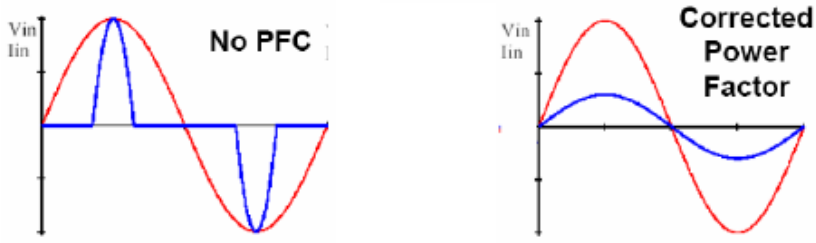

Fig. 8: *Internal schematics of IRAMS Intelligent Power Module.*

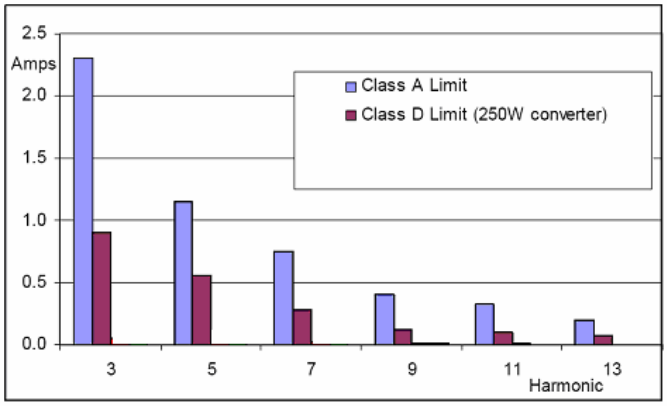

Fig. 9: *Harmonic limits for Class A and Class D equipment.*

In low cost, textile-application induction motor drives, the current sensing becomes a cost sensitive issue. Traditional Hall-effect current sensors, used in high performance drives are too bulky and too costly for a 50W-100W converter that should stay within the cost boundaries of 20-30 EUR. In Fig. 10, the usage of PCB-mount magnetic resistive bridge is illustrated. The stator current flows through the PCB traces below the bridge. Magnetic field caused by the stator current circulation causes a variation of the resistance within the bridge. Subsequently, desired analog signal, proportional to the stator current is derived. Allegro Microsystems manufactured first commercial PCB-mount current sensor for cost-sensitive applications (Fig. 11). It is an open-loop Hall-effect device with the performance quite compatible with the requirements imposed by 50-100W textile drives.

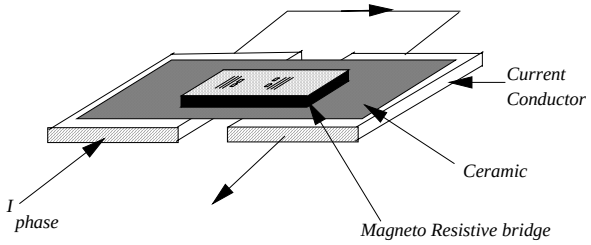

Fig. 10: *Usage of mageto-resistive bridge in current sensing*

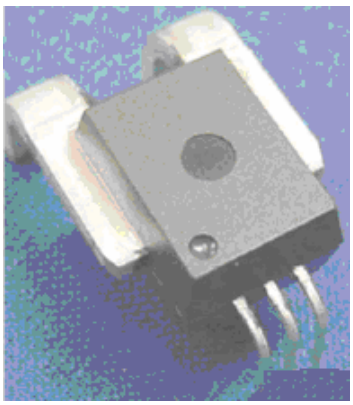

Fig. 11: *Allegro Microsystem ACS750 current sensor for PCB mounting*

7. LARGE POWER, MEDIUM VOLTAGE DRIVE CONVERTERS

Large power AC drives are found in rolling mills, petroleum industry, water supply and many other applications where the rated power exceeds 300 kW and the nominal stator voltage falling into the medium voltage range (2300, 4160 or 6600 V). The main problem in this class of electric drives is the design of controlled three phase variable frequency source in the megawatt range. Until recently, the variable frequency, medium voltage drives were not available due to the absence of high voltage semiconductor power switches. The need for the economic use of energy, miniaturization of electrical systems, and reactive power compensation have been the motives for the revolutionary development of high voltage, high current power semiconductors. For their high power rating, Gate turn-off thyristors (GTO) are considered the main switching device for the construction of multi-level high power three phase inverters. The power losses occurring in the GTO at turn off limit the GTO's normal operating voltage to the range from 30 to 40% of the breakdown voltage, thus limiting the dc-link voltage of a conventional GTO inverter to 1500-2500 V. High-power inverters with dc-link voltage up to 4000 V and existing GTO's cannot be made with conventional six-switch topology. Several converter configurations for the realization of a large capacity inverter with more than 4000 V dc-link voltage are possible. One of them is the six-switch configuration with each of the switching elements being made out of several series connected GTO's. However, the direct series connection method of GTO's has the problem of blocking voltage unbalance during turn-off transient, due to the different turn-off characteristics of each device. Whenever additional equipment is used to overcome this problem, the overall system becomes more complex and expensive. Besides the circuit complexity, a limited switching frequency of GTO's causes large harmonic components of the output voltage and current. Split DC-link voltage three-level converter topologies configurations are being developed for the large capacity inverters, capable of solving the above mentioned problems. Appreciable research effort is devoted to switching rules for a multilevel inverter capable of reducing the commutation stress while maintaining at the same time acceptable ripple amplitude and the spectral content of the output current.

8. LINEAR ELECTRIC SERVO MOTORS

The power converters for linear AC drives do not differ in topology with respect to their counterparts supplying rotary servo actuators. Though, the reactive power of linear AC motors is higher, and their N/A ratio is less favorable when compared to conventional servo motors.

Most of the operations of an automated production machine involve linear translation of machine parts, work pieces and tools. On the other hand, common electric motors are rotary electromechanical converters producing the torque at the output shaft. Transmission mechanisms such as the rack and pinion, ball screw and gear systems convert the rotary into linear motion. Dry friction, backlash, elastic coupling and the torsional resonance intrinsic to all the rotary – to – linear transducers severely limit the servo loop bandwidth.

Relatively large rotational masses constrain the peak acceleration of the system. On the other hand, large equivalent inertia filters out the torque ripple and the quantization excited ± 1 LSB torque chatter, alleviating in such a way the tracking error. Imperfection of the transmission mechanism may be eliminated by the application of direct drive concept with linear electric motors. As the tolls are coupled directly to the motor moving parts, the problems of mechanical resonance exist no more. The absence of rotational masses results in a much larger peak acceleration of the overall system, while the ratio between the peak driving force and the friction increases several time when compared to a servo axis with a rotational actuator.

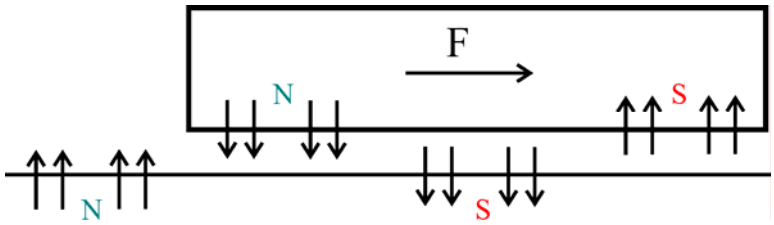

Fig. 12: Linear electrical actuator – principles of operation.

Contemporary linear motors exhibit the top speed of 3-5 m/s and offer the positioning accuracy down to 1 mm. Exceptionally, low inertia stresses the torque ripple and the chatter related problems. Due to the motor imperfection and the finite resolution of the sensors, the driving force exhibits (the same way as the driving torque of a rotational servo motor) high frequency oscillations – the chatter – with an amplitude of 1-3 LSB. The smaller the inertia, the larger the speed and position fluctuations caused by the jitter in the driving force. Dissipativity based approaches to the servo loop synthesis permit significant reduction of the chattering problems, but do not solve completely the torque/force ripple problems. For this reason, the force ripple minimization is one of the main design requirements for linear electric servo actuators.

Modern linear motors are mostly asynchronous or synchronous permanent magnet motors. They have magnetic, hydrostatic or the air bearings. The stiffness coefficient of linear motors (200 N/m) is much better than the stiffness of the fluid power actuators (50 N/m). It is possible to move the weights above 50 kg and attain the driving forces up to 2000 N. Low equivalent inertia of motion control systems employing linear motors results in a speed loop bandwidth of 130-200 Hz and the peak acceleration well above 100 m/s^2.

When designing the power converters for linear AC drives, similar design rules apply, and the only difference is an elevated reactive power and higher stator currents.

9. CONCLUSION

Power converters in motion control systems are accountable for converting the electric energy obtained from the primary source and adjusting the frequency and the amplitude of the output voltages and currents. The output quantities are suited according to the needs of the electric servo motor. The elements of motion control systems, and in particular the power electronic units became commodity products, their cost becoming one of the main issues. At the same time, the energy efficiency, a higher peak-to-rated power ratio, the energy quality and the regenerative braking imposed new standards to power converter topologies and solutions.

This article outlines the impact of recent trends in motion control systems on the power converter topologies used in electric drives. Both high volume, low performance applications and the cutting edge applications are pointed out, including as well the insight into most recent power electronics products and solutions, offered by leading PE manufacturers. It is found that the recent trends in motion control system and introduction of low power, electronic controlled drives in textile machines and similar applications deeply affect the topology of power electronic devices and create the need for new PE solutions. New drive applications require the drive power converters with a higher peak-to-RMS ratio, much longer life time and storage time, and built-in safety features such as the anti-free-wheeling. Power factor correction and regenerative braking becomes common requirement, while the proper thermal management becomes main competitive feature. Although with a mature technology and the basic problems already solved, power converters for electrical drives are still in the intense development phase. Numerous control problems and the problems of energy conversion yet need to be solved. The said problems will attract the attention of many young engineers world-wide at Universities, research laboratories and companies involved in controlled electrical drives development and production.

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DISCRETE-TIME QUASI-SLIDING MODE CONTROL SYSTEMS - Part I

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Abstract – *This paper is dedicated to the digitally controlled variable structure systems operating in sliding mode. In the introductory part of the paper, the significance of such systems is emphasized. A brief attention is paid to the continuous-time sliding mode control systems, as an initial theoretical background for developing the discrete-time counterpart. The major part of the paper is devoted to the digital sliding modes and the control algorithms for their realization. Two well-known control algorithms are described shortly. First of them provides zigzag motion around the sliding hypersurface, whereas the second one ensures digital sliding mode.*

Keywords: variable structure systems, sliding modes, quasi-sliding modes, digital sliding modes.

1. INTRODUCTION[1]

A quarter of century has passed since the beginning of the intensive research of digital sliding modes, as a logical extension of the development of the continuous-time sliding mode control systems. The exceptional properties of the sliding mode control systems (the theoretical invariance to disturbance actions, *a priori* knowledge of the transient process, the reduced order dynamics, the linearization of nonlinear systems, the weak requirements to plant parameter identification, the simplified design of control system, the compatibility with power electronics switching elements, etc.), on one hand, and the significant development of devices and systems for digital signal processing, such as microprocessors, on the other hand, have induce the interest in research of the possibilities and the methods of digital sliding mode realization. The investigations have shown that digital sliding modes have some specialties. First, even in ideal conditions, the digital sliding modes do not have the theoretical invariance to the disturbances, because they are not subjected to the discretization process. Besides, the sliding mode can not be realized, but only the *quasi-sliding mode* arises. However, systems with digital quasi-sliding modes retain the significant robustness property, giving them a considerable advantage with respect to the conventional control algorithms. A review of the evolution of these systems, basic definitions and notions as well as directions for further research are given in this paper, from the viewpoint of the one of the pioneers and the active participants in the digital sliding mode development. A dominant part of the paper is dedicated to the algorithms, which have been developed by the authors of this paper. Besides the theoretical contributions, the paper also presents experimental results obtained from the laboratory prototypes.

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The paper is composed of two parts. The first part is organized as follows. The basic principles of sliding modes in the continuous-time variable structure control systems, as a framework for development of the digital quasi-sliding modes, are given in the section 2. The notion of digital quasi-sliding mode is introduced in the section 3, followed by the basic definitions and the detailed description of two control algorithms. The second part of this paper presents some novel control algorithms for the digital sliding mode control systems performance improvement.

2. THEORETICAL FUNDAMENTALS OF THE SLIDING MODE CONTROL SYSTEMS

Let the dynamic system be modeled as

$$\dot{\mathbf{x}}(t) = (\mathbf{A} + \Delta\mathbf{A})\mathbf{x}(t) + (\mathbf{B} + \Delta\mathbf{B})\mathbf{u}(t) + \mathbf{D}\mathbf{v}(t)\,, \qquad (1)$$

where: $\mathbf{x} \in \Re^n$ - is the state vector, $\mathbf{u} \in \Re^m$ - is the control vector, $\mathbf{v} \in \Re^l$ - is the exogenous disturbance vector, $\mathbf{A} \in \Re^{n\times n}$, $\mathbf{B} \in \Re^{n\times m}$, $\mathbf{D} \in \Re^{n\times l}$ are the nominal values of the state, control and disturbance input matrices, respectively. The eventual parameter disturbances are represented by the matrices $\Delta\mathbf{A} \in \Re^{n\times n}$, $\Delta\mathbf{B} \in \Re^{n\times m}$. It is assumed that all the disturbances are bounded. The control task is to drive the system state, described by (1), from an arbitrary initial position $\mathbf{x}(0)$ into the desired final state $\mathbf{x}(t_f)$ by applying appropriate control signal $\mathbf{u}(t)$. Let the matrix pair (**A**,**B**) be fully controllable and all state coordinates be accessible for measuring.

System model (1) can be transformed into the form

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) + \mathbf{d}(t)\,, \qquad (2)$$

where $\mathbf{d}(t) = \Delta\mathbf{A}\mathbf{x}(t) + \Delta\mathbf{B}u(t) + \mathbf{D}\mathbf{v}(t)$ is the overall disturbance vector, which incorporates parameter and external disturbances. It is supposed that the system (1) fulfills the so called *matching conditions* [1]:

$$rank\left[\mathbf{B} \,\vdots\, \Delta\mathbf{A} \,\vdots\, \Delta\mathbf{B} \,\vdots\, \mathbf{D}\right] = rank\mathbf{B}\,. \qquad (3)$$

In that case, system motion in the sliding mode is *completely invariant* to the disturbances.

Sliding mode is organized in the following way:

1) m hypersurfaces (hyperplanes) are chosen in the state space, described by

$$\mathbf{g}(t) = \mathbf{C}\mathbf{x}(t); \mathbf{g} \in \Re^m; \mathbf{C} \in \Re^{m\times n}\,, \qquad (4)$$

each of which crosses the state space origin $\mathbf{x}=\mathbf{0}$;

2) control vector $\mathbf{u}(t)$ is determined, which provides sliding motion along the intersection of all hypersurfaces.

Control should ensure reaching the intersection of the hypersurfaces and the subsequent sliding motion along the intersection. There are four possible sliding hypersurface reaching strategies [2]:

(1) *fixed order switching scheme*, where hypersurfaces are reached in a prescribed order with corresponding sliding modes on them,

(2) *free order switching scheme*, where any hypersurface is reached first and afterwards the others in natural order, with associated sliding modes,

(3) *eventual sliding mode scheme,* where only the intersection of all hypersurfaces is necessarily reached,

(4) *decentralized control*, where the system is treated as *m* single input subsystems, each having a scalar hypersurface with its associated sliding mode.

In each case, sliding motion in its final stage takes place on the intersection of *m* hypersurfaces, which is described by differential equation of (*n*-*m*)th order [4].

If the condition (3) is fulfilled, the easiest way of sliding mode realization on the intersection of all hypersurfaces is to employ decentralized control, where control of the multivariable system is transformed to the control of *m* scalar subsystems, which is to be the case in further discussion. In this strategy, the interactions of the other subsystems are treated as the disturbances, which should be neutralized by the control action. Hence, the control problem is now reduced to the design of the scalar control $u(t)$ in the system

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{b}u(t) + \mathbf{d}(t)\,, \tag{5}$$

which provides a stable sliding mode on the hypersurface

$$g(t) = \mathbf{c}\mathbf{x}(t); \mathbf{c} \in \Re^{1\times n}\,. \tag{6}$$

A stable sliding mode appears if the conditions [3],

$$\lim_{g(t)\to 0^+} \dot{g}(t) < 0; \quad \lim_{g(t)\to 0^-} \dot{g}(t) > 0\,, \tag{7}$$

are satisfied.

The conditions (7) are the sliding mode existence conditions, locally defined in the vicinity of the hypersurface $g(t)=0$. They may be interpreted as a requirement for the system trajectories to be oriented towards the hypersurface, from both sides. Since the system trajectories are directed towards the hyperplane, once they reach the hyperplane, they cannot leave it anymore and continue to slide along the hyperplane towards the equilibrium. Therefore, system motion in the sliding mode may be axiomatically identified with the hyperplane equation (6). This means that system motion is insensitive to system parameters and disturbances, and only depends on the parameter of the vector **c**. If the elements of the vector **c** in the relation

$$g(t) = \mathbf{c}\mathbf{x}(t) = 0\,, \tag{8}$$

representing differential equation of (*n*-1)th order in the state space, are chosen to be the coefficients of Hurwitz polynomial, the system trajectories will slide along the hypersurface towards the zero equilibrium state.

Since the system trajectories from the different sides of the hypersurface (8) are directed to each other, the sliding control must be a discontinuous function of the state coordinates, that is

$$u(t) = \begin{cases} u^+(t) & \text{for } g(t) > 0, \\ u^-(t) & \text{for } g(t) < 0, \end{cases} \tag{9}$$

which commutates with an infinite switching frequency. Differential equation (5) has discontinuous right-hand side, so the Lipschitz conditions for existence and uniqueness of the solution are violated. This problem is overcame by employing *regularization technique*, using *Filippov method* or *equivalent control method.* The latter method is dominant in sliding mode control theory, which is based on the proposition that motion velocity vector is always tangential to the sliding hypersurface (8), that is, both the conditions (8) and

$$\dot{g}(t) = \mathbf{c}\dot{\mathbf{x}}(t) = 0\,, \tag{10}$$

are simultaneously fulfilled. Replacing (5) in (10) and solving the resulting relation with respect to $u(t)$, give the *equivalent control*

$$u_{eq}(t) = -(\mathbf{cb})^{-1}\left[\mathbf{cA}x(t) + \mathbf{cd}(t)\right], \tag{11}$$

whose substitution into (5) yields the differential equation

$$\dot{\mathbf{x}}(t) = [\mathbf{A} - \mathbf{b}(\mathbf{cb})^{-1}\mathbf{cA}]\mathbf{x}(t) + [1 - \mathbf{b}(\mathbf{cb})^{-1}\mathbf{c}]\mathbf{d}(t)\,, \tag{12}$$

which describes system motion in the sliding mode.

The control only serves to provide sliding conditions and formally is not present in the sliding mode equation. The sliding mode motion is generated by the equivalent control, which may be physically interpreted as a mean value of the discontinuous control. Therefore the following relation must hold

$$u^-(t) < u_{eq} < u^+(t)\,. \tag{13}$$

Unfortunately, the equivalent control cannot be obtained in the real sliding mode applications, but only serves in the mathematical description of such motion. However, a lot of control algorithms employ equivalent control as a component of the real control, which is usually defined as

$$u(t) = u_{eq}(t) + u_{sw}(t)\,, \tag{14}$$

where u_{sw} is a discontinuous control component. This control component is commonly used in the form

$$u_{sw} = M\,\mathrm{sgn}(g); M = \left\{\sigma; \alpha\left|\mathbf{x}\right|\right\}; \sigma, \alpha = const > 0\,. \tag{15}$$

The discontinuous control component should provide reaching of the hyperplane (5) from an arbitrary initial state as well as the robustness with respect to the disturbances. In (15), two possibilities of the discontinuous control component are suggested: the relay $M = \sigma$ and the quasi-relay $M = \alpha\left|\mathbf{x}\right|$. The relay control component gives powerful control signal and better robustness, but may induce the chattering phenomenon - undesirable oscillations due to unmodeled dynamics, such as time delays present in actuators or neglected inertial dynamics. The quasi-relay component does not produce chattering in the steady state, but the control system is less robust to disturbances.

Due to the previous discussion it may be noticed that the system motion comprises two phases: reaching phase and sliding motion phase. Generally, the reaching phase lasts shortly, followed by the permanent sliding mode, if there is not a change of disturbance magnitude. The system will effectively finalize the reaching phase if the following condition [4] is satisfied

$$g\dot{g} < 0\,, \tag{16}$$

which is obtained by using direct Lyapunov method, with the Lyapunov function candidate $V(t) = 0.5g^2(t)$, where the sliding hypersurface represents the equilibrium state.

The control concept that governs motion in the reaching phase as wellis proposed in [2]. The general form of reaching law may be defined by

$$\dot{g}(t) = -q\,\mathrm{sgn}(g) - kf(g). \quad (17)$$

Based on the selection of the parameters q and k, there are several reaching laws, and several control algorithms, consequently (se [2] for details).

The control is determined using (17). The system model (5) is replaced in the total time derivative of the equation (6). The obtained relation is compared with the right hand side of (17), yielding the required control as

$$u(t) = -(\mathbf{cb})^{-1}[\mathbf{cAx}(t) + \mathbf{cd}(t) + q\,\mathrm{sgn}(g) + kf(g)]. \quad (18)$$

The substitution of (18) into (5) gives the differential equation that describes system motion. The most interesting case is the power rate reaching law

$$\dot{g}(t) = -k|g(t)|^{\beta}\,\mathrm{sgn}(g); 0 < \beta < 1, \quad (19)$$

when the hyperplane is reached in finite time. System trajectories softly lends onto the sliding hyperplane, which eliminates the chattering phenomenon.

3. DISCRETE-TIME QUASI-SLIDING MODE

The introduction of discrete-time signal processing in the system (5) requires evaluation of the discrete-time model. One of them may be defined as

$$\delta\mathbf{x} \overset{\Delta}{=} \frac{\mathbf{x}(k+1) - \mathbf{x}(k)}{T} = \mathbf{A}_{\delta}\mathbf{x}(k) + \mathbf{b}_{\delta}u(k) + \mathbf{d}_{\delta}(k), \quad (20)$$

that is

$$\mathbf{x}(k+1) = \mathbf{A}_d\mathbf{x}(k) + \mathbf{b}_d u(k) + \mathbf{d}_d(t), \quad (21)$$

where

$$\mathbf{A}_d = e^{\mathbf{A}T} = \mathbf{I} + T\mathbf{A}_{\delta}; \mathbf{b}_d = \int_0^T e^{\mathbf{A}T}\mathrm{d}\tau = T\mathbf{b}_{\delta};$$

$$\mathbf{d}_d = \int_0^T e^{\mathbf{A}t}\mathbf{d}((k+1)T - \tau)\mathrm{d}\tau = T\mathbf{d}_{\delta}(\mathrm{k}).$$

Relation (6) becomes

$$g(k) = \mathbf{c}_d\mathbf{x}(k). \quad (22)$$

Control algorithms for the sliding modes organization in digital systems may be classified in various manners. No matter of the applied control algorithm, it is not possible to realize motion exactly on the sliding hypersurface, even in the case of the nominal system without disturbances. The reason is the inherent time delay, due to the discretization process with period (T). Considering only the nominal systems, and observing the system motion in the discrete time instants, control algorithms may be divided into two groups. The first group represents the control algorithms with a zigzag motion in the vicinity around the sliding hyperplane, fig. 1, trace A. The second group includes the control algorithms that forces the system state to be exactly on the sliding hypersurface in the sampling instants, fig. 1, trace B. The intersample motion will deviate from the sliding hypersurface and will be confined into some vicinity of the hypersurface, due to the continuous-time nature of the plant and a D/A converter behaving as a zero-order hold circuit. In both cases, the obtained motion differs from the sliding mode in the authentic sense, and it has been referred to as quasi-sliding mode [6], or pseudo-sliding mode [10]. In order to distinguish the mentioned realizations of the quasi-sliding mode, the first type (fig. 1A) will be labeled as the zigzag regime, and the second (fig. 1B) as the digital sliding mode.

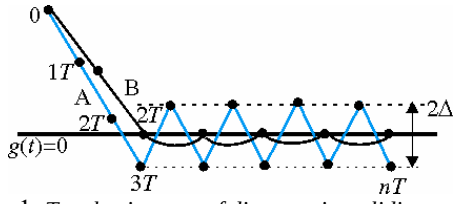

Fig. 1. *Two basic types of discrete-time sliding mode:* A-*zigzag motion regime,* B- *digital sliding mode.*

3.1 Zigzag motion regime

Investigations of the zigzag motion have been initiated in [5], [6], and continued in [8]-[12], [3], and others. The special approach to the zigzag motion has been established in [13], with organization of the so called *invariant sliding sector*. A more detailed review of the investigations in the discrete-time sliding mode control systems is given in [7].

The zigzag motion regime may be defined as follows:

Definition 1. *Zigzag regime is a motion in a vicinity of the sliding hypersurface g=0 that once the system trajectories first crosses the switching hyprrsurface it will cross it again optionally in every sampling time and stay in the predefined region* $|g(kT)| \le \Delta$.

The necessary condition for the appearance of a zigzag motion was formulated in [5], [6], in the form of

$$g(kT)\Delta g(kT) < 0; \Delta g(kT) = g((k+1)T) - g(kT) \quad (23)$$

but the necessary and the sufficient conditions are given in [15], [8], [14], [11], respectively as:

$$|g((k+1)T)| < |g(kT)|; \quad (24a)$$

$$\Delta g(kT)\,\mathrm{sgn}(g(kT)) < 0, \quad [g((k+1)T) + g(kT)]\,\mathrm{sgn}((g(kT)) \ge 0; \quad (24b)$$

$$g^2((k+1)T) - g^2(kT) < 0; \quad (24c)$$

$$|g((k+1)T)g(kT)| < g^2(kT). \quad (24d)$$

3.1.1 Gao's algorithm

Gao et al., [3], have proposed the discretized version of the reaching law (17) as:

$$\Delta g(k) = -qTg(k) - \varepsilon T\,\mathrm{sgn}(g(k)), q, \varepsilon, (1 - qT) > 0. \quad (25)$$

This reaching law ensures the necessary and the sufficient conditions for the existence of the zigzag motion regime. The system trajectories are constrained into a vicinity of the sliding hyperplane, which is crossed in each sampling period. The width of the zigzag region is defined by

$$\Delta = 2\varepsilon T/(1 - qT). \quad (26)$$

The control is determined in the following manner: according to (21) and (22), $g(k)$ and $g(k+1)$ are expressed, forming the difference $\Delta g(k)$, whose right hand side is equalized with the right hand side of (25), giving the control term

$$u(k) = -(\mathbf{c}_d\mathbf{b}_d)^{-1}\mathbf{c}_d\mathbf{A}_d\mathbf{x}(k) + (\mathbf{c}_d\mathbf{b}_d)^{-1}[(1 - qT)g(k) - \varepsilon T\,\mathrm{sgn}(g(k))]. \quad (27)$$

The substitution of (27) in (21) yields the equation of discrete-time system motion

$$\mathbf{x}(k+1) = \mathbf{A}_d\mathbf{x}(k) - \mathbf{b}_d(\mathbf{c}_d\mathbf{b}_d)^{-1}[\mathbf{c}_d\mathbf{A}_d\mathbf{x}(k) - (1-qT)g(k) + \varepsilon T \operatorname{sgn} g(k)]. \quad (28)$$

The motion in the zigzag regime is depicted in fig. 1A, where the width of the zigzag region depends on the parameters *T, q* and ε, in compliance with (26).

In [12] has introduced a time-varying sliding hypersurface and additional integral action, which has improved the system performance, by reducing the zigzag region.

3.2. Digital sliding mode

The digital sliding modes have been introduced in [15], and [16], and further investigated in [17]-[21], and others.

The digital sliding mode is defined as follows:

Definition 2. *The digital sliding mode is the such motion where*

$$g(k) = 0 \ , \forall k > k^* < \infty. \quad (29)$$

For the sake of simplicity, it is assumed that the disturbances can be detected and compensated (which will be presented later). Hence, the nominal system (21) without disturbances is considered.

According to definition 2, the digital sliding mode exists if the following two conditions hold:

$$\begin{matrix} g(k) = \mathbf{c}_d\mathbf{x}(k) = 0, \\ g(k+1) = \mathbf{c}_d\mathbf{x}(k+1) = 0: \end{matrix} \Leftrightarrow \begin{matrix} g(k) = g(k+1) = 0, \\ \forall k > k^* \in N_o \subset R^+. \end{matrix} \quad (30)$$

Replacing $\mathbf{x}(k+1)$ from (21), with zero disturbance term, in $g(k+1)=0$, and taking into account $g(k)=0$, gives the relation from which *the digital equivalent control* may be determined as

$$u_{eq}(k) = -(\mathbf{c}_d\mathbf{b}_d)^{-1}\mathbf{c}_d\mathbf{A}_d\mathbf{x}(k). \quad (31)$$

Its employment in (21) yields the digital sliding mode dynamics

$$\mathbf{x}(k+1) = [\mathbf{A}_d - \mathbf{b}_d(\mathbf{c}_d\mathbf{b}_d)^{-1}\mathbf{c}_d\mathbf{A}_d]\mathbf{x}(k). \quad (32)$$

It may be noticed from (32) that the appropriate choice of $\mathbf{c}_d$ guarantees system stability with the desirable dynamics.

The equivalent control (31) is determined under the condition that the system state is on the sliding hyperplane in the sampling instant and remains on it in future. However, it is necessary to secure the system state to arrive on the sliding hyperplane from an outside position exactly in the sampling instant. According to the requirement $g(k+1)=0$, $\forall g(k)$, it may be written

$$\mathbf{c}_d\mathbf{A}_d\mathbf{x}(k) + \mathbf{c}_d\mathbf{b}_d u(k) = 0, \quad (33)$$

which gives required control identical to the equivalent control (31). Therefore, the control that is necessary for the digital sliding mode realization is unique in both reaching and sliding phase. This is a linear control, which differs substantially from the zigzag regime concept and the continuous-time sliding mode principle.

However, this control is rarely used in practice. The main reason for this is the requirement for the width of the quasi-sliding region to be as small as possible and to be reached in minimum time. This demands a very small discretization period, which results in very large control effort at the beginning of the reaching phase. A more realistic approach is to allow reaching with maximum permitted speed, regardless of the discretization period, and to realize the sliding mode with as small as possible discretization period, dictated by digital hardware. This concept is used in [20] and [21]. The latter approach will be presented in details.

3.2.1. Golo's algorithm

This control algorithm has been published in [21]. It is based on the fusion of soft reaching algorithm [15], which is actually a kind of *dead-beat algorithm*, and reaching law (27) [3].

Herein, the reaching law is defined by the relation

$$\delta g(k) = -\min\begin{Bmatrix} T^{-1}|g(k)|, \\ \sigma + q|g(k)| \end{Bmatrix} \operatorname{sgn}(g(k)), \sigma >, q \geq 0, \quad (34)$$

where

$$\delta g(k) \overset{\Delta}{=} \frac{g(k+1) - g(k)}{T} = \mathbf{c}_\delta(T)\delta\mathbf{x}(k), \quad (35)$$

using the discrete-time model (20).

It can be easily proved that the necessary quasi-sliding mode existence conditions (23) is satisfied by this reaching law.

If $\delta\mathbf{x}(k)$ from (20) is applied in (35), and the obtained right hand side of (35) is equalized with (34), the required control law, under the condition $\mathbf{c}_\delta(T)\mathbf{b}_\delta(T) = 1$, may be extracted as

$$u(k) = -\mathbf{c}_\delta\mathbf{A}_\delta\mathbf{x}(k) - \min\begin{Bmatrix} T^{-1}|g(k)|, \\ \sigma + q|g(k)| \end{Bmatrix} \operatorname{sgn}(g(k)). \quad (36)$$

As it can be seen, the first term of the control (36) is the equivalent control (31) that is linear. Notice that in (27) the equivalent control is present also. The second component is nonlinear, in the first place because of the presence of the function "$\min\{\bullet\}$". When the system state is far from the sliding hyperplane, the active component is $\sigma\operatorname{sgn}(g(k)) + qg(k)$, which, in the case of $q = 0$, becomes pure relay type $\sigma\operatorname{sgn}(g(k))$. Hence, the selection of the parameter σ defines dominant part of the reaching phase. When the system state enters certain region around the hyperplane, the linear component $T^{-1}g(k)$ is activated. Therefore, final stage of the reaching phase is governed by the linear control

$$u_k(k) = -\mathbf{c}_\delta\mathbf{A}_\delta\mathbf{x}(k) - T^{-1}g(k). \quad (37)$$

Using (37) in (21) gives $g(k+1) \equiv 0$, which means that the system state arrives onto sliding hyperplane precisely in one discretization instant, i.e. in one step. The further motion is only governed by the equivalent control, since $g(k)=0$ in (37). In that way, the motion depicted in the fig. 1B is established.

For the completion of the presented algorithm it is necessary to determine elements of the vector $\mathbf{c}_\delta$. There are several methods. The following procedure is proposed in [21].

Let the eigenvalues of the system (20), in a digital sliding mode, be real and distinct, laying inside the unit disc in the complex *z*-plane. They are defined by

$$\delta_i(T)=\frac{e^{-\alpha_i T}-1}{T},\qquad \begin{matrix}\alpha_i>0, i\neq j, \alpha_i\neq\alpha_j,\\ i,j=1,2,...,n-1.\end{matrix} \tag{38}$$

The elements of the vector $\mathbf{c}_\delta$ are calculated according to the transformed vector [21]

$$c_i=\frac{1}{(i-1)!}\frac{\mathrm{d}^{i-1}\prod_{j=1}^{n-1}(\delta-\delta_j(T))}{\mathrm{d}\delta^{i-1}}\Big|_{\delta=0}, \tag{39}$$

using the relation

$$\mathbf{c}_\delta(T)=\begin{bmatrix}c_1 & c_2 & ... & c_n & 1\end{bmatrix}\mathbf{P}_1^{-1}, \tag{40}$$

where $\mathbf{P}_1$ is a transformation matrix

$$\mathbf{P}_1=\mathbf{M}_c\begin{bmatrix}a_2 & a_3 & ... & a_n & 1\\ a_3 & & & 1 & \\ . & . & . & . & . \\ a_n & 1 & & \mathbf{0} & \\ 1 & & & & \end{bmatrix}; \tag{41}$$

with $\mathbf{M}_c$ being the controllability matrix of the system (20), and $a_i, i=2,...n$ being the coefficients of the system (20) characteristic polynomial

$$\det[\delta\mathbf{I}-\mathbf{A}_\delta]=\delta^n+a_n\delta^{n-1}+...+a_2\delta+a_1. \tag{42}$$

The robustness of the proposed control system is rigorously analyzed in [21]. It is demonstrated that the system is more robust if the discretisation period is smaller. If the discretization period tends to zero, $T\to 0$, the system will become invariant to the disturbances, which is the property of the continuous-time sliding mode control systems.

4. CONCLUSION

The basic elements of the sliding mode control theory are given in this paper. First, the continuous-time sliding mode control concept is emphasized, as a theoretical framework for the development of the quasi-sliding modes in digital control systems. After a brief review of the discrete-time sliding mode evolution chronology, the two dominant concepts are presented: the zigzag motion regime and the digital sliding mode. Two control algorithms within these concepts (Gao's and Golo's) are presented.

In the part two of this paper, methods for the improvement of Golo's algorithm as well as disturbance estimation and compensation problems will be considered and experimentally verified on the positioning servo-mechanism with dc motor.

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DISCRETE-TIME QUASI-SLIDING MODE CONTROL SYSTEMS -Part II

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Abstract – *This paper is dedicated to the improvement of the performances of the discrete-time variable structure control systems operating in the digital sliding mode. A new control algorithm is presented, which improves system tracking capabilities in the case of complex referent signals, as well as robustness to the disturbance actions. Also, a recently developed disturbance compensator, based on digital sliding modes, is briefly described. The combination of the proposed controller and the disturbance compensator results in a high-quality control system. The characteristics of the composed control system are illustrated on the example of a servo-system with a DC motor, by digital simulation and experimentally obtained results from the laboratory prototype.*

Keywords: ***variable structure systems, quasi-sliding modes, digital sliding modes, integral control, disturbance compensator.***

1. INTRODUCTION[1]

The first part of this paper [1] has presented theory fundamentals of the discrete-time variable structure control systems operating in the digital quasi-sliding mode. It has been shown that there are a number of approaches to the organization of such motion. Considering nominal system without disturbances, it has been concluded that the term "quasi-sliding mode" comprises two different types of motion in a vicinity of the sliding hyperplane. The first type has been named as a *zigzag motion regime*, whereas the second is *a digital sliding mode*. The zigzag regime is characterized by the obligatory crossing of the sliding hyperplane each discretization period [2] or nonobligatory crossing [3]. The digital sliding mode ensures motion, which coincides with the sliding hyperplane in the discretization instants [4], [12]. Due to a continuous-time plant and the presence of D/A converters, this overall motion essentially take place also in a vicinity of the sliding hyperplane. Therefore, the term *"quasi-sliding mode"* mutually addresses both motion types.

According to the analysis in [1], the digital sliding mode control algorithms are widely accepted for the major class of the control problems, since control signals need not to be discontinuous, which implies absence of the chattering – undesirable phenomenon in the variable structure systems. This is the reason why the special attention in [1] has been paid to Golo's algorithm [4], as the most suitable for the digital sliding modes. However, this algorithm has its drawbacks, such as limited capabilities in tracking of the complex referent signals and in rejection of the complex disturbances.

A method for the performance improvement of Golo's algorithm, by means of introduction of an additional integral control component, is described in the second section. In the third section attention is focused on the estimation and the compensation of the disturbances, which increase robustness. A disturbance compensator proposed in [5] is presented. An example of the application of the described algorithms in the synthesis of a high-quality DC motor based servo-system is given in the forth section. The simulation and the experimental results illustrate the performances of the considered control algorithms.

2. MODIFIED GOLO'S ALGORITHM

Let the control system be described by the model

$$\delta\mathbf{x} \overset{\Delta}{=} \frac{\mathbf{x}(k+1)-\mathbf{x}(k)}{T} = \mathbf{A}_\delta \mathbf{x}(k) + \mathbf{b}_\delta u(k) + \mathbf{d}_\delta(k); \quad (1)$$
$$\mathbf{A} \in \Re^{n\times n}; \mathbf{b} \in \Re^{n\times 1}; \mathbf{x} \in \Re^{n\times 1}; u \in \Re; \mathbf{d} \in \Re^{n\times 1},$$

where $\mathbf{x}(k)$ is the system state vector, which elements are tracking error signal and its n-1 time derivatives. The control signal $u(k)$ is given by

$$u(k) = u_{eq} - \Phi(k)\,\mathrm{sgn}(g(k)); \Phi(k) = \min\{v(k), w(k)\},$$
$$v(k) = T^{-1}|g(k)|, w(k) = \sigma + q|g(k)|; \sigma, T > 0, q \geq 0, \quad (2)$$
$$u_{eq} = -\mathbf{c}_\delta \mathbf{A}\mathbf{x}(k);$$

synthesized by virtue of Golo's algorithm [4], which ensures the digital sliding mode on the hyperplane

$$g(k) = \mathbf{c}_\delta \mathbf{x}(k) = [c_{\delta 1} \quad c_{\delta 2} \quad \ldots \quad c_{\delta n}]\mathbf{x} = 0, \quad (3)$$

in the nominal system. In (2) $u_{eq} = -\mathbf{c}_\delta \mathbf{A}\mathbf{x}(k)$ denotes digital equivalent control, T is the discretization period, and σ, q are the parameters defining the reaching dynamics of the hyperplane (3).

In continuous-time variable structure control systems, where sliding mode is organized and all elements of the vector $\mathbf{x}$ are measurable, it is possible to obtain the perfect tracking of the referent signals $r(t) = \sum_0^{n-1} r_p t^p$. If the only first m elements of the vector $\mathbf{x}$ are measurable, the tracking capability is expressed by the steady-state error, defined by the relation [6]:

$$e(\infty) = \begin{cases} 0 \text{ za } p < m, \\ m!\dfrac{c_{m+1}}{c_1} r_p \text{ za } p = m, \\ \infty \text{ za } p > m. \end{cases} \quad (4)$$

The relation (4) is approximately valid for the digital systems with Gao's type zigzag regime [2].

Since the control system (1)-(3) in the final phase of reaching becomes linear [1], its capabilities in tracking of typical referent signals, as well as steady-state error, depends

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on the system type number and DC gain. The variable structure control systems in sliding mode allow larger gains with respect to the conventional control systems, hence the system (1)-(3) may only have smaller steady-state error than the conventional solutions. The considered system with type number one will have zero error in the case of the step references, and the constant error in the case of the ramp reference signals. Therefore, the control system (1)-(3) with type number one is unable of tracking the parabolic referent signals, which is the standard requirement in high-quality servo-systems.

Continuous-time sliding mode control systems, in which the matching conditions [7] are fulfilled, exhibit invariance to parameter and external disturbances, whereas in quasi-sliding mode systems, the invariance property is reduced to a significant robustness. In the system (1)-(3), which is linear in the steady-state, its steady-state error due to external disturbances may be determined in the classical way. As is well known, the disturbance rejection capabilities depend on the number of the integrating elements that are in the front of the disturbance entry point. If the controller does not include the integral action, in the case of the constant disturbance, the steady-state error will occur, which is inversely proportional to DC gain. If the controller posses at least one pure integrator, the steady-state error will disappear.

Since the controller (2) does not have an integral action, the steady-state error will arise under the action of external disturbances. According to this drawback, a question emerges: is it possible to improve the performances of the system (1)-(3) by the introduction of an integral action and how to do that?

The investigations considering this question has started from the fact that sliding mode control systems are robust to the introduction of the proportional-integral (PI) action (with appropriate parameters) between the variable structure controller and the plant. Such system augmentation does not violate the sliding mode existence conditions. Furthermore, it may even make them less conservative. This idea has been originally applied in [8], practically tested in [9] and thoroughly explained in [10]. The continuous-time sliding mode control has been used in the cited papers. The same approach has been applied to the digital sliding mode control systems in [11], [12] [13], and rigorously analyzed in [14].

The investigations in [13], [14] have shown that the simple introduction of PI action between the controller and the plant induces an undesirable effect: an overshoot arises in the system response in the case of abrupt changes of the reference signal. This is caused by the strong nonlinear term $\sigma\,\mathrm{sgn}(g(k))$ in control (2), which guaranties fast reaching. This signal saturates the integrator in the reaching phase producing integrator windup in the eventual reaching. This problem may be overcome if the variable structure principle is applied to the introduced PI action, which is a constitutive part of the digital controller. Since Golo's algorithm posses a linear control mode, this is the most convenient phase to activate the introduced integral action. Therefore, the modified Golo's control algorithm assumes the following form [13]:

$$u(k) = u_{PI}(k) = u_s(k) - u_i(k), \tag{5}$$

$$u_s(k) = u_{eq} - \Phi(k)\,\mathrm{sgn}(g(k)), u_{eq} = -\mathbf{c}_\delta \mathbf{A}_\delta \mathbf{x}(k), \tag{6}$$

$$u_i(k) = \begin{cases} 0 & \text{if } \Phi(k) = w(k), \\ hg(k) + u_I(k-1)) & \text{if } \Phi(k) = v(k), \end{cases} \tag{7}$$

$$0 < h < 1/T\,. \tag{8}$$

However, even this control may lead to a small overshoot. The complete overshoot elimination is obtained if the integral component is chosen as in [14]

$$u_I(k) = \begin{cases} 0 & \text{if } \Phi(k) = w(k) \vee |x_2| - \rho > 0; \\ hg(k) + u_I(k-1) & \text{if } \Phi(k) = w(k) \wedge |x_2| - \rho < 0; \end{cases}$$
$$0 < \rho < 1, \tag{11}$$

with the appropriate selection of ρ.

The control law (11), applied to a DC motor based servo-system, ensures tracking of parabolic signals, $r(t) = r_p t^2/2$, with the error [14]:

$$e(\infty) = \frac{r_p T}{bc_{\delta 1}} \frac{a}{h}, \tag{12}$$

where a is the pole of DC motor transfer function with the neglected electrical time constant. The obtained error (12), in the parabolic signal tracking, is h times smaller then the steady-state error of the initial Golo's control system in the tracking of ramp signals.

Golo's control algorithm results in the steady-state error

$$e(\infty) = \frac{d_o T}{K c_{\delta 1}}, \tag{13}$$

under the action of constant external disturbances, where K is the gain of the power amplifier, d_o is the value of the load torque, acting as external disturbance.

The control system with the modified algorithm (11) will have h times smaller steady-state error under the action of ramp disturbances than Golo's initial control system under the action of constant disturbances with the same magnitude d_o.

3. DISTURBANCE ESTIMATOR

According to the previous discussion, it is obvious that Golo's control algorithm, as well as its modification, do not exhibit complete invariance to disturbances. Although, the modified algorithm completely eliminates constant disturbances, and posses a small tracking error in the case of ramp disturbances, in some specific applications, such as in high accuracy systems, it is necessary to provide better robustness in the case of other bounded disturbances.

For example, the experiments carried out on the DC motor servo-system have shown that the considered algorithms are not able to neutralize errors caused by Columb friction. Columb friction as a disturbance is a serious obstacle in control theory and practice of electro-mechanical systems. The attempt to use a model of Columb friction in the form of *sign* function with gain, in order to compensate its action, does not give considerable improvement. Therefore it is necessary to introduce a disturbance compensator in the control system.

3.1 Disturbance compensator

One of the easiest disturbance compensation methods relies on the one step delayed disturbance estimator [15]. The estimator uses system model

$$\mathbf{x}(k+1) = \mathbf{A}_d \mathbf{x}(k) + \mathbf{b}_d u(k) + \mathbf{d}_d(k) \qquad (14)$$

obtained from (1), according to which one step delayed disturbance estimate may be evaluated as

$$\mathbf{d}_d(k-1) = \mathbf{x}(k) - \mathbf{A}_d \mathbf{x}(k-1) - \mathbf{b}_d u(k-1). \qquad (15)$$

This estimate is easy to compute if all state coordinates are measurable. Assuming that disturbances are not abruptly changing, it holds $\mathbf{d}_d(k) \approx \mathbf{d}_d(k-1)$, which substitution in (14), and solving $g(k+1) = 0$ gives the equivalent control

$$u_{eq} = -(\mathbf{c}\mathbf{b}_d)^{-1}[\mathbf{c}\mathbf{A}_d \mathbf{x}(k) + \mathbf{c}\mathbf{d}_d(k-1)]. \qquad (16)$$

Using (16) in (6) ensures reduction of the disturbance impact down to the accuracy of $O(T^2)$.

Beside this method, there are some other approaches reported in literature. An approach proposed in [5], will be briefly presented hereafter.

The main concept is to compensate action of the equivalent disturbance, consisting of model uncertainties and external disturbance, by feedback of the observed equivalent disturbance, and thereby to obtain nominal model behavior. Consider the control structure proposed in Fig. 1., which is composed of the real plant and the disturbance estimator in the local loop. The extraction of the equivalent disturbance q in the disturbance estimator is obtained using discrete transfer function of the nominal model $G_n(z)$. The mismatch between the real plant and the nominal model inevitably exists due to the uncertainties of the plant parameters. The real plant may be reliably described by

$$G(z) = G_n(z)(1 + \delta G(z)), \qquad (17)$$

where its perturbation is limited by the multiplicative bound of uncertainties $\left|\delta G\left(e^{j\omega T}\right)\right| \le \gamma(\omega),\ \omega \in [0, \pi/T]$. According to (17) and Fig. 1., the extracted equivalent disturbance is

$$q(k) = d(k) + G_n(z)\delta G(z) u_k(k). \qquad (18)$$

In order to improve the disturbance estimator robustness, an active controlling structure is employed instead of conventionally used passive digital filter. A reasonable choice is a digital sliding mode control (DSMC) system due to its emphasized robustness property. The signal $\hat{q}$ is the estimation of the compensated equivalent disturbance portion. If DSMC ensures $\hat{q} = q$ (an ideal sliding mode occurs), the control signal may be described as $u_{sm}(k) = G_n^{-1}(z) q(k)$. It can be easily proved that the system output behaves as the nominal model $y(k) = G_n(z) u(k)$. Since DSMC systems enable only quasi-sliding mode, certain but small bounded error between q and $\hat{q}$ will exist, whose value depends on the employed control algorithm.

The robustness against the model uncertainties is actively gained by providing the sliding mode existence conditions. Thus, the robustness and the good external disturbances rejection property are no longer contradi ctory requests. From the control design aspect, the proposed method of equivalent disturbance compensation may be treated as discrete-time tracking control problem with measurable but unknown in advance reference signal $q(k)$. Since the digital controller steers the nominal model not the real plant, all state variables are available. This enables variety of DSMC algorithms to be utilized, which successfully handle this control task.

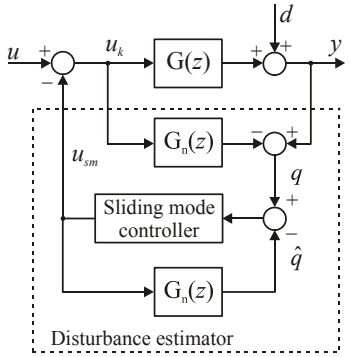

Fig. 1. *Structure of DSMC based disturbance estimator.*

4. SERVO-SYSTEMS DESIGN

In the first part of this section, the design procedure of the servo-system with DC motor using the modified control algorithm will be demonstrated. Since the disturbance estimator may use the same control algorithm for handling the same nominal plant, the design procedure comprises selection of the parameters that are employed in both controllers.

The mathematical model in the tracking error space of the servo-system with DC motor, in the case of the neglected electrical time constant, viscous and Columb friction, may be written as

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{b}u + \mathbf{d}f;\ \mathbf{A} = \begin{bmatrix} 0 & 1 \\ 0 & -a \end{bmatrix};\ \mathbf{b} = \begin{bmatrix} 0 \\ -b \end{bmatrix};\ \mathbf{d} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \qquad (19)$$

where: $\mathbf{x}(t) = [e(t), \dot{e}(t)]^{\mathrm{T}} = [x_1, x_2]^{\mathrm{T}}$, $e(t) = \theta_r(t) - \theta_m(t)$, $f(t) = \frac{M_L}{J} + \frac{\mathrm{d}^2\theta_r}{\mathrm{d}t} + a\frac{\mathrm{d}\theta_r}{\mathrm{d}t}$ is the external disturbance, M_L is the load torque, $\theta_r = r(t)$ is the referent angular position, θ_m is the angular motor shaft position, J is the moment of inertia of the motor with load, $a = 1/T_m$, T_{m} is the mechanical time constant, $b = K/cT_m$, c is the motor constant, $u_r(t)$ is the rotor voltage, control is given by $u(t) = u_r(t)/K$ and K is the amplifier gain. The model fulfills the matching conditions [7]:

$$\mathrm{rang}[\mathbf{b} \mid \mathbf{d}] = \mathrm{rang}[\mathbf{b}]. \qquad (20)$$

Using δ –transformation, the discrete-time model of (19) is obtained as (1).

Further on, the control design will be considered using the nominal system model (1), but without the disturbance term $\mathbf{d}_\delta(kT)$. The above described disturbance estimator will be used to compensate the disturbance effects.

The control $u(kT)$ is chosen to provide a stable digital sliding mode, on the switching manifold (3), where $\mathbf{c}_\delta = [c_{\delta 1} \quad c_{\delta 2}];\ \mathbf{c}_\delta \mathbf{b}_\delta = 1$.

4. 1 Control system parameters selection

The parameters that have to be selected in the design procedure are: the sampling period T, the switching function coefficients $c_{\delta 1}, c_{\delta 2}$, the constants σ, q, the integral action gain h and parameter ρ.

According to the steady-state error expressions with respect to the referent signal (12) and the disturbance (13), the sampling period should be as small as possible. Its lower limit is set by the calculation speed of the microprocessor. The sampling period selection determines the system discrete-time model (1), which affects the choice of the switching function coefficients. There are few strategies in the choice of switching function coefficients. The approach from [4] is used here.

First, the real eigenvalue of the system (16) is found from the relation

$$\delta_1(T) = \frac{e^{-\alpha T} - 1}{T}, \alpha > 0, \qquad (21)$$

and the elements of the transformed vector $\mathbf{c}$ are derived as

$$c_1 = -\delta_1(T). \qquad (22)$$

Afterwards, the elements of vector $\mathbf{c}_\delta$ are calculated as

$$\mathbf{c}_\delta = [c_1 \mid 1]\mathbf{P}_1^{-1}, \qquad (23)$$

where $\mathbf{P}_1$ is a transformation matrix

$$\mathbf{P}_1 = \mathbf{M}_c \begin{bmatrix} a_{2\delta} & 1 \\ 1 & 0 \end{bmatrix}, \qquad (24)$$

with $\mathbf{M}_c$ being the system (1) controllable matrix, and $a_{2\delta}$ being the coefficient of the characteristic polynomial

$$D(\delta) = \det[\delta \mathbf{I} - \mathbf{A}_\delta] = \delta^2 + a_{2\delta}\delta + a_{1\delta}. \qquad (25)$$

Regarding the fact that the steady-state accuracy of the system in the digital sliding mode depends on the switching function coefficient ratio (see relation (4)), this ratio should be as large as possible. In the considered second-order system, this ratio is actually equal to the value of the parameter α, which is comparable to the sliding line slope coefficient in the corresponding continuous-time variable structure control systems.

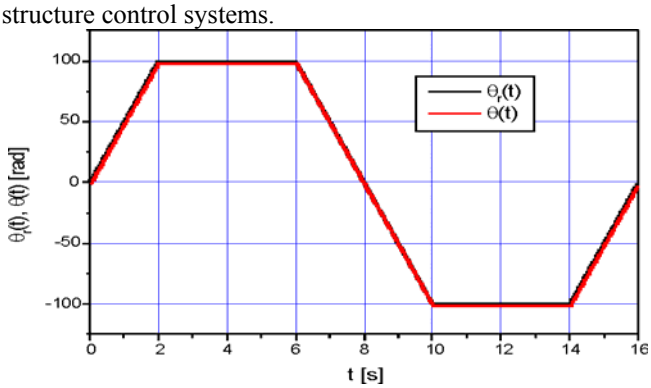

Fig. 2. *Referent position profile $\theta_r(t)$ and obtained motor shaft position $\theta(t)$ using the proposed control.*

Finally, the integral action gain h is chosen. It has to be selected in compliance with the relation (8), as well as with the required steady-state accuracy. Notice that an excessively large gain may induce the unmodeled dynamics excitation and the chattering.

The parameters $\sigma > 0$ and $q \geq 0$ define the reaching speed. A too large values of these parameters may also excite the unmodeled dynamics.

4.2 An illustrative example

In this section a design example of a low power servomechanism is carried out. The controller parameter design is given in the first part. The results of the proposed solution are compared with the results of the original Golo's algorithm [4]. The improvements in the servomechanism steady-state accuracy, obtained by the introduction of the adjustable integral action, keeping the same dynamics, are demonstrated by simulation. The experimentally obtained results on a servomechanism laboratory prototype are given. These results show a remarkable correspondence between the simulated and the measured system's quantities.

The experimental servomechanism uses a Bautz DC motor, type E586M6B, with the following nominal parameters: $M_{\max} = 0.22$ Nm, $I_{\max} = 3.7$ A, $n_{\max} = 6000\ \text{min}^{-1}$, the voltage constant $k_e = 5.85\ \text{V}/1000\ \text{min}^{-1}$, the torque constant $k_t = 0.056\ \text{Nm/A}$. A PWM power amplifier with the carrier frequency of 15 kHz drives the motor. A quadrature incremental encoder with 1000 lines (the increment of $2\pi/4000$ rad) is used for the position measurement. The DC motor with the power amplifier is represented by the equation (14) with $a = 16, b = 680$. A PC with an acquisition and control card realizes the digital control algorithm. A 12-bit D/A converter conveys the control signal to the system. The minimal possible sampling period of $T = 0.4$ ms is used in this case. The discrete-time model of the nominal system (14) is given with

$$\mathbf{A}_d = \begin{bmatrix} 0 & 0.9968 \\ 0 & -15.9489 \end{bmatrix}; \mathbf{b}_d = \begin{bmatrix} -0.13571 \\ -677.828635 \end{bmatrix}.$$

The matching conditions (20) do not hold, but due to the small sampling period, degradation of the matching conditions may be neglected.

The value of α is set to 15, as in Golo's system [4]. The calculated controller parameters are: $[c_{\delta 1} \ \ c_{\delta 2}] = [-0.0221 \ \ -0.0015]$, $\mathbf{c}_\delta \mathbf{A}_\delta = [0 \ \ 0.0015]$. The switching gains are chosen to be $\sigma = 10$ and $q = 0$.

The tracking error derivative is obtained as a difference between the derivative of the referent signal and the observed velocity by the asymptotic observer.

Figure 2 shows the referent angular position signal and the experimentally obtained DC motor shaft angular position. It can be seen that the quite accurate tracking is accomplish. A better view is given in fig. 3, where the tracking error, obtained by simulation (for the proposed as well as tGolo's system) and experiment, is depicted. The experimentally obtained signal contains a significant noise, due to quantization. However, in the static state tracking error is within encoder resolution.

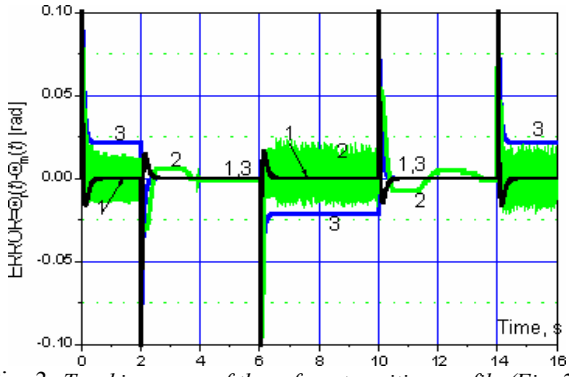

Fig. 3. *Tracking error of the referent position profile (Fig. 2): the proposed system* (ρ*=0.5, h=16)***:** *1- simulation, 2-experiment, 3-the Golo's system (simulation).*

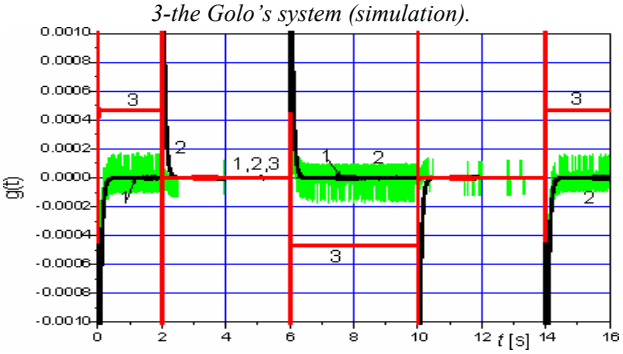

Fig. 4. *Switching function dynamics in tracking of the referent profile (Fig. 2): the proposed system: 1 - simulation; 2 - experiment; 3-the Golo's system (simulation).*

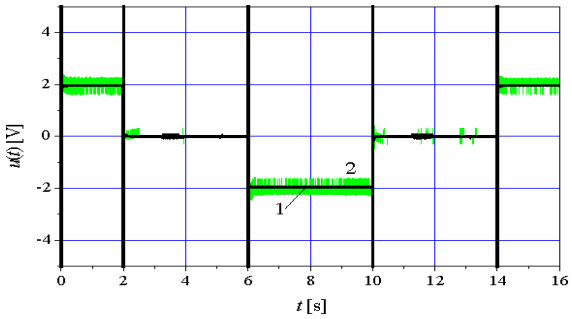

Fig. 5. *Control signal of the proposed system for tracking the referent profile (Fig. 2): 1 - simulation; 2 - experiment.*

The switching function $g(t)$ is given in fig. 4, indicating that the digital sliding mode occurs, since $g(t)=0$ holds almost everywhere, except in the short intervals of the disturbance action, which appears due to the reference signal being compensated in a very short time.

The control signal is plotted in fig 5, showing the non-switching nature of the control algorithm. The present noise is caused by the quantization process.

5. CONCLUSION

The paper presents discrete-time control algorithm for the realization of the digital sliding mode on given hyperplane in the state space. The core of the considered algorithm is based on the algorithm that is proposed in [4], to which the variable structure integral action is superimposed. This increments the control system type number by one, making the system invariant to the constant disturbances and capable of parabolic signals tracking with high accuracy. Further improvement is obtained by using active DSMC based disturbance estimator, which incorporates the same controller within its control subsystem. Performances of the considered control system are demonstrated using DC motor based servo-system. The results obtained from the experiments
carried out on the laboratory prototype indicate the high resemblance level between the theoretically predicted and practically obtained results.

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REALIZATION OF ELECTRONIC FUNCTIONS IN ENERGY PROCESSING BY MEANS OF GYRATORS

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Abstract: *The aim of this paper is to demonstrate that certain electronic functions in energy processing can be efficiently performed by means of power gyrators. Thus, it is intended to show that power gyrators are canonical elements in the construction of energy processing systems. The investigation is devoted to some properties directly derived from the G or R nature of power gyrators as, for example, current addition or current to voltage conversion. Another property studied in this paper is the use of power gyrators for impedance matching, particularly for maximum power point tracking in photovoltaic systems.*

Key Words: ***Power Electronics, switching converters, sliding mode, power gyrators, applications***

1. INTRODUCTION

The gyrator is an ideal circuit element that, unlike the other four elements (resistor, inductor, capacitor and ideal transformer) that directly arise from modelling electromagnetic phenomena, was originally postulated, without immediate experimental verification, as the most simple linear, passive and non-reciprocal element. The term gyrator was introduced by Tellegen [1] who developed the gyrator theory and designed possible realisations without achieving feasible solutions. Hogan [2] was the first to design a device that, operating at microwave frequencies, approximated the behaviour of an ideal gyrator. The physical principle of the first gyrator was the Faraday rotation in biased ferrites, a solution essayed previously by Tellegen unsuccessfully at low frequencies where the nonreciprocal properties of ferrites are not observed. Some years later, the nonreciprocal behaviour was obtained by means of active elements, this leading to the gyrator realisation at low frequencies [3]. Since then, the use of the gyrator at low frequencies is mainly constrained to active filtering due to its facility to emulate inductors with high quality factor.[4-6]

The introduction of the gyrator concept in power processing circuits is due to Singer [7-9] who related the power gyrator to a general class of circuits named POPI (power output = power input), describing the ideal behaviour of a switched-mode power converter. Later, the notion of power gyrator was used to model an inverse dual converter [10], and double bridge converters were reported to behave naturally as gyrators [11]. More recently, a gyrator realisation based on the combination of a transmission line and a switching network was reported in [12].

On the other hand, the increasing importance of modularity in many applications of power electronics such as, for example, UPS realisations or photovoltaic installations, leads one way or another to parallel connection of the output ports of power converters. Paralleling switching converters increases the power processing capability and improves the reliability, since stresses are better distributed and fault tolerance is guaranteed. In this context, a power gyrator with good static and dynamic performances could be a useful canonical element in certain cases of converter paralleling. This hypothesis is based on the nature of certain types of gyrators, i.e., G-gyrators with controlled output current, in which the output current is proportional to the input voltage, and that, in turn, the input current is proportional to the output voltage with the same proportionality factor.

It was demonstrated in [17] that the buck converter with input filter (BIF) and the Cuk converter can behave as power G-gyrators with controlled output current if damping networks are inserted and certain parametric conditions are accomplished. BIF converter-based G-gyrators with controlled output current have been proved to be more efficient than the same type of gyrators based on the Cuk converter and, hence, are the chosen candidates for converter paralleling [18].

It has been also proved that the boost converter with output filter (BOF) and the Cuk converters make possible the realization of unconditionally stable G-gyrators with controlled input current. Moreover, it has been shown that BOF converters can exhibit stable R-gyrator characteristics in sliding-mode or in limit cycles [18].

The main goal of this paper is to demonstrate that each type of the above mentioned gyrators performs a specific electronic function in Energy Processing. Thus, it will be shown that the addition of currents is inherent to G-gyrators with controlled output current. Also, it will be proved that R-gyrators are suitable for current to voltage conversion and that can constitute an important building block in the realization of high power converters requiring voltage regulation. In addition, G-gyrators with controlled input current are shown to be efficient interfaces for impedance matching of a DC generator and a DC load.

The outline of the paper is as follows. Addition of currents based on parallel connection of G-gyrators with controlled output current is described in Section II. Applications of power R-gyrators in the current to voltage conversion is presented in Section III. The use of G-gyrators with controlled input current for impedance matching is covered in Section IV. A concluding discussion is given in Section V.

2. ADDITION OF CURRENTS

The addition of the output currents of several converters can be easily performed if the converters behave as current sources at their respective output ports. As demonstrated in [17], a G-gyrator with controlled output

current has a current source nature at the output port. Hence, connecting in parallel the output ports of G-gyrators will result in a direct addition of currents. This fact will be a central element in the development of voltage regulators for high power applications.

Fig. 1 shows the block diagram of a switching regulator with gyrator characteristics. It consists of a switching converter which is controlled by means of a sliding-mode regulation loop whose switching surface is given by $S(x)=i_2-gv_1$. In steady-state $S(x)=0$, i.e., $I_2=gV_1$ which automatically implies $I_1=gV_2$, since the converter in Fig.1 is ideal and therefore is a POPI structure (DC Power output = DC Power input) [8].

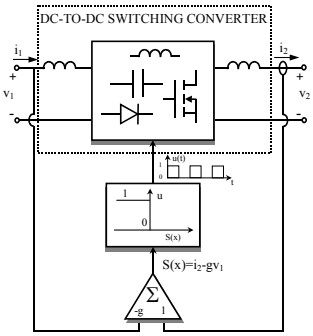

Fig. 1 Block diagram of a dc-to-dc switching regulator with gyrator characteristics

It has to be pointed out that imposing a sliding-mode regime to the output current requires i_2 to be a continuous function of time [13], this implying the existence of a series inductor at the output port. On the other hand, in order to minimise EMI levels, a pulsating current will not be allowed at the input port and therefore the power gyrator will also require a series inductor at the input port. The most simple converters with such constraints at both ports are of fourth order, namely, buck with input filter (BIF), boost with output filter (BOF), Čuk converter and Čuk converter with galvanic isolation (Fig. 2).

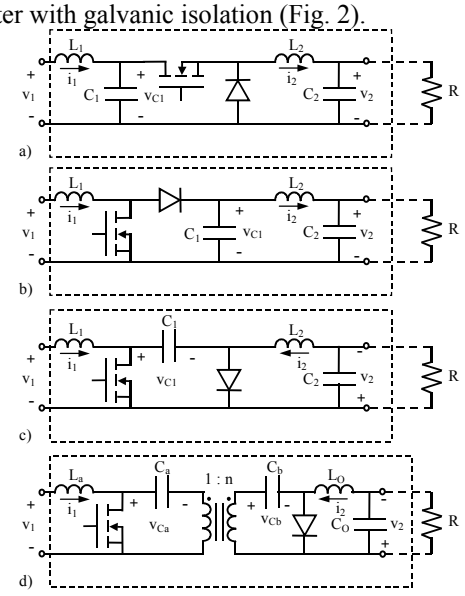

Fig. 2 Fourth order converters with non-pulsating input and output currents a) buck converter with input filter b) boost converter with output filter c) Čuk converter d) Čuk converter with galvanic isolation

In the case of the BIF converter, the block diagram depicted in Fig.1 has been implemented as shown in fig.3 where the complete converter and its control circuit are depicted in detail. Note that the sliding surface is implemented by means of an analogue multiplier and an operational amplifier-based linear circuit, while the ideal comparator function is performed by a hysteretic comparator. The gyrator parameters satisfy the stability conditions found in [17] and are given by the set of values $V_g = 20\ V$, $R = 1\ \Omega$, $g = 0.5\ \Omega^{-1}$, $L_1 = 12\ \mu H$, $C_1 = 12\ \mu F$, $C_d = 100\ \mu F$, $R_d = 2.2\ \Omega$, $L_2 = 35\ \mu H$, $C_2 = 6.6\ \mu F$. R_dC_d is a damping network connected in parallel with C_1 that stabilizes the sliding dynamics. R_aL_a, in turn, is a damping network that improves the dynamic behaviour of the gyrator state variables.

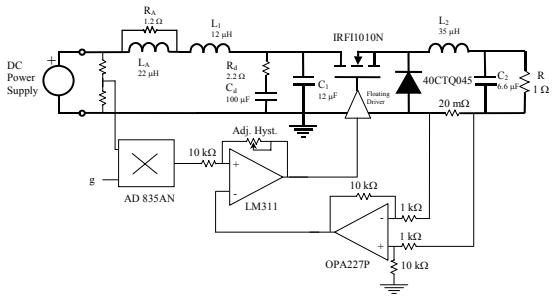

Fig. 3 Practical implementation of a BIF converter-based gyrator L_1=12 μH, L_2=35 μH C_1=12 μF , C_2=6.6 μF C_d=100 μF R_d=2.2 Ω, L_a=22 μH R_a=1.2 Ω, g=0.5 Ω^{-1} R=1 Ω

The practical implementation of three BIF converter-based G-gyrators of the type of figure 3 connected in parallel is shown in Fig. 4.

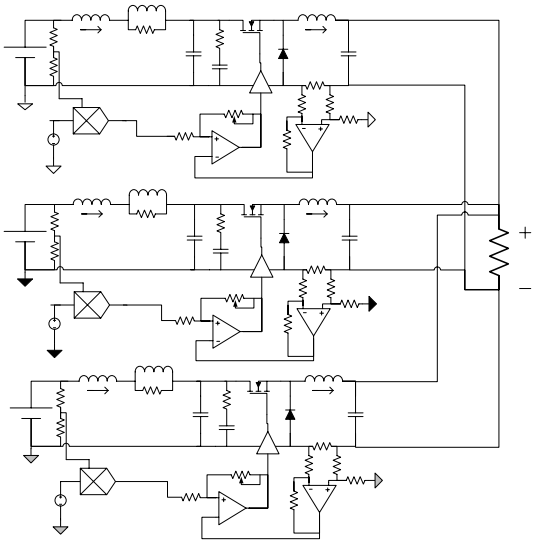

Fig. 4 Practical implementation of the parallel connection of three Buck converters with input filter G-gyrators.

The nominal input voltage of each gyrator is $V_{g1} = 20\ V$, $V_{g2} = 18\ V$ and $V_{g3} = 16\ V$ and the output load is R=0.26Ω. Figure 5 illustrates the experimental response to a ± 4 V input voltage perturbation of step type superposed

on the nominal input voltage of gyrator 1. It can be observed that output currents of gyrators 2 and 3 remain constant at 9 A and 8 A respectively. On the other hand, the output current of gyrator 1 reproduces proportionally the input voltage variations by changing from 10 A to 12 A and finally returning to 10 A. The parallel connection delivers 189 W to the load and this power is distributed as follows: 70 W is supplied by gyrator 1, 63 W by gyrator 2 and 56 W by gyrator 3.

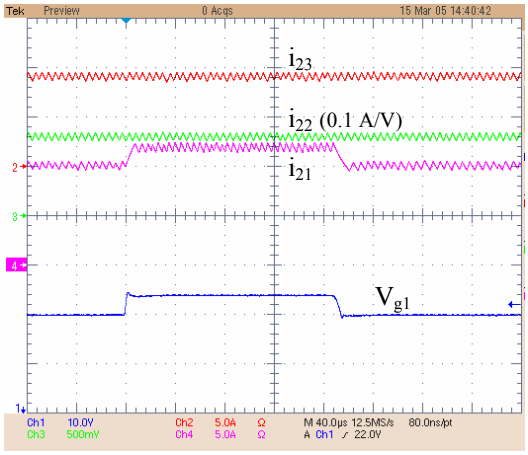

Fig. 5 Experimental behaviour of 3 paralleled BIF converter-based G-gyrators to a pulsating input voltage in gyrator # 1.

3. COMBINING OF V-I AND I-V CONVERSION

Switching structures used in the design of power gyrators are not versatile, i.e., a G-gyrator cannot be adapted to perform R-gyrators functions. Note, for example, that a current source at the input port of the circuit depicted in Fig. 1 will not be compatible with the series inductor and therefore such circuit cannot be used for the current-voltage transformation. Hence, the block diagram of a power R-gyrator can be represented as shown in Fig. 6 where i_g is the input current source to be transformed into an output voltage source by means of the gyrator action. It can be observed that S(x) = 0 in steady-state, i.e., $V_2 = r\, I_g$ which implies $V_1 = r\, I_2$.

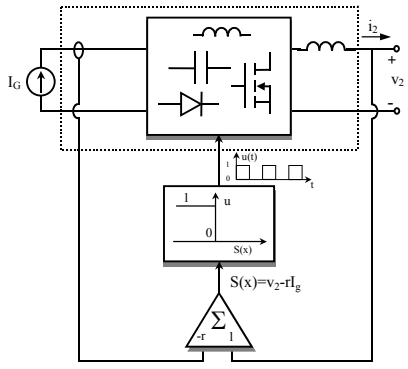

Fig. 6 Block diagram of a dc-to-dc switching regulator operating in sliding-mode with R-gyrator characteristics

The most simple converters with the topological constraints depicted in the block diagram of Fig. 6 are derived by slight modification of the BOF converter, Čuk converter and Čuk converter with galvanic isolation.

A circuit scheme of a BOF converter-based R-gyrator is illustrated in Fig. 7 for the set of parameters I_g=10 A, C_1 = 20 µF, L_2 = 12 µH, C_2 = 2 µF, r = 2 Ω and R= 4.7 Ω.

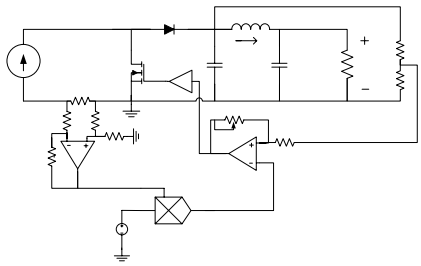

Fig. 7 Practical implementation of a BOF converter-based R-gyrator

In the context of transforming an energy source into its dual representation, we can think of a combined transformation performing the v-i-v conversion. Thus, a cascade connection of a G-gyrator and a R-gyrator would performed this conversion.

The practical implementation of the cascade connection is shown in Fig. 8. Note that inductance L_2 of the G-gyrator is used as the L_1 inductance of the Boost converter with Output Filter (BOF) R-gyrator.

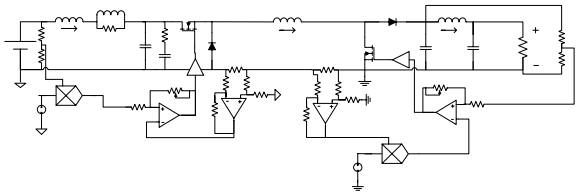

Fig. 8 Practical implementation of the cascade connection of a buck converter with input filter G-gyrator and a boost converter with output filter R-gyrator.

Figure 9 shows the practical realization of v-i-v conversion for the case of 3 paralleled G-gyrators. Note that the v-i conversion is carried out by means of the parallel connection of 3 G-gyrators whose output is the input of a power R-gyrator. The G-gyrators are based on the Buck converter with Input Filter (BIF) while the R-gyrator is based on the BOF converter. The input voltage of each G-gyrator is $V_{g1} = 14\ V$, $V_{g2} = 12\ V$ and $V_{g3} = 12\ V$.

Figure 10 shows the experimental response to a 50% step change in the load resistance. Note that the output voltage remains constant and the load perturbation is absorbed by output current of the R-gyrator. Note that the output voltage is 1.035 times the value of the sum of G-gyrator output currents. This value is practically the theoretical one, which is 1.1 times the value of this sum.

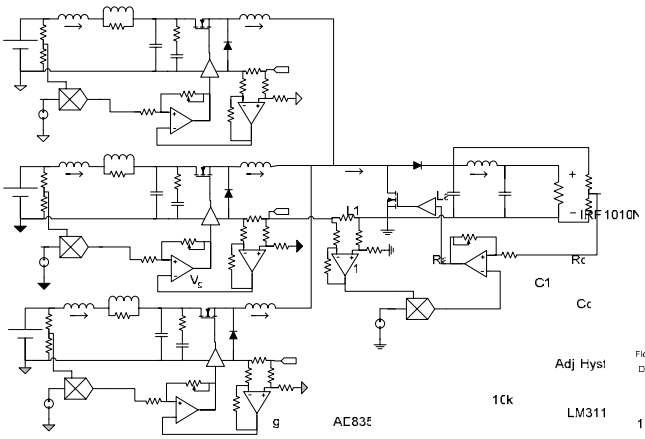

Fig. 9 Practical implementation of a cascade connection of 3 paralleled power G-gyrators and a power R-gyrator

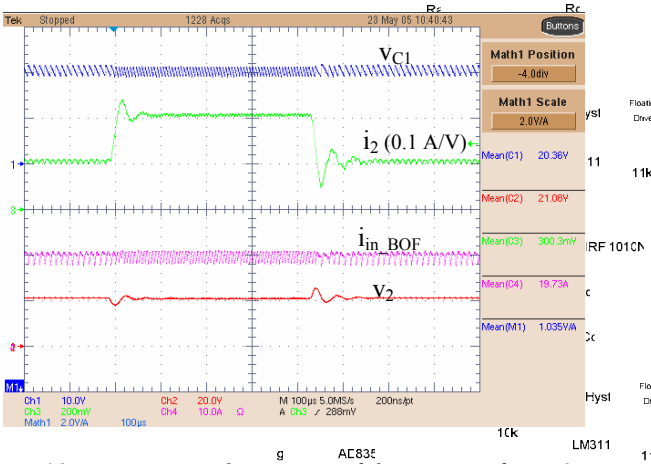

Fig. 10 Experimental response of the circuit of Fig. 9 to load variations of step type

4. IMPEDANCE MATCHING

Impedance matching in power electronics basically means solving the problem of maximum power transfer between a dc generator and a dc load. In particular, the maximum power transfer from a photovoltaic panel to a dc load is an important technological problem in many practical cases dealing with the optimization of a PV conversion chain.

It has been demonstrated in [18] that the application of an extremum seeking control algorithm [19] to a BIF converter-based G-gyrator makes possible an efficient and stable maximum power point tracking. It has been also shown that this algorithm can be efficiently adapted with the same purpose to a BOF converter-based R-gyrator. It has been experimentally verified the validity of both approaches by developing two battery chargers. Thus, a 12 V battery has been charged from a standard solar array (around 20 V of open circuit voltage) and by using a BIF converter-based G-gyrator with controlled output current as interface. Similarly, with the same PV array, a 24 V battery has been charged by means of a BOF converter-based R-gyrator. However, a Cuk converter-based G-gyrator with controlled input current has been proved to be the most versatile system for PV battery chargers. Due to its step-up or step-down characteristics, a Cuk converter-based G-gyrator with controlled input current can be used to charge indistinctly a 12 V or a 24 V battery from a standard solar array. Figure 11 shows the circuit scheme of this gyrator whose corresponding prototype is depicted in Figure 12.

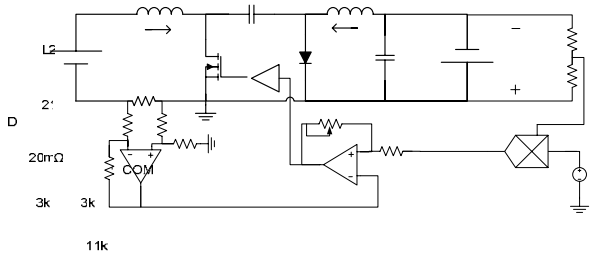

Fig. 11 Circuit scheme of a Cuk converter-based G-gyrator with controlled input current.

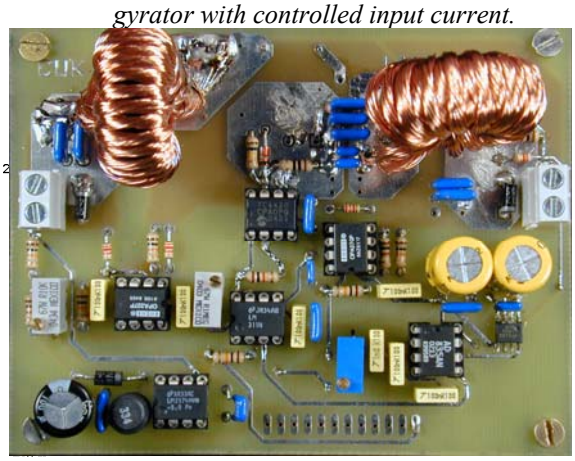

Fig. 12 A 75W Cuk converter-based G-gyrator with con trolled input current.

Figure 13 shows the practical implementation of a Cuk converter-based G-gyrator with controlled input current for maximum power point tracking.

The PV panel is a solar array of monocrystalline cells with an open circuit voltage of 22.1 V and a nominal voltage value at the maximum power point of 18 V. Note that the output of the analog multiplier AD835 is the product of g times a negative signal proportional to $-V_2$. The gyrator parameters are L_1 = 75 µH, C_1 = 10 µF, L_2 = 75 µH, and V_2 = 12 V (24 V).

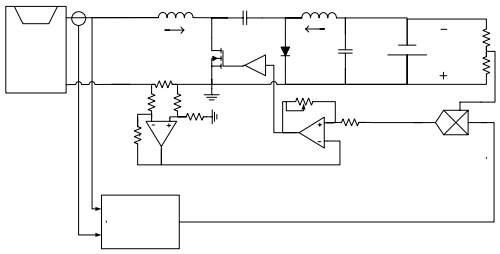

Fig. 13 Cuk converter-based G-gyrator with controlled input current with MPPT function

Fig. 14 shows the charge of a 24 V battery by means of the power gyrator with MPPT function. Note that the search of the maximum point is performed by controlling g (depicted in channel 3) which takes negative values in this case. The MPPT efficiency is of 99 % when the gyrator delivers 57.47 W to a 12 V battery and 98.6 % efficiency when it supplies 57.4 W to a 24 V battery.

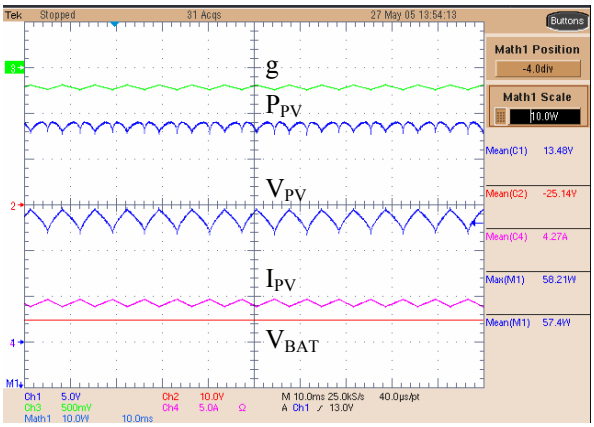

Fig. 14 Steady-state waveforms of a Cuk converter-based G-gyrator with controlled input current supplying 24 V battery.

5. CONCLUSIONS

It has been shown in this paper that power gyrators can perform efficiently basic electronic functions in energy processing. Namely, voltage to current conversion, current to voltage conversion, combination of both conversions and impedance matching. Reports on the use of power gyrators for voltage regulation are in progress.

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COMPLEX MODEL OF LOW-VOLTAGE TRACTION ASYNCHRONOUS DRIVE

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Abstract: *Independent low-voltage traction drives are now used in many application. This paper deals with creation of an exact model of low-voltage traction drive which is used in battery stacker fed from batteries with nominal voltage 24 V. This complex model consists of particular models of induction machine, inverter model, load model and battery model. The model of induction machine is a standard model with considering magnetic circuit saturation. The inverter model includes impact of output voltage distortion by dead times, on-state voltage drops on switching elements and DC-link voltage ripple. The load model is a model of mechanical part of battery stacker considering inertia masses, rolling resistance, air resistance and inclination on slant plane. DC-link is approximated by DC-voltage source with internal resistance and low-pass filter for simulation of a capacitor. All the simulations were done in MATLAB-SIMULINK.*

Key Words: ***Independent Traction/Induction Machine/ Modeling/Simulation/Simulink/Low-Voltage Drive***

1. INTRODUCTION

One of the main problems in independent traction is high ratio of weight and capacity of accumulator. For that reason it is important to research losses in the individual parts of the independent traction drive (Fig. 1: battery – inverter – motor – gear – wheel). Decreasing these losses and thereby increasing efficiency is important for usable qualities of the vehicle.

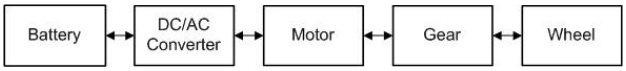

Fig. 1. *Components of the electrical vehicle*

In the article a model of battery stacker drive is described. It contains particular models of drive parts. All the models are connected together. Block scheme of the simulation structure is in Fig. 2.

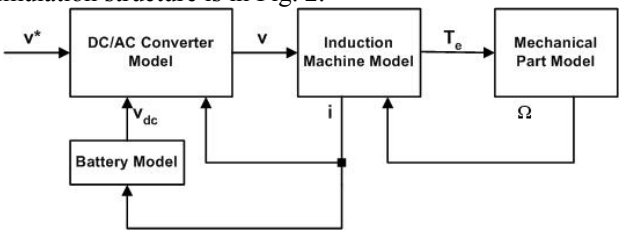

Fig. 2. *Block scheme of the simulation structure of the electrical vehicle*

There is used an induction machine with nominal voltage 14 V which is fed from the accumulator with nominal voltage 24 V. In order for the motor to reach the same torque and power using this voltage as compared to supplying it from the mains, the phase currents have to be much stronger. These currents cause voltage drops on inner resistance of the accumulator and on switching elements of the inverter. These effects have significant influence on features of the whole low-voltage drive.

2. MODEL OF THE INDUCTION MACHINE

The mathematical model of low-voltage induction machine is assembled from voltage equations of the machine in general reference frame, as in [1]:

$$\bar{v}_s^k = R_s \cdot \bar{i}_s^k + \frac{d\bar{\psi}_s^k}{dt} - \omega_k \cdot \bar{\psi}_s^k \qquad (1)$$

$$\bar{v}_r^k = R_r \cdot \bar{i}_r^k + \frac{d\bar{\psi}_r^k}{dt} + j(\omega_k - \omega) \cdot \bar{\psi}_r^k \qquad (2)$$

where R_s, R_r are stator and rotor phase resistances, $\bar{i}_s^k$, $\bar{i}_r^k$ are stator and rotor current space vectors and $\bar{\psi}_s^k$, $\bar{\psi}_r^k$ are stator and rotor linkage flux space vectors. ω is electrical speed of motor shaft.

To the model the equation for linkage flux space vectors in general rotating reference frame are added:

$$\bar{\psi}_s^k = (L_h + L_{s\sigma}) \cdot \bar{i}_s^k + L_h \cdot \bar{i}_r^k \qquad (3)$$

$$\bar{\psi}_r^k = (L_h + L_{r\sigma}) \cdot \bar{i}_r^k + L_h \cdot \bar{i}_s^k \qquad (4)$$

2.1. Impact of temperature on motor resistances

To include impact of temperature on motor resistances, constant resistances were replaced by variables depending on temperature by equation:

$$R_2 = R_1(1 + \alpha \Delta \vartheta) \qquad (5)$$

where α is thermal coefficient of resistance and Δυ is thermal difference.

2.2. Saturation of main magnetic circuit

Considering saturation of main magnetic circuit is done by replacing constant value of main inductance L_h in equations 3 and 4 by approximated curve dψ/di according to figure 3b. Based on knowledge of instantaneous magnetizing current is taken off instantaneous main inductance.

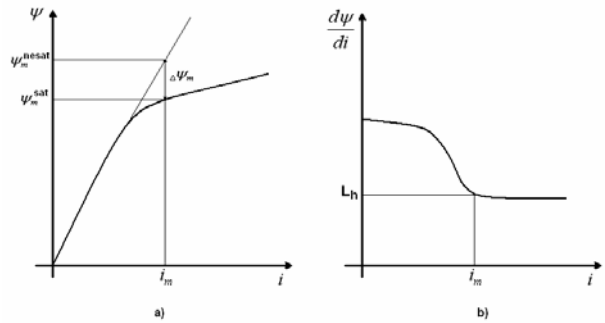

Fig. 3. *Magnetizing curve (a) and its derivation by magnetizing current (b)*

3. MODEL OF THE LOAD

On battery stacker affect many mechanical forces and inertia masses which are necessary to consider for getting an exact model. In the model are considered: force by inclination on slant plane, wheels rolling resistance, air resistance and losses in the gearbox. Moments of inertia are transferred on motor shaft and by adding motor moment of inertia we get the total moment of inertia of the whole drive J_l. After converting forces in torques on the rotor shaft T_l and inserting it in the moving equation 6 is the model of load done.

$$T_e - T_l = J_l \frac{d\omega_m}{dt} \tag{6}$$

4. MODEL OF THE INVERTER

In the model of the inverter special attention was focused on description of impact of dead time and on-state voltage drops on switching elements. Voltage drops on inverter switching elements and dead times cause distortion of inverter output voltage and affect magnitude of the first harmonic of output voltage. It can significantly affect machine torque.

Voltage drop on transistor is described by threshold voltage V_{pT} and dynamic resistance R_{dT}.

$$V_T(t) = V_{pT} + R_{dT} \cdot i_T(t) \tag{7}$$

The similar situation occurs with voltage drop on diode:

$$V_D(t) = V_{pD} + R_{dD} \cdot i_D(t) \tag{8}$$

V_{pD} is threshold voltages and R_{dD} is dynamic resistances of the diode.

Introduction of dead time into switching sequence of top and bottom transistor causes a distortion of inverter pole output voltage and affects voltage applied on the motor. Sign of distortion depends on phase current.

Two models of inverter were created. Both of them allow a choice of considering of impact of on-state voltage drops and dead times. By this is possible to research their impact at the whole drive system.

4.1. Pulse model of the inverter

The scheme of pulse SIMULINK model of inverter is shown in figure 4.

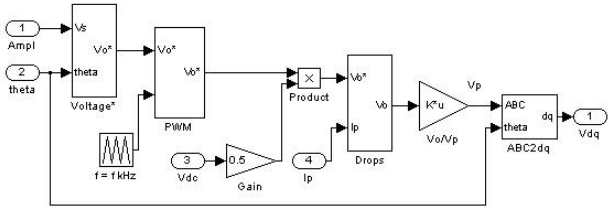

Fig. 4. *Scheme of pulse model of inverter*

From desired value of magnitude and frequency are created three desired pole voltages which are modulated in PWM block and multiplied by instantaneous value of DC voltage and shifted. In "Drops block" are computed distorting voltages from instantaneous phase currents by equations 7 and 8 and they are added to output pole voltages. After it these output voltages are converted into phase voltages and transformed in *dq* reference frame.

4.2. Discrete model of the inverter

The scheme of discrete SIMULINK model of inverter is shown in figure 5.

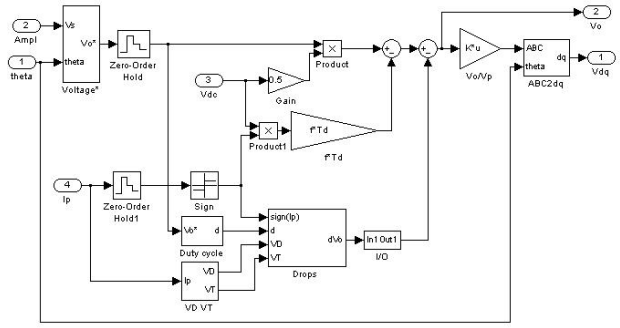

Fig. 5. *Scheme of discrete model of inverter*

From desired value of magnitude and frequency are created three desired pole voltages which are sampled with switching frequency. They are decreased by distorting voltages which simulate on-state voltage drops and dead time effect.

Distorting voltage by dead time is computed in each switching period by:

$$V_{DT} = f \cdot T_D \cdot V_{DC} \cdot \mathrm{sgn}(i_p) \tag{9}$$

where f is switching frequency, T_D is dead time, V_{DC} is DC-link voltage and i_p are individual phase currents. Similarly, voltage drops are computed by equation 7 and 8 and distorting voltage is given by following equations [2]:

$$\Delta V_o = V_D + d(V_T + V_D) \qquad i_p > 0 \tag{10}$$

$$\Delta V_o = -V_T + d(V_T + V_D) \qquad i_p < 0 \tag{11}$$

Symbol d is duty cycle in particular pole.

After correction pole voltages by both of these effects are again computed phase voltages and transformed into *dq* reference frame.

5. MODEL OF THE WHOLE DRIVE

By connection of previously described particular models we get a model of the whole drive which is shown in figure 6. The model of DC-link (Battery) allows computing instantaneous value of DC-link voltage V_{DC}, when we know instantaneous DC-link current.

$$V_{DC} = V_{DC0} - R_i \cdot i_{DC} \tag{12}$$

V_{DC0} is internal battery voltage and R_i is its internal resistance. I_{DC} is instantaneous current of DC-link. The model allows switch between constant or computed DC-link voltage and also can be switched on or off effect of dead times and on-state voltage drops.

Block of Discrete Furrier Transform DFT, as in [3] for possibility of comparison simulation results was added into both of these models.

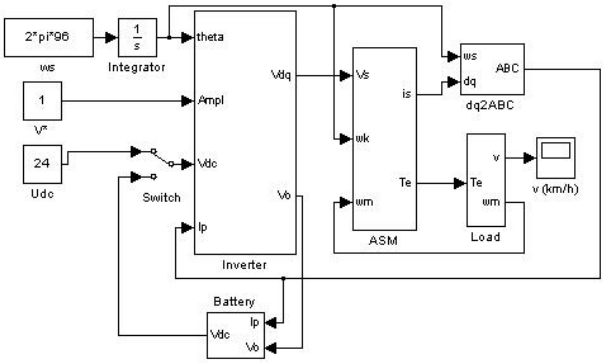

Fig. 6. *The* w*hole drive model*

6. SIMULATION RESULTS

The four-pole induction machine with nominal voltage 14 V and nominal frequency 96 Hz was simulated. System was fed by battery with nominal voltage 24 V with internal resistance 0.005 Ω. Threshold voltage of inverter transistor was 0 V and diode 0.4 V. Dynamical resistances were 7.5 and 6 mΩ. Inverter switching frequency was 4 kHz.

6.1 Inverter model

In figures 7 – 12 are shown inverter output pole voltages and their harmonic analysis produced by pulse and discrete model. Both models are simulated without and with considering voltage drops on switching elements. It is shown in "pulse inverter" the impact of DC-voltage ripple on the course of output pole voltage. There is also shown in "discrete inverter" the impact of dead time on the course of output pole voltage.

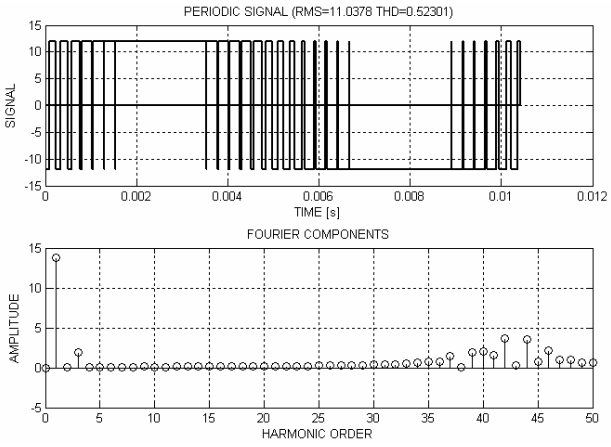

Fig. 7. *Inverter output pole voltage and harmonic analysis in inverter pulse model. Switching elements voltage drops are not considered*

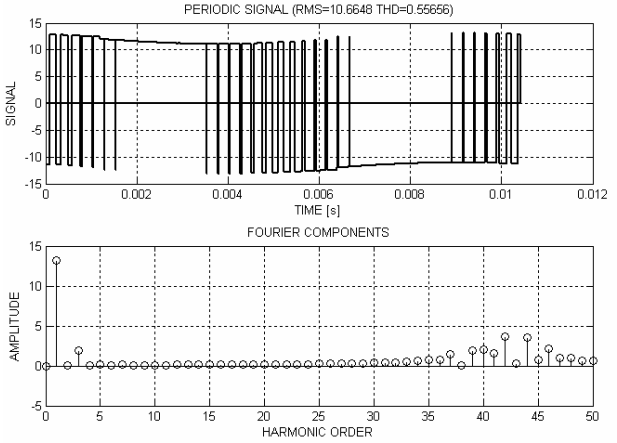

Fig. 8. *Inverter output pole voltage and harmonic analysis in inverter pulse model. Switching elements voltage drops are considered*

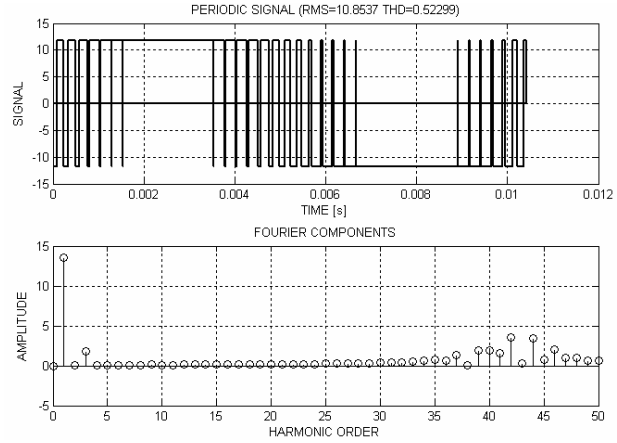

Fig. 9. *Inverter output pole voltage and harmonic analysis in inverter pulse model. DC-voltage ripple is considered*

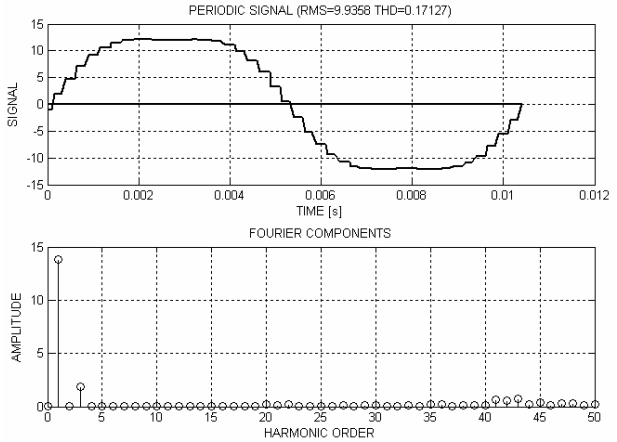

Fig. 10. *Inverter output pole voltage and harmonic analysis in inverter discrete model. Switching elements voltage drops are not considered*

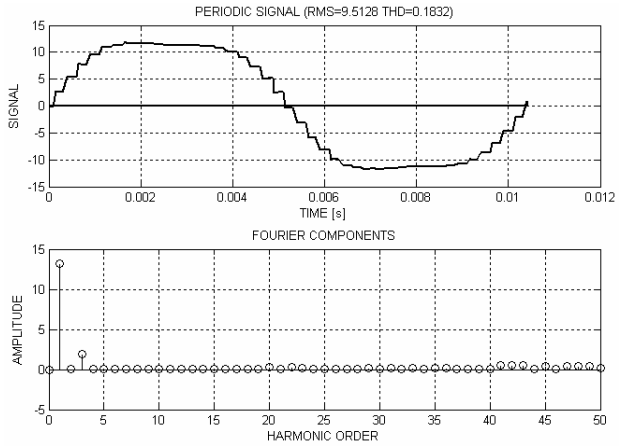

Fig. 11. *Inverter output pole voltage and harmonic analysis in inverter discrete model. Switching elements voltage drops are considered*

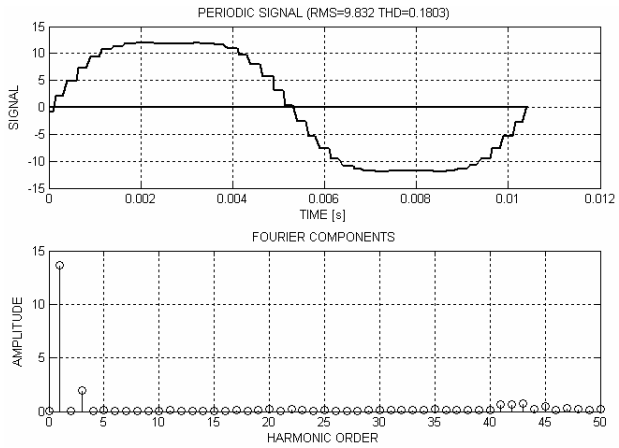

Fig. 12. *Inverter output pole voltage and harmonic analysis in inverter discrete model. Dead times (T_d = 2e-6 s) is considered*

Following table presents values of first and third harmonic of pole voltages in cases of both types of models. There is shown, that the including of non-idealities of inverter decreases first harmonic of pole voltage and also of phase voltage, because both are identical. It is evident, that results are the same for both types of model and both can be used for simulation of low-voltage drive. An advantage of "discrete model" is much faster computing.

Table 1. *Values of first and third harmonic of pole voltages*

		First Harmonic	Third Harmon.	
Pulse model	Ideal	13.83	1.89	V
	Volt. Drops	13.18	1.97	V
	With battery model	13.60	1.86	V
Disc. Model	Ideal	13.85	1.87	V
	Volt. Drops	13.23	1.96	V
	Dead time	13.68	1.93	V

6.2. Modelling of whole drive

Parameters of battery stacker are shown in table 2:

Table 2. *Parameters of load*

Motor moment of inertia	0.00105	$kg.m^2$
Gear moment of inertia	0.000244128	$kg.m^2$
Wheels moment of inertia	0.028733	$kg.m^2$
Gear efficiency	90	%
Driving wheel radius	0.11	m
Gear ratio	30	-
Weight of vehicle	800	kg
Slope	3	%
Front area of vehicle	2	m^2

Figure 13 shows mechanical speed during vehicle start with above presented load

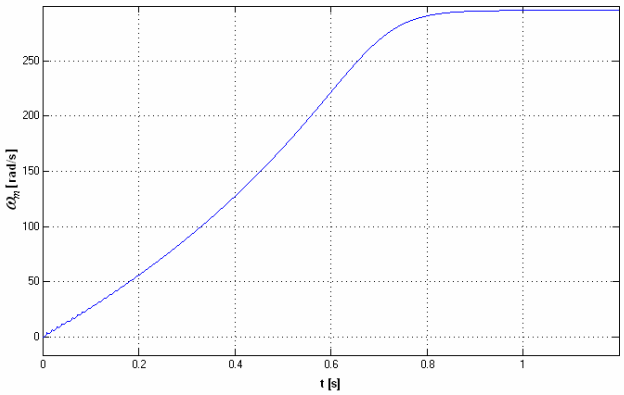

Fig. 13. *Mechanical speed course during vehicle start*

There is possible to watch distribution of power and losses in the model. Figure 14 shows course of total losses in mechanical part ΔP and input and output power P_1 and P_2 during acceleration.

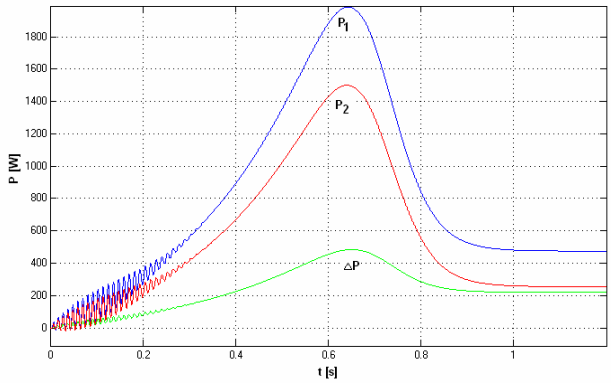

Fig. 14. *Input and output power and total losses course in drive mechanical part during vehicle start*

Figure 15 presents particular compounds of losses in mechanical part. There it is possible to see instantaneous power consumed in acceleration of rotating mass of inertia (gear ΔP_{jp}, motor ΔP_{jm} and wheels ΔP_{jk}). ΔP_t and ΔP_p are losses by rolling and gear friction resistance and ΔP_v are losses by air resistance. ΔP_s is power consumed in inclination on slant plane.

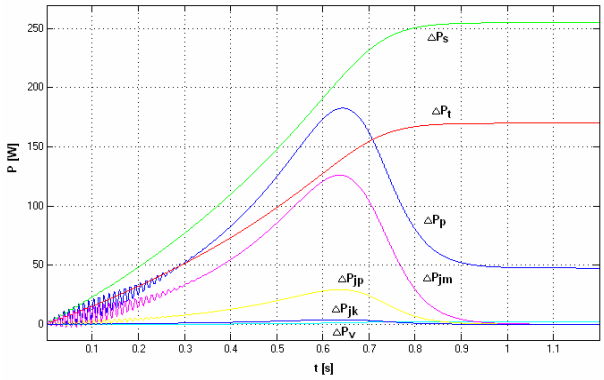

Fig. 15. *Losses distribution in mechanical part of the drive*

7. CONCLUSION

In the article the complex model of low-voltage traction asyncronnous drive for baterry stacker is described. Model considers mechnical part (wheels, gear and motor) losses and allows simulation of load for battery stacker dynamic parameters testing upon inclination on slant plane. Electromagnetic model of the motor considers saturation of main magnetic circuit. Inverter model incudes impact of dead times and on-state voltage drops on inverter switching elements. Last, model of accumulator is simulated as DC voltage source with internal resistance.

For computing speed increasing was created “discrete model” of inverter which has the same qualitative results for whole drive simulation.

Thanks to this complex model is possible observing of drive feature during an operation. The knowledge of behavior of the whole system (instantaneous value of DC-link voltage, magnitude of first harmonic of inverter output voltage, course of load torque and inner machine torque) can serve for optimization of inverter control processes and for optimized design of driving system.

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AN EFFICIENT BRAKING ALGORITHM FOR INTERIOR PERMANENT MAGNET SYNCHRONOUS MOTORS

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Abstract: *This paper presents an efficient braking algorithm for a permanent magnet synchronous motor drives with a diode front end rectifier. Regenerative braking energy is dissipated in stator windings which act as a braking resistor, without adding any additional braking choppers and electronic control circuits. Application of this braking algorithm results in maximum power losses in stator windings and relatively high braking torque, all within inverter current and voltage capabilities. Also, this algorithm determines braking dynamics by regulating voltage on a DC link capacitor well bellow critical limit.*

Key Words: ***Braking/Permanent Magnet Synchronous Motor.***

1. INTRODUCTION

Permanent magnet synchronous motor drives can operate in all four quadrants of torque-speed characteristics. Beside the work in motoring and generating mode, braking mode is particularly interesting for speed regulated drives. Nowadays large number of commercially available electric drives come with diode front end rectifiers (due to their low price), which have irreversible nature; hence it is not possible to drive recuperative energy back to the mains. Instead, this energy largely contributes to the raise of voltage on a DC link capacitor. A common way of solving this problem is to add switching and passive element (braking transistor and resistor) in parallel with DC link capacitor, though creating a braking chopper. Chopper maintains voltage on a DC link capacitor and dissipates regenerated braking energy. However, this device also increases drive complexity and price and decreases reliability; therefore it is worthy considering different methods for braking, which employ main motor operating features instead of using additional electronics. Holtz [1] presented and efficient braking scheme for induction motor drive with diode front end rectifier. Paper [2] deals with efficient braking methods for surface permanent magnet synchronous motors. In this paper, in order to maximize braking torque without adding any braking resistors, a braking algorithm suitable for interior permanent magnet synchronous motors that employ both permanent magnet and reluctance torque has been proposed.

2. EFFICIENT BRAKING CRITERIA

Braking methods within electrical motor drives can be classified into three main groups – inertial, soft and active braking.

a) Inertial, passive braking (coast down) is achieved simply by turning off the inverter. The whole braking process relies on rotor inertia, mechanical load, viscous and ventilating friction. This braking method has no practical value when being used at high motor speeds, due to very long stopping time. Also, this way of braking is recommended for low speeds only. In case of high speeds, where field weakening algorithm is used (with notoriously high direct axis currents), electromotive force can be relatively high (several kV). In case of high current trip situation, it is required from stator windings to be shorted, in order to protect stator stack. This on the other hand, interrupts braking process and makes it less efficient.

b) Soft braking (ramp down) represents a controlled deceleration of motor. With this type of braking, speed control loop normally follows linearly falling reference signal (speed ramp) and generates limited braking torque. Gradient of speed ramp is most commonly limited by raise of DC link capacitor voltage due to appearance of recuperative braking energy. The value of stator current in the case of soft braking is not necessarily the highest possible and therefore it is not possible to dissipate complete braking energy, nor give maximum braking torque. This braking method gives good results for mid and low speed ranges, but still it is not the most efficient method.

c) Active braking provides maximum braking torque, by having maximum dissipated power (losses) in motor stator windings. To achieve maximum losses in stator copper, stator current has to be highest possible, which is normally constrained by inverter capabilities. This is the most efficient and the fastest braking method which results with the shortest stopping time.

In order to get optimal torque during active braking sequence, it is pertinent to define three criteria that have to be met:

1) DC link capacitor voltage has to be limited to a maximum allowable value that prevents capacitor destruction (dielectric breakthrough).

2) Maximization of stator current within voltage and current inverter limits has to result in quickest dissipation of generated energy.

3) Braking torque has to be maximized in order to reduce motor braking (stopping) time.

3. ACTIVE BRAKING WITHIN VECTOR CONTROLLED IPMSM DRIVE

In case of vector controlled interior permanent magnet synchronous motor (IPMSM) drive, definition of active braking scheme is effectively a definition of reference current trajectories in d-q reference frame. Starting point for definition of these trajectories is a mathematical model of interior permanent magnet synchronous motor in d-q synchronously rotating reference frame [3]:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} R_s + sL_{sd} & -\omega_e L_{sq} \\ \omega_e L_{sd} & R_s + sL_{sq} \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_e \psi_m \end{bmatrix} \quad (1)$$

$$T_e = \frac{3}{2} p i_{sq} \left[\psi_m + \left(L_{sd} - L_{sq} \right) i_{sd} \right] \quad (2)$$

where v_{sd} and v_{sq} are d and q-axis stator voltages, i_{sd} and i_{sq} are d and q-axis stator currents, R_s is stator phase resistance, L_{sd} and L_{sq} are d and q-axis stator synchronous inductances, ψ_m is flux linkage of rotor permanent magnets, ω_r is rotor mechanical speed, p is number of rotor pole pairs, $\omega_e = p\omega_r$ is rotor electrical speed and T_e is electromagnetic torque.

Power generated during braking can be defined with following expression

$$P_g = T_e \omega_r \approx \frac{3}{2} p \psi_m i_{sq} \omega_r \quad (3)$$

Reluctance component of electromagnetic torque can be neglected in this case, assuming that ZDAC (*Zero D-Axis Current*) control strategy is being used. Also, in the case of IPMSM motors, inductance L_{sq} is generally greater than L_{sd} resulting in negative reluctance torque for positive values of i_{sd} current. Due to very high value of braking currents, stator core (iron) losses are negligible in comparison with stator copper losses ($P_{Fe} \approx 0$). The copper losses in stator windings can be expressed as

$$P_{Cu} = \frac{3}{2} R_s \left(i_{sd}^2 + i_{sq}^2 \right) \quad (4)$$

DC link capacitor voltage is highly dependant on the difference between generated and dissipated power in stator windings, and by simultaneous regulation of both powers it is possible to meet first criterion (limitation of DC link capacitor voltage). Available d and q-axis currents have to meet a power limit condition, which dictates that dissipated power (4) has to be greater or equal than regenerated (braking) power (3) ($P_{Cu} \geq P_g$):

$$i_{sd}^2 + \left(i_{sq} + \frac{p\psi_m \omega_r}{2R_s} \right)^2 \geq \left(\frac{p\psi_m \omega_r}{2R_s} \right)^2 \quad (5)$$

This curve, when represented in d-q plane has form of an ellipse with the centre in (0, $-p\psi_m\omega_r/2R_s$). To maximize braking power, q-axis current must be maximized, whilst at the same time, both d and q-axis current must meet inverter current and voltage boundaries (second criterion). The d-axis and q-axis voltages v_{sd} and v_{sq} are limited by the maximum available output voltage of the inverter V_{smax}. Since maximum available inverter voltage is a function of instantaneous DC bus voltage and assuming that inverter can operate also in overmodulation, voltage limit imposed through stator currents i_{sd} and i_{sq} can be formulated as (limiting curve is an ellipse in d-q plane with the centre in ($-\psi_m/L_{sd}$, 0)):

$$\left(\frac{L_{sd}}{L_{sq}} \right)^2 \left(i_{sd} + \frac{\psi_m}{L_{sd}} \right)^2 + i_{sq}^2 \leq \left(\frac{V_{s\max}}{p\omega_r L_{sq}} \right)^2 \quad (6)$$

In order to avoid overmodulation region, a common practice is to adopt that maximum available output voltage equals fundamental voltage harmonic (which is $2V_{dc}/\pi$ for wye and $3V_{dc}/\pi$ for delta connected stator). Current limit of inverter in d-q reference frame can be defined as:

$$\sqrt{i_{sd}^2 + i_{sq}^2} \leq I_{s\max} \quad (7)$$

where I_{smax} is a peak inverter current, and the whole limiting curve represents a circle in d-q plane.

During braking from high speed, power limit and voltage limits (5) and (6) are applied simultaneously on reference values of i_{sd} and i_{sq} currents. The voltage boundary angular speed for which current under the voltage limit reaches that of the current limit (7), is given by

$$\omega_{rv} = \frac{V_{s\max}}{p(L_{sd} I_{sw\max} + \psi_m)} \quad (8)$$

Bellow speed ω_{rv}, reference stator currents are governed by power and current limits (5) and (7). The trajectory of stator current space vector during optimized active braking is shown in Fig. 1.

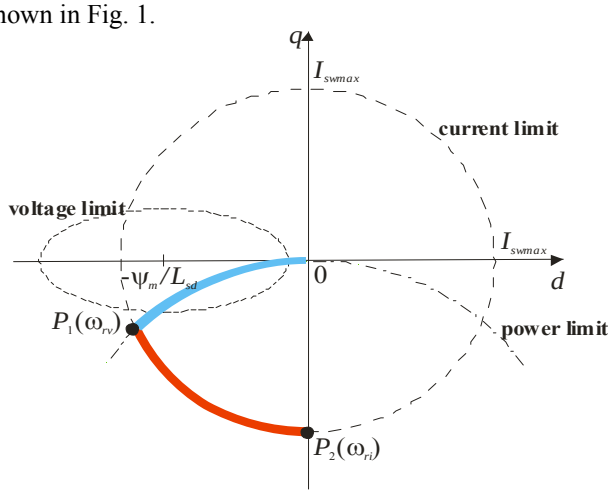

Fig. 1 *Trajectory of stator current space vector during braking*

During operation in area limited by power and current, stator current vector is shifted towards q-axis, finally having zero direct component and maximum negative quadrature component currents (i_{sd} = 0, i_{sq} = $-I_{swmax}$) at rotor angular speed

$$\omega_{ri} = \frac{R_s}{p\psi_m} I_{sw\max} \quad (9)$$

Bellow speed ω_{ri}, regenerated power is lower than maximum dissipated power in stator windings. Reference current trajectories for d and q-axis currents can be derived as functions of rotor angular speed ω_r with different equations for different speed regions (defined with boundary values ω_{ri} and ω_{rv}).

$$i_{sdref} = \begin{cases} -\left(\frac{\psi_m}{L_{sd}} + \frac{V_{s\max}}{pL_{sq}\omega_r} \right) & ,\omega_r > \omega_{rv} \\ -I_{swmax} \left[1 - \left(\frac{R_s}{p\psi_m\omega_r} \right)^2 \right]^{1/2} = -\left(I_{swmax}^2 - i_{sqref}^2 \right)^{1/2} & ,\omega_{ri} < \omega_r \leq \omega_{rv} \\ 0 & ,\omega_r \leq \omega_{ri} \end{cases} \quad (10)$$

$$i_{sqref} = \begin{cases} -\frac{R_s}{p\psi_m\omega_r} \left(\frac{\psi_m}{L_{sd}} + \frac{V_{s\max}}{pL_{sq}\omega_r} \right)^2 = -\frac{R_s i_{sdref}^2}{p\psi_m\omega_r} & ,\omega_r > \omega_{rv} \\ -\frac{R_s}{p\psi_m\omega_r} I_{swmax}^2 & ,\omega_{ri} < \omega_r \leq \omega_{rv} \\ -I_{swmax} & ,\omega_r \leq \omega_{ri} \end{cases} \quad (11)$$

Fig. 2 shows the proposed control block topology applied during active braking in discrete z domain. Operating regions during braking are determined by the actual motor speed, which also determines which particular equation may be used to calculate reference d and q-axis currents i_{sdref} and i_{sqref}. Reference signal V_{dcmax} in voltage PI regulator serves to limit DC link capacitor voltage. If the braking power exceeds maximum system losses ($P_g > P_{Cu}$), then this regenerated power has to be reduced. Otherwise, it can significantly contribute to the raise of DC link capacitor voltage. In case of motoring, $V_{dc} < V_{dcmax}$ and consequently $\Delta i_{sqref} < 0$, which contributes to the motoring torque, having $i'_{sqref} > 0$. However, in the case of regenerative braking (having $i'_{sqref} < 0$), for $V_{dc} > V_{dcmax}$ output of voltage PI regulator gives positive corrective value $\Delta i_{sqref} > 0$ which decreases amount of braking torque.

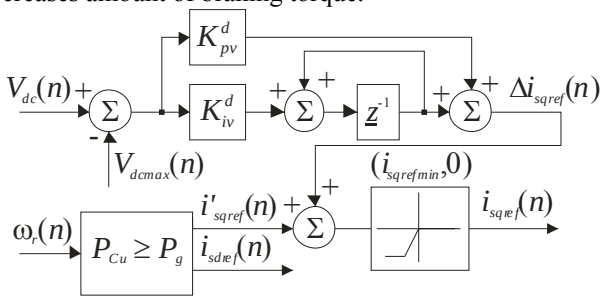

Fig. 2 *Block-diagram of braking control system*

4. SIMULATION RESULTS

An extended set of simulation tests has been performed for performance investigation of proposed braking scheme. The data of the 1.1 kW IPM synchronous motor for simulation setup are collected in Table 1. Motor has rated voltage of 230Vrms and rated speed of 3500rpm. Maximum mechanical speed is 8000rpm. Maximum inverter current is 10A, whilst maximum voltage on a DC link capacitor is 500V. IPMSM drive operates at 20 kHz switching frequency, using SVPWM symmetrical switching pattern. Current regulation loop works at 10 kHz and speed regulation loop works at 500Hz. Also, PI current loop bandwidth is tuned at 500Hz and PI speed loop bandwidth is tuned at 20Hz. To improve current regulation dynamics, both magnetic decoupling and electromotive force feed forward compensations have been included in current regulation scheme.

Table 1. *IPMSM motor data and parameters*

Quantity	Symbol	Value
Torque constant	K_t	0.61 Nm/A
EMF constant	K_e	0.039 V/rpm
Viscous friction	K_{vf}	5.5E-6Nm/rpm
Stator resistance	R_s	2.4Ω
Rotor inertia	J	1.6E-5kgm^2
Pole pairs	p	2
PM flux linkage	ψ_m	0.123Wb
d-axis inductance	L_{sd}	5.7mH
q-axis inductance	L_{sq}	12.5mH

Figure Fig. 3 shows commanded rotor speed signal ω_{rref} and actual speed ω_r during active braking sequence. In Fig. 4 it is possible to see waveforms of stator i_{sd} and i_{sq} currents during steady state and braking period. In steady state, i_{sq} has positive value and i_{sd} has zero value. During braking, i_{sd} starts with a large negative value which quickly falls down to zero; meanwhile i_{sq} falls from positive value (motoring torque) to negative value (braking torque).

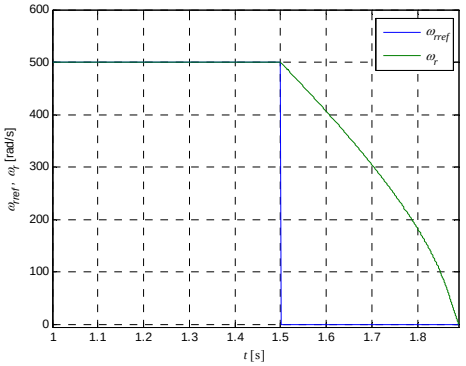

Fig. 3 *Reference and actual motor speed during braking*

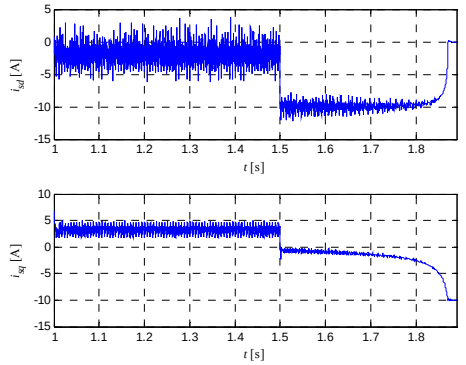

Fig. 4 *Stator d and q-axis currents during braking*

Fig. 5 depicts traces of DC link capacitor voltage V_{dc} and DC link current I_{dc}. Raise of V_{dc} during braking is easily noticeable. However, in this case, due to relatively light load (approx. 1Nm), instantaneous value of V_{dc} never crossed limiting value V_{dcmax}, and hence never activated voltage PI regulator. Figure Fig. 6 shows motor input (electrical power) p_e which equals zero during braking interval, and also waveforms of motor electromagnetic torques (both real and estimated values T_e and T_{eest}, respectively) which vary from 2Nm (motoring) to almost -4Nm (braking).

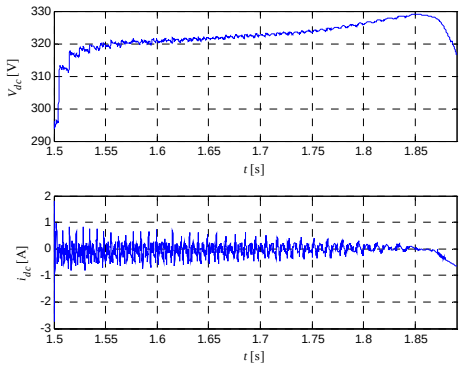

Fig. 5 *DC link voltage and current during braking*

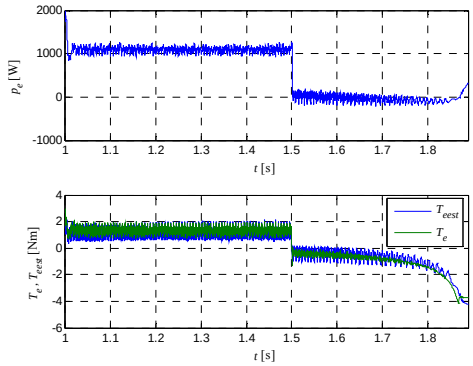

Fig. 6 *Motor electrical power and electromagnetic torque during braking*

5. CONCLUSION

A braking algorithm for interior permanent magnet synchronous motor drives has been proposed. Also, different operating modes within the inverter voltage and current limits have been analyzed. Regenerative braking power is regulated indirectly, thru stator d and q-axis currents regulation, using pre-defined current trajectories which maximize braking torque. The whole system operates within inverter voltage and current capabilities, having DC link capacitor voltage maintained bellow critical limit by using an additional PI regulator.

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MODULAR TRANSFORMER WITH ANY TURN-TO-TURN RATIO

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Abstract: *Modular transformer, based on coaxial primitive transformers, of one-to-one turns ratio, is described in the paper. The proposed transformer is arranged in m-modules that in turn are built from primitive transformers. The description is based on theory, FEM analysis and measurements. It confirmes the transformer has higher efficiency and higher coupling coefficient between windings than those of classical ones.*

Key Words: ***Modular/ transformer/turn-to-turn ratio/efficiency/FEM***

1. MOTIVATION

The need for the transformer of the possible highest efficiency and the possible highest coupling between primary and secondary has motivated this work. The coaxial transformer based on single transformers each of which has one turn of primary and one turn of secondary [1], [3] is a candidate of such searched solution.Using single transformers it is possible to build transformer of near any turn-to-turn ratio.

2. IDEA

Fig.1 presents a *n-module* thet is built-up from *n* of single transformers of one turn of primary and one turn of secondary. In sequel the single transformer is called primitive transformer. The primary windings of primitive transformers are in series connection and secondary windings are parallely connected. Such connection guarantees the equal load of single primitive transformer. The secondary voltage is *1/n* of voltage of the primary. The *n-module*'s turn-to-turn ratio is given by formula (1).
The *n-module*'s turn-to-turn ratio of such module (Fig. 1) is limited to integer number.

$$k = \frac{U_1}{U_2} = \frac{U_1}{\frac{1}{n} \cdot U_1} = n \qquad (1)$$

where:
- k - *n-module* turn-to-turn ratio
- U_1 - primary voltage
- U_2 - secondary voltage
- n - number of primitive transformers.

In general case the transformer' turn-to-turn ratio differs from integer number *n*, therefore it is necessary to combine *m* different modules where each one consists of n_i primitive transformers. The arrangement of such transformer, is depicted in Fig. 2. It is called modular transformer. The voltage of secondary winding of modular transformer is given by formula (2).

$$U_2 = U_1 \cdot \sum_{i=1}^{m} \frac{1}{n_i} \qquad (2)$$

where:
- m - number of modules
- n_i - number of primitive transformers in a module *i*.

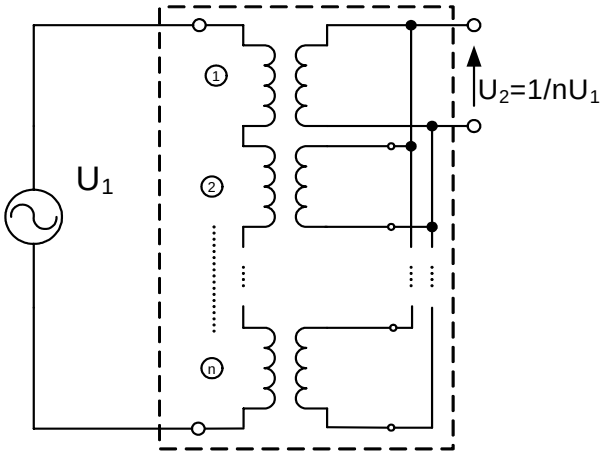

Fig. 1. *n-module*

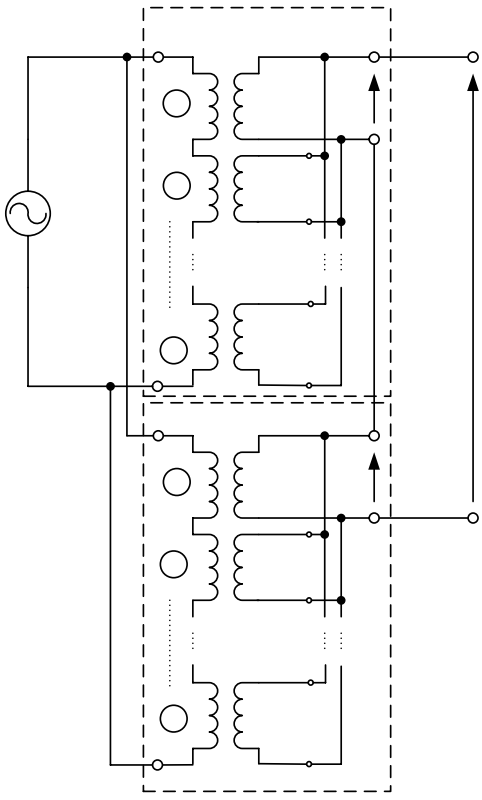

Fig. 2. *Example of modular transformer with (m=2, with any n_1, n_2)*

Therefore the turn-to-turn ratio for *m* modules that each of them consists n_i primitive transformers is described by formula (3).

$$k = \frac{U_1}{U_2} = \frac{U_1}{U_1 \cdot \sum_{i=1}^{m} \frac{1}{n_i}} = \frac{1}{\sum_{i=1}^{m} \frac{1}{n_i}} \tag{3}$$

Example:

The example transformer that consists 5 primitive transformers connected into two modules is depicted in Fig.3. The first module, m_1 contains 3 primitive transformers while the second one, m_2 has 2 primitive transformers. The secondary voltage of the modules $U_{21}=1/3U_1=1/3E$ and $U_{22}=1/2U_1=1/2E$ respectively. The secondary voltage of modular transformer (series-parallel connection of modules) is $U_2=U_{21}+U_{22}=5/6E$. The module turn-to-turn ratio is given by formula (4).

$$k = \frac{U_1}{U_2} = \frac{U_1}{5/6 U_1} = \frac{6}{5} = 1.2 \tag{4}$$

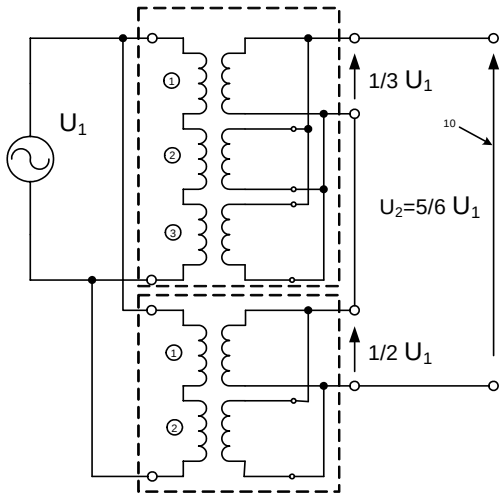

Fig. 3. *Example of modular transformer with k=1,2 (m=2, $n_1=3$, $n_2=2$)*

It is also possible to exchange the sides of the module of the transformer (Fig. 4.). In such conection secondary side voltage of single module will be equal nU_1. Turn-to-turn ratio for such case is described by formula (5).

$$k = \frac{U_1}{U_2} = \frac{U_1}{n \cdot U_1} = \frac{1}{n} \tag{5}$$

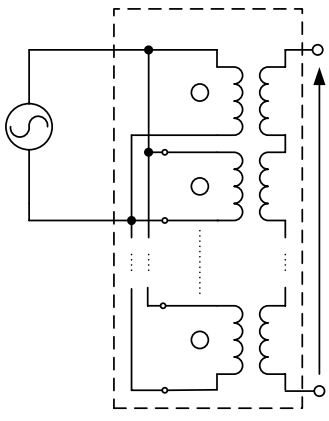

Fig. 4. *n-module*$^{-1}$

For the case of *m* modules of type *n-module*$^{-1}$, connected as in Fig. 5 the secondary voltage of such modular transformer is given by formula (6).

$$U_2 = \frac{1}{\sum_{i=1}^{m} \frac{1}{n_i}} \cdot U_1 \tag{6}$$

Using (6) turn-to-turn ratio of modular transformer is given by formula (7).

$$k = \frac{U_1}{U_2} = \frac{1}{\frac{1}{\sum_{i=1}^{m} \frac{1}{n_i}}} = \sum_{i=1}^{m} \frac{1}{n_i} \tag{7}$$

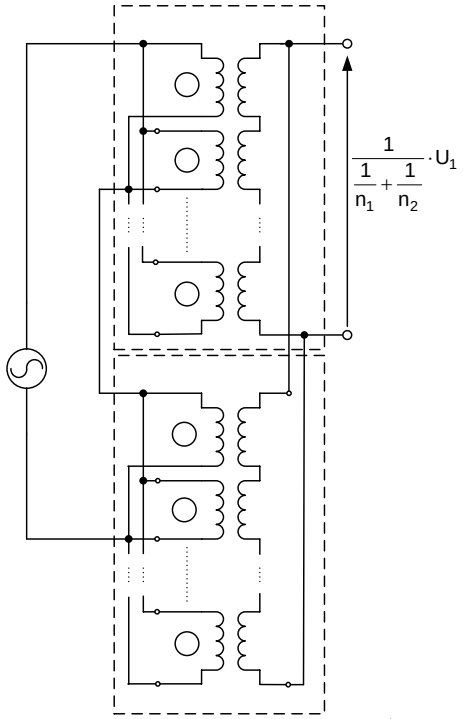

Fig. 5. *Scheme diagram of two n- modules*$^{-1}$ *transformers*

3. ANSYS MODEL

The ANSYS software (FEM) was used to computational analysis/verification of presented above idea. The model of the modular transformer with interwinding connections was created and analysed. The transformer consists of three one-to-one turn-to-turn ratio primitive transformers (cf. Fig. 8 and Fig. 7a). Turn-to-turn ratio of the whole examined transformer is *k=3/2.* Each primitive transformer consists of two segments, which cross-section is shown in (Fig. 6). Length of each segment is 50 mm. There are three primitive transformers, each having two segments connected in series. The windings are made of copper coaxial pipes that are put inside magnetic core (ring ferrite of 3F3 Philips Ferroxcube). The model includes losses in ferrite core. The ANSYS model has two parts. The first one is actual finite element model. The second part of the model is external circuit with interwinding connections between segments that is depicted in Fig. 7. The transformer operates at frequency of 1 MHz. ANSYS model reflects only electromagnetic of the transformer.

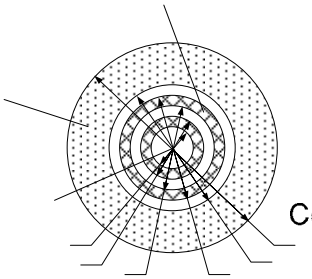

Fig. 6. *Cross-section of transformer*

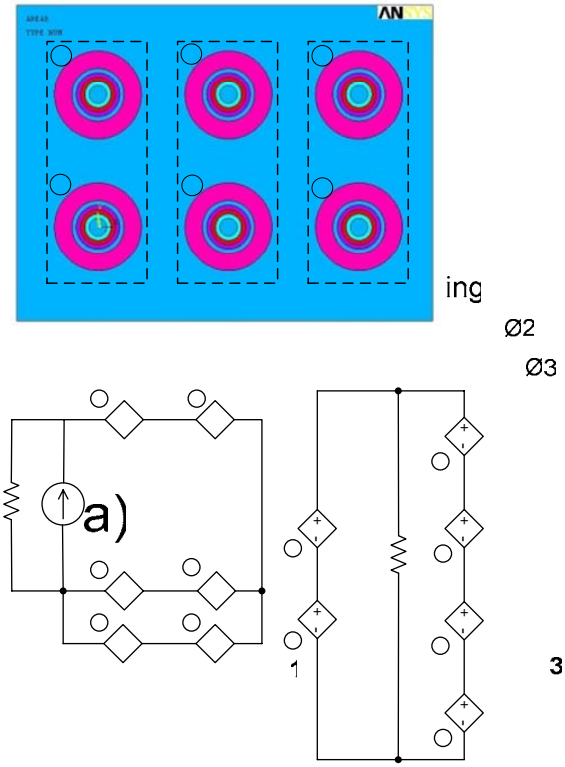

Fig. 7. *Model in ANSYS a) finite area b) external circuit of modular transformer*

4. EXPERIMENTAL TRANSFORMER

The experiment has been used to verification of the transformer operation predicted theoretically and analysed in ANSYS. The essential data of experimental transformer is given in section 3. Its photograph is presented in Fig. 8. Transformer is cooled by water flowing inside of winding pipes.

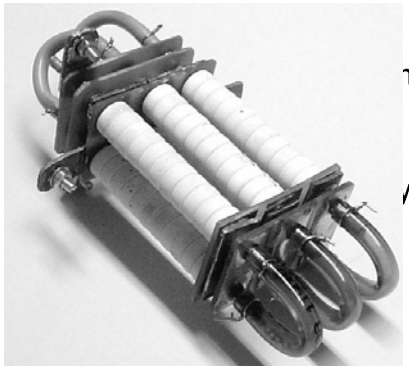

Fig. 8. *Experimental transformer*

5. RESULT OF THE CALCULATIONS AND MEASUREMENTS

5.1. Turn-to-turn ratio

The turn-to-turn ratio of transformer was calculated using ANSYS and measured by oscilloscope waveforms. Transformer was connected to output of sinusoidal voltage generator at 1 MHz of frequency . The input and output voltage are shown in Fig. 8.

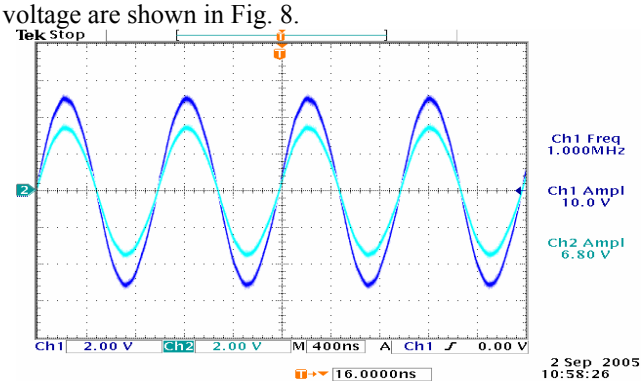

Fig. 9. *Voltage waveforms of transformer*

The results obtained analytically, derived in ANSYS calculations and from laboratory test are gathered in Table 1.

Table 1. *Turn-to-turn ratio*

Theoretical	ANSYS	Experimental
1.50	1.50	1.47

5.2. Currents in the transformer

Currents in each of transformer winding were calculated using ANSYS. The current distribution was calculated in each primitive transformers separately. The results of calculation of currents marked in Fig. 10 are given in Table 2.

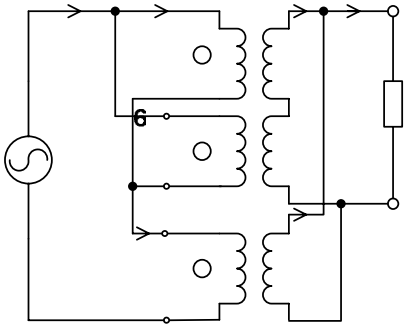

Fig. 10. *Scheme of windings configuration in experimental transformer*

Table 2. *Currents of transformer*

Current	Theoretical	ANSYS
I_1	15 A	15 A
I_{11}	7,5 A	7.5 A
I_{12}	15 A	15 A
I_2	22.5 A	22.47 A
I_{21}	7.5 A	7.49 A
I_{22}	15 A	14.98 A

5.3. Efficiency

The efficiency of modular transformer was calculated using ANSYS. Calculated efficiency was made under assumption that maximum power loss in transformer is 20 watts. Efficiency diagram are shown in Fig. 11. The maximum efficiency of the transformer is 99.24 % where the copper loss is 10.91 W and the ferrite core loss is 9.09 W. The output power of the transformer is 2.6 kW at the highest efficiency.

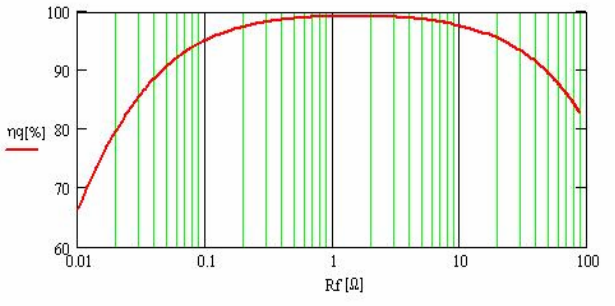

Fig. 11. *Efficiency vs. output resistance calculated using ANSYS*

The coefficient of coupling of the experimental transformer taken from ANSYS analysis is 0.9996.

To obtain efficiency by measurements the transformer was supplied by E class DC/AC inverter at 1MHz frequency. The output was loaded by resistance 1.12 Ω.

The measurement of efficiency was realized using calorimetric method. The load was cooled by water where water flow and inlet and outlet temperatures were measured. Because the load was thermally insulated the output power can be expressed as (8):

$$P = c \cdot d \cdot f \cdot \Delta T \tag{8}$$

where:

P - active power
c - specific heat (4186 J/kgK)
d - water density (982 kg/m^3)
f - flow
ΔT - temperature rise

The losses of the transformer is given by the same formula (8).

Efficiency diagram of the experimental transformer are shown in Fig. 12.

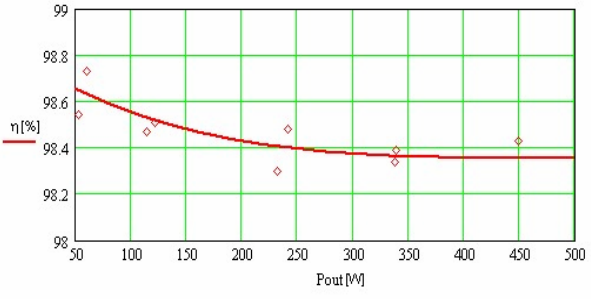

Fig. 12. *Efficiency vs. output power of experimental transformer*

For the outputs power equal 500 W, the results are in Table 3.

Table 3. *Efficiency at P_{out}=500 W*

ANSYS	Experimental transformer
99.2%	98.4 % (~98.36)

The resulted figures of efficiency confirm that the efficiency is virtually not dependent on the output power.

6. UTILIZATION OF TRANSFORMER

6.1. Utilization coefficient

The proposed transformer has some drawbacks. A part of constructional difficulties its power utilization is lower than in classical transformer. The power utilization is measured by utilization coefficient K_u. This notion and its definition is elucidated basing on the experimental transformer (section 4). The reference for coefficient K_u is installed power of the transformer that is given by the (8)

$$P_i = \sum_{1}^{2 \cdot n_i} U_k \cdot I_k \tag{8}$$

where:

n_i – number of primitive transformers
U_k, I_k – RMS value of rated voltage and rated current of winding k

Each primitive transformers in modular transformer operates under different voltage and current. Therefore for calculation of utilization coefficient one should calculate quantity called actual power P_a, defined by formula (9) . It reflects actual total load on the transformer that is derived from the actual load on each primitive transformer.

$$P_a = \sum_{1}^{2 \cdot n_i} U_{ak} \cdot I_{ak} \tag{9}$$

where:

U_{wk}, I_{wk} – RMS value of actual voltage and actual current of winding k

Therefore utilization coefficient is given by (10).

$$K_u = \frac{P_a}{P_i} = \frac{\sum_{1}^{2 \cdot n_i} U_{ak} \cdot I_{ak}}{\sum_{1}^{2 \cdot n_i} U_k \cdot I_k} \tag{10}$$

The utilization coefficient is defined assuming that modular transformer is built using the same primitive transformers. It means that the coefficient is calculated due to the worst case. For experimental transformer that is in scope of analysis utilization coefficient is described by the (11).

$$K_u = \frac{P_a}{P_i} = \frac{1}{n_i} \sum_{l=1}^{n_m} \frac{1}{n_l} \tag{11}$$

where:

n_m – number of modules
n_l – number of primitive transformers in module.

Inserting n_m, n_l into (11) one obtains (12) that is not high value.

$$K_u = \frac{1}{n_i}\left(\frac{1}{n_1} + \frac{1}{n_2}\right) = \frac{1}{3}\left(\frac{1}{1} + \frac{1}{2}\right) = 0.5 \tag{12}$$

6.2. Power density

To calculation of power/mass density (W/kg) and power/volume density (W/m^3) is made assuming that maximum total power losses in transformer are 20 W. Since the mass of experimental transformer is 100 g at the output power of 2.6 kW the power density is 25 kW/kg. Power/volume density is 19 W/cm^3. Assumed 20 W of the total losses of the transformer have been taken with safety margin. The analysed transformer can dissipate much higher losses than 20 W. Therefore the power/mass density and the power/volume density are much higher. It is necessary to add that typical power/mass density of power electronics transformers reported in literature is several kW/kg (typical range 0.1-25 kW/kg).

6. CONCLUSION

1. It is possible to construct modular transformer of turn-to-turn ratio that this integer or rational number.
2. Comparing with classical transformers modular transformer has higher efficiency and higher coupling between primary and secondary windings.
3. Utilization of transformer is less then one, and depends on number of modules and number of primitive transformers in module. In mass production it could be closer to one when diversity of construction of primitive transformers is permitted.
4. In the future the modular transformer should be compare with multiturn coaxial winding transformer [4]
5. The future research work should be devoted to technological aspects of the proposed transformer and to its features at lower frequencies.

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A UNIVERSAL A/D CONVERTER PROTOCOL DEVICE FOR LOGGING TOOLS APPLICATIONS

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Abstract: *In this paper an implementation of the universal A/D converter protocol device for logging tools applications is presented. This device is used for conversion analog to digital data from sensors in logging tools and a communication between a Telemetry system, a Surface unit, and logging tools. These tools have analog outputs and can be used for measurement of pipe diameter, pressure and temperature in boreholes. The communication is done according to SIPLOS (Simultaneous Production Logging String) protocol used by Hotwell company [1] as a part of a larger system for borehole investigations.*

Key Words: ***A/D conversion, communication protocol, borehole, measurement, logging tool.***

1. INTRODUCTION

Systems for boreholes investigation [2] consist of: a Surface unit for analysis and presentation of measurement results, logging tools, a cable for mechanic and communication link between logging tools and the Surface unit and equipment for relocating tools (Fig. 1).

Digital systems for borehole measurement measure more parameters at the same time than analogue systems. Because of this advantage, the process of logging is much shorter and cheaper. Establishing digital systems the complexity of processing data from sensors and communication between tools and the Surface unit are larger. At the same time, more parameters are measured and processed data are sent to the Surface unit. Because of larger number of sensors and electric devices for processing data and smaller dimensions of digital tools than analogue tools, projecting of mechanical parts and PCBs (Printed Circuit Board) are much more difficult. Digital logging strings are smaller, more reliable and more effective for processing and storing data than analogue logging strings.

The digital system for borehole investigation – SIPLOS consists of the Surface unit, the Telemetry tool and other tools in a logging string. The SIPLOS is projected to work in high temperature conditions, up to 180ºC and under high pressure, up to 103.4 MPa (15000 psi). Logging tools have to be very reliable because these measurements are very expensive, take a lot of time and should be completed in the first attempt.

The Surface unit is located in a special motor vehicle near the borehole pipe, where the measurement is performed. It provides, via a cable, DC supply for logging tools. The Surface unit consists of a computer with Warior software which collects, processes and shows graphical and numerical formats of data. There is also a control table for display of the voltage that supplies the tools and current that is necessary for the tools. Warior is a universal program for display of data from various types of tools. In addition, there is a possibility for calibrating and adjustment of data received from boreholes.

There are also programs for analyzing measured values. Based on this analysis, the final report of a borehole potential is done.

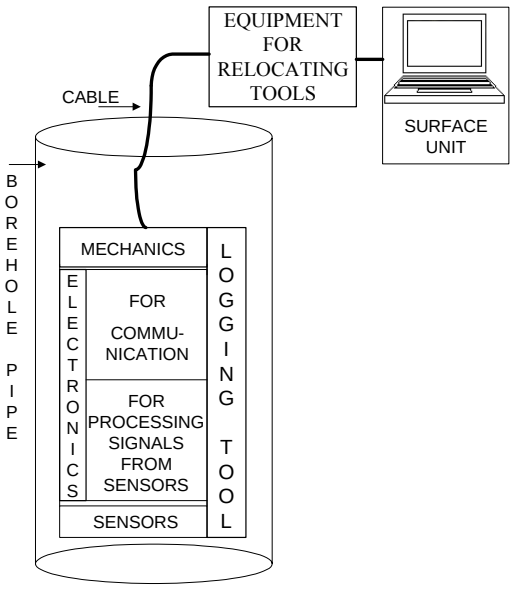

Fig. 1. *A block diagram of a system for boreholes investigation.*

2. THE UNIVERSAL A/D CONVERTER PROTOCOL DEVICE

The universal A/D converter protocol device performs the following functions:

- The measurement and converting bipolar voltage input levels to unipolar ones and the A/D conversion of the 11 analog signals from sensors in logging tools.
- Communication between logging tools, the Telemetry system and the Surface unit (which synchronizes and transmits measured data in accordance with the SIPLOS protocol).

The universal A/D converter protocol device has two functional parts (Fig. 2):

- An analog section, which converts bipolar voltage input levels to unipolar, consists of an analog multiplexer 16/1 and operation amplifiers. An unipolar voltage is necessary because the A/D converter in a microcontroller PIC 16F819 works only with positive input voltage. Operation amplifiers are used as buffers and noninverting summator.
- A digital section is built around the Microchip's microcontroller PIC 16F819 (or similar pin compatible: PIC 16F818). The microcontroller collects analog data from sensors, the A/D conversion algorithm and line driving according to the SIPLOS protocol.

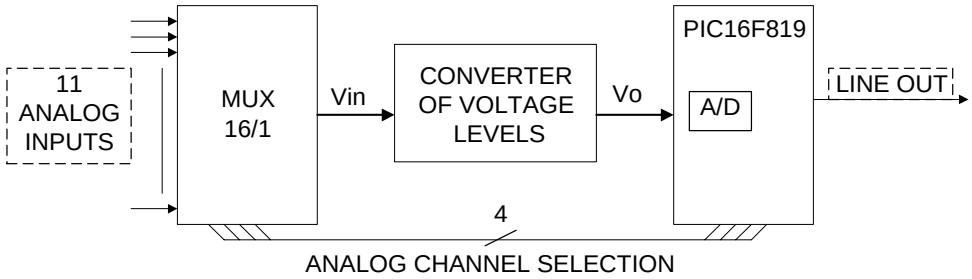

Fig.2. *A block diagram of the universal A/D converter protocol device*

The converter of voltage levels has operation amplifiers used as buffers and noninverting summator (Fig. 3).

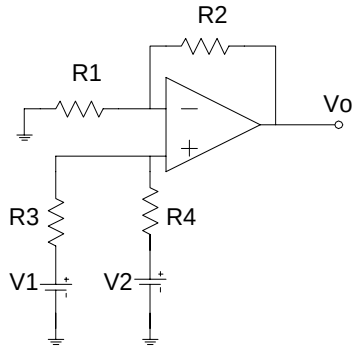

Fig. 3. *Noninverting summator.*

The output equation of this circuit is

$$V_o = \left(1+\frac{R_2}{R_1}\right)\left[V_2 + \frac{R_4}{R_3+R_4}\left(V_1 - V_2\right)\right]. \quad (1)$$

More simple equation is

$$V_o = \left(1+\frac{R_2}{R_1}\right)\frac{V_1+V_2}{2}, \quad (2)$$

when we take into account that $R=R_3=R_4$.

We can transform a very wide range of bipolar voltage inputs (V_{in}) in a wide range of unipolar voltage (V_o), see Fig. 2. For example, if we have analog inputs in range of (-1,1)V and microcontroller has references for A/D: V_{REF-} = 0 V and V_{REF+} = 3.325 V. We should convert the voltage range (-1,1)V in (0, 3.325)V to obtain maximum resolution of ADC. If we take $V_1=V_{in}$, V_2=1V and $R=R_3=R_4$=10kΩ, we should take resistors R_1=4k3 and R_2=10k to obtain the required voltage interval. For this example, typical 10-bit digital representatives are:

- -1V=0_{dec}=0x00
- 0V=512_{dec}=0x200
- +1V=1023_{dec}=0x3FF

For this example, typical 8-bit digital representatives are:

- -1V=0_{dec}=0x00
- 0V=128_{dec}=0x80
- +1V=255_{dec}=0xFF

3. AN ALGORITHM FOR COMMUNICATION IN THE MICROCONTROLLER

Fig. 4. depicts the block diagram of the connection between the universal A/D converter protocol device and a line driver. The line driver is a device that converts line voltage into CMOS voltage level, discriminates pulses from a LINE signal and makes LINE_IN signal. In this project PIC 16F819 is chosen for a microcontroller, because when tested on higher temperature it worked very reliably [3]. LINE is a bi-directional signal from the Telemetry tool that consists of a line voltage (70V) and negative pulses (START, STOP, SYNC and DATA bits) according to SIPLOS protocol [4]. The line voltage is transmitted by the Surface unit to all tools. The Telemetry tool transmits START, STOP and SYNC pulses to all other tools. DATA bits are transmitted by all measuring tools to the Surface unit in a determined interval of time.

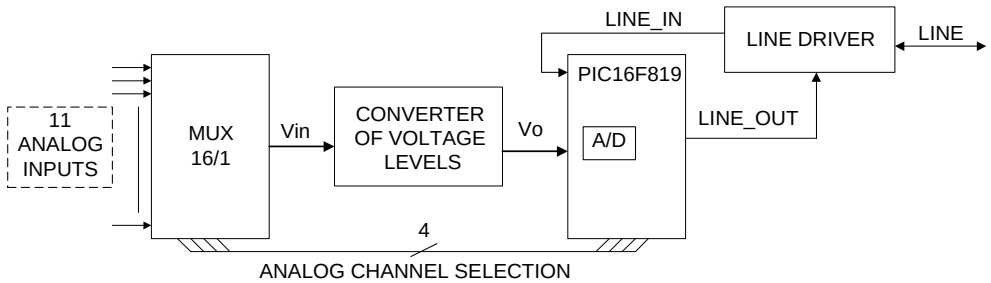

Fig.4. *The block diagram of the connection between the universal A/D converter protocol device and a line driver.*

The LINE_IN signal contains START, STOP and SYNC pulses that determine timing for sending DATA from logging tools to the Surface unit. The line driver receives a LINE_OUT signal from the microcontroller PIC 16F819. This signal is converted into corresponding pulses, positioned in the middle of a data-bit frame, whose duration is 50μs ± 10%, and sent to the Surface unit. An algorithm for programming the microcontroller has to work reliably for both high and variable temperature conditions. Oscillator's frequency (internal or RC) can be decreased even for 30%.

The algorithm for programming the microcontroller PIC 16F819 is shown in Fig. 5. There is one main part, after the initialization and sinhronization pause (16.667 ms), which is always repeated. After A/D conversion and storing digital values, all these data are summed with previous values in memory and transferred to the Surface unit every 200 ms.

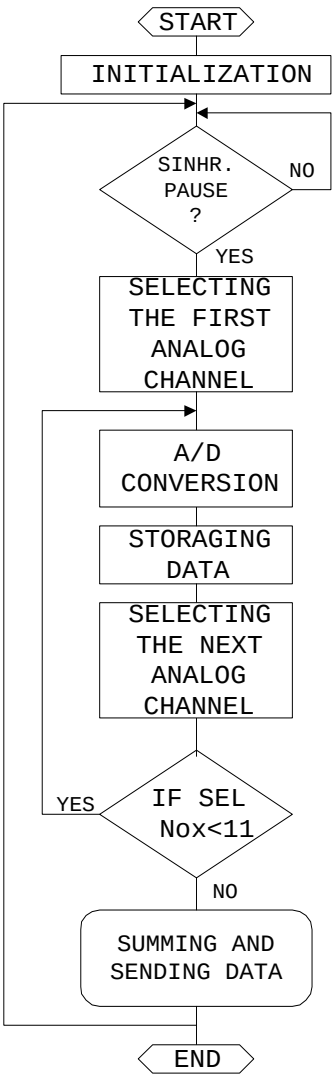

Fig. 5. *The algorithm for the PIC 16F819.*

Because of the varying internal frequency of the microcontroller clock, it is not reliable to calculate time intervals based on it. The calculating of time intervals has to be performed based on measuring timings on the LINE_IN signal. In the initial mode of measuring timings, counting the number of pulses and calculating initial parameters are performed in the interval of 200 ms. The initial parameters involve time intervals when START, STOP and DATA bits appear on LINE. If there are too many or too few pulses or their duration is not proper, the microcontroller is restarted by a Watchdog Timer. After that the measuring duration of 12 bytes and calculating parameters without modulation (sending DATA according to the SIPLOS protocol) is performed. In the normal mode the address where data should be transmitted via the LINE_OUT signal is determined. After that the modulation is performed according to the SIPLOS protocol based on measured time intervals.

The microcontroller has internal protection against software lock-up (Watchdog timer) and possible power-supply transients (brown-out reset), which ensures the necessary level of reliability and robustness of the tool.

4. SIMULATION RESULTS

Simulations of the work of the microcontroller PIC 16F819 were performed successively by MPLAB IDE [5] and PIC IDE programs. Simulator Stimulus options were used to simulate input signals. Some signals were simulated by Asynchronous Stimulus option where it is possible to change the state of a particular pin during the simulation. The LINE_IN signal was simulated by Pin Stimulus option setting the duration of sequence '0' and '1' in the SIPLOS protocol form. The output signals, SFR registers and the memory content were observed during the simulation step by step [6]. All of the input signals were simulated for the ideal and the worst temperature conditions [7] and the expected output signals were obtained.

5. EXPERIMENTAL RESULTS

The universal A/D converter protocol device was tested by using the appropriate analog input signals from a function generator, whilst the output signals were observed by an oscilloscope. These input and output signals were similar to those obtained by the software simulation. The first serial of PCBs has been made and the complete measurement system has started working in practice. The first results are very good.

6. CONCLUSION

The SIPLOS protocol is used in the digital system for borehole investigations. Digital systems measure more parameters at the same time than analogue systems. Because of this advantage, the process of logging is much shorter and cheaper. Digital logging strings are smaller, more reliable and effective than analogue logging strings. Based on the software simulation and the experimental results we can conclude that the universal A/D converter protocol device satisfies the SIPLOS protocol and works properly.

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Many thanks to Hotwell Ges. m. b. H. Austria for supporting this work.

APPLICATION OF PARAMETRIC ANALYSIS TO AUTOMATIC TESTING USING GENERAL-PURPOSE CIRCUIT SIMULATORS

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Abstract: *An approach is proposed to automatic testing of electronic circuits using PSpice-like general-purpose circuit simulators. It is based on parametric analysis. Using postprocessing of the obtained results in the graphical analyzer Probe, a pass-failed analysis is performed. By macrodefinitions in Probe, the number of detected faulty variants is calculated and the fault coverage is obtained. Parameterized faulty models are developed for generation of hard and soft faults in the circuit elements. The models are defined in the form of parameterized library elements for the Cadence PSpice simulator. An example is given illustrating the proposed approach.*

Keywords: ***Fault Modeling/ Circuit Simulation/Pspice***

1. INTRODUCTION

The fault analysis is an important step in the design and investigation of large electronic circuits and systems. A number of approaches are proposed to modeling of catastrophic and parametric faults of electronic circuits based on behavioral modeling, macromodeling, statistical modeling, etc. [1,2]. The fastest and most accurate methods for analyzing faults use CAD systems. The advantage of *PSpice*-like circuit simulators is the universally working interface combined with flexible and fast program tools [3,4,5].

The automatic investigation and diagnosis of faults is not implemented in the *PSpice* simulator. In this paper an approach is developed to automatic testing of electronic circuits using *Cadence PSpice*. The automatic fault generation in analog circuits is based on parameterized faulty models and parametric analysis using *Cadence PSpice.*

2. FAULTY MODELS OF CIRCUIT ELEMENTS

The development of faulty models is realized by the graphical editor *Cadence Capture.* It allows parameterized model definitions, which are directly converted in the circuit netlist. *Capture* offers the opportunities for creating elements and including them in the user-defined libraries.

The possibilities of the IF-THEN-ELSE statement definition in the *PSpice*-like simulators are used for construction of the parameterized faulty models of the basic circuit components.

2.1. Faulty model of a resistor

In the faulty model of a resistor there are two kinds of considered faults: catastrophic (hard) faults ("short circuit" and "open circuit") and parametric (soft) faults due to deviations from the nominal. A schematic diagram of the model is presented in Fig.1. The three faults ("short", "open" and "parametric" are modeled by voltage controlled current sources (VCCS). The VCCS controlled by its own voltage is equivalent to a resistor. The type of the sources is GVALUE, whose controlling parameter provides any transfer function.

All the parameterized values of the elements of the model are given in brackets {}. Denoted parameters in the scheme are:
p – fault number; *p* is in the range from 1 to p_{max};
k_sh – number of the fault "short circuit" of the resistor;
k_op – number of the fault "open circuit" of the resistor;
k_dev – number of the "parametric fault" of the resistor;
R_op – the resistance of an open circuit;
R_sh – the resistance of a short circuit;
pd – parameter defining the relative deviation from the nominal *R*.

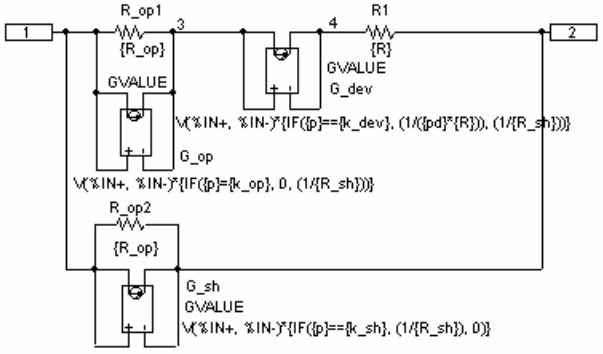


Fig. 1. *Schematic diagram of the resistor faulty model*

The VCCS element *G_op* models an open circuit. The current of *G_op* is defined in the form:

$$V(\%IN+, \%IN-)*\{if(p==k\_op,0,(1/R\_sh))\} \quad (1)$$

where *V(%IN+, %IN-)* is the control voltage.

When $p=k\_op$, the current of *G_op* equals 0 and *G_op* is equivalent to an open circuit. The resistance of the branch between nodes 1 and 3 is equal to *R_op*. When $p \neq k\_op$ the second condition is met and $G\_op = U/R\_sh$, then *G_op* is equivalent to a short circuit and *R_op1* is shortened. The resistance between nodes 1 and 3 is *R_sh*.

The VCCS element *G_sh* models a short circuit. The current of *G_sh* is defined in the form:

V(%IN+, %IN-){if({p}=={k_sh},(1/{R_sh}),0)}* (2)

When *p=k_sh*, the current of *G_sh* equals *U/R_sh*, then *G_sh* is equivalent to a short circuit and *R_op2* is shortened. The resistance between nodes 1 and 2 is *R_sh*. When $p \neq k\_sh$, the current of *G_sh* is 0. Then *G_sh* is equal to an open circuit.

The VCCS element *G_dev* models a parametric fault. The current of *G_sh* is defined in the form:

*V(%IN+, %IN-)**
if({p}=={k_dev},(1/({pd}{R})),1/{R_sh})}* (3)

When p=*k_dev* the first condition is met and the current of *G_dev* is *U/(pd*R)*, i.e. the resistance between nodes 3 and 4, defined by this source, is equal to the deviation in respect to the nominal value *R*. Then the equivalent resistance between nodes 3 and 2 is R*(1+pd). When $p \neq k\_dev$ the second condition is met and the current of *G_dev* is *U/R_sh*, which is equivalent to a short circuit between nodes 3 and 4.

When $p \neq k\_dev$, $p \neq k\_sh$, $p \neq k\_op$, the model gives a fault-free element with a nominal value *R*. Then the three VCCSs meet their second conditions: *G_op* и *G_dev* are equivalent to resistors of value *R_sh*. The VCCS *G_sh* is a resistor whose value is *R_op*. Then the equivalent resistance between nodes 1 and 2 is *R*, i.e. the nominal value.

The automatic fault generation is illustrated by a parametric analysis of the inverting amplifier shown in Fig. 2.

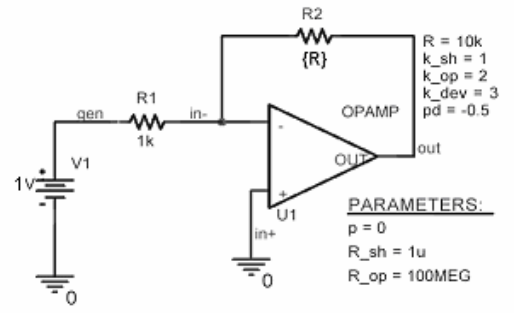


Fig. 2. *DC Amplifier with a faulty model for R_2.*

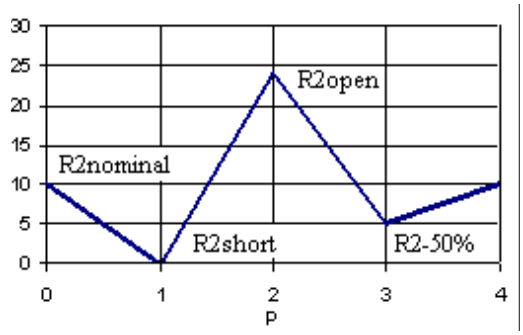


Fig.3. *Values of V(out) versus the fault number p*

The resistor R_2 is defined by the faulty model in Fig. 1. The following faults are generated depending on the parameter *p*:

$p = 0$ – R_2 is fault-free with a nominal value $R_2 = 10\text{k}\Omega$;

$p = 1$ – a "short" of R_2 ($R_2 = 1\mu\Omega$);

$p = 2$ – an "open" of R_2 ($R_2 = 100\text{M}\Omega$);

$p = 3$ – a deviation of R_2 with (-50%) ($R_2 = 5\text{k}\Omega$);

The graphical results from the simulations of the output voltage *V(out)* versus the fault number *p* are shown in Fig. 3.

The graphical analyzer *Probe* interpolates the values between the obtained values for *V(out)* when $p = 0; 1; 2; 3$ with lines. The nominal value *V*(*out*)=10V is obtained for $R_2 = 10\text{k}\Omega$ and coincides with the simulation result for $p = 0$. When $p = 1$ the value is *V*(*out*) = 1pV, which corresponds to a short circuit ($R_2 = 1\mu\Omega$). When $p = 2$ (open circuit) V(out) is limited to the OpAmp power supply. When $p = 3$ (parametric fault) $R_2 = 5\text{k}\Omega$.

2.2. Faulty model of a capacitor

In the faulty model of a capacitor both catastrophic and parametric faults are realized.

The schematic diagram of the model is shown in Fig. 4 and it is similar to the one shown in Fig. 1. The difference is in the part modeling a fault of the kind "out of the tolerance" between nodes 3 and 4.

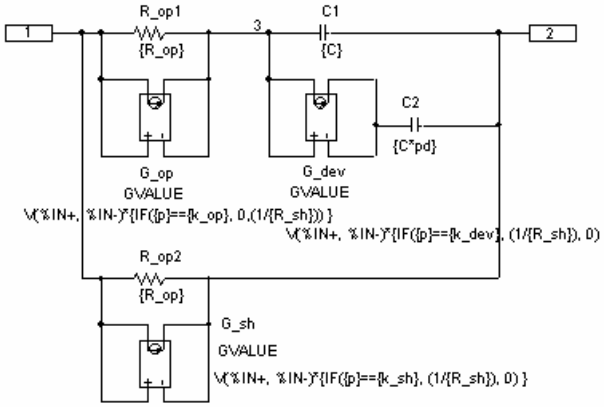


Fig. 4. *Schematic diagram of the capacitor's faulty model*

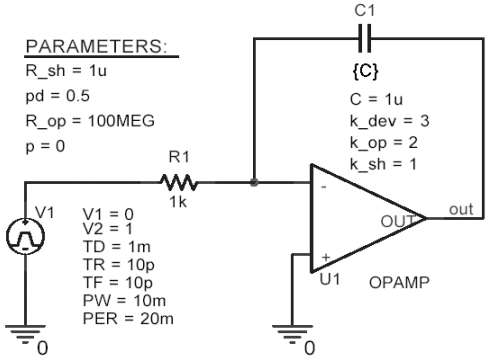


Fig. 5. *Integrator with faulty model of C*

The nominal value C of the capacitor is defined by C_1. The capacitor C_2 models the deviation C*dp from the nominal value, where pd is the relative deviation.

The VCCS element *G_dev* is equivalent to a short circuit, connecting C_2 in parallel with C_1 only when $p=k\_dev$. Then the value of the equivalent capacitor between nodes 1 and 2 is $C_{12}= C *(1+pd)$. In this case *G_op* models a short circuit and *G_sh* models an open circuit. Similarly to the resistor faulty model, all the variants of the faults can be described.

The adequate performance of the model is verified by the time-domain analysis of the integrator shown in Fig. 5. The simulation results for *V*(*out*) are shown in Fig. 6.

An impulse voltage source is connected at the input and a parametric transient analysis is carried out. The slew rate of the output voltage is observed. The steepest line of the model corresponds to a fault "open circuit" (p = 2). The next line corresponds to the nominal analysis (p = 0), the third one – to a positive deviation (+50%) from the nominal value (p = 3), and the last line (p = 1) lays on the X-axis and corresponds to a short circuit.

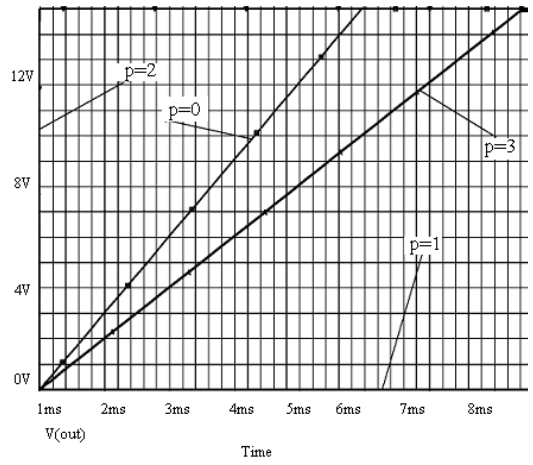


Fig. 6. *Transient response V(out) when p is a parameter*

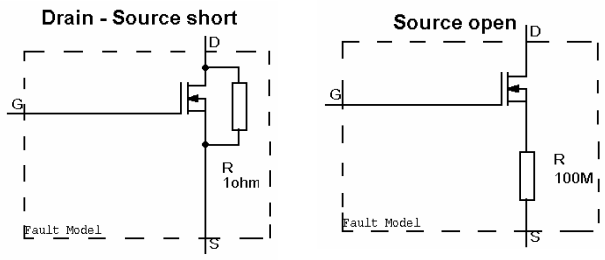


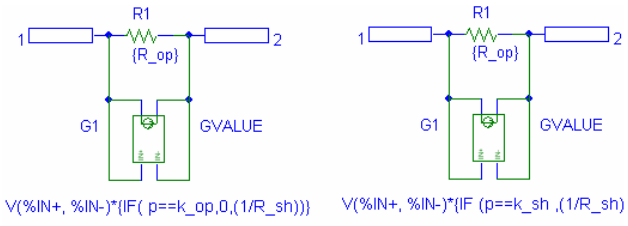
Fig.7. *Catastrophic faulty models of nMOS transistor*

2.3. Faulty model of a transistor

The catastrophic faults in a transistor are an open pin or short circuit between two pins. In Fig. 7 such models of nMOS transistor are shown. The model with shortened source and drain is presented by a resistor of value 1Ω connected between these two pins. In the model with an open source a resistor of value 100MΩ is connected in series. The other faulty models can be created in the same way.

2.4. Faulty models of an "open" and a "short" circuit

The faulty models of an "open" circuit and a "short" circuit are shown in Fig. 8.



a) b)

Fig. 8. *Faulty model of an "open" circuit(a) and of a "short" circuit (b)*

3. PARAMETERZIZED LIBRARY ELEMENTS FOR THE CADENCE PSPICE

A parameterized library element can be created in the powerful graphical editor *Capture*. The main steps of the methodology for creating a model are shown in Fig. 9. The user is guided by the intuitive instruments available in *Capture*. The presence of ready to use elements generating faults whose parameters the user can assign is the base of the automatic diagnostics.

1. Draw a circuit in *Cadence Capture*;
2. Put the parameters in parenthesis {} ;
3. Create a subcircuit of the model;
4. Make additional lines
+PARAMS:… ;
5. Save the description in a library;
6. Create a schematic symbol of the element;
7. Assign the parameters;
8. Create a *PSpice Template*;
9. Save the schematic symbol with attached model defined in a library.
10. Include the new created library to the simulator.

Fig. 9. *Basic steps for creation of the parameterized library element*

4. AN AUTOMATIC FAULT GENERATION APPROACH BASED ON STATISTICAL ANALISIS

The statistical (*Monte Carlo*) analysis can be successfully applied to pass-failed analysis using *PSpice*-like simulators. The methodology for investigating parametric faults by *Cadence PSpice* is shown in Fig. 10.

The steps 1 to 4 in Fig. 10 are standard. The specific aspect of the procedure is the creating of macros in *Probe* for finding out the faulty and faulty-free variants after the *Monte Carlo* analysis (step 5).

1. Creating electronic circuit in the graphical editor;
2. Assigning the tolerances of the circuit elements;
3. Defining the basic and Monte Carlo analyses.
4. Executing the basic and *Monte Carlo* analyses;
5. Finding out faulty and faulty-free variants from the histograms by creating macros in *Probe*;
6. Creating a table with the summarized results.

Fig. 10. *Methodology of faulty analysis using Monte Carlo analysis*

Let us denote the output characteristic under test by F_o. Its nominal value is denoted by $F_{o,nom}$.

If the maximal relative error required for the fault-free circuit is $\delta_{F\max}$, then the relative error δ_F of F_o must satisfy the following inequality:

$$\delta_F = \left| \frac{F_o - F_{o,nom}}{F_{o,nom}} \right| \le \delta_{F\max} \qquad (4)$$

Then, if the circuit is fault-free, the difference between the required maximal error and δ_F has a positive sign. When the circuit is faulty, the sign of this difference is negative. Using this function the following equations are satisfied:

$$sign\left(\delta_{F\max} - \delta_F\right) = 1 \qquad (5)$$

for the fault-free circuit and

$$sign\left(\delta_{F\max} - \delta_F\right) = -1 \qquad (6)$$

for the faulty circuit.

After the nominal and Monte Carlo analyses are carried out, all quantities for F_o are available in the *Probe* analyzer. It is possible to separate the faulty and the fault-free variants using the obtained histogram based on equations (5) and (6). The parameter *ena* is calculated for this purpose in the following way:

$$ena = 0.5\left(sign\left(\delta_{F\max} - \delta_F\right) + 1\right) \qquad (7)$$

It is seen that *ena* = 1 for the faulty-free variants and *ena* = 0 for the faulty variants.

When creating a histogram, multiplying the available calculated characteristic F_o under control by *ena* (Fo*ena) will give a zero result, thus collecting all faulty variants at zero place. Similarly, the product (Fo*(1-ena)) will put all fault-free variants at zero place.

4.1. Example

For example, the characteristic under control is the maximum output voltage in the node *in1* of the Buck-Boost DC-DC converter shown in Fig. 11 (F_o corresponds to V(in1)). The maximal required error is 1%. The maximal nominal value is (-14V).

The graphical result for V(in1) is shown in Fig. 12. The histogram of the product Max(V(in1))*ena is shown in Fig. 12b. The faulty variants, collected at the zero place in the histogram, are 16%. Thus, the yield is 84%.

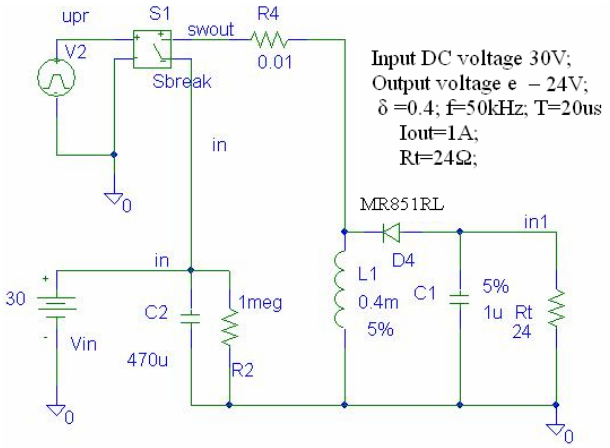


Fig. 11. *A DC-DC converter, the scheme under test*

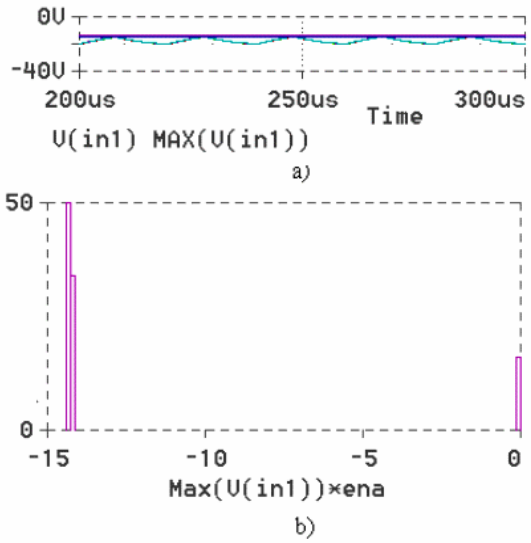


Fig. 12. *Simulation results*

5. CONCLUSIONS

An approach to automatic testing of electronic circuits using *Cadence PSpice* has been developed based on parameterized faulty models. The fault generation is reduced to a parametric analysis of the circuit. Using postprocessing of the simulation results and macrodefinitions in *Probe*, the yield is automatically obtained. An example of a power circuit has been simulated and pass-failed analysis using the approach proposed has been performed.

6. ACKNOWLEDGEMENT

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A DIRECT FOC OF A INVERTER FED INDUCTION MOTOR

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Abstract: *Speed-controlled electrical drives represent one of the technological keys of the modern industry. The field-oriented control (FOC) principle is based on the analogy between AC machines and the separately excited DC ones. Thus, the application of the space-phasors leads to a simple mathematical model of AC machines separating the active quantities from the reactive ones and so two independent control loops are obtained. This paper shows a possibility of modeling and simulation of a direct field orientation control (FOC) scheme for torque control using a voltage-regulated PWM inverter. For field orientation, controlling stator current is more direct than controlling stator voltage. A completely algorithm use Matlab-Simulink was elaborated. In this paper we will implement a simulation of a three-phase, 50 Hz, four poles, 220 V, 2.2 kW, induction motor.*

Key Words: ***direct field oriented control (FOC), voltage-regulated PWM inverter, torque control, Simulink model***

1. INTRODUCTION

The induction motor used in the adjustable drive systems raises a series of problems regarding their supply from the frequency static converters and also due to the adjusting complexity. The most important problem is the control and adjustment of the electromagnetic torque. In order to adjust the torque with high dynamic performances (with low inertia and proper damping), the adjustment proceedings based on the field orientation principle have been resorted too. The field orientation principle relies on the analogy of the alternative current machines and continuous current ones, determining the separation of the magnetic and mechanic values which, finally, leads to two independent adjusting curls, with adjusting values in continuous current.

The concept of field orientation results from the fact that the direction of the flux determines the two components of the current, the active and reactive ones, which separate the mechanic phenomena of the machine from the magnetic ones. The structure of an adjusting system conceived in relation to the field orientation principle is determined by many factors. The most important ones are: the sensors, namely the reacting values of the adjusting loop; the frequency static converter which supplies the electric motor; the flux according to which the field orientation is performed (stator, rotor or air gap).

The most frequently used orientation method, which is also exploited in the present study, is the one according to the rotor flux, because the adjusting measures simply results from the outputs of some PI controllers. This is the most often approached method in the literature due to the simplicity of the adjusting loop and to the calculation of the command measures. If the inductivity of the rotor leaks is neglected, then the air gap flux (measured and calculated) is mixed up with the rotor flux according to which the orientation is done. The errors are not, first and foremost, due to module of the flux, but to its direction, according to which the stator current orients itself, decomposing it in components that become adjusting measures. On this ground, the recent methods do not neglect the leaks inductivity of the rotor $L_{\sigma r}$. Under these circumstances, the adjusting structure is little complicated, because out of the indirect and direct measured flux of the air gap, the rotor flux must be calculated, without having any access to the rotor currents.

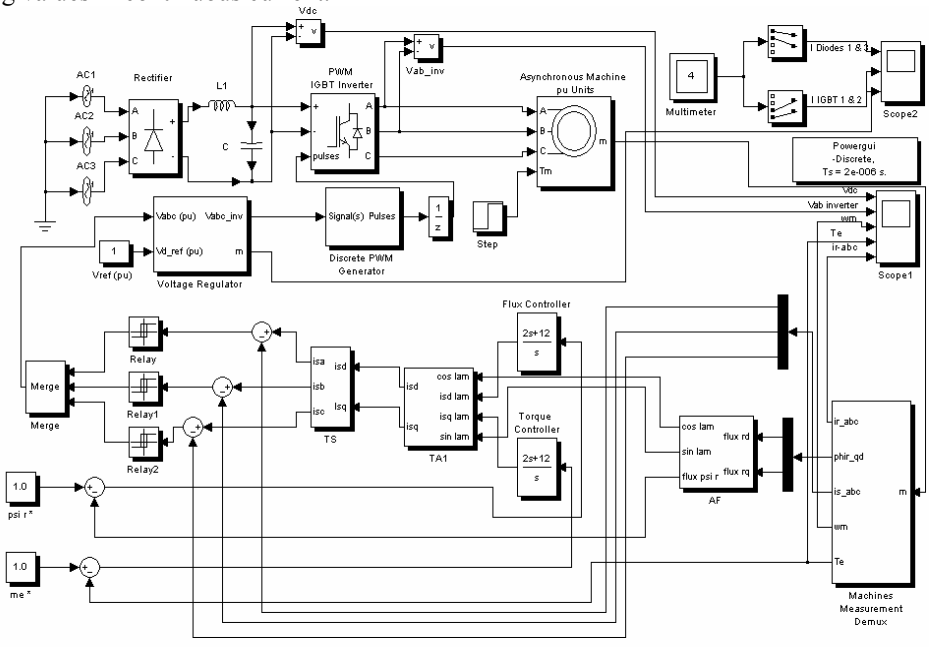

Fig. 1. *The adjusting scheme of the induction motor torque supplied through a voltage-regulated inverter with direct measure of the field and with rotor flux orientation.*

2. THE ADJUSTING SCHEME OF THE INDUCTION MOTOR TORQUE FED BY A VOLTAGE-REGULATED INVERTER

Figure 1 suggests a simulation model of a direct field orientation control (FOC) scheme for torque control using a voltage-regulated PWM inverter with orientation according to the rotor flux. The frequency static converter with intermediary continuous current circuit is composed by a rectifier and an inverter, displaying at the exit an appreciatively sinusoidal current. In the intermediary circuit the voltage is filtered. This voltage will be commuted by the inverter on the stator phases. The commutations in inverter take place according to the output current which is bi-positional controlled, following the references sinusoidal signals.

The air gap field can be measured with specially fitted search coils or Hall-effect devices placed in slots. The three-phase system of the flux is transformed with a block T (fig.2) in the bi-phase system compared to the stator axes system. In the same way is transformed the currents three-phase system.

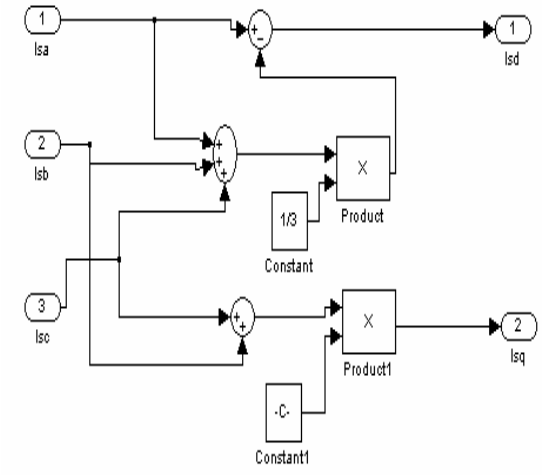

Fig. 2. *The T block.*

In the case of a three-phase machine, the current, voltages and flux sensors provide information of three-phase sizes. Also the frequency static converters need command sizes of three-phase system. Thus, on the reaction loops, in the adjusting schemes the T blocks will appear, which performs the transformation of the three-phase system sizes (g_a, g_b, g_c) in bi-phase system (g_d, g_q), based on the relations:

$$\begin{cases} g_d = g_a - g_0 \\ g_q = \dfrac{g_b - g_c}{\sqrt{3}} \end{cases} \qquad (1)$$

This transformation is given by the relation:

$$[g]_{\perp} = [A] \cdot [g] \qquad (2)$$

where [A] is :

$$[A] = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \qquad (3)$$

The inverse transformation is also necessary, namely of the bi-phase system measures in three-phase systems measures (fig.3). This is made by using the transforming block Ts, using the inverse matrix $[A]^{-1}$:

$$[A]^{-1} = \frac{2}{3} \cdot \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \qquad (4)$$

It is obtained:

$$\begin{cases} g_a = g_d + g_0 \\ g_b = -\dfrac{g_d}{2} + \dfrac{\sqrt{3}}{2} g_q + g_0 \\ g_c = -\dfrac{g_d}{2} - \dfrac{\sqrt{3}}{2} g_q + g_0 \end{cases} \qquad (5)$$

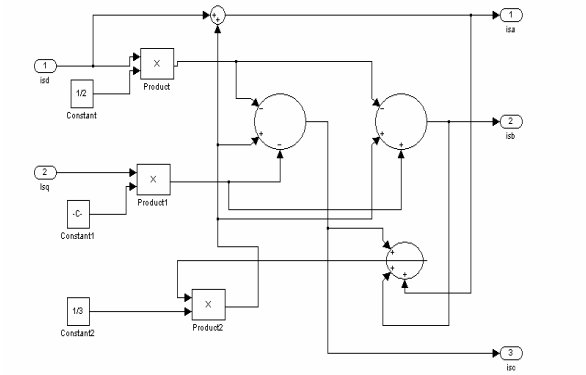

Fig. 3. *The block of the transformation of the bi-phase system in three-phase system of measures – unfolded scheme*

The components of the stator current do not present any problem because the adjusting system usually possesses these measures. In the compensation of the flux, errors can be input due to the iron saturation.

Applying the field orientation principle involves to know the position of magnetizing flux. The block which provides the information regarding the field and which does the flux orientation is the phasor analyzer block AF (fig.4).

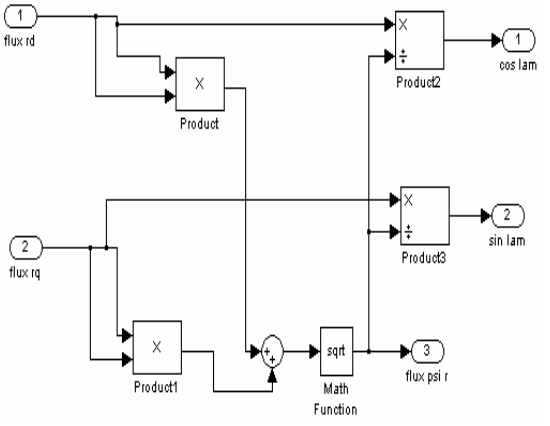

Fig. 4. *The phasor analyzer AF– unfolded scheme.*

The phasor analyzer identifies the position and the module of the flux phasor. The flux components Ψ_d and Ψ_q, reported to a fixed statoric axes system d-q are obtained through measurements or calculation.

The orientation of the stator current is done by help of the axes transformation block TA1 (fig. 5), knowing the position of λ_r of the rotor flux.

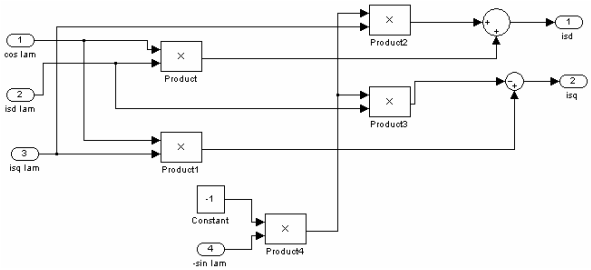

Fig. 5. *The axes transformation block TA1– unfolded scheme.*

The field orientation measures can be expressed with those of the bi-phase model, fixed in space, by the relations:

$$\begin{cases} i_{sd\lambda} = i_{sd}\cos\lambda + i_{sq}\sin\lambda \\ i_{sq\lambda} = -i_{sd}\sin\lambda + i_{sq}\cos\lambda \end{cases} \qquad (6)$$

The operations in the relations (6) are performed by the analogical or numeric TA1 block.

The imposed measures for the flux Ψ_r* and the torque m_e* are compared to the corresponding values in the motor. There result the adjusting measures i^*_{sdr} respective i^*_{sqr}, the reactive and active components of the stator current oriented after Ψ_r.

The machine's rotor is short-circuited, and the stator is fed by a PWM inverter, built with following Simulink blocks: Constant/Sources, Gain/Math Operations, Product/ Math Operations, Clock/Sources, Sum/Math Operations, Math Function/Math Operations, Trigonometric Function/Math Operations.

3. SIMULATION RESULTS

In this paper we implemented a simulation of a three-phase induction motor. The parameters of the machine are those found in the pu Units dialog box (fig. 6).

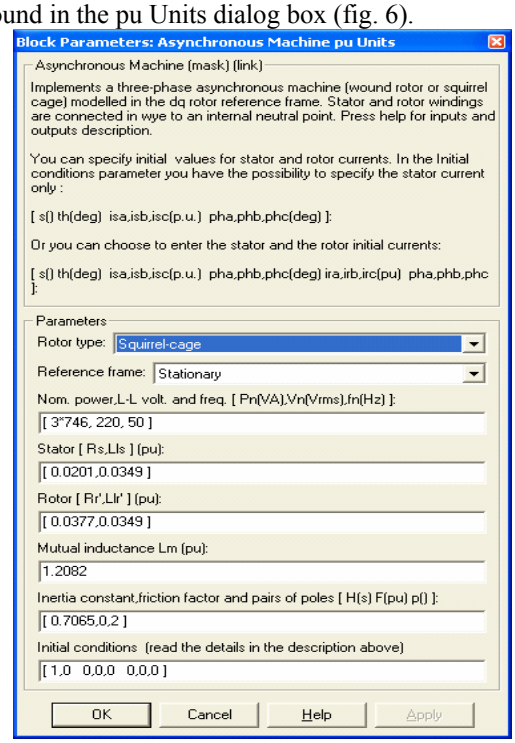

Fig. 6. *The parameters of the induction motors.*

The results of the simulation are shown in fig. 7 (Scope 2) and fig. 8 (Scope 1).

Fig. 7. *Simulation results-waveforms Scope2.*

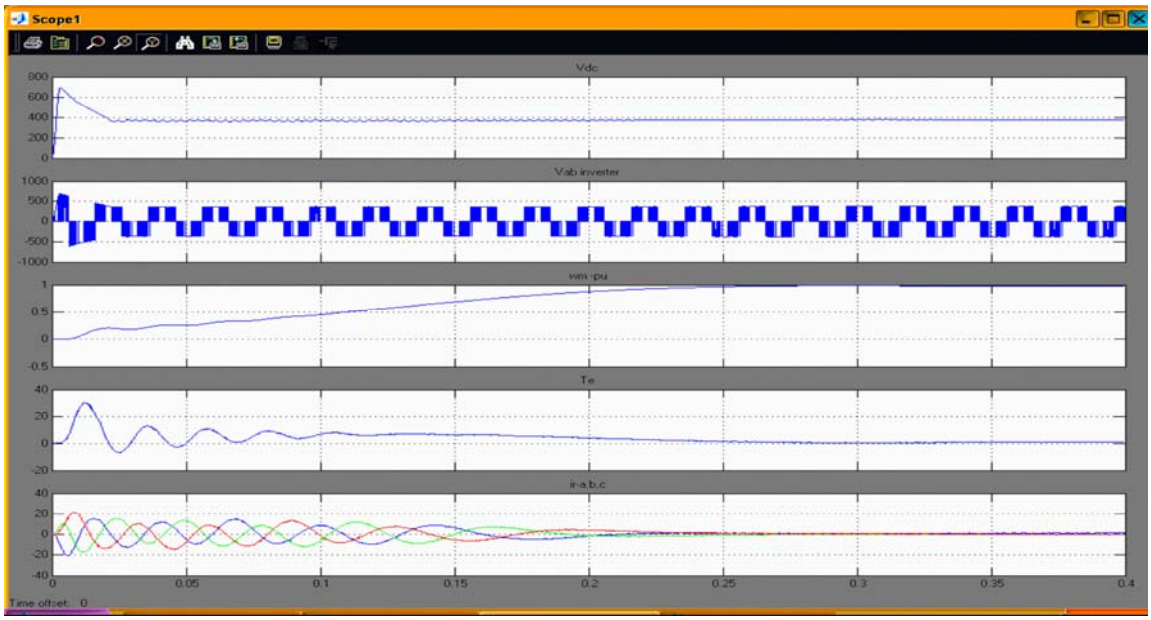

Fig. 8. *Simulation results-waveforms Scope1.*

4. CONCLUSIONS

This paper shows a possibility of modeling and simulation of a direct field orientation control scheme for torque control using a voltage-regulated PWM inverter.

A completely algorithm uses Matlab-Simulink was elaborated. In this paper has been implemented a simulation of a three-phase, 50 Hz, four pole, 220 V , 2.2 kW, induction motor.

5. REFERENCES

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FPGA IMPLEMENTATIONOF AN RFID HUB

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Abstract: *What exactly is RFID? RFID stands for Radio Frequency Identification. A typical system consists of a radio-enabled device that communicates or interrogates some tags or labels. If we will use RFID technology in security applications, we will need much more than one reader. There are two commercial solutions: each reader has one computer (or embedded device) or we can use a RFID multiplexer. First solution is very expensive and the second is time consuming, as we will see later. Our solution is to design a so-called "RFID hub" using FPGA technology and Xilinx embedded software tools.*

Key Words: ***RFID, FPGA, SoC, MicroBlaze, Xilinx EDK, embedded***

1. INTRODUCTION

RFID technology is often envisioned as a replacement for UPC (Universal Product Code) or EAN (European Article Numbering) bar-codes, having a number of important advantages over the older bar-code technology. The main advantages of RFID technology over old bar-code technology are: the ability to hold much more data, the ability to change the stored data as processing occurs, RFID does not require line-of-site to transfer data, and is very effective in harsh environments where bar code labels won't work.

What is a RFID hub and why should we develop one? The most RFID systems consist of one reader that is connected to a PC or some other device that read/write data from/to tags. If you want to develop a security system with 8 doors, you will have to use 8 PC's or 8 RFID dedicated embedded systems and 8 readers. This, of course will be a pretty expensive system.

Another solution is to use a RFID multiplexer witch in fact is an electronic device that allows a reader to have more than one antenna. Each antenna scans the field in a preset order. This reduces the number of readers needed to cover a given area, such as a dock door, and prevents the antennas from interfering with one another. From the costs point of view this is the best solution. However, there are some major disadvantages: the read time is 8 times slower and the write procedure can be a tricky issue because we don't know exactly haw faster the tags are trespassing the reader area.

To solve these problems we design a system that will have a much better average read/write speed with only one so called "RFID hub" witch is using at the same time up to 8 RFID readers.

2. RFID HUB STRUCTURE

In order to implement the RFID hub, we used Xilinx FPGA's. For embedded SoC design and FPGA synthesis we used Xilinx EDK (Embedded Development Kit) and XILINX ISE. Our system consists of (see Fig.1):

- one Spartan II FPGA
- an application for the Microblaze processor that will read/write tags (using the RTOS operating system)
- a PC server application that can handle multiple RFID hubs

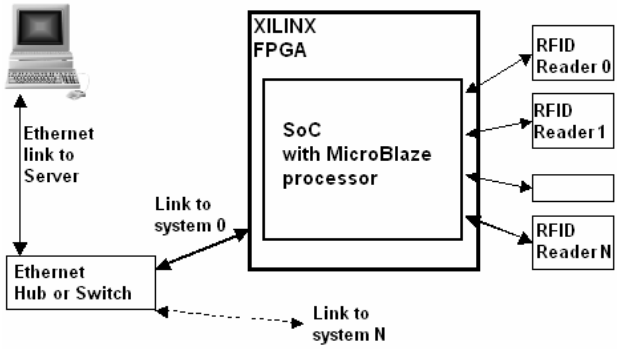

Fig. 1. *RFID Hub implementation*

This solution will be at the middle if we think at costs, but will solve the security holes that can appear with a multiplexer solution.

2.1. TE-XC2S Board

In order to test our SoC design we used the TE-XC2S board from Trenz Electronic Gmbh, which is equipped with a XILINX Spartan II FPGA. TE-XC2S development system provides a cost-effective and fast access to FPGA technology to engineers and students. It is designed for small to medium-sized designs and it could cover the most aspects of everyday usage. The system has four expansion connectors and is equipped with SRAM, FLASH, 7-segments displays, and could be equipped with other peripheral circuits also. [1]

2.2. RFID Reader

As RFID readers we used ISC.M02-B (Fig. 2) from FEIG Electronic GmbH which works with Smart Labels with an operating frequency of 13.56 MHz (ISO 15693, EPC).

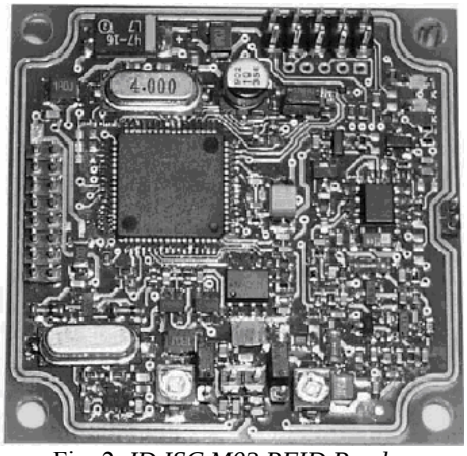

Fig. 2. *ID.ISC.M02 RFID Reader*

The Read/Write PCB has a maximum reading distance of up to 10 cm* by using the integrated antenna. By using external antennas, distances of 7 cm (antenna size 30 x 40 mm) resp. 14 cm (antenna size 100 x 100 mm) will be reached. To communicate with a PC or some other embedded device it uses UART (RS232-TTL) interface.

3. SOC STRUCTURE

The SoC is implemented using Xilinx specific software tools: Xilinx EDK for MicroBlaze development and Xilinx ISE for FPGA place and route and synthesis.

For the first tests we used just 4 UART interfaces, because just one compilation (generate libraries, build user applications, generate linker script, generate netlist, generate bitstream, download) of such a SoC is taking about 10 minutes (see Table 1 – just the FPGA routing part of the process).

Table 1. *Total Real Time for FPGA route*

Phase	Unrouted	Total Real Time (secs)
1	11457	32
2	10163	39
3	3457	45
4	3457	46
5	3917	114
6	4044	130
7	0	261
8	0	265

The SoC that will have synthesized contains (see Fig. 3):

- 1 Microblaze processor
- 4 UART cores for every processor we use that are synthesized in the same FPGA
- 1 Ethernet core for sending data to the central PC
- 1 debug core
- 1 Generic External Memory core

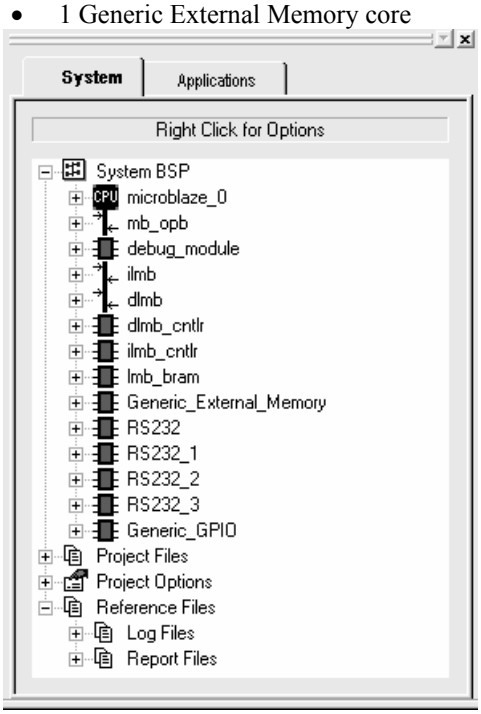

Fig. 3. *SoC Structure (Xilinx EDK)*

The "Generic_External_Memory" core is a Xilinx core and is using the SRAM Memory from TE-XC2S board (512 K). This is needed because the BRAM memory (with Xilinx EDK) that Spartan 2 XC2S200 is using for local data and instruction memory is just 4K bytes and is not enough for our applications.

Generic External Memory core , debug core and UART cores (from RS232 to RS232_3) are connected to the OPB (On-chip Peripheral Bus) of the MicroBlaze processor.

The debug core is used to control the processor and his peripherals. All the OPB cores are in fact memory mapped addresses that can be readed / writed using XMD debugger from Xilinx EDK (see Fig. 5).

The entire SoC designed and developed for the RFID hub is using 1453 out of 2352 (61%) slices from a XC2S200 FPGA.

3.1. Ethernet core [2]

The Ethernet core consists in fact in two separate Verilog modules: one for reception that is using just one input from the FPGA (rxd) and another module for sending data to the PC, which is using two output ports (txdp, txdm). This part of the SoC is using a 48Mhz clock so, if another target system is used, some DLL's (Delay-Locked Loop) should be instantiated in order to assure a clock that is closer to this value. From our tests, a clock between 46MHz and 50Mhz should work just fine.

The Ethernet interface was implemented using the 10BaseT standard so we have a maximum speed of 10Mb/s.

For the receiver part we used:

- a differential receiver circuit (see Fig. 4);
- a clock extraction circuit ;
- a preamble synchronizer, de-serializer and Ethernet checksum checker.

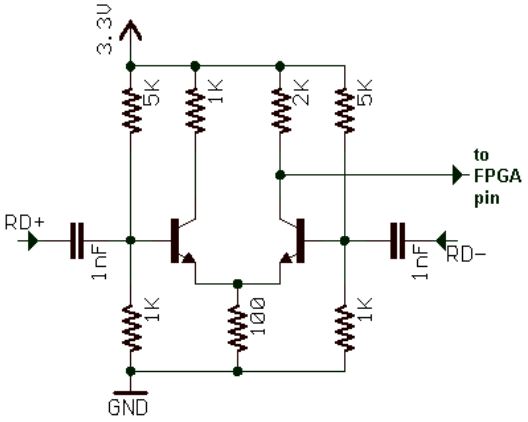

Fig. 4. *Differential circuit for reception*

The differential circuit for receiving data is used because Spartan 2 FPGA's does not offer differential inputs / outputs. However, this is not the case if you are using Spartan 3 or Virtex FPGA's.

After synthesis the Ethernet part of the SoC is using just 3% of our target (XC2S200).

We didn't use the Xilinx Ethernet core because is too complex and use too much space on the FPGA. Our core was developed in fact for another SoC [1] but we imported [3] to this specific MicroBlaze project using "Create – Import Peripheral" tool which comes with Xilinx EDK software.

3.2. UART core and IEE 15693 commands

RFID readers we used (ID.ISC.M02) use UART RS232-TTL port in order to be connected to a PC or another embedded device. The settings we used for every UART port inside the SoC are: 38400, 8 data bits, 1 stop bit and odd parity.

In order to communicate with RFID readers we implemented the next C functions that send ISO 15693 commands:

- OBID_Baud_Rate_Detection() : to detect baud rate of the reader;
- OBID_Inventory() : returns the number of transponders on the field and their unique ID's;
- OBID_Read() : read data from one transponder;
- OBID_Write() : write data to transponder;
- OBID_RF_Reset() : resets the RFID reader;
- CalcCRC16CheckSum() : to calculate the CRC sum of packets sent or received from RFID device.

4. THE SERVER PROGRAM

In order to send/receive different commands to/from a PC linked to this type of SoC we developed a PC server program. Because we use our own Ethernet core, we just modified the "Ethernet IDE application" [1] and used the SRAM part like useful data. All mapped addresses (see Fig. 5) inside the MicroBlaze SoC can now be accessed through this application. Also, there are 2 variables (one unsigned char and the other unsigned char [100]) at fixed addresses on the MicroBlaze part that are used for receive/send commands/data from/to the PC server application.

eripherals | Bus Connections | Addresses | Ports | Parameters

Assign Address ranges for all peripherals and bus arbiters

Instance	Prefix	Base Address	High Address
mb_opb			
debug_module		0x41400000	0x4140ffff
dlmb_cntlr		0x00000000	0x00000fff
ilmb_cntlr		0x00000000	0x00000fff
Generic_External...	MEM0	0x20080000	0x200fffff
RS232		0x40660000	0x4066ffff
RS232_1		0x40640000	0x4064ffff
RS232_2		0x40620000	0x4062ffff
RS232_3		0x40600000	0x4060ffff
Generic_GPIO		0x40000000	0x4000ffff

Fig. 5. *Address ranges for SoC peripherals*

The program was developed using Microsoft Visual C++ and the WinPCap Ethernet sniff library developed and maintained at Politecnico di Torino, Italy.

For a faster Ethernet performance we used two windows threads: one for writing the data over the Ethernet interface and one for reading' it.[1]

4. CONCLUSIONS AND FUTURE WORK

Because the commercial RFID multiplexers can be slow sometimes, we tried to de design a low-cost RFID hub. Using FPGA and SoC technologies we succeeded in our attempt to offer another solution for security applications which use RFID technology. In the future we will try to adapt our own SoC [1] for an RFID hub, without using the MicroBlaze processor and Xilinx EDK. This way, the so-called RFID Hub can be implemented no matter the FPGA vendor.

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4. IEE 15693 Standard
5. IEE 802.3 Standard

PROPAGATION AND SINGLE-TUNED FILTER BASED MITIGATION OF HARMONICS IN DISTRIBUTION NETWORKS

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Abstract: *The paper analyses harmonic propagation and mitigation in realistic, large distribution network under different operating conditions. Total voltage harmonic distortion (THD_V) levels are established for different loading and operating conditions and different network topologies. Once the range of THD_V variation for different scenarios is established, single tuned passive filters are designed to improve the overall network harmonic performance. A large number of simulations were performed taking into account different filter size, tuning frequency, operating conditions, network topologies and load composition in order to optimise the size, the number and the location of the filters in the network. The optimal filtering solution for the test network resulting in significantly reduced harmonic levels is proposed. A generic distribution network, based on typical UK distribution network is used in all simulations. Harmonic analysis was performed using commercially available software package, SuperHarm.*

Key Words: ***Power quality, harmonics, single tuned filters***

1. INTRODUCTION

One of the main purposes of a power system is to deliver electric power to customers at specified quantity and quality. If the supply is constant, i.e. the quantity requirement is satisfied, the focus turns towards the quality of delivered energy. The quality of the electricity supply generally refers to voltage having constant frequency, amplitude, symmetry and sinusoidal waveform [1]. Depending on the sensitivity of the equipment connected to the network, variation in power quality may result in substantial financial consequences.

One of the important factors contributing to the quality of electricity supply is harmonics. They are defined as sinusoidal component of a periodic waveform having a frequency which is an integer multiple of the fundamental frequency [2].

The presence of harmonics have a negative impact on power systems. They may lead to harmonic resonance, increased losses, degradation of dielectric characteristics of cables and capacitors, malfunction of equipment, interference with communication circuits and power measurement, etc. [1],[2],[3],[4]. Ultimately this may result in reduction of the lifespan of devices, increased maintenance cost and the need to oversize the equipment.

There is a need therefore, to consider appropriate mitigation techniques to reduce the level and propagation of harmonics in the network. In spite of natural and forced harmonic cancellation (due to different phase angles, supply via transformers having different winding connection, etc.) it is often necessary to include appropriately designed passive harmonic filters in distribution networks.

Before any harmonic mitigation measure is considered however, it is necessary to assess the overall harmonic characteristics and propagation of harmonics in distribution network.

In the analysis of harmonic propagation and mitigation presnted in this paper, SuperHarm, a commercial grade harmonic simulation software is used in all simulations. A generic distribution network, based on typical UK distribution network, is modeled. Total harmonic voltage distortion levels (THD_V) are established for different loading and operating conditions and network topologies. Frequency scan is performed to determine resonant conditions in the network.

Once the range of THD_V and the resonant conditions of the network are established for different load scenarios, single tuned passive filters are designed and tuned to improve the overall network harmonic performance. Several simulations taking into account different filter size, tuned frequency, operating conditions, network topologies and load compositions are performed to determine the optimum size, number and location of the filters in the network

2. MODELLING OF THE TEST NETWORK

2.1. Network model

A realistic distribution network shown in Fig.1 is fed from the transmission system at two high voltage substations at 400kV and 275kV. It consists of 289 buses, of which 24 are 132kV, 25 are 33kV, 233 are 11kV, and 4 are 3kV buses. 21 step-down transformers are also modelled. There are 300 lines, of which majority are 11kV underground cables, and the rest are 33kV overhead lines. (The 33kV network is predominantly meshed, whereas the 11kV network is of predominantly radial configuration.) Topology of the generic network is changed in simulations from predominantly meshed to predominantly radial by switching on/off some of the 24 available circuit breakers and switches.

The system is modeled as single-phase model using per unit values. Overhead lines and underground cables are modelled by their π equivalent circuit, linear loads as frequency dependent resistance in parallel with inductance, and nonlinear loads as harmonic current sources [5] (only the 5^{th}, 7^{th} and 11^{th} harmonic are included in harmonic spectra of nonlinear loads).

2.2. Load/Consumer classes

Aggregate loads are categorized based on three typical consumer classes:

a) Residential loads, where nonlinear loads are typically television sets, personal computers, low power home appliances with electronic converters, and discharge lamps;

b) Commercial loads, where fluorescent lighting, computers and their peripherals form the majority of nonlinear load;

c) Industrial loads, where nonlinear loads are mainly adjustable speed drivers and converters.

Aggregate nonlinear loads are connected at 146 out of 289 buses in the network. Ten of those are industrial loads, 30 are commercial and 106 are residential. (See Fig. 1)

3. CASE STUDIES

Nine different cases (combination of three network topologies and three characteristic loading scenarios) are considerd in order to eastablish boundaries and levels of harmonic distortion and propagation in the network.

3.1. Network topologies

The following three network topologies are considered:

T1 - predominantly meshed topology where all breakers and switches are closed (See Fig. 1). This topology is considered to be the base case network.

T2 - predominantly radial topology obtained by opening 22 characteristic breakers and switches.

T3 - split network topology, obtained by opening 4 characteristic lines. In this case the network is practically divided into two almost equal parts, with connection at 132kV level (right and left part).

3.2. Loading scenarios

Taking into account different composition of linear and nonlinear loads in each consumer sector and variation of load demand with time of day and day of week, three loading scenarios are considered:

L1 - day peak load, i.e., from 10:30 - 11:30 am of a weekday,

L2 - night peak load, i.e., from 7:30 - 8:30 pm of a weekday,

L3 - off peak load period, i.e, from 10:30 - 11:30am of a weekend

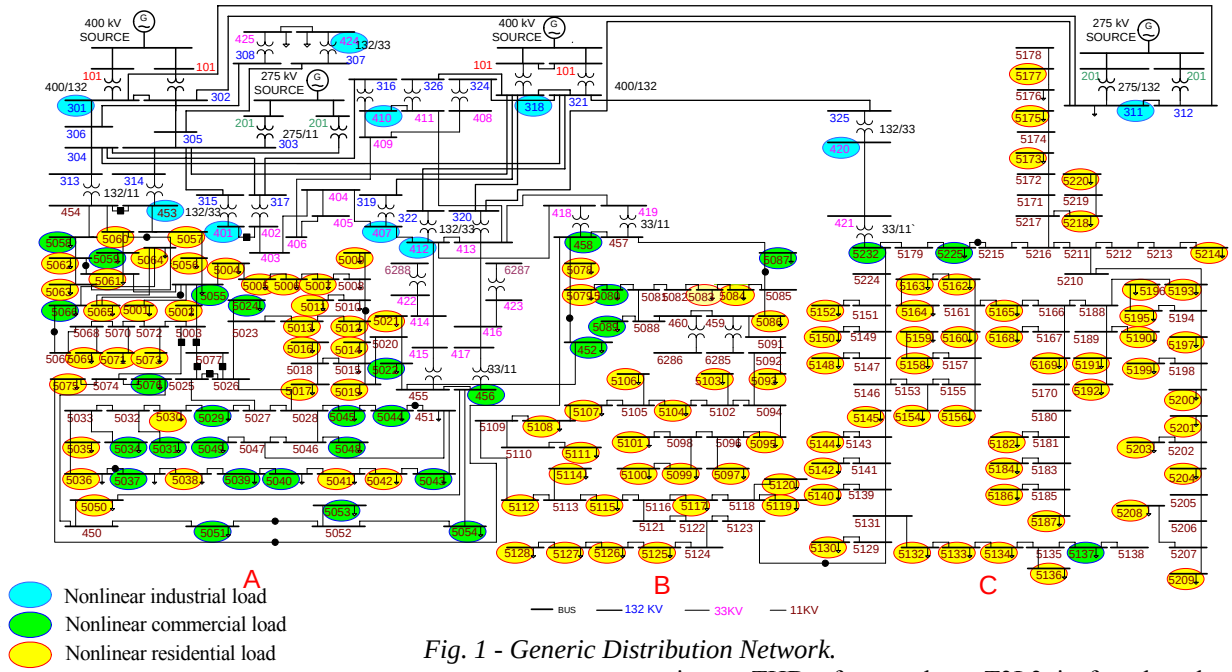

Fig. 1 - Generic Distribution Network.

4. HARMONIC CHARACTERISTIC OF THE NETWORK

4.1 The influence of network topology and loading conditions on THD_V

In order to assess the influence of network topologies and load scenarios on harmonic voltage distortion, THD_V is calculated for every bus and for every case study (Fig.2). According to IEEE 519-1992, THD_V limit for 69kV and lower voltage level is 5%, and for $69kV<U_N\leq161kV$ is 2,5%. None of the cases investigated exceeded the specified limits.

Higher values of THD_V are noticed for buses at 11kV level. The maximum THD_V is 4.18% at bus B5037 in the case of T2L2 combination. High THD_V is also observed at all buses in the radial part of the network regardless of the operating condition.

The lowest THD_V is observed during off peak (L3) period as usage of nonlinear devices is at its minimum. The maximum THD_V for topology T3L3 is found to be only 0.905%.

The results obtained for the two characteristic cases are shown in the sequel.

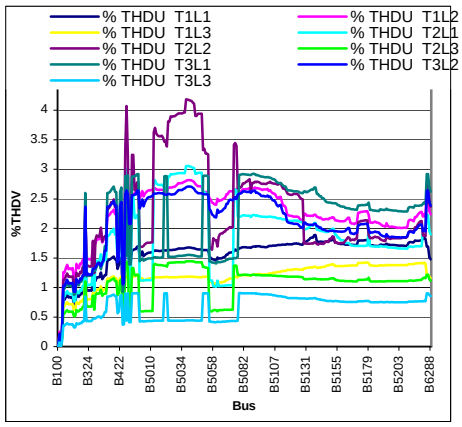

Fig.2 - *THDV of all buses for all topologies and load scenarios.*

4.2 The influence of network topology and loading conditions on voltage levels

Fundamental voltages at all buses in the network are determined for all cases of different network topologies and loading scenarios as shown in Fig. 3.

It can be observed that the largest magnitude occurs during the off peak period (L3), when the system is most lightly loaded. The region C (see Fig. 1) experienced significant voltage drop for all 9 cases primarily due to long lines effect.

The most significant drop in fundamental voltage occurs during the night peak, in particular at 11kV buses where there are a large number of residential consumers. Case T2L2 is the most problematic as the voltage at bus B5209 dropped to 0.62 p.u., which is attributed to the radial network topology. The under voltage problem observed in these cases can be successfully resolved by installing switched capacitors at appropriate buses in the network.

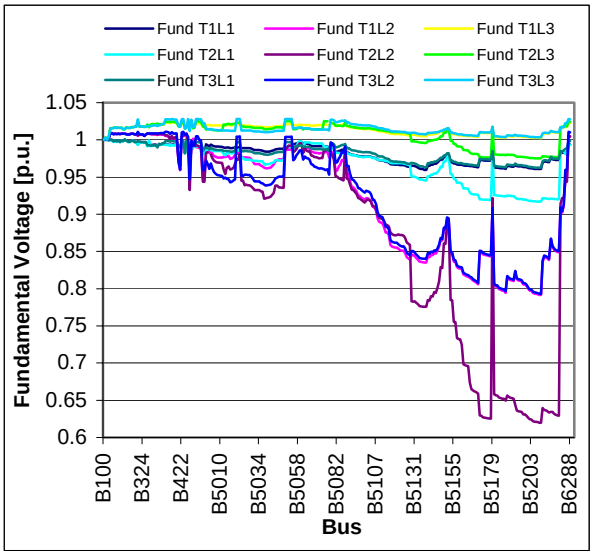

Fig.3 - Fundamental voltage profile for all buses.

4.3 Frequency response of the characteristic cases

Resonant conditions in the network are assesssed by performing frequency scan for characteristic cases, T2L2 (Fig.4) and T3L3 (Fig.5). Frequency scan is performed by injecting $1\angle 0°$ p.u. harmonic currents (within frequency range of 50 (h=1) and 1500 Hz (h=30)) at buses of interest (B412, B450 and B5106). In frequnecy scan mode, voltage sources are short circuited and harmonic current sources representative of nonlinear loads are open circuited. Based on $\boldsymbol{Y_f}$ x $\boldsymbol{v_f} = \boldsymbol{i_f}$, (where $\boldsymbol{Y_f}$ is admittance matrix and $\boldsymbol{i_f}$ harmonic current), the nodal voltage vector $\boldsymbol{v_f}$ is calculated at every frequency of interest. A parallel resonance in the network is indicated by a sharp rise in voltage. The frequency at which it occurs is dependent on the ratio of the equivalent network capacitance and inductance [4].

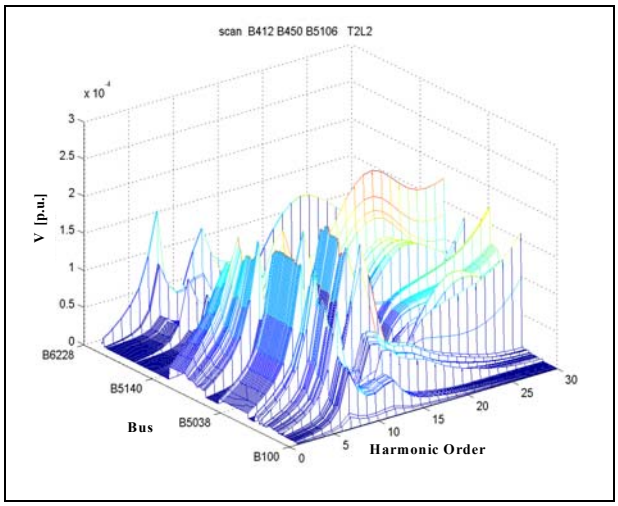

Fig.4 - *Voltage frequency response for caseT2L2.*

For the case T2L2, it is observed that parallel resonance occurs at the 7th and 12th harmonic at 132kV buses. At the 33kV buses, parallel resonance occurs at the 7th harmonic with sigfnicantly higher peak voltage. At the 11 kV buses of the region A of the network, parallel resonance occurs at the 7th and 12th harmonic with the peak voltage which is about 25% higher than that at the 33kV buses. Similar frequency response is observed in regions B and C of the network, as well as at the 3 kV buses.

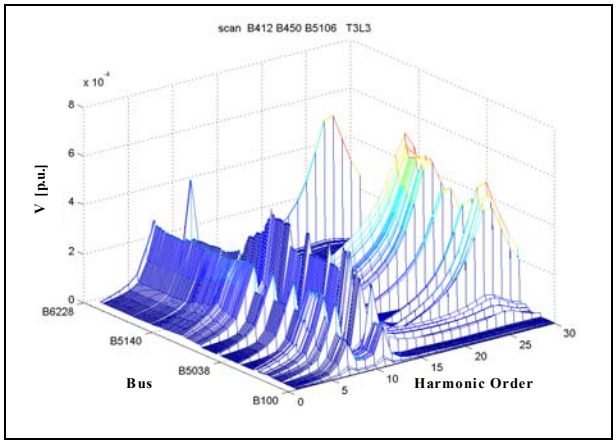

Fig.5 - *Voltage frequency response for caseT3L3*

For case T3L3, parallel resonance is observed at the 7th, 11th, and 26th harmonic. The 7th and the 11th harmonic are characteristic for all the buses, whereas the 26th harmonic is mostly observed at buses from the region B (see Fig. 1) of the network.

In this study, harmonics of interest are 11th and below. Harmonic currents with frequencies higher than the 11th harmonic are considered to be negligible and therfor are not included in the nonlinear load model.

Comparing harmonic responses for cases T2L2 and T3L3, it can be seen that network topology and loading scenario have a significant impact on the peak voltage as well as on the resonant frequency. The peak voltage in case T3L3 is almost doubled compared to that observed in case T2L2. This is mainly due to the loading condition of the network which has a direct effect on damping of harmonic voltage. For all cases considerd in this analysis the resonance at the 7th harmonic is the most dominant.

5. HARMONIC MITIGATION

Simulation results indicate that maximum THD_V at the 11 kV buses is 4.18%, which is within typical limits of 5%. However, assuming constant growth in the usage of nonlinear loads in customer installations, overall increase in THD_V is expected and hence harmonic mitigation should be considered.

Frequency scan indicates that the 7th harmonic is the common resonant frequency for all cases under investigation. Therefore, harmonic filters tuned to the 7th harmonic are considered for mitigating harmonic propagation in the distribution network and to improve overall harmonic performance.

Single tuned passive filters are chosen, as they are simple to design, reliable and the least expensive.

Generally, the best location to place a filter is at the harmonic source. However, this is not feasible in the network with huge amount of nonlinear loads. Therefore, the aim is to place the minimum number of filters to improve the overall network harmonic characteristics.

Multiple simulations were performed taking into account filter sizes, tuned frequency, and location to establish optimum locations and number of filters required for the network.

5.1 The nfluence of tuning factor on frequency response

Dielectric materials of capacitors generally degrade over the time which results in decrease in capacitance. A consequence of this is the increase in resonant (tuned) frequency of the filter and it may become less effective. To compensate for this phenomenon, harmonic filters are tuned typically to a value slightly below the resonant frequnecy. The usual value of filter "tuning factor" is a=(3 -10)% [4].

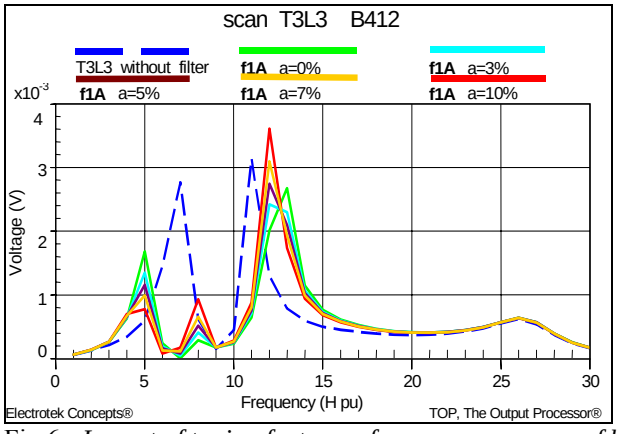

Fig.6 - *Impact of tuning factor on frequency response of bus B412*

Fig.6 shows the frequency response at bus B412 of case T3L3 with and without filter. Configuration **f1** refers to a filter (**f1A**) placed at bus B412 tuned to h=6.65 (a=3%), rated capacity of 6.5 p.u., and a filter placed at bus B5165 tuned to h=10.45, rated capacity of 1p.u. In subsequent cases, filter tuning factor (a) at bus B412 was changed from a=0% => h=7, a=3%, a=5%, a=7%, up to a=10% => h=6.3.

It can be seen from Fig. 6 that filter completely damps tuned harmonic. Reduction in tuning factor **a** (from the original value, say 5%) leads to voltage increase (reduced damping effect) at lower harmonics and decrease at higher harmonics. Therefore, as capacitor units grow old (**a** reduces) lower harmonics become less damped and higher slightly more.

5.2 The influence of filter size on frequency response

Case T3L3 with filter configuration **f1** is used to investigate the influence of filter size on frequency response. Frequency response curve at bus B412 is shown in Fig. 7. Filter size at bus B412 is varied from 50%, 100% and 150% of base value. The results are compared with the case without the filter in Fig.7.

It can be seen that as the filter size increases the frequency response of harmonics close to the tuned harmonic reduces. Also, higher filter size moves resonant frequencies away from tuned frequency: the 50% sized filter causes results in peaks (harmonic resonance) at the 5th, 8th and the 12th. harmonics; for 100% sized filter, the peak is at the 12th harmonic , while the peaks at 5th and 8th are much smaller; for 150% sized filter, the dominant resonant frequency is moved to the 4th and the 13th harmonic.

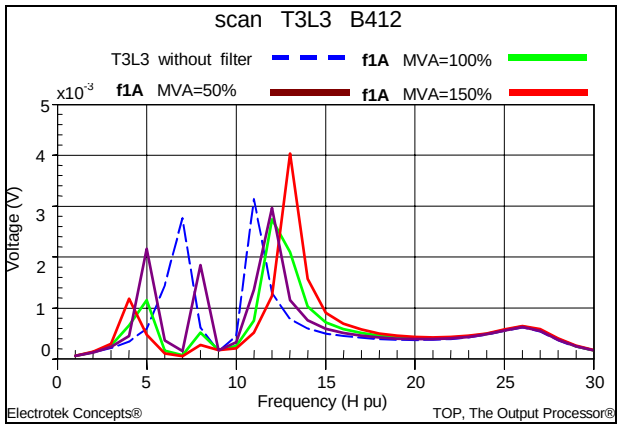

Fig.7 - *Impact of filter size on frequency response of bus B412.*

6. OPTIMAL FILTER PLACEMENT

A large number of simulations were performed with filters placed at nodes with high THD_V which are nodes with large harmonic sources. As there are many cases of different network topologies and load scenarios, it is difficult to find the right combination that will satisfy all cases. One of the major problems was with filter placement that caused a reduction in THD_V in all cases, but the fundamental voltage exceeded permitted limit of 105%. There are other cases where filter combinations resulted in optimal fundamental voltage regulation but no significant reduction in THD_V. Further course of investigation led to placement of filters closer to sources of supply, as the impact on all topologies would be more equalized.

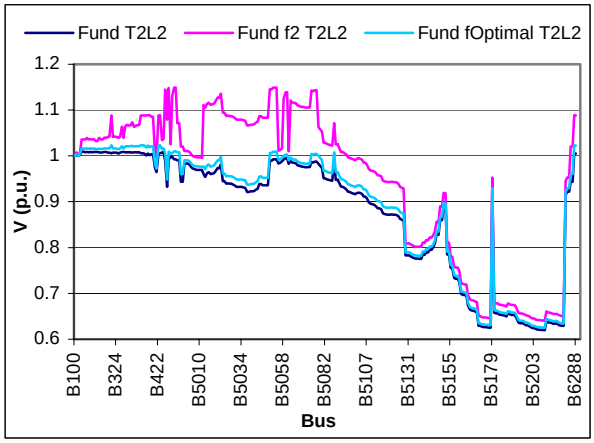

Fig.8 - *Fundamental voltage profile for situation without filters, with **f2** and with **fOptimal** for case T2L2.*

Fig.8 and 10 show fundamental voltage profile of the network for cases T2L2 and T3L3 respectively.

Fig. 9 and 11 show THD_V of the network for cases T2L2 and T3L3, respectively. In the case of **f2,** three filters are tuned to frequency 6.65x50Hz (a=5%), with rating equal to 20 p.u. and placed at the bus having the largest nonlinear load in each consumer sector, i.e, bus B412, B456 and B5060.

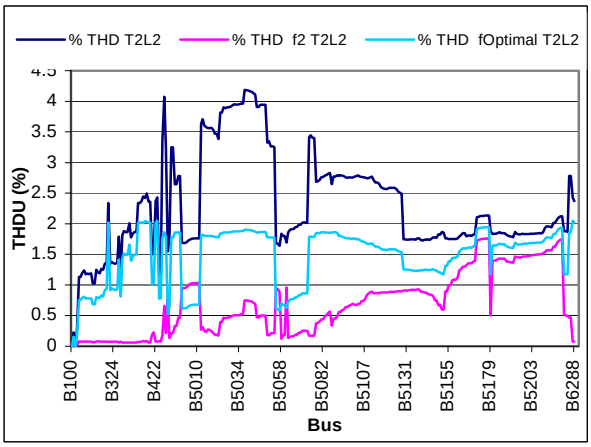

Fig.9 - *THDV profile for situation without filters, with **f2** and with **fOptimal** for T2L2.*

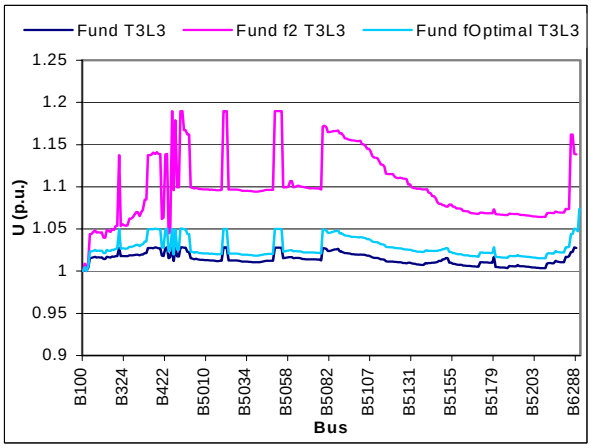

Fig.10 - *Fundamental voltage profile for situation without filters, with **f2** and with **fOptimal** for T3L3.*

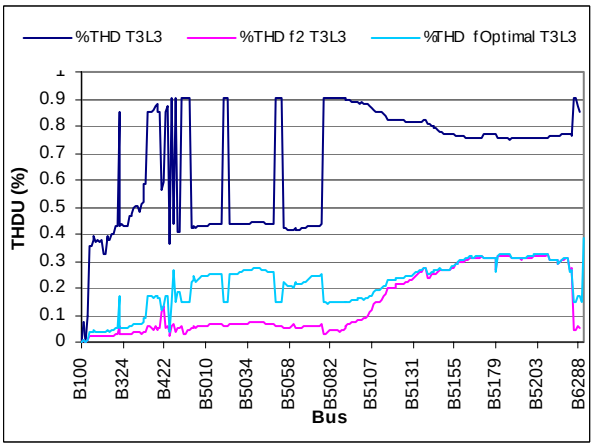

Fig.11 - *THDV profile for situation without filters, with **f2** and with **fOptimal** for T3L3.*

The case **fOptimal** refers to filters placed at 2 buses with the largest nonlinear loads disregarding consumer sector. At bus B412, the filter is sized at 8 p.u., whereas at bus B301 it is 10 p.u.Both filters are tuned to 6.65x50Hz (a=5%).

Combination **f2** is found to perform better in terms of THD_V, than combination **fOptimal**. However, combination **f2** resulted in voltages higfher than statutary limits in both of cases (T2L2 and T3L3).

Amongst all the filter combinations, only **fOptimal** satisfied fundamental voltage limits and desired THD_V for all cases of network topologies and loading scenarios. For case T2L2, THD_V decreased from maximal value of 4.18% to 2.02%, and for case T3L3 from 0.9% to 0.33%.

A three-dimensional representation of frequency response for case T2L2 with optimal filter configuration **fOptimal**, based on $1\angle 0°$ p.u current injection at buses B412, B450 and B5106 is shown in Fig.12.

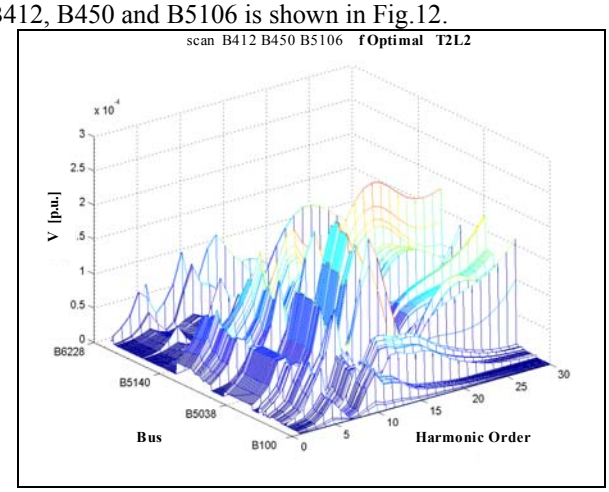

Fig.12 - *Voltage frequency response for case T2L2 with optimal filter configuration **fOptimal** and $1\angle 0°$ p.u current injection at buses B412, B450 and B5106.*

Significant damping is observed at the 7^{th} harmonic for buses in regions A and B, while at the same time new set of resonant frequencies is at the 4^{th}, 5^{th}, 9^{th} and 13^{th} harmonic. In the region C of the network (see Fig. 1), the 7^{th} harmonic voltage is almost completely damped, but new set of resonant frequencies (5^{th} and 9^{th}) is observed. The filters have no significant impact on harmonics greater then the 21^{st}.

6. CONCLUSION

Presented analysis showed that network topology and loading scenario have a significant impact on harmonic

performance of distribution network in terms of THD_V and fundamental voltage.

The influence of harmonic filter tuning on network harmonic performance is also investigated. The level of harmonic voltage reduction for the respective frequencies is dependent on the frequency at which harmonic filters are tuned. Similarly, the size of harmonic filters affects the range of frequencies at which the filter is effective in damping harmonic voltages.

After detailed analysis of different influences on frequency characteristics of the network, determining characteristic cases according to maximum THD_V and establishing critical conditions for resonance, the single tuned passive filters are designed to improve the overall network harmonic performance.

A large number of simulations was performed taking into account different filter sizes, tuning frequencies, operating conditions, network topologies and load compositions in order to optimise the size, number and location of the filters in the network. It is shown that the proposed optimal filtering solution (with only two 7^{th} harmonic filters) results in significant reduction in harmonic voltage levels.

Finaly, it is observed that placing filters for damping particular harmonics in the network, results in new resonant conditions in the network. Depending on the severity of new resonances, new filters might need to be placed in the network.

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CONTROL OF VARIABLE SPEED WIND TURBINE UNDER GRID DISTURBANCES

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Abstract: *This paper proposes modified dual vector current control (DVCC) for the wind turbine application. It prevents uncontrolled increase in converter output current under unbalanced grid voltage conditions through imposing limit in magnitude of the grid current. Furthermore, modified DVCC fulfills requirements for average unity power factor with suppressed oscillations in active power flow.*

Key words: ***wind turbine / unbalanced / voltage sag / DVCC / anti-resonant filter***

1. INTRODUCTION

The new E.ON grid connection regulations require a wind turbine (WT) to have supporting effect on the supply grid in cases of grid disturbances [2]. The most critical demand is that the wind turbine must supply highest possible apparent power for the duration of the disturbance even at extremely low voltages (down to 15% of the nominal value, marked area in Fig. 1.b). Fully-controlled WT with induction generator (IG), shown with Fig 1.a, can fulfil these requirements.

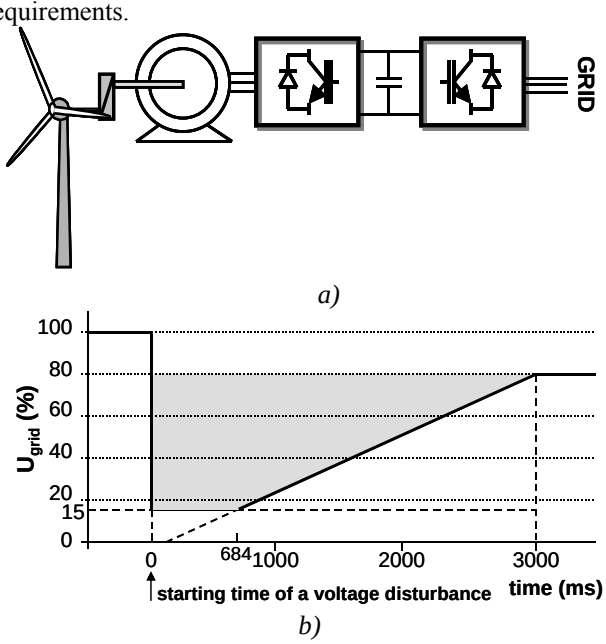

Fig. 1. *a) Wind turbine with fully- controlled IG; b) E.ON requirements for a WT grid connection*

The solutions proposed in the literature employ dual vector current control (DVCC) of the grid side converter in cases of unbalanced grid voltage disturbances [3,4]. DVCC is based on control of bought positive and negative sequence currents, which enables transfer of the active power at the system frequency while suppressing its oscillations at double the frequency and average unity power factor. However, during the dips there is no control over the magnitude of the line current that can, for deep sags, reach values several times higher than nominal.

This paper proposes modification of the conventional DVCC control with imposed limit in the line current and its implementation in the wind turbine system.

2. MODIFIED DVCC WITH IMPOSED CURRENT LIMIT

An unbalanced system of three phase voltages, which is general case of grid voltage sag, can be represented with its positive ($u^p_{dq} = u^p_d + j \cdot u^p_q$) and negative ($u^n_{dq} = u^n_d + j \cdot u^n_q$) sequence components as it is given with Equ. 1:

$$u_{\alpha\beta} = e^{j\omega t} \cdot u^p_{dq} + e^{-j\omega t} \cdot u^n_{dq} \tag{1}$$

where ω is the grid frequency. In such a circuit unbalanced currents also appear and they could be represented in analogous way as in (1). Regarding this, apparent power S is defined with:

$$S = u_{\alpha\beta} \cdot i^*_{\alpha\beta} = P(t) + j \cdot Q(t) \tag{2}$$

with active $P(t)$ and reactive power $Q(t)$ obtained in the form [3]:

$$P(t) = P_0 + P_{C2} \cdot cos(2\omega t) + P_{S2} \cdot sin(2\omega t) \tag{3}$$

$$Q(t) = Q_0 + Q_{C2} \cdot cos(2\omega t) + Q_{S2} \cdot sin(2\omega t) \tag{4}$$

where P_0 and Q_0 designate average powers' value, while P_{C2}, P_{S2}, Q_{C2} and Q_{S2} are magnitudes of powers' oscillation caused by the unbalance. Conventional DVCC for the grid side converter implies control of the positive (i^p_d, i^p_q) and negative (i^n_d, i^n_q) current components in order to achieve transfer of the active power at the system frequency, $P_0 = P^{ref}_{DC}$, while nullifying the fluctuations at double the frequency, $P_{C2} = P_{S2} = 0$, and average unity power factor, $Q_0=0$. Hence, the references for the current control loops (i^{pref}_d, i^{pref}_q, i^{nref}_d, i^{nref}_q) have to be extracted from the following expression:

$$\begin{bmatrix} P_0 \\ Q_0 \\ P_{C2} \\ P_{S2} \end{bmatrix} = \begin{bmatrix} P^{ref}_{DC} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} u^p_d & u^p_q & u^n_d & u^n_q \\ u^p_q & -u^p_d & u^n_q & -u^n_d \\ u^n_q & -u^n_d & -u^p_q & u^p_d \\ u^n_d & u^n_q & u^p_d & u^p_q \end{bmatrix} \cdot \begin{bmatrix} i^{pref}_d \\ i^{pref}_q \\ i^{nref}_d \\ i^{nref}_q \end{bmatrix} \tag{5}$$

In the WT system P^{ref}_{DC} is determined by the power yield of the turbine. Consequently, for a deeper sag grid currents would reach unacceptably high values, several times higher than nominal. From the point of reliability and protection issues of the drive this situation should not be permitted. Therefore, here the modified DVCC for the grid side converter is proposed that imposes limit I_{LIM} on the magnitude of the grid current $|I_{GRID}|$. This is achievable by altering control objective during sags, according to Equ. (6).

$$\begin{bmatrix} |I_{GRID}|^2 \\ Q_0 \\ P_{C2} \\ P_{S2} \end{bmatrix} = \begin{bmatrix} I_{LIM}^2 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} i_d^{pref} & i_q^{pref} & i_d^{nref} & i_q^{nref} \\ u_q^p & -u_d^p & u_q^n & -u_d^n \\ u_q^n & -u_d^n & -u_q^p & u_d^p \\ u_d^n & u_q^n & u_d^p & u_q^p \end{bmatrix} \cdot \begin{bmatrix} i_d^{pref} \\ i_q^{pref} \\ i_d^{nref} \\ i_q^{nref} \end{bmatrix} \quad (6)$$

Namely, first condition concerning desirable power flow is now substituted with current limiting condition, while the actual active power is determined by the grid voltage. Solution of (6), providing the current references, is given in the Appendix.

Modified DVCC uses the same control structure as conventional DVCC which is shown by Fig. 2 [3]. The only difference comes from the calculator of the current references. The operational principle and the structure of the anti-resonant filter (ARF), used for the extraction of positive and negative voltage and current components, is discussed in the following Chapter.

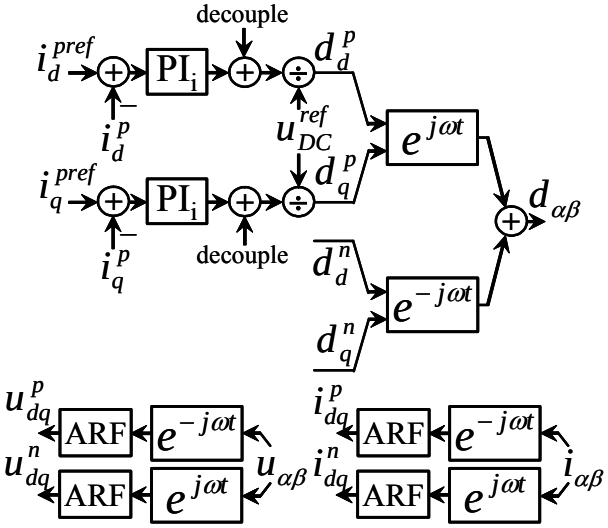

Fig. 2. *DVCC control structure*

3. ANTI-RESONANT FILTER

Positive and negative voltage and current components can be extracted from the measured grid voltages $u_{\alpha\beta}$ and currents $i_{\alpha\beta}$ after employing transformation of rotation to positive $(e^{-j\omega t})$ and negative $(e^{j\omega t})$ reference frame, respectively. For voltages, using (1), this is:

$$u_{\alpha\beta} \cdot e^{-j\omega t} = u_{dq}^p + u_{dq}^n \cdot e^{-j2\omega t} \quad (7)$$

$$u_{\alpha\beta} \cdot e^{j\omega t} = u_{dq}^p \cdot e^{j2\omega t} + u_{dq}^n \quad (8)$$

In analogous way, currents are transformed in the same manner. It can be seen that in positive reference frame, apart from positive components u_{dq}^p that appear as DC values, there are negative components u_{dq}^n at twice the grid frequency. In the negative reference frame it's vice versa.

Evidently, AC components in (7) and (8) have to be removed. One of the possible solutions is application of anti-resonant filter (ARF) whose main advantage is that it requires adjustment of only one parameter - anti-resonant frequency f_{ARF} [5]. Its control diagram is shown in Fig 3. The filter combines direct input signal and the same one delayed by $1/(2 \cdot f_{ARF})$.

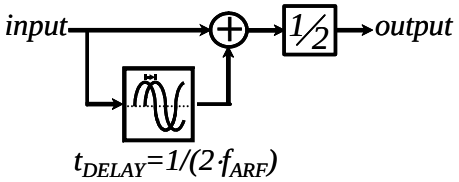

Fig. 3. *Control diagram of ARF*

Fig 4. illustrates ARF response to the step change in input signal oscillating at f_{ARF}. After characteristic transient period due to time delay function, filter ideally suppresses spectral component at f_{ARF}.

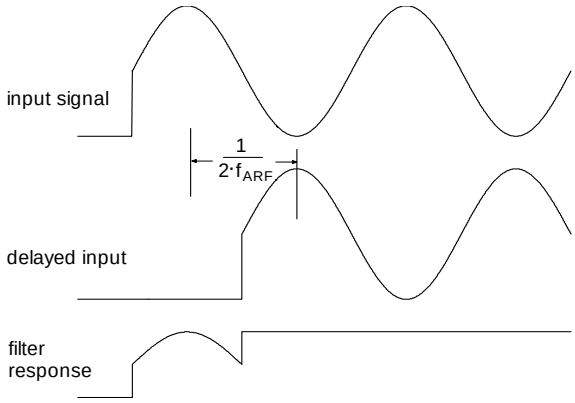

Fig. 4. *Time response of ARF*

4. WT CONTROL STRUCTURE

WT control structure (Fig. 5) incorporates vector control of IG implemented in the WT side converter and management of the power flow to the grid accomplished by the grid side converter. In normal grid conditions torque reference m_{WT}^{ref} for IG controller is obtained based on optimal turbine power characteristic $P_{WT}^{ref} = f(n)$ [6]. At the grid side, in normal conditions conventional DVCC is used. There, power transfer reference command P_{DC}^{ref} comes from the output of DC voltage controller and reference average reactive power is set to $Q_0 = Q_{GRID}^{ref} = 0$.

After the voltage sag has been detected, control structure has to be altered so that modified DVCC imposes current limit in the output current and WT side converter takes over DC voltage control. Obviously, power flow through the back-to-back converter would be reduced. Therefore, the WT mechanical input has to be restricted by means of the pitch control [6]. The control structure completes sag detector that manipulates the switching between the two control objectives.

5. CONTROLLERS' SETTING AND SIMULATION RESULTS

In order to verify control principle proposed in this paper and shown in Fig 5., detailed model of the system has been developed with space vector modulated (SVM) back-to-back converter at switching frequency f_S=10kHz. Current controllers are set based on symmetrical criterion: for WT torque controller proportional gain is $K_{Pi(WT)} = \frac{\sigma \cdot x_S \cdot f_S}{\omega_B}$ and integral gain $K_{Ii(WT)} = \frac{\sigma \cdot x_S \cdot f_S^2}{2 \cdot \omega_B}$, while for DVCCs proportional and integral gains are $K_{Pi(DVCC)} = \frac{x_{GRID} \cdot f_S}{\omega_B}$ and $K_{Ii(DVCC)} = \frac{x_{GRID} \cdot f_S^2}{2 \cdot \omega_B}$ respectively, where IG and grid parameters are given in the Appendix. Since the both current loops have the same dynamics, the DC voltage controllers on both sides could have equal parameters. Those, $K_{P(DC)}$=16 and $K_{I(DC)}$=1600 are obtained experimentally. Furthermore, the PI controllers are transformed to discrete so that current loops sampling period is $T_i=1/f_S$ and for DC voltage loops $T_{DC}=8/f_S$.

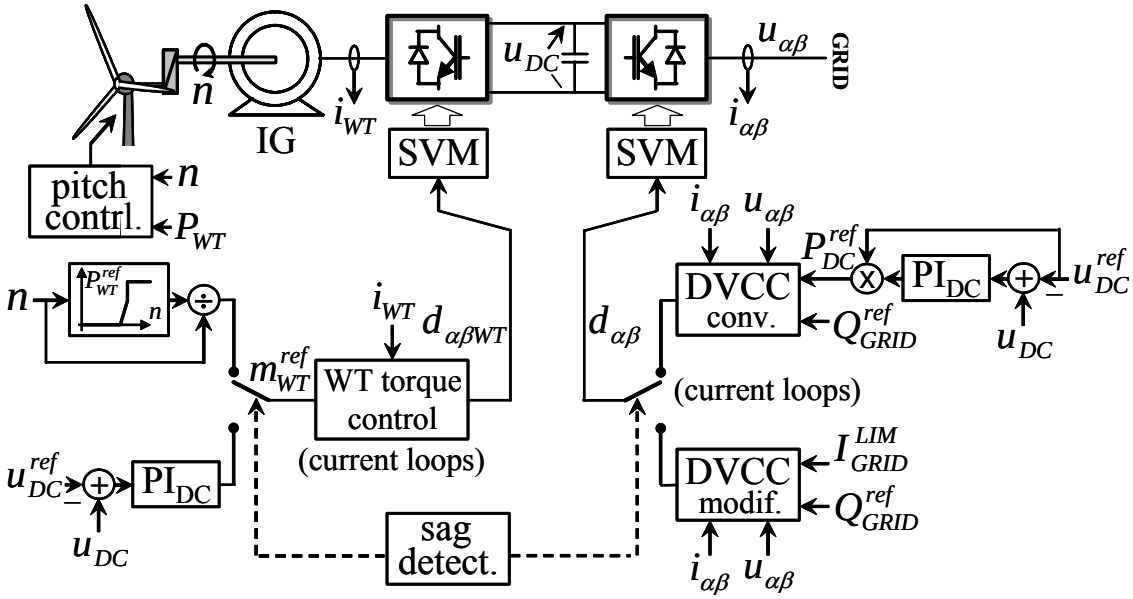

Fig. 5. *WT control structure*

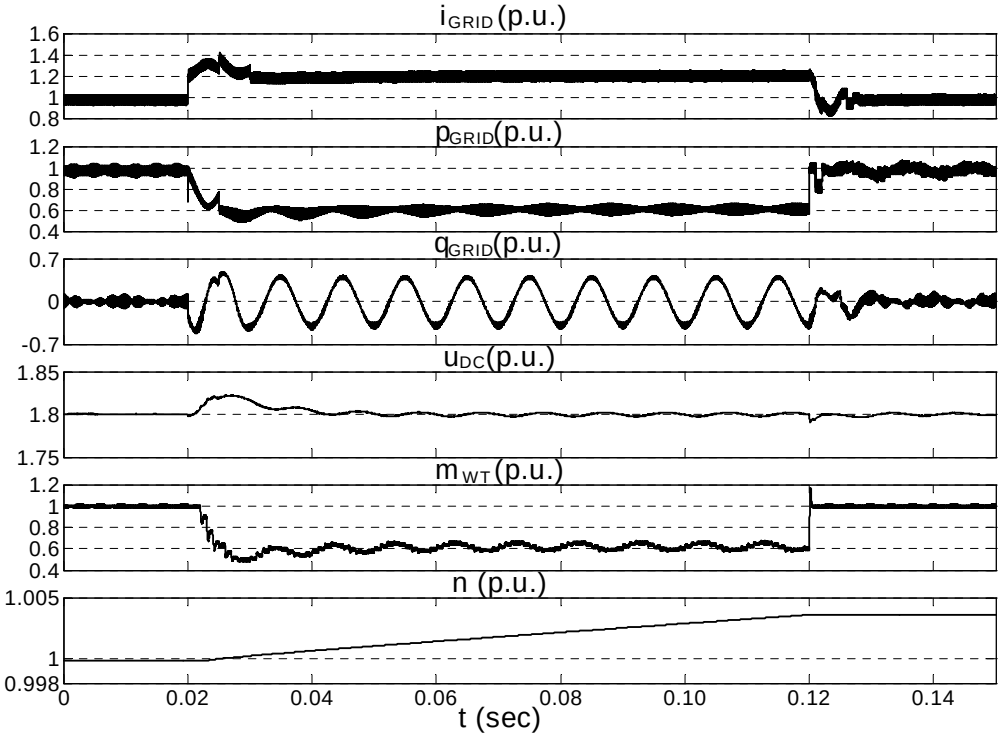

Fig. 6. *Simulation results*

Simulation results given by Fig. 6 show system's response to unbalanced voltage sag, where two phase voltages fall to 40% of nominal value followed by phase angle jump of 30° in third phase. Wind speed is constant and nominal $v_{WIND}=1(p.u.)$ yielding nominal power flow in regular grid conditions. During the sag, proposed modified DVCC in effective way limits magnitude of the grid current $|I_{GRID}|$ to $I_{LIM}=1.2(p.u.)$, while keeping the ripple of the active power flow and zero average reactive power as commanded. Lower grid voltage and limited grid current implies decreased active power flow p_{GRID} and consequently lower WT torque m_{WT}. Stable DC voltage response, around $u_{DC}^{ref}=1.8\,(p.u.)$, indicates that the power transfer is correctly managed. Temporary misbalance between unchanged mechanical input and decreased electrical output results in slight increase in WT speed n. If n reaches higher than nominal value, pitch control will gradually bring it back to the nominal.

5. CONCLUSION

Proposed modified dual vector current control (DVCC) prevents uncontrolled increase in converter output current under unbalanced grid voltage conditions through imposing limit in magnitude of the grid current. Furthermore, it fulfills requirements for average unity power factor with suppressed oscillations in active power flow. This approach has been verified in detailed model of variable speed wind turbine application.

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APPENDIX

Modified DVCC current references:

$$i_d^{pref}=I_{LIM}\cdot\frac{u_d^p}{D},\ i_q^{pref}=I_{LIM}\cdot\frac{u_q^p}{D},$$

$$i_d^{nref}=-I_{LIM}\cdot\frac{u_d^n}{D},\ i_q^{nref}=-I_{LIM}\cdot\frac{u_q^n}{D}$$

where $D=\sqrt{(u_d^p)^2+(u_q^p)^2+(u_d^n)^2+(u_q^n)^2}$

WT and grid parameters:

stator resistance:	$r_S=7.7m\ (p.u.)$
rotor resistance:	$r_R=9.0m\ (p.u.)$
stator reactance:	$x_S=3.56\ (p.u.)$
rotor reactance:	$x_R=3.53\ (p.u.)$
magnetizing react.:	$x_M=3.47\ (p.u.)$
total leakage factor:	$\sigma=41m\ (p.u.)$
base angular speed:	$\omega_B=100\cdot\pi\ (rad/s)$
grid resistance:	$r_{GRID}=6.4m\ (p.u.)$
grid reactance:	$x_{GRID}=40m\ (p.u)$
DC bus capacitance:	$C=1000\mu F$
base impedance:	$Z_B=16\Omega$

NEW ASPECTS ABOUT POWER DEFINITION IN ELECTRIC CIRCUITS

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Abstract: *We present the definition of electrical power by Standard IEEE 1459 – 2000. We compare this with the electrical powers of nonsinusoidal regim introduced by profesor Budeanu. The calculation exemple justifies the differences between the two ways of broaching the electrical powers problem.*

Key Words: ***Electric circuits/ Nonsinusoidal regims/ Electrical powers***

1. INTRODUCTION

More and more electric consumers are sensitives when they are perturbed by breakouts, excess voltage, fluctations in the main voltage, distorsion of current and voltage curves, etc [1], [2] so that it has appeared as a necesity to redefine electric powers in electric networks and circuits.

The increase of the efficiency in using and transport of the electric energy made that the electric instalations become more and more complex. Electric drives with variable speed, induction devices (oven, furnace), some equipments for electrotechnologies, condenser banks with automatic switching equipment for compensating the reactive power or for compensating the rectance of transportation electric lines, etc., increase the level of harmonics of the main frequency (voltage and current), respectively of the nonsymetry of the three-phase sistems (voltage and current) in electric distribution networks. Under these conditions the perturbations in the electroenergetic system, namely the nonquality of the electric energy, must be monitorized and analysed in order to limit as efficient as possible the bad effects, using in this purpose new definitions for electric powers, quality meters and advanced tchniques [3], including expert systems and genetic algoritms [4].

The researchers in this field are trying for a long time to define properly the electric powers and by cosequence the power factor, so that to be as general as possible in order to caracterise most correctly the perturbated electric regims, but most of all to express the efficiency of the power and energy transfer from sources to consumers.

In the case of sinusoidal and balanced conditions the expresions of the new defined powers must be identical to the classic well known definition. If so, the electric powers can be taken as quality indicators of the electric energy. If for the active power definition in electric circuits there are no differences in the point of view of researchers, for the definition of the other powers : reactive power, power due to nonsimetry, deformative power and especially the apparent power the problem is very difficult because the oppinions are extremely different.

For single-wire circuits the definition or the electric powers is completely solved, no matter which is the functioning regime. Not the same is the situation for poly-phased circuits , in nonsinusoidal regims and nonequilibrated [5], where different authors have introduced different definitions for the elctric powers. These definitions are completely diferent in Europe from those in America and this differences represent a dificulty in the development of electric equipments for data aquisition and monitorising. This conflict does not involve technical performances (harware) of the devices, but involves the sofware of the equipments, sofware that is essentialy modified if different power definitions are used. The differences in electric power definition have lead to different interpretations on the evolution of the same events and even in the actions made in order reduce the perturbations. In order to eliminate these aspects national and international normatives have been established (CEI, CENELEC, Standards of IEEE [6]) for a more accurate definition and sistematisation of the elements speciffic to this field. It is also remarcable the preocupation of some researchers to reconsider the definition of electric powers in order to make more obvious the new aspects that occure nowadays in the function of the electroenergetic dydtems. We have to mention her the profesor Țugulea [7], Emanuel [8] and especialy Akagi and Nabac who have proposed the generalised teory of instantaneous reactive power [9] starting from Clarke components.

The present paper presents some aspects connected to the definition of the apparent power and its components, so that are presented in IEEE Standard 1459-2000 [6], and afterwards we make some calculations related to the problem. In the mentioned Standard are presented also the expresions of electric powers (reactive and deformatiing power) such as professor Budeanu has introduced them; this confirms the value of the romanian electrotechnic school.

2. THE DEFINITION OF ELECTRIC POWERS IN NONSINUSOIDAL REGIMS , ACCORDING TO STANDARD IEEE 1459-2000

In the year 1996 the working group of IEEE for nonsinusoidal regims [5] has proposed a definition of the apparent single-wire power containing two terms: the fundamental apparent power $\boldsymbol{S_1}$ – wich puts in evidence the apparent power of the first harmonic, and, the nonfundamental apparent power $\boldsymbol{S_N}$ – related to the components due to the other harmonics. The nonfundamental apparent power includes in fact three components as followes:the distorsion power of the current D_I, the distorsion power of the voltage D_U and the apparent distorsion power S_H. These definitions have been taken from the standard IEEE 1459 – 2000.

2.1. The definition of the active power and of the reactive power

For a single-wire circuit in sinusoidal regim with the applied voltage of the expresion $u = \sqrt{2} \cdot U \cdot \sin(\omega t)$, the current trough circuit is $i = \sqrt{2} \cdot I \cdot \cos(\omega t - \varphi)$, and in Standard IEEE 1459-2000 [6] some aspects of the expresion

of the instantaneous power a revealed. This power is devided into two components:

$$p = u \cdot i = p_a + p_q \quad (1)$$

where: p_a is the instaneous power produced by the active component of the current or, we may call it the instantaneous pulsatory power and p_q is the instaneous power produced by the reactive power of the current or, we may call it the instantaneous oscillating power.

The expressions of the two mentioned components of the instantaneous power are:

$$p_a = U \cdot I \cdot \cos\varphi \cdot [1 - \cos(2\omega t)] = P \cdot [1 - \cos(2\omega t)],$$

where $P = U \cdot I \cdot \cos\varphi$

$$p_q = -U \cdot I \cdot \sin\varphi \cdot \sin(2\omega t) = -Q \cdot \sin(2\omega t),$$

where $Q = U \cdot I \cdot \sin\varphi$ (2)

The active power P is defined as the average value of the instantaneous power , on several periodes , *k,* so that the time interval is $k \cdot T$:

$$P = \frac{1}{k \cdot T} \cdot \int_{\tau}^{\tau + k \cdot T} p \cdot dt = U \cdot I \cdot \cos\varphi \quad (3)$$

and the reactive power, Q, represents the amplitude of the oscillations of the reactive component of the intantaneous power , p_q .

In nonsinusoidal single-wire stationary regime, the voltage *u* and the current *i* can be decomposed, each, into two components, one of them at the first harmonic u_1, respectively i_1, and the other one containing the components of all the other frequencies, of integer and noninteger values, u_H , respectively i_H .

$$u_1 = \sqrt{2} \cdot U_1 \cdot \sin(\omega t - \alpha_1);$$
$$i_1 = \sqrt{2} \cdot I_1 \cdot \sin(\omega t - \beta_1) \quad (4.1)$$
$$u_H = \sqrt{2} \cdot \sum_{h \neq 1} U_h \cdot \sin(h\omega t - \alpha_h);$$
$$i_H = \sqrt{2} \cdot \sum_{h \neq 1} I_h \cdot \sin(h\omega t - \beta_h) \quad (4.2)$$

Direct current component is obtained for h=0.

If we note the effective values at the first harmonic with U_1, respectively I_1, and the effective values of all the other components with U_H, respectively I_H, we get for the effective values of voltage, U, and current, I :

$$U^2 = U_1^2 + U_H^2 \text{ and } I^2 = I_1^2 + I_H^2 \quad (5)$$

where the direct current components are included in U_H and I_H .

By consequence the active power becomes:

$$P = P_1 + P_H \text{ where } P_1 = U_1 \cdot I_1 \cdot \cos\varphi_1 \text{ and}$$
$$P_H = \sum_{h \neq 1} U_h \cdot I_h \cdot \cos\varphi_h \quad (6)$$

These components are called P_1 – the fundamental active power, and P_H – the harmonic active power.

Also, in quite the same manner, for the reactive power:

$$Q = Q_1 + Q_H \quad (7)$$

where $Q_1 = U_1 \cdot I_1 \cdot \sin\varphi_1$ and

$$Q_H = \sum_{h \neq 1} U_h \cdot I_h \cdot \sin\varphi_h \quad (8)$$

We make the remark that $Q_1 + Q_H$ represents exactely the reactive power defined by the professor Budeanu and in the followings shall be noted as Q_B .

2.2. The apparent power

Based on relations (5),for the apparent power can be obtained:

$$S^2 = U^2 \cdot I^2 = (U_1^2 + U_H^2) \cdot (I_1^2 + I_H^2) = \\ = (U_1 \cdot I_1)^2 + (U_1 \cdot I_H)^2 + (U_H \cdot I_1)^2 + (U_H \cdot I_H)^2 = S_1^2 + S_N^2 \quad (9)$$

with S_1 being the fundamental apparent power, $S_1 = U_1 \cdot I_1$, and S_N is the nonfunamental apparent power:

$$S_N^2 = D_I^2 + D_U^2 + S_H^2 \quad (10)$$

In the relation (10):

$$D_I = U_1 \cdot I_H = U_1 \cdot I_1 \cdot THD_I = S_1 \cdot THD_I$$

is called current distortion power and is measured in [VAr];

$$D_U = I_1 \cdot U_H = I_1 \cdot U_1 \cdot THD_U = S_1 \cdot THD_U$$

is called voltage distorsion power, measured also in [VAr];

$$S_H = U_H \cdot I_H = S_1 \cdot THD_U \cdot THD_I$$

is called harmonic apparent power, measured in [VA], and has two components , in quadrature, P_H and D_H . Namely : $S_H^2 = P_H^2 + D_H^2$, D_H being the harmonic distortion power measured in [VAr], and P_H was already defined above

In the expresions of the powers D_I , D_U and S_H THD_I and THD_U represent the total distortion coefficient of the current, respectively of the voltage.

Emanuel shows in [8],[10] that:

$$S_N \approx S_1 \cdot \sqrt{THD_I^2 + THD_U^2} \quad (11)$$

In the same standard the nonactive power N is defined as $N^2 = S^2 - P^2$. This power is mesured in [VAr], so as the distortion power defined by the professor Budeanu, noted with D_B, and which satisfies the relation $D_B^2 = S^2 - P^2 - Q_B^2$, wher Q_B is the reactive power defined by professor Budeanu.

2.3 The Power Factor

For the fundamental frequency the power factor is:

$$P_{F1} = \cos\varphi_1 = \frac{P_1}{S_1} \quad (12)$$

and is called frequntly DPF (Displacement Power Factor). The power factor of the circuit is defined as (definition used also by professor Budeanu):

$$P_F = \frac{P}{S} = \frac{P_1 + P_H}{\sqrt{S_1^2 + S_N^2}} = \frac{P_1}{S_1} \cdot \frac{1 + P_H/P_1}{\sqrt{1 + (S_N/S_1)^2}} = \\ = P_{F1} \cdot \frac{1 + P_H/P_1}{\sqrt{1 + THD_I^2 + THD_U^2 + (THD_I \cdot THD_U)^2}} \quad (13)$$

and if we add this to (11):

$$P_F \approx P_{F1} \cdot \frac{1 + P_H/P_1}{\sqrt{1 + THD_I^2 + THD_U^2}} \quad (14)$$

Under this condition the power factor in nonsinusoidal conditions is expressed related to the power factor for the fundamental frequency (active power and apparent power of the fundamental frequency), the active power given by the harmonics and the total distortion coefficients.

3. THE POWER LOSS

The standard shows that the active power loss ΔP from a network that suplies a cunsumer with the applied star voltage *U*, in effective value is:

$$\Delta P = \Delta P_l + \Delta P_t \quad (15)$$

where ΔP_l represents the longitudinal active power loss produced in the series equvalent resistance of the network (Thévenin) – r_e, so that:

$$\Delta P_l = \frac{r_e}{U^2} \cdot S^2 \quad (16) \text{ with}$$

S representing the apparent power absorbed by the consumer, and

ΔP_t represents the transversal active power loss, produced in the transversal resistance of the network R_e, so that :

$$\Delta P_t = \frac{U^2}{R_e} \quad (17)$$

The two values for the resistances r_e and R_e are obtained by equivalence of total (real) power loss.

This means losses due to the fundamental, due to harmonics and interharmonics and to the powers corresponding to relations (16) and (17).

4. CONSIDERATIONS ON THE DEFINITION OF THE APPARENT POWER AND ITS COMPONENTS.

For a single wire nonsinusoidal conditions:

The apparent power is defined as being the maximum of the active power that can be supplied by a source to the consumer, under the condition of an imposed active power of the consumer and sinusoidal condition for the network;

The apparent power *S* can be considered as being the maximum active power that can be transfered to the load supplied by constant terminal voltage *U* and with constant power losses; in fact for given *S* and *U*, the line coefficient of utilisation is maximum when $P = S$. Using this definition of the apparent power, the power factor represents a measure of power losses on the line (network);

- The nonfundamental component S_N of the apparent power, respectively S_N/S_1 allows the estimation of the suplimentary solicitation of the electric line due to the harmonics injected in the transport line by nonlinear consumers and also the estimation of the harmonic filters;

Because in most of the situations $P_H << P_1$ it is very dificult to evaluate the harmonic active power directly by measurements, being simplier to measure THD_I, THD_U and P_1. Good accuracy can be obtained if harmonic filters (digital) are used. In this way it is possible to meter the harmonic active energy;

If $THD_U < 5\%$, and $THD_I > 40\%$, it is much easier using (18) instead of (14) in order to calculate the power factor:

$$P_F = \frac{P_{F1}}{\sqrt{1 + THD_I^2}} \quad (18)$$

Even if the Standard takes into account also the reactive power in nonsinusoidal conditions in the way that Budeanu did, and notes it with Q_B, as well as the distortion power D_B, the measure unit for both of them is considered being [VAr]. The Budeanu reactive power, Q_B can be greater or smaller than Q_1, depending on how is Q_H, greater or smaller than 0.

Mainly the Standard divides the apparent power into two components: a fundamental one and a no fundamental one. The apparent fundamental power corresponds to the active and reactive power of the fundamental frequency, P_1 and Q_1, and the apparent nonfundamental power corresponds to a harmonic apparent power S_H and to some power components due to current and voltage , powers which are noted as distortion powers D_I and D_U they are measured in [VAr], the same as a reactive power. Also, the harmonic apparent power has two components: the active one P_H and the distortion harmonic power D_H, which in fact is a reactive power. In this way due to presence of the harmonics only one active power appears and several supplementary reactive powers: one due to current distortion, one due to voltage distortion and the third one due to both distortion signals, of voltage and current. Maybe it would be more accurate to call P_H as active distortion power and D_H as reactive distortion power.

5. APPLICATION

It is the 110/27 kV transformer from Ortisoara railroad station that was studdied. The u(t) and i(t) curves on one of the transformer primary phases are shown in fig.1. [11]. The harmonics of voltage and current, the active power and reactive power for each harmonic were measured during the

experiment. In table 1 besides this mesured values some calculeted values are presented as well, such as : the phase difference between voltage and current for each harmonic, the effective value of voltage and current, the total active power $\sum P$, the total reactive power (puterea reactivă Budeanu) $\sum Q = Q_B$, the active harmonic power P_H, the reactive harmonic power Q_H, the effective value of voltage harmonics U_H, the effective value current harmonics I_H.

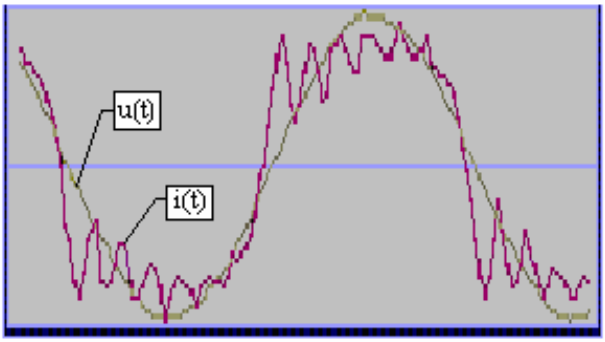

Fig. 1. *Current and voltage curves.*

For the total voltage distortion factor results THD_U = 0,00594, and for the total current distortion factor THD_I = 0,316. In table 2 are presented calculations according to the deffinition in Standard IEEE 1459 – 2000. Using the definition of professor Budeanu we have D = 368.263 VAd, and for the power factor the value is k_P = 0,86224. Comparing the total power factor according to Standardu IEEE 1459 – 2000 with the one according with Budeanu definition, we observe that the two values are almost identical (difference of 0.0023%). This minimum difference is due to calculation because, in fact, the deffinition of the power factor is essentially the same.

Also the apparent nonfundamental power with the expresion of Emanuel (S_E from table 2) differs only with 0.022% to that from Standard IEEE 1459 – 2000. In this case the simplier relation of Emanuel can be used in order to calculate the nonfundamental apparent power

6. CONCLUSIONS

The Standard 1459-2000 has elaborated a practical methodology for measurements of the apparent power and of its components, in electric circuits with nonlinear and non balanced consumers. In this purpose the definitions of active , reactive and apparent power are made according to the practical possibilities of making the measurements in electric networks.In the expresions of these powers are put in evidence the components due to the perturbations of voltages and currents (nonsymetry and distortion).

The components of the apparent power due to voltage distortion, due to current distortion and the component due to both voltage and current distortion are put in evidence

In the standard we can find the reactive power and the distortion power according to the Budeanu concept, but for the last one, in the standard it is measured in VAr and not in VAd. By other words the apparent power has two components : the active one and the nonactive one. The nonactive power has two components of the same signification, that of reactive power. This last statement is arguable, but it is practical sustained: in order to eliminate the harmonics filters are used, and mainly the filters are made of reactive elements, L and C.

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Table 1

Order of harmonic	U[V]	I[A]	Phase difference between voltage and current [^{0}]	P[W]	Q[Var]
1	68.035	15,6	25,2	960.520	427.548
3	143	3,56	162	- 484	118,8
5	154	2	186,8	- 305,8	- 36,5
7	286	1,32	289,1	123,2	- 360,8
9	45,1	1,08	250,5	- 16,3	- 44
11	55	0,96	242,2	- 24,6	- 48,4
13	143	1,64	254,8	- 61,6	- 224,4
15	73,7	1,12	259	- 15,8	- 79,2
	U_H = 404,1	I_H = 4,93		P_H = - 784,9	Q_H = - 674,5
	U = 68.036,2	I = 16,36		$\sum P$ = 959.735,1	$\sum Q = Q_B$ = 426.873,5

Table 2

S[VA]	S_1[VA]	S_N[VA]	S_H[VA]	D_I[Var]	D_U[VAr]	P_{F1}	P_F	S_E[VA]
1.113.072	1.061.346	335.372	1992,2	335.413	6304	0,905	0,86222	335.445

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ДОЂИТЕ ДА СЕ ДОГОВОРИМО!

INSTRUCTION FOR AUTHORS

Name of the author/s, Affiliation/s

Abstract: *Short instruction for authors is presented in this paper. Works that are to be printed in the review "Electronics" should be typed according to this instruction.*
Keywords: *Review Electronics, Faculty of Electrical Engineering in Banjaluka, Instruction for authors.*

1. INTRODUCTION

In the review "Electronics", we publish the scientific and professional works from different fields of electronics in the broadest sense like: automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. In addition to the scientific and professional works, we present new products, new books, B. Sc., M. Sc. and Ph.D. theses.

In order to enable the unification of the technical arrangement of the works, to simplify the printing of the review "ELECTRONICS", we are giving this instruction for the authors of the works to be published in this professional paper.

2. TECHNICAL DETAILS

2.1. Submitting the papers

The works are to be delivered to the editor of the review by the E-mail (elektronika@etfbl.net) or on floppy (or CD) by post mail to the address of the Faculty of Electrical Engineering (Elektrotehnicki fakultet, Patre 5, 78000 Banja Luka, Republic of Srpska, Bosnia and Herzegovina).

2.2. Typing details

The work has to be typed on the paper A4 format, 8.27" width and 11.69" height (21.0x29.7 cm), upper margin of 1" (2.54 cm) and lower margin of 0,59" (1,5 cm), left and right margins of 1,57" (2 cm) and 0,39" (1cm) (mirrored margins). The header and footer are 0,5" (1.27cm) and 57" (2 cm). The work has to be written in English language. Our suggestion to the authors is to make their works on a PC using the word processor MS WORD 97/2000, and for the figures to use the graphic program CorelDraw, if the graphs are not going from the original programs, i.e., from the programs received (like MATLAB).

The title of the work shall be written on the first page, in bold and 12 pt. size. Also, on the first page, moved for one line spacing from title, the author's name together with the name of his institution shall be printed in the letter size (10pt, *Italic)*. The remaining parts of the manuscript shall be done in two columns with 0.5cm distance. The work shall be typed with line spacing 1 (Single) and size not less than 10 pt (like as this instruction). After the title of the work and the name of the author/s, a short content in English language follows, written in italics. The subtitles in the text shall be written in bold, capital letters of the size as in the text (not less than 10 pt.). Each work shall, at the beginning, comprise a subtitle INTRODUCTION, and, at the end, the subtitles CONCLUSION and BIBLIOGRAPHY / REFERENCES.

The operators and size marks that do not use numerical values, shall be written in common letters. The size marks that can use numerical values shall be written in italics. The equations shall be written in one column with right edge numeration. If the breaking of equations or figures is desired, those may be placed over both columns.

Illustrations (tables, figures, graphs etc.) may be wider than one column if necessary. Above a table there shall be a title, for instance: Table 2. *The experimental measuring results.* The same applies to figures and graphs but the accompanying text comes underneath the figure of graphs, for instance: Fig.3: *Equivalent circuit diagram...*

The work should not be finished at the beginning of a page. If the last manuscript page is not full, the columns on that page should be made even. Number of pages should not go over 6.

3. CONCLUSION

This short instruction is presented in order to enable the unification of technical arrangement of the works.

4. REFERENCES

At the end of work, the used literature shall be listed in order as used in the text. The literature in the text, shall be enclosed in square brackets, for instance: ...in [2] is shown ...

ELECTRONICS, Vol. 9, No. 2, December 2005.