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PREFACE

This issue of the international journal "Electronics" is dedicated to VI Symposium on Industrial Electronics / INDEL 2006. The Symposium was held on the 10th and 11th November at the Faculty of Electrical Engineering in Banjaluka. More than hundred scientists and experts followed the work of the Symposium. There were 69 papers divided into 10 thematic areas: Materials and Components; Power Electronics; Analog and Digital Circuits; Electrical Machines and Drives; Measurement Methods and Systems; Signal Processing; Modeling, Identification and Process Control; Industrial Computers; Information Technologies; Telecommunication Technologies.

The 150th Anniversary of Nikola Tesla's birth was observed by the Plenary Session. Professor Milić Stojić was talking quite inspiringly about Nikola Tesla's life, work and overall contribution to the world's science. Professor Stojić, in his own manner, realistically portrayed Nikola Tesla's character and work. He integrated a sound recording of the Mayor of New York farewell speech at Nikola Tesla's funeral into his story.

For the first time a students' Competition called «Hardware and Software» was organized at the Symposium. The teams of four Electrical Engineering Faculties: Belgrade, Niš, Novi Sad and Banja Luka took part in the Competition. The task was to make Hardware and Software for remote control of the water-heating boiler through GSM. The teams had been working for 3 days, 12 hours a day. Each team had solved the task successfully. The Commission pronounced the solution of the team of the Faculty of Electrical Engineering from Novi Sad as the most successful one.

We have selected 11 papers for this issue of the Journal: three invited papers and eight papers upon proposition of the Chairpersons of the sessions. The invited paper «MODERN POWER ELECTRONICS TECHNOLOGIES IN WIND TURBINES» by Vladimir Katić presents an overview of application of modern technologies in renewable energy sources, i.e. conversion of wind into electric power. The focus is on power electronics converters and their complex control algorithms. Several models for connecting wind turbines into wind park are presented. The authors, Predrag Pejović and Predrag Božović; in their paper «THREE-PHASE LOW-HARMONIC RECTIFIERS IN THE DISCONTINUOUS CONDUCTION MODE» present a review of three versions of low-harmonic rectifiers that apply current injection and discontinuous conduction mode of the main three-phase diode bridge. All three of the proposed rectifier topologies have their own application area. The invited paper «CONTEMPORARY MOTION CONTROL SYSTEMS», by Slobodan N. Vukosavić, outlines the state of art and current trends in the field of motion control systems, focusing on the power converter topologies and sensors. This article outlines the impact of recent trends in motion control systems on the power converter topologies used in electric drives.

For the specificity of its contents, the paper «PROGRAMME OF ESTABLISHING A RECYCLING SYSTEM OF ELECTRONIC COMPUTER EQUIPMENT», by Jelena Milojković and Vančo Litovski, deserves to be emphasized. The research results presented in this paper were obtained through the research related to the end of existance of electronic computers in Serbia.

I would like to express my gratitude to the authors and to invite all the researchers interested in the field of electronics to present their development and research results in one of the following issues of the international journal of Electronics.

I would also like to invite all readers of the Electronics journal to take an active participation at the VII Symposium on Industrial Electronics / INDEL 2008, in November 2008.

President of the Symposium

Prof. Branko Dokić, PhD

MODERN POWER ELECTRONICS TECHNOLOGIES FOR WIND POWER PLANTS

- Invited paper -

Vladimir Katić, Faculty of Technical Sciences, Novi Sad, Serbia

Abstract: *The paper presents an overview of modern technologies applications in wind power plants, i.e. in conversion of wind to electric energy. The focus is on power electronics converters and their complex control algorithms. The aim of the paper is to presents place, role and significance of their application. Different solutions are presented, but all showing that power electronics converters have a key role in connecting a variable source - wind power to very stable system - electric power system. The most advanced solutions are presented with their mathematical and computer models. Design of special control circuits with vector-oriented control is described. Several model of connecting wind turbines into wind park are presented. The role of power electronics converters in such connections is discussed. It is shown that without application of modern power electronics converters high efficiency and cost effectiveness of wind plants is not possible.*

Keywords: *Wind Power, Power Electronics, Synchronous generators*

1. INTRODUCTION

The beginning of the XXI century is marked with fast increase of energy consumption, especially fossil fuels, indicating that they might soon be exhausted. These trend lead to slow but constant increase of oil prices, continued from the end of previous century, and also to global worries for future energy supplies and development of mankind.

Another characteristic of this period is further increase of concentration of CO_2 and other gases in atmosphere resulting in green house effects, i.e. global warming and climate changes. Despite of world wide accepted agreement of lowering the level of CO_2 emission (Kyoto protocol from 1997), situation in 2007 is even worse.

At the same time, the increase of public ecological awareness and activities of green movements political parties forced that in many countries nuclear energy is abounded or even banned, although it is more powerful, energy effective and cheaper, but for the environment very risky energy source.

These trends at the end of XX century have led the most developed, industrial countries all over the World, European Union (EU) before the others, to turn to wide usage of renewable energy sources (RES). At that period EU have used only 6% of its total energy needs from RES (mostly from large hydro power station and bio-mass), while 79% came from fossil fuels (oil and derivates 41%, natural gas 22 % and coal 16%), and rest from nuclear sources (Fig.1.up).

As a result of this situation a strategic decision has been adopted in a form of EU directive No.2001/77/EC [2]. It stated that the share of "green" energy have to be increased from 6% in 1998 to 12% up to 2010. This decision was crucial for fast development of usage of all kinds of renewable sources.

Use of the RES for production of electrical energy is of special interest, as this type of energy is the most suitable for every day need of human life. At the time of above-mentioned directive (1998), the share of RES in electrical energy production in 15 EU countries was between 1,1% (Belgium) up to 70% (Austria), in average 14%. Directive has stipulated that such a share should be increased to 22% in 2010. Fig.1. (down) presents a renewable energy sources distribution in 1998. It can be seen that the vast majority of produced energy came from large hydro power station, while other sources contributed far less. The wind share was only 3,2%.

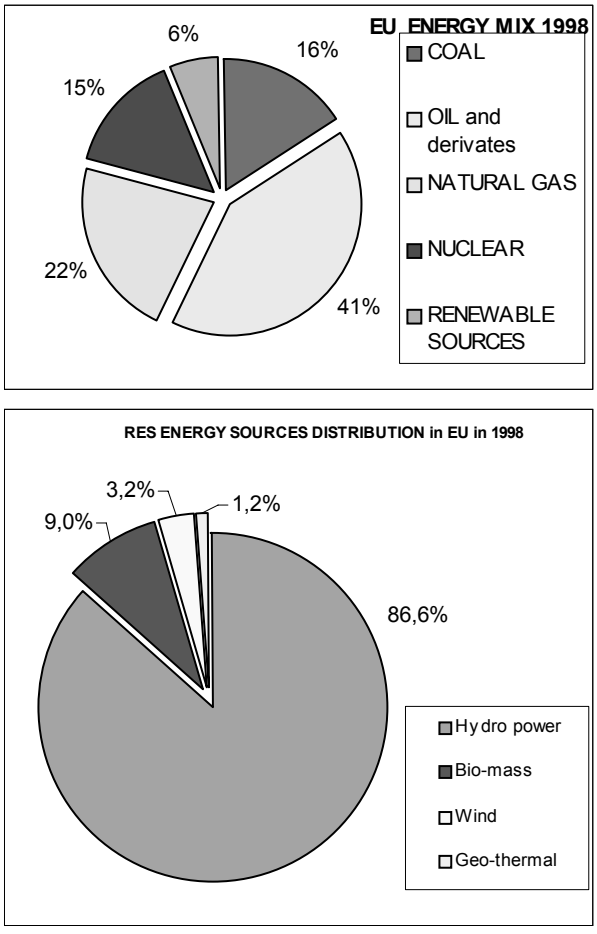

Fig. 1: *EU energy mix in 1998 (up) and RES distribution in EU production of electrical energy in 1998 (down).*

However, the possibilities for further increase of usage of hydro power were very limited, as almost all significant hydro potential has been already used or its exploitation was too costly and with significant negative environmental effects. In that situation attention of researches, designers, industry, investors and others have turn toward wind and sun energy, as sources, where efficiency, developed technology and availability in EU countries were the most convenient. As a result a large amount of research and financial resources have been invested during Framework Program 5 in

development of technology and end-user solutions. It led to very fast grow of wind power industry especially, comparable only to progress in computer industry. Fig.2 represents this increasing trend of installed capacities of wind power with prediction up to year 2020 and its effects on CO_2 reduction. It is obvious that wind power plants significantly reduce emission of gasses (CO_2) and therefore contributes to improvements of environment conditions.

Fig. 3 gives a look into present situation (end of 2006) regarding installed wind power capacities, according to data of European Wind Energy Association – EWEA [3]. It can be noticed that Germany, Spain, Denmark, Great Britain, Holland and Portugal have the largest installed wind power. At the same time, in the area of West Balkan (Albania, Bosnia and Herzegovina, Macedonia, Montenegro and Serbia), there is not a single wind power station. Still, it should be mentioned that in Montenegro exists one wind power unit of 0,5MW at Vilusi, but it is not operational, as it was destroyed by lighting in 2005 and not repaired yet [4].

Inclusion of wind power and other RES into electric power system brings new possibilities for restructuring of such system. Taking advantages of deregulation process and electrical energy market, wind power plants can be connected as distribution generators, too. Anther possibility is to form micro-grids, which are more flexible and resilient to system disturbances, but more complexes for control.

In this paper the latest technology of high power wind power plants is presented, as well as some aspects of their grouping in wind farms. The role of power electronics is specially emphasized regarding achievement of maximum efficiency by using advanced control algorithm.

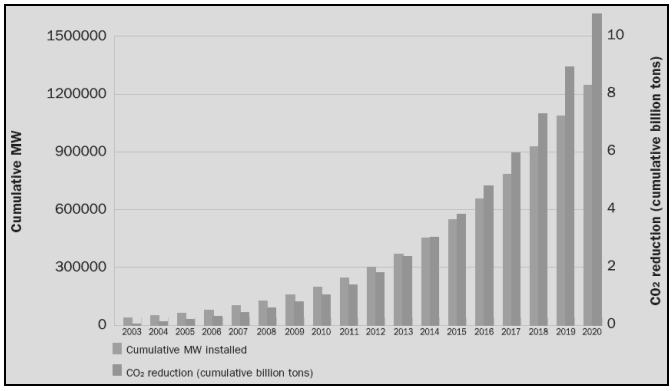

Fig. 2: *Installed wind power in EU, with prospects of grows up to year 2020 and effects on CO_2 reduction [3].*

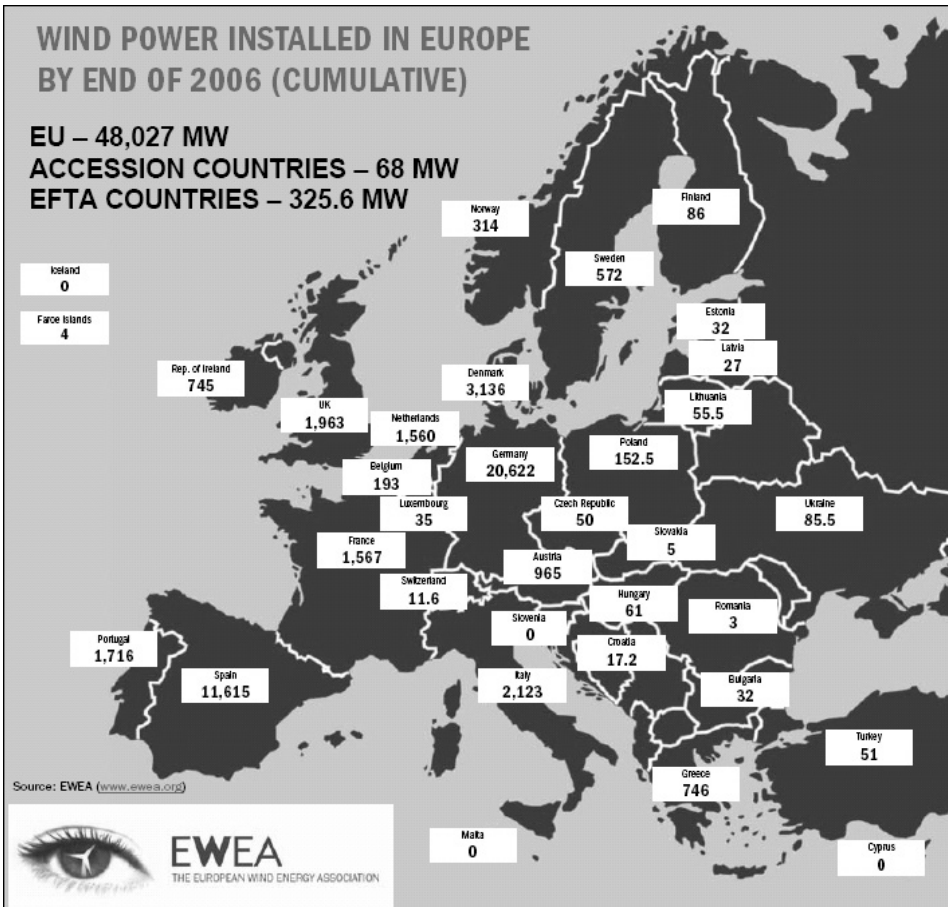

Fig. 3: *Installed wind power capacities in Europe (end of 2006) [3].*

2. WIND POWER PLANT

Today's wind power plants are of MW size. In wind to electric conversion sub-system, they consist of wind-turbine and electric generator connected via power electronic converters, power transformer and medium voltage (MV) line to the nearest distribution network grid. Wind-turbine has a three blades rotor, with possibility of pitch and stall control, a low speed shaft and a gearbox. It is located on a top of high tower, as it is shown on Fig.4. Kinetic (mechanical) energy of wind is converted to kinetic energy of rotating mass of wind

turbine, which is further leading via gearbox, for speed multiplication, to electric generator high speed shaft (Fig.5). Mechanical energy is now converted into electrical, but with non-stable parameters. Power electronics converters make further conversions, but this time from electrical to electrical in order to produce output with stable electrical parameters, as it is requested by the electric power system. This conversion puts power electronics converter in a role of buffer zone between two very different power systems: mechanical, powered by the non stable and often very variable energy of wind; and electrical, with very stable parameters and low tolerances. Transformer and MV line enable transfer of electrical energy to the power system [1,5].

Fig. 4: *Output look of a wind power plant of 4.5 MW.*

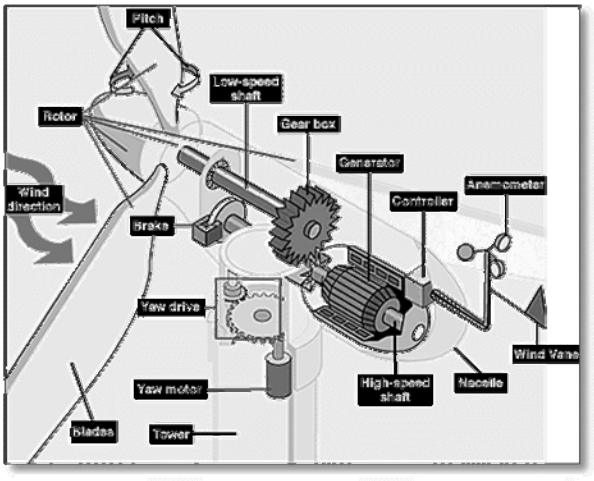

Fig. 5: *Inside look of wind to electric conversion part.*

3. ROLE OF POWER ELECTRONICS CONVERTERS IN WIND POWER PLANT

Fig.6 shows the place and role of power electronics converters in the wind power plant. Their role is to connect two electrical systems, electrical system of wind power plant, which is producing electrical energy with non-stable electrical parameters (voltage, frequency, phase shift), with public electrical power system, which demands very stable parameters. Additional demand is that whole system should operate with high efficiency. This role is more or less achieved with different solutions depending on type of generator, power level, and methods of operation and control of power electronics converters.

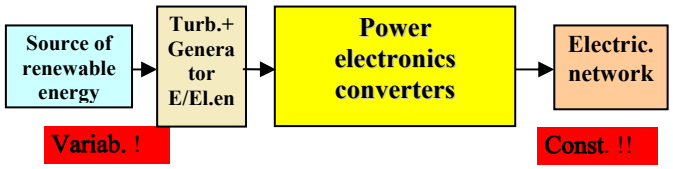

Fig. 6: *The role of power electronics converters in wind power plant.*

3.1 Overview

Nowadays wind power plants use either asynchronous or synchronous electrical machines as generator, so there are several possibilities for their direct or indirect (via power electronics converters) connection to the network. In Table 1 an overview of different possible solutions is presented, while in Table 2, a classification according to speed and power control type is given [6]. Asynchronous generators are mostly used for units below 1MW, while synchronous for powers above 500kW. The most modern wind power units nowadays use synchronous generators.

At the beginning wind power units have used asynchronous generators with fixed speed (Type A), where power control was performed as Stall control (Type A0), Pitch control (Type A1) or Active stall (Type A2). Nowadays technology uses a variable speed control principle, which controls electrical parameters of generator and power converters and enable more flexible and efficient operation (Types B to D). All types of mechanical control are also present (stall, pitch or active stall). Figures 7 and 8 represent different schematics of some of the mentioned solutions with asynchronous (Fig. 7) or synchronous (Fig. 8) generators.

3.2 Asynchronous generator

Asynchronous machine is characterized with low price and high reliability in different operating conditions, and therefore has advantage over synchronous machine. These were the reasons why the first wind turbines have used asynchronous generator. Nowadays, they are still in use applying both rotor constructions: cage and wound.

Asynchronous generators with cage rotor use power electronics converters for soft start (Fig. 7.a). Such solution was very popular with Danish manufacturers of wind turbines, so it is known as Danish concept. The converter is design with anti-parallel thyristors in each phase and operates on voltage regulation using phase control principle. The role of power converter is to ease current stresses during generator connection on the grid. Capacitor bank gives necessary reactive energy for generator field operation. The generator is

of fixed speed and is declared as Type A (Table 1). Mechanical connection and adaptation to wind-turbine speed is achieved through mechanical gearbox. Power control uses Stall (Type A0), Pitch (Type A1) or Active stall (Type A2) control principles.

Another design, which is represented in Fig. 7.b, uses asynchronous generator with cage rotor connected to the grid via fully-controlled frequency converter (series connection of a rectifier and inverter via DC link). Such solution has disadvantage of higher price of power electronic converter circuit and more complex control, but enables speed variation and therefore better characteristics.

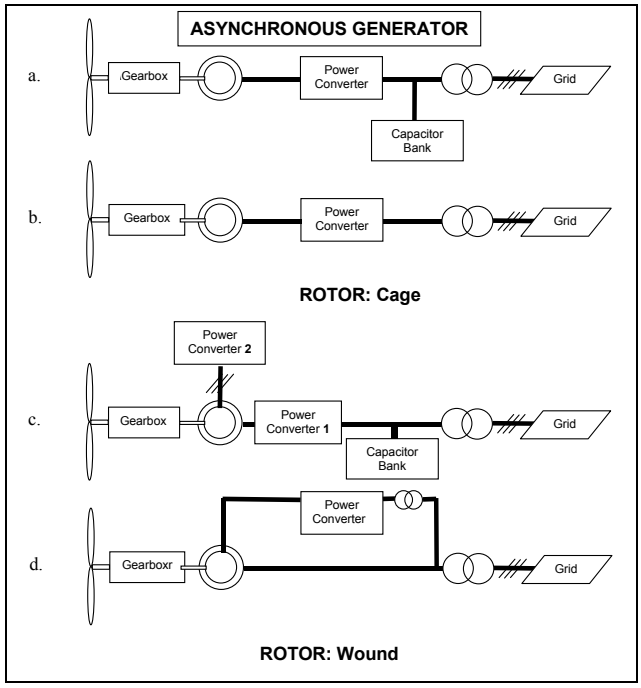

Fig.7: *Wind power plants with asynchronous generator.*

Asynchronous generators with wound rotor are in use in two configuration, which are presented in Figs. 7.c and 7.d. Both designs are with variable speed, so they are declared as Type B and Type C [6]. Mechanical power control is done by changing blade angle (pitch control), while other methods are rarely used (that's why they are shaded gray in Table 2).

Type B, in fact, has limited speed control possibilities, as power converter 1 has a soft start role, while power converter 2 has a variable resistor role. Such solution is also favorable at Danish manufacturers (Vestas), which have unique way of maintenance of slip rings. They have placed the power converter 2 very close to the shaft, connected it optically with control circuit and in such way eliminated slip rings. Speed control range depends on power converter 2 size and typical ranges are 0-10% above synchronous speed.

The solution with double converter in rotor circuit (Type C) is very popular in modern realizations. It is known as Doubly Fed Induction Generator (DFIG). Power converter is around 30% of generator size, which make it economically attractive, and speed control range is much wider than in type B case. Remaining problems are slip rings maintenance and protection from network faults.

However, for high performance drives an asynchronous machine has several disadvantages:

- Rotor losses
- Complexity of control algorithm, as slip estimation and variable rotor parameter compensation (rotor resistance) is needed.
- High nominal speed, which demand usage of mechanical speed multiplication (gearbox).

Table 1 – Overview of wind power generator solutions.

	Type of generator	Rotor	Gearbox	Power Converter		Type
				Rotor circuit	Stator circuit	
1.	**Asynchronous**	**Cage**	**Gearbox**	/	/	**A**
2.	**Asynchronous**	**Cage**	**Gearbox**	/	**AC/AC (Soft-start)**	**A**
3.	**Asynchronous**	**Cage**	**Gearbox**	/	**AC/DC/AC**	**C**
4.	**Asynchronous**	**Wound**	**Gearbox**	**Variable resistor**	**AC/AC (Soft-start)**	**B**
5.	**Asynchronous**	**Wound**	**Gearbox**	**AC/DC/AC + Transf.**	/	**C**
6.	**Synchronous**	**Wound - Field**	**Gearbox**	**AC/DC**	/	**A**
7.	**Synchronous**	**Wound - Field**	**Gearbox**	**AC/DC**	**AC/DC/AC**	**D**
8.	**Synchronous**	**Wound - Field**	/	**AC/DC**	**AC/DC/AC**	**D**
9.	**Synchronous**	**Permanent magnetized**	/	/	**AC/DC/AC**	**D**

Table 2 - Speed/Control Classification [6].

Speed \ Control		Control		
		Stall	Pitch	Active Stall
Fixed speed	**Type A**	**Type A0**	**Type A1**	**Type A2**
Variable speed	**Type B**	**Type B1**	**Type B1**	**Type B2**
	Type C	**Type C1**	**Type C1**	**Type C2**
	Type D	**Type D1**	**Type D1**	**Type D2**

3.3 Synchronous generator

Improvements in control theory, as well as development of technologies for implementing such theories, led to introduction of vector control principles for AC machines. Such control algorithms enable that nonlinear and non-stationary control object, such as synchronous or asynchronous machines, move closer to performances of DC machines, and in some aspects even overrides them (price, reliability, loading possibilities, torque and size rate, etc.).

Application of such control methods have led to significant advantages of synchronous machines, i.e. synchronous generators. In general two types of generator construction are possible: with field wounded at rotor (Figs. 8.a,b,c) or with permanent magnetized field on rotor (Fig. 8.d).

In the first group, power converters are applied in three configurations: 1. as simple rectifiers with a task to give DC field for rotor wounding (Fig. 8.a), 2. as combination of two power converters of which one is rectifier, which provides DC supply for rotor field wounding, and the other is frequency converter, which enable variable speed operation (Fig. 8.b), and 3. this is the same as 2nd configuration, but with fully-controlled four-quadrant power converter application. In this case installation of a multi-pole generator is possible, i.e. operation without mechanical speed multiplication (gearbox) (Fig. 8.c). The first two configurations are relatively rare in application, as additional cost arises for slip ring maintenance, while the third one is attractive due to significant cost reduction for gearbox.

However, in modern drives the construction with synchronous machine with permanent magnetization at rotor (Surface Mounted Synchronous Machine - SMSM) is much more suitable regarding control. In manufacturing the permanent magnets rare earth materials are used (Samarijum-Kobalt or similar). One of their characteristics is that rotor current is very low, almost negligible, so beside its angular position value, there is no other parameter of rotor effecting on dynamics of the drive. Such fully controlled wind power unit, presented in Fig. 8.d, consists of wind turbine directly connected to the permanent magnet synchronous generator. Stator winding of the generator is connected to the grid, via fully controlled frequency converter, which enable it variable speed operation. The control is designed in such a way that at every moment and at each wind speed, maximum power is extracted from the wind. Such task is possible to fulfill with complex algorithms of vector control of SMSM and power converters, combined with active turbine control (pitch control). Such configuration is classified as type D and nowadays is one of the common designs for large wind power units (over 1 MW). According to data sources from 2002 [4], these units covers 20,3% of the wind market, i.e. have 1471,3 MW of installed capacity.

4. WIND GENERATOR CONTROL

In above mentioned solution a fully controlled power electronics converter is applied, which consists of fully controlled AC/DC converter, DC link and IGBT DC/AC converter, similar to previous solutions (Fig. 9). Operation and control of the power converter are defined with complex wind power conversion expressions, maximum power tracking algorithm, as well as vector control principles and a special task of output voltage adaptation to the grid demands.

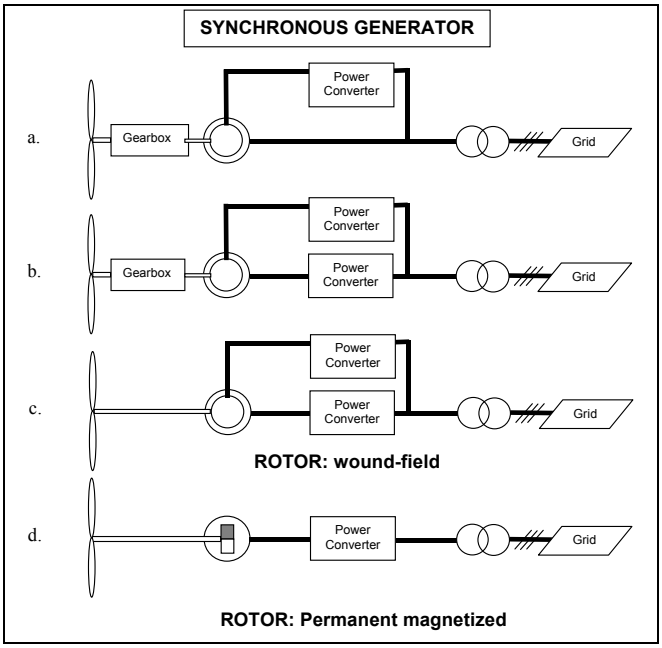

Fig.8: *Wind power plants with synchronous generator.*

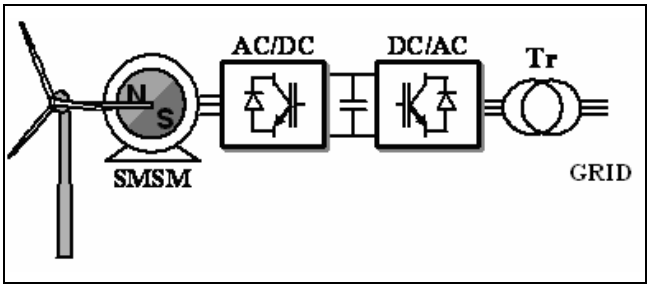

Fig. 9: *Wind-generator with SMSM controlled by power electronics converter.*

Fig. 10.a shows dependence of wind turbine power p_{el} on turbine speed n with family of curves, each representing one wind speed v_{WIND}. To obtain maximum power flow at any wind speed v_{WIND}, the wind turbine should be controlled in such a way that it follow the curve $p_{OPT}=f(n)$ [1,3]. Also, two power control areas can be spotted:

1. variable speed zone (*A* part of the curve), where speed of the drive is controlled depending on the wind speed.
2. power control zone (*B* part of the curve), which corresponds to speeds above nominal and in which output power is maintained at nominal value.

In Fig. 10.b an approximate wind generator characteristics, which is modeled in the paper is given. The characteristic is actually an approximation of p_{OPT} curve. Based on it, it is possible to determine the referent value of output power p_{el}^{ref} for the given rotor speed n, and further referent value of electromagnetic torque.

On the other hand, the wind power can be modeled with $p_{WIND} = v_{WIND}^3$. For wind speeds less than nominal, input mechanical power p_m is equal wind power. However, for wind speed above nominal, the p_m should be kept at nominal value. This is achieved with pitch (active) and stall (passive) control.

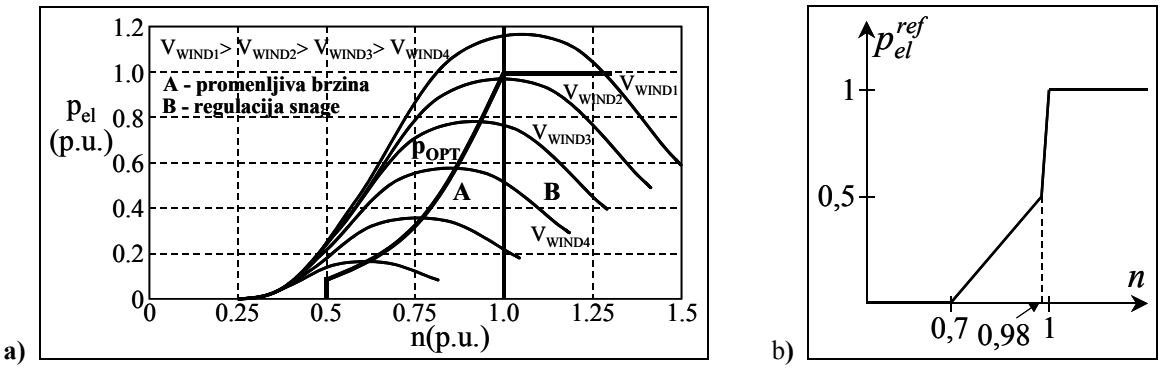

Fig. 10. *a) Wind turbine characteristic with variable speed (A) and power control (B) zones. b) Approximation of optimal control characteristics of wind turbine.*

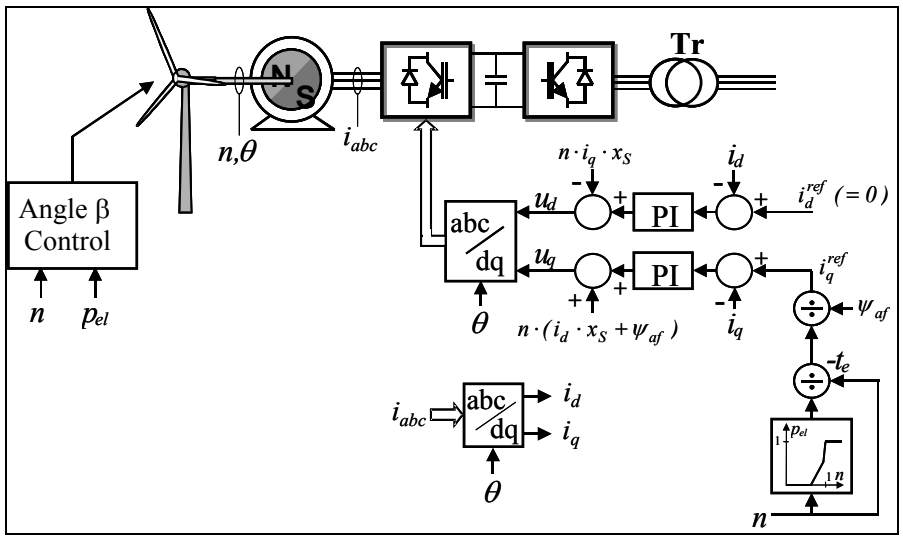

Fig. 11: *Control scheme with SMSM wind power generator.*

5. MODEL OF THE WHOLE DRIVE

Model of the complete drive with SMSM generator and fully-controlled power electronics converter is shown in Fig.11. The control structure of the converter connected to the generator, which enable decoupled torque and flux control, use the algorithm described in [5,6]. In control structure of torque regulator, the reference is read from wind generator characteristic $p_{el}^{ref} = f(n)$ (Fig. 10.b), after parameter p_{el}^{ref} is divided with actual speed *n*. Developed model enables computer simulations of different operating conditions during variable input wind power, as well as different operating conditions at the output, i.e. electric power system. Some of these results are presented in [6].

6. WIND PARKS

By connecting several or more wind power units at the same output grid, a problem of stability, i.e. variable output power can be solved and at the same time, more power achieved. That is why single unit wind power plants are rarely erected nowadays. The role of the power electronics converters in this case is in connection, coordination and control of all this units.

The most common are series and star connections of wind power units. Power electronics converters enable connection at DC or AC link level or with two DC levels. In the first case number of converter is high, but they are of lower power rating and therefore cheaper. In the second case, number of converters is lower, but their power rating is as power of a series and a star branch is, and therefore much more expensive for initial investment. In the third case, the structure of the converters is similar to second one, but by applying additional DC level cheaper and more efficient connection by underwater cable is achieved. Figs. 12, 13 and 14 show the above mentioned cases for series and star structure of wind power units in a wind park.

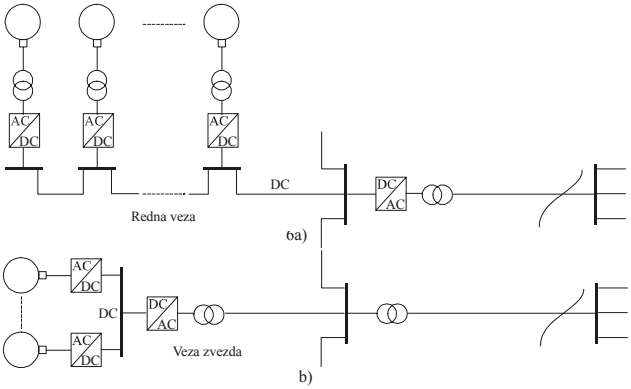

Fig. 12: *Connection with common DC link: a) series, b) star.*

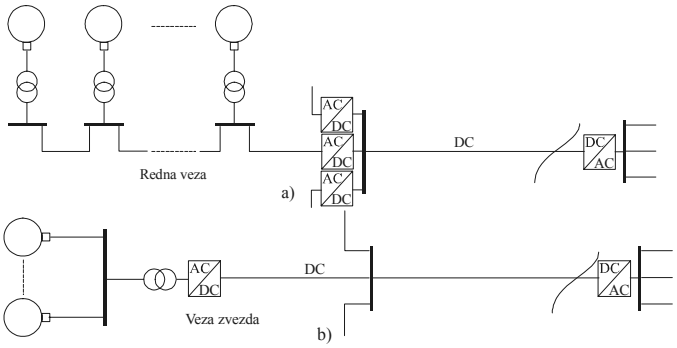

Fig. 13: *Connection with common AC link: a) series, b) star.*

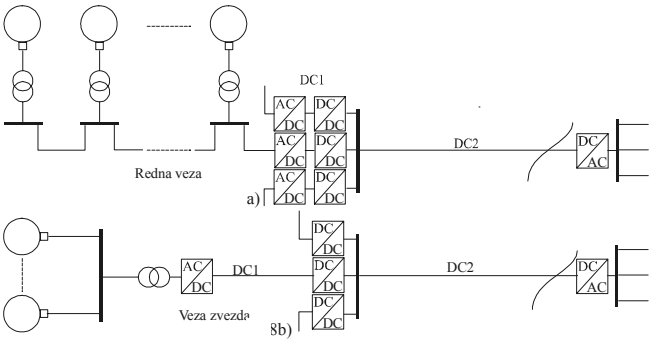

Fig. 14: *Connection with two DC links: a) series, b) star.*

7. CONCLUSION

The paper gives an overview of power electronics converters application in modern renewable energy sources and particularly in wind power plants. It gives the place, role and its significance in achieving the maximum energy conversion and the highest power efficiency.

It is shown that power electronics converters have the key role in modern wind power plants where the aim is to achieve high conversion rate and efficiency of operation. These achievements are result of application of complex algorithms of vector control, which gave sophisticated speed control of the whole wind drive, as well as fast responses to grid condition variation.

The solution where synchronous machine with permanent magnets in rotor is applied as generator has been especially considered. In such a case, fully controlled power electronics converters give possibility of decoupled flux and generator torque control application. Developed model of mechanical sub-system, which is briefly described in the paper, enable further improvement in design of high efficiency wind power control algorithms.

The task of connecting wind power units in wind parks or wind farms is presented also, but from a view of application of power converters. In this case they have key role, also. Their application and high quality of operation make it possible to obtain the best design and optimum solution in every case of wind power plant application (on-shore or off-shore).

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THREE-PHASE LOW-HARMONIC RECTIFIERS THAT APPLY CURRENT INJECTION IN THE DISCONTINUOUS CONDUCTION MODE

- Invited paper -

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Abstract: *This paper presents a review of three versions of low-harmonic rectifiers that apply current injection and discontinuous conduction mode of the main three-phase diode bridge. All three of the proposed rectifier topologies are compared according to the total harmonic distortion of the input currents and according to the circuit complexity. It is shown that all three of the topologies have their own application area, since each of them provides specific properties favoring the rectifier for one application, and discrediting it for another. References where detailed analyses for each of the topologies could be found are provided, containing the rectifier analysis, design considerations and experimental results.*

Keywords: *AC–DC power conversion, converters, harmonic distortion, power conversion harmonics, power quality, rectifiers.*

1. INTRODUCTION

Current injection is a method to reduce total harmonic distortion (THD) of the input currents in three phase diode bridge rectifiers supplied from voltage sources. Structure of this class of rectifiers is presented in Fig. 1, where two subsystems responsible for the current injection are identified: a current injection network and a current injection device. Detailed analysis of this class of rectifiers can be found in [1]. To reduce the reference list, this reference will be frequently cited, even in cases when the origin of the idea is not in [1], but [1] presents the idea and provides the original reference.

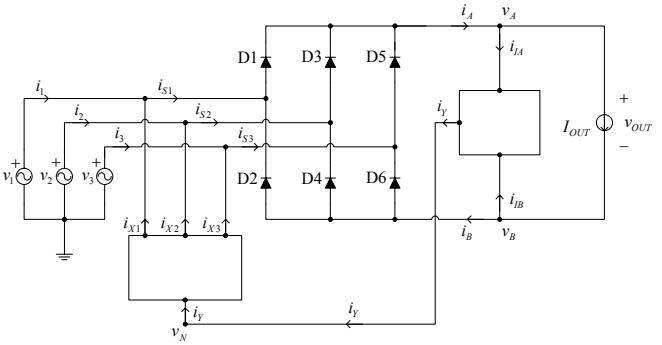

Fig. 1: *Structure of a current injection based rectifier.*

In the analysis that follows, we will assume that the rectifiers are supplied by a symmetrical undistorted three-phase voltage system, specified by

$$v_k = V_m \cos\left(\omega_0 t - (k-1)\frac{2\pi}{3}\right). \qquad (1)$$

The current injection device shown in Fig. 1 is a magnetic device that satisfies the following three element equations over the voltages and currents

$$i_{X1} = i_{X2} = i_{X3} = \frac{1}{3} i_Y \qquad (2)$$

and

$$v_N = \frac{1}{3}(v_1 + v_2 + v_3). \qquad (3)$$

The element characteristic specified by (2) and (3) can be satisfied with many different device constructions, some of them described in Chapter 4 of [1]. Current experience favors two of the constructions: (1) construction based on a zigzag connected autotransformer, and (2) construction that applies a front end transformer with delta-connected primary and wye-connected secondary, the current being injected in the neutral point of the secondary winding system. The second construction is favored in cases when the rectifier is supplied from a high-voltage supply line, and the voltage level adjustment is required. For the analysis that follows, construction details of the current injection device will not be relevant, and it will be sufficient that he device satisfies (2) and (3).

The current injection network, indicated in Fig. 1, will be a "degree of freedom" for the analysis presented in this paper. Our attention will be focused to the case that the main three-phase diode bridge conducts in the discontinuous conduction mode, only.

The first analyses of the rectifiers that apply the current injection method were performed assuming the continuous conduction mode, when $i_A > 0$ and $i_B > 0$ during the whole period. In that case, the rectifier output voltage is given by

$$V_{OUT} = \frac{3\sqrt{3}}{\pi} V_m \approx 1.65\, V_m \qquad (4)$$

and it is not dependent on the output current, assuming negligible losses. Total harmonic distortion of the input currents depends on the construction of the current injection network, and in theory it is possible to achieve zero distortion of the input currents in the case of the optimal current injection, as described in [1], Chapter 7. In the case of the optimal third-harmonic current injection, total harmonic distortion of the input currents of about 5% can be achieved, as described in Chapter 5 of [1], while in the case of the square-wave current injection achievable THD of the input currents is about 15%, which will be discussed here. All of the current injection networks that correspond to these waveforms of the injected current differ in complexity and in some other parameters, like the sensitivity on the supply frequency variation.

It can be shown, [1], that in the continuous conduction mode the current injection network takes about 8% of the input power from the diode bridge output terminals in order to reduce the input current THD. The power taken by the current injection network slightly depends on the current injection method applied. The power taken by the current injection network could be dissipated on the current injection network resistors or restored at the rectifier output applying resistance emulators.

In this paper, only current injection networks that result in the discontinuous conduction mode of the main three-phase diode bridge will be analyzed. This mode is characterized by the time intervals in which the diode bridge output terminal currents are equal to zero, $i_A = 0$ or $i_B = 0$. Analysis of these circuits is complex, since the state changing instants are determined by transcendental equations that do not have closed-form solutions. This causes simulation of normalized piecewise-linear model of the circuit to be the main analysis method. Development of suitable analysis methods for this kind of circuits was a difficult task, and the time elapsed from the first paper where applicability of the discontinuous conduction mode was indicated to the papers where the complete analysis is presented was about five years, as documented in [1]. Advantage of the discontinuous conduction mode in comparison to the continuous conduction mode is in simple recovery of the power taken by the current injection network by an increase of the rectifier output voltage. The increase of the average value of the output voltage is achieved by increased instantaneous value of the output voltage during the discontinuous conduction intervals. Unfortunately, this makes the output voltage dependent on the output current, but this variation will be shown to be moderate, limited to the output voltage range from the voltage in the continuous conduction mode to the voltage 13% above this voltage.

The current injection network is the "degree of freedom" that will be analyzed. The first current injection network contains two capacitors, an inductor and a transformer, only. The remaining two configurations contain passive voltage loaded resistance emulator which provides lower variation of the output voltage and lower THD of the input currents. The first two of the analyzed current injection networks apply resonant circuits tuned to the third harmonic of the line voltage. Thus, these two circuits are not convenient for application in systems where significant variations of the supply frequency is expected. The third current injection network does not apply resonance, and the input current waveform is not dependent on the supply frequency, but the input current THD is higher than provided by previously described two current injection networks that apply resonance.

2. THE BASIC STRUCTURE FOR OPERATION IN THE DISCONTINUOUS CONDUCTION MODE

The simplest structure of the current injection network that provides the rectifier operation in the discontinuous conduction mode is shown in Fig. 2. Analysis of the rectifier that applies this current injection network is shown in [2], and even more detailed analysis is presented in [1]. The current injection network of Fig. 2 is derived from the current injection network intended for the third harmonic current injection in the continuous conduction mode in such a way that the resistor intended to dissipate the power taken by the current injection network is omitted from the network. This modification yields to the discontinuous conduction operating mode of the main three-phase diode bridge, causing recovery of the power taken by the current injection network in the continuous conduction time intervals during the discontinuous conduction time intervals.

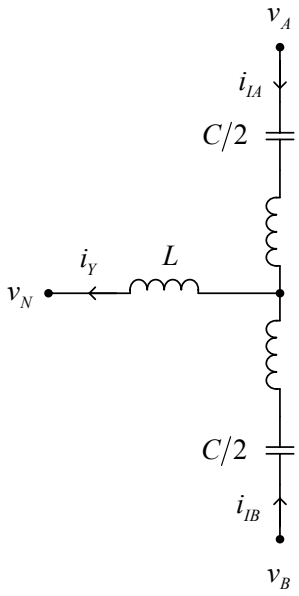

Fig. 2: *Basic current injection network.*

To provide the current injection in order to reduce the input current THD, components of the current injection network should provide resonance at the triple of the line frequency, i.e., they should satisfy a resonance constraint

$$LC = \frac{1}{9\omega_0^2}. \tag{5}$$

This resonance constraint causes the rectifier performance to be sensitive on variations of component parameters, as well as on variations of the input voltage frequency. Detailed analysis of these effects can be found in [1] and [2]. Results of the analyses presented in [1] and [2] can be summarized to a conclusion that the sensitivity is higher for the higher *Q*-factor values of the current injection network. On the other hand, high values of the *Q*-factor are convenient to reduce the input current THD.

In the case the *Q*-factor of the current injection network is high enough, the injected current i_Y can be assumed sinusoidal, with the only spectral component at the triple of the line frequency. In that case, the average of the output voltage is

$$V_{OUT} = \frac{27\sqrt{3}}{8\pi} V_m \approx 1.86\, V_m \tag{6}$$

Waveform of the input current at the first phase that corresponds to this case is shown in Fig. 3, while the THD of the input currents obtained in this way is

$$THD = \frac{\sqrt{224\pi^2 - 2187}}{27\sqrt{3}} \approx 10.43\,\%. \tag{7}$$

In the case that the current injection network has a finite value of the *Q*-factor, which is always the case in practice, the THD value is higher than specified by (7), while the output voltage depends on the output current, varying from the value specified by (6) to the value given by (5). This output voltage variation is 13% of the value (5), and for many applications it is acceptable.

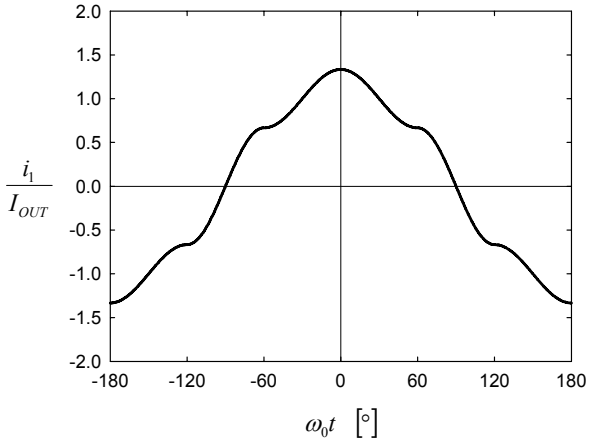

Fig. 3: *Waveform of the input current, basic current injection network.*

3. THE RECTIFIER THAT APPLIES A RESISTANCE EMULATOR

To reduce the THD and to reduce variations of the output voltage, the current injection network of Fig. 2 is supplied by a voltage loaded resistance emulator, resulting in the current injection network shown in Fig. 4. The resistance emulator consists of the transformer with the turns ratio 1:*n* and four diodes, DR1 to DR4. The elements of the current injection network should satisfy the resonance constraint (5) in this case, also. Detailed exposition of the rectifiers that apply this current injection network can be found in [3] and [4], and a detailed analysis is given in [1]. It should be noted here that the current injection network of Fig. 4 is proposed in [4] for the first time.

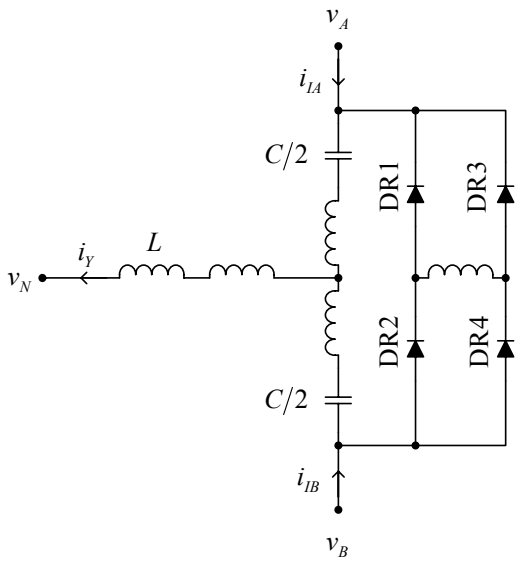

Fig. 4: *Resonant current injection network that applies a resistance emulator.*

The resistance emulator introduced provides an additional degree of freedom in the form of the choice of the transformer turns ratio. Several optimization criteria were applied in [1]. In the case that losses in the current injection system can be neglected, the rectifier operates in the discontinuous conduction mode, and the optimal value for the turns ratio is

$$n_{DCM} = 6\frac{7\pi - 20}{36 - 11\pi} \approx 8.28\,. \tag{8}$$

Total harmonic distortion of the input current in this case is given by

$$THD = \frac{\sqrt{936\pi^4 - 3424\pi^3 - 16377\pi^2 + 89640\pi - 104976}}{9(13\pi - 36)} \tag{9}$$

which is

$$THD \approx 7.71\% \tag{10}$$

approximately. Waveform of the input current that corresponds to this case is given in Fig. 5.

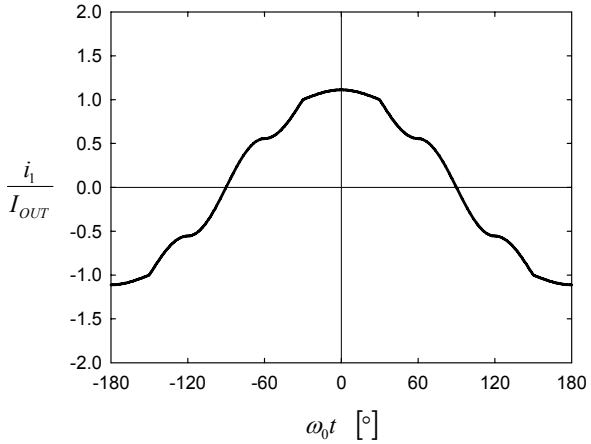

Fig. 5: *Waveform of the input current, resonant current injection network with a resistance emulator.*

However, application of the resistance emulator with the transformer having the turns ratio given by (8) even at low losses causes the rectifier to operate in the continuous conduction mode. Optimization of the transformer turns ratio in the continuous conduction mode provides somewhat different value of the resistance emulator transformer turns ratio,

$$n = 10\,. \tag{11}$$

In this case, with the optimal amplitude of the injected current the input current THD is reduced to

$$THD = \frac{1}{3}\sqrt{\pi^2 - \frac{69}{7}} \approx 3.72\%\,. \tag{12}$$

The rectifier with the transformer with the turns ratio $n = 10$ in the discontinuous conduction mode provides somewhat higher THD of the input currents than the value given by (10), equal to

$$THD = \frac{1}{9}\sqrt{\frac{61\pi^2 - 36\pi - 486}{6}} \approx 7.79\%\,. \tag{13}$$

Fortunately, the minimum of the input current THD over the transformer turns ratio is not sharp, thus small deviations from the optimal value negligibly affect the rectifier operation. In practice, the rectifier provides the input current THD in the range from 3% to 8%, with the output voltage characterized by low dependence on the output current, with the value close to the value specified by (4).

The rectifier that applies the resonant circuit and the resistance emulator in the current injection network provides the lowest input current THD of all three of the rectifiers analyzed in this paper. However, the performance is achieved for the price of increased circuit complexity and the resonance constraint imposed to the current injection

network. The resonance constraint causes sensitivity of the rectifier performance on the component parameter variations, as well as on the variations of the line frequency.

4. TWELVE-PULSE RECTIFIER THAT BASED UPON CURRENT INJECTION

The third current injection network to be analyzed in this paper is presented in Fig. 6, and in comparison to the current injection network of Fig. 4 it differs in structure only by the inductor L that is omitted in the network of Fig. 6. In this case, it is not possible to satisfy the resonance constraint (5), thus the current injection network is being designed as a non-resonant, thus $C/2$ capacitors are chosen such that ac component of their voltage is negligible in comparison to the output voltage ripple. In this manner, the current injection networks, as well as the rectifier as a whole, in steady-state operation behave as a resistive circuit, having response that is not frequency dependent. This property is important for the rectifier applications in systems where significant variation of the supply frequency is expected, such as vehicles and autonomous power supply systems. On the other hand, it is important to note that capacitance of the capacitors in the current injection network should be large enough, but exact capacitance is of low relevance; thus, the system sensitivity on this parameter is low. Detailed analysis of the rectifiers that apply current injection network of Fig. 6 can be found in [5] and [7]. In this paper, only the basic performance parameters will be shown, to provide information necessary to perform comparison.

The current injection network shown in Fig. 6 is inspired by the rectifier proposed in [6], where the square-wave current injection was also applied. However, in [6], the current injection is provided applying a current-loaded resistance emulator.

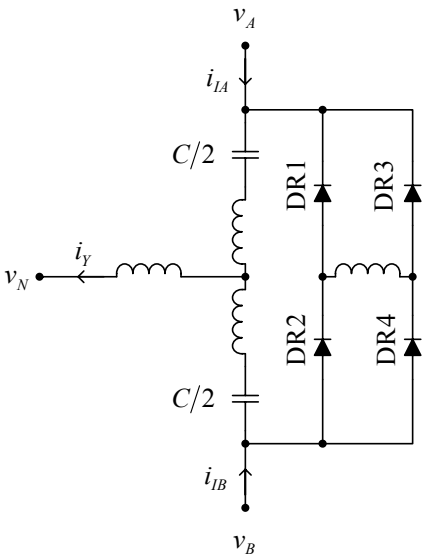

Fig. 6: *Non-resonant current injection network that applies a resistance emulator.*

Applying the same methodology as in the optimization of the transformer turns ratio for the resonant current injection network with resistance emulator, for the circuit of Fig. 6 optimization of the transformer turns ratio is performed in order to minimize the THD of the input currents. Optimization result, presented in detail in [7], and in somewhat less detail in [5]. is that the optimal turns ratio is

$$n_{OPT} = 6 + 4\sqrt{3} \approx 12.93 . \quad (14)$$

The input current waveforms are the same as in the case of a common twelve-pulse rectifier. The waveform of the input current at the first phase is presented in Fig. 7. THD of the current is

$$THD = \frac{1}{6}\sqrt{\left(2+\sqrt{3}\right)\pi^2 - 36} \approx 15.22\% . \quad (15)$$

Increased THD of the input currents is the price paid for reduced influence of the component parameter variations and variations of the supply source frequency. Besides, in the absence of losses, the non-resonant current injection network provides constant output voltage, not dependent on the output current, given by

$$V_{OUT} = \frac{9\sqrt{2} - 3\sqrt{6}}{\pi} V_m \approx 1.71\, V_m . \quad (16)$$

The experimental results, presented in [5] and [7], indicate that the THD values of the input currents in real cases that include losses in the current injection network are significantly lower, around 10%, while the output voltage depends on the output current to some extent, but significantly lower than in the case of the current injection network shown in Fig. 2.

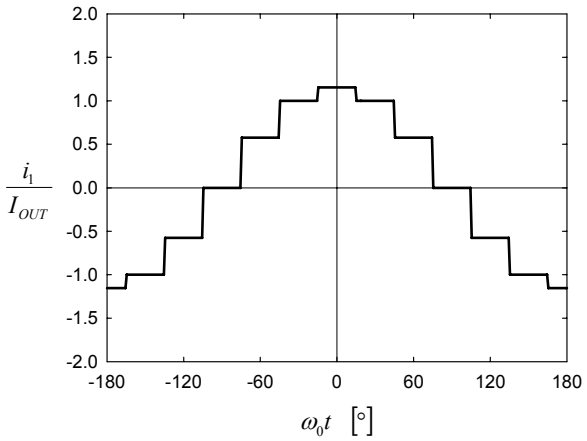

Fig. 7: *Waveform of the input current, non-resonant current injection network with a resistance emulator.*

5. COMPARISON OF THE CURRENT INJECTION NETWORKS

The three current injection network types analyzed here can be compared according to many criteria. All of the three are passive in the sense they do not require controlled switches. The first two of the current injection networks are resonant, with the resonance tuned to the triple of the line frequency. Thus, these two current injection networks are sensitive on variations of component parameters, as well as they are sensitive on frequency variations of the supply source. The second of the current injection networks is more complex than the first one, but provides significantly lower THD of the input currents than the current injection network that does not apply the resistance emulator. Besides, variation of the output voltage is significantly lower, as well as the dependence of the input current THD on the output current, as shown in [1]. The third of the current injection networks is

not resonant and it provides the lowest sensitivity on variations of the component parameters. Also, this current injection network is not sensitive on frequency variations of the supply source. In comparison to the second current injection network, the resonant one with the resistance emulator, the inductor is omitted from the circuit, which simplifies the circuit. Unfortunately, the increase in robustness is paid for by increased THD of the input currents, up to about 15%, the same as in the case of conventional twelve-pulse rectifiers.

Other comparisons of the rectifiers that apply proposed current injection networks, including comparisons of the influence of losses and comparisons of rated power of the components, can be found in [7].

On the basis of presented analyses, possible application areas for the rectifiers that apply proposed current injection networks can be foreseen. The first of the current injection networks is convenient for application in cases when the price is the key decision factor, although in these cases the third of the current injection networks should also be taken into consideration as an alternative solution. The THD of the input current is about 10%, with significant dependence on the output current. Also, in the case of the first current injection network, the dependence of the output voltage on the output current is significant. In cases where the best performance is required, the second current injection network is superior. The THD of the input current is in the range from 3% to 8%, with low variations of the output voltage. Unfortunately, this current injection network is sensitive on variations of component parameters, as well as on variations of the supply source frequency. When the robustness is a key issue, the third of the realizations is a convenient choice in applications that tolerate the input current THD of about 15%. This current injection network results in the rectifier design characterized by low dependence of the input current THD and the output voltage on the output current, requiring circuitry of medium complexity.

6. CONCLUSIONS

In this paper, three current injection networks intended for application in low-harmonic three-phase rectifiers that operate in the discontinuous conduction mode of the main three-phase diode bridge are analyzed. Main properties of these current injection networks are presented, as well as the constraints that have to be satisfied. Information about expected THD values of the input currents and the dc components of the output voltages are provided. Presented current injection networks are compared according to complexity, the THD of the input currents, variations of the output voltage caused by variations of the output current, and according to the sensitivity on the component parameter variations and the variations of the supply source frequency. Guidelines for the choice of a suitable current injection network according to the rectifier specifications and application area are given. Detailed analysis of the presented current injection networks can be found in [1] and [7].

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CONTEMPORARY MOTION CONTROL SYSTEMS

- Invited paper -

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Abstract: *This paper outlines the state of the art and current trends in the field of motion control systems, focusing on the power converter topologies and sensors. Contradictory motion control requirements of reducing the cycle time and increasing accuracy are pointed out and related to mechanical problems, finite resolution of the sensors and the quantization noise. Sample numerical methods for the resolution enhancement and the noise reduction are derived and presented, along with the implementation guidelines and test results. Power converters in motion control systems are accountable for converting the electric energy obtained from the primary source and adjusting the frequency and the amplitude of the output voltages and currents. The output quantities are suited according to the needs of the electric servo motor. At present, electric drives in general absorb two thirds of all the electric energy produced in an industrial country. Recent progress in motion control systems requires new power electronics technologies, solutions and components. The growth of high performance drives depends on the investments in new production sites. Recent trends of replacing production sites to countries where the labour cost is lower calls for a more advanced motion control systems, requiring less maintenance and skilled workers. The elements of motion control systems, and in particular the power electronic units became commodity products, their cost becoming one of the main issues. At the same time, the energy efficiency, a higher peak-to-rated power ratio, the energy quality and the regenerative braking imposed new standards to power converter topologies and solutions. This article outlines the impact of recent trends in motion control systems on the power converter topologies used in electric drives. Both high volume, low performance applications and the cutting edge applications are pointed out, including as well the insight into most recent power electronics products and solutions, offered by leading PE manufacturers.*

Keywords: *Motion Control Systems, Dynamic Braking, Servo Motors*

1. INTRODUCTION

Contemporary motion control systems employ DSP controlled AC drives. The growth of electric drives is determined by the current level of technology. High reliability, long lifetime, relatively low maintenance and short startup times of electric drives are in consort with their ecological compatibility: low emission of pollutants. The quality of electric drives is extended by a high efficiency, low no-load losses, high overload capability, fast dynamic response, the possibility of recuperation, and immediate readiness for the full-featured operation after the drive startup. Electric drives are available in a wide range of rated speeds, torques and power, they allow for a continuous speed regulation, reversal capability, and they easily adapt to different environment conditions such as the explosive atmosphere or clean room requirements. Unlike the IC engines, electric motors provide for a ripple-free, continuous torque and secure a smooth drive operation.

During the past two decades, the evolution of powerful digital microcontrollers allowed for a full-digital control of the electromechanical conversion processes taking place in an electrical drives. The process automation made significant progress in the fifties, thanks to the introduction of numerical control (NC). Although not flexible and fully programmable, NC systems replaced relays and mechanical timers common on the factory floor in the first half of the century. As the first reliable and commercially available microcontrollers were made in the sixties, they were advantageously used for the purpose of a flexible control of electric drives in production machines. As from then, the hydraulic and pneumatic actuators gradually disappear and give space to DC and AC electric motors. Among the first applications of variable speed frequency controlled AC drives were pumps, fans and compressors, where the speed regulation feature eliminated mechanical damping of the fluid flow and reduced the associated power losses and turbulence. For their increased reliability, low maintenance, and better characteristics, the frequency controlled induction motors gradually replaced DC drives in many of their traditional fields of application. Further technological improvements made the frequency controlled AC drives the cheapest actuators ever. Compact digital controllers emulate the functions traditionally implemented in the analog form and allow also the execution of nonlinear and complex functions that could not have been completed by analog circuitry (ANN, nonlinear estimators, spectrum estimation and others). Highly evolved observers of the drive states allow reduction of the number of sensors. The drives with minimum number of sensors and the shaft sensorless drives are more robust and reliable than their sensored counterparts. The lack of sensors and associated cables makes the drive cheaper and the installation simpler and faster. In the development phase are the advanced parallel control structures such as the direct and incremental torque control that make the use of a large numerical throughput to implement a non-cascade control concept thereupon augmenting the response speed and overall drive dynamic performance.

The growth of high performance drives depends on the investments in new production sites. Recent trends of replacing production sites to countries where the labour cost is lower calls for more advanced motion control systems, requiring less maintenance and skilled workers. The elements of motion control systems, and in particular the power electronic units became commodity products, their cost becoming one of the main issues. At the same time, the energy efficiency, a higher peak-to-rated power ratio, the energy quality and the regenerative braking imposed new standards to power converter topologies and solutions.

The article discusses the problems and future trends in each group of electric drives. Particular attention is paid to the motion control algorithms and to the developments in the

power conversion control. Specific influence of an ever increased number crunching capability of modern digital controllers on the drive controller structures is probed deeply. Performance enhancements of semiconductor power switches are outlined and their influence on the drive converter topology and characteristics is briefly analyzed. Finally, the needs and the possibilities are outlined for a digitally controlled drive to assume versatile adaptation and self -commissioning features, reducing in such a way the need for the operators intervention in both the installation and regular operation phases.

2. DESIGN APPROACH

Traditional approach in designing production automata, used during most of the 20th century, included following steps:

- Decision on basic motion needs, based upon the set of desired operations, tools, materials and production technology
- Decision on the transmission technology and couplings
- Preliminary estimates on the tooling and electric actuators
- Design and prototyping of the robot mechanics
- Preliminary testing with provisional electric actuators (in most cases, parallel runs are made with several competitive drive&controls suppliers).
- Detecting the most critical compliance problem, the problems of mismatched motor-load-controls, insufficient bandwidth and precision, and similar).
- Correcting the design, in general, by adding components and modules, and specifying the key elements having a higher grade and cost than planned.
- Considering power electronic devices, the robot performance problems are often resolved by specifying higher peak and RMS currents than planned.

In brief, mechanical, electric and control designs did not overlap. As a consequence, the total weight of the production machine moving parts was higher, increasing the cost, reducing the energy efficiency and impairing the overall performance. Due to reasons well known, contemporary production machines are expected to have a competitive cost, and to achieve as short as possible cycle time. The later implies an elevated bandwidth and precision, bringing up the issue of transmission elements to a critical level. In many cases, the usage of linear motors is a must. All of the performance criteria listed is highly dependent on the total weight of the moving parts. Therefore, there is a pressing need to reduce the weight of the moving parts, and this is possible through the contemporaneous design, organized through a synergic link between mechanic, electric and information technologies.

The structure of an intelligent motion control system applied in industry includes:

- Communication link of the production cell with the production site host computer.
- Hardware and software resources for the high-level interpretation and optimization.
- Diagnostic and supervision on the technology level.
- Diagnostic, protection and supervision on the motion control level.
- Coordination, profiling, cinematic calculations, interpolation.
- Single-axis micro-interpolation, torque, speed and position control.

Traditional design approach is illustrated in Fig. 1.

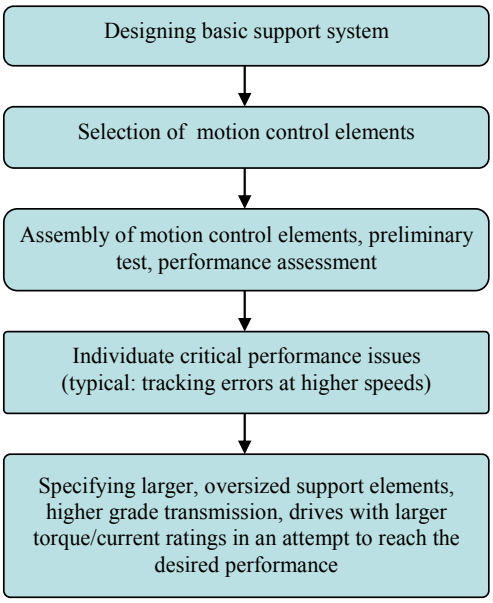

Fig. 1: *Traditional design approach.*

As a consequence, the peak and RMS current ratings of servo motors is generally above the essential minimum. This in turn leads to an increased cost and size of power converter active components. At the same time, the power conversion losses are increased, and the problem of thermal management adds to the system size and cost. In Fig. 2, recently adopted design procedure is given, organized through a synergic link between mechanic, electric and information technologies.

Concurrent design of electrical, mechanical and control subsystems requires an extensive use of computer simulations. In particular, mechanical supports, transmission and transducers have to be simulated by using real-time finite-element packages, taking into account the form and the grade of materials. At the same time, standard transducers and transmission elements, normally obtained from third parties, have to be accompanied with the necessary models, facilitating such simulation. In a way, the procedure of simulating the dynamic behavior of the prototype robot resembles simulation of electric circuits in Pspice, with Pspice models of individual components being supplied from the supplier in a standardized form.

Real –time simulation of industrial robots is not fully automated yet, and it requires a great deal of on-site programming, relating to the current needs to relate, interface and integrate the available software packages, focused on narrower application fields such as the electrical (power electronics, motors), mechanical and control domains. On an average, proper simulation allows an accurate performance prediction (Comau). In subsequent drive selection, a saving of up to 50% is possible in terms of the peak/RMS current and torque ratings.

Further reduction of the drive ratings is obtained by scrutinizing the load torque prediction. The available computer tools allow for a more precise calculation of several

load torque components for each individual motor, based on the motion profile, the ambient conditions and the temperature range, the cycle times, production processes, the quality of materials involved and characteristics of the MCS elements used. It is possible to identify and sum the following torque components:

- Load torque related to gravity,
- Viscous friction,
- Resistive torques related to tools and work materials, including cutting resistance, drilling, punching, and similar,
- Static/dry friction forces and torques,
- Torque disturbances coming from transmission and other elements,
- Inter-axis coupling related to the MCS dynamics,
- Inertial torques (acceleration, deceleration).

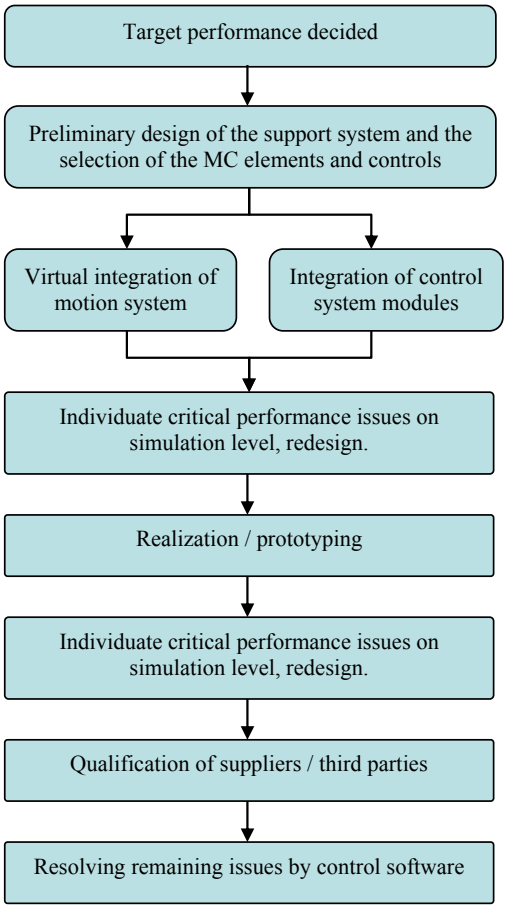

Fig. 2: *Contemporary design of the MCS.*

Finally, in a cost optimized design, the rated torques and currents of servo motors involved are reduced to a necessary minimum. On the other hand, the needs to increase the productivity and reduce the cycle times lead to elevated acceleration torques. As a consequence, the peak torque/current values tend to increase, while preserving or reducing the rated RMS values. Therefore, the power converters are required to withstand higher short-term overloads, while their passive components and cooling systems can be designed to much lower average values. Considering the cost and weight structure of power converters, the power semiconductors and sensors are going to prevail while the passive components tend to shrink. When specifying thermal management elements and heatsinks, their thermal capacity becomes more important than the thermal resistance.

3. LIFETIME REQUIREMENTS

Reduced availability of trained servicemen at oversees production sites requires an extended operating life of all the power electronics components and systems. Besides, considering the use and practice related to spare parts, the average storage life has to be extended as well. Major issue in this regard is related to power electrolytic capacitors. Their lifetime is limited essentially by the process of loosing the electrolyte and drying out. Their aging is highly accelerated at elevated temperatures and an increased RMS current ratings. While other passive and active components tend to shrink, the electrolytic capacitors increase their relative part in the converters size and cost. A strenuous effort is made to achieve power converter designs free from electrolytic capacitors, relying on next generation metalized polypropylene and other capacitor technologies.

Electrolytic capacitors do limit the storage life as well. In cases where a new part has never been connected to power for years, and used to be stored instead, it would have to be re-formed before use. Otherwise, in cases when the unit comprising such a capacitor is directly connected to the rated voltage, the electrolytic capacitor would exhibit a very low resistance (i.e. a short), causing a fatal failure. An effort is made to prolong the storage life of power capacitors (Panasonic, Nichicon).

In some cases, it is necessary to provide a backup power supply for auxiliary circuits, capable of keeping the control circuitry and processors active during the powerdown intervals. Lead-acid or nickel-cadmium batteries are frequently used to suit such needs. Whenever an extended lifetime is needed, super-capacitors are used. Still immature in technology, the super-capacitors are available for low rated voltages only (2-3V).

4. DYNAMIC BRAKING

Multiple servo drives have their acceleration/ deceleration phases spaced in time, according to the multiaxis motion profile. The intermediate circuit of relevant power converters (i.e. the DC-bus) are in most cases paralleled, to allow for the exchange of the energy between the accelerating and braking motors. Though, as the acceleration/braking phases may not overlap, the system occasionally has an excess of energy in the intermediate circuit. Traditionally, Dynamic Braking Resistor (DBR) circuit is used, equipped with an active power switch. Whenever an excessive voltage in the intermediate circuit is detected, the active power switch (T7 in Fig. 3) is turned on and the energy is dissipated in resistor R, eventually turning into heat.

In some applications, thermal management is critical, and the additional heat cannot be handled. In other cases, safety issues prevent the use of a braking resistor. Namely, due to elevated surface temperatures of the resistors, dust deposits in textile and similar industries can be set to fire. Therefore, it is of interest to manufacture and deploy regenerative front-end converters (see Fig. 4).

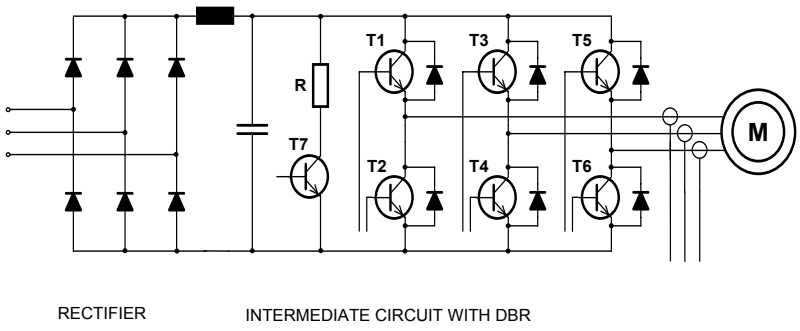

Fig. 3: *Dynamic braking resistor (R) and an active power switch (T7) in DC-link circuit.*

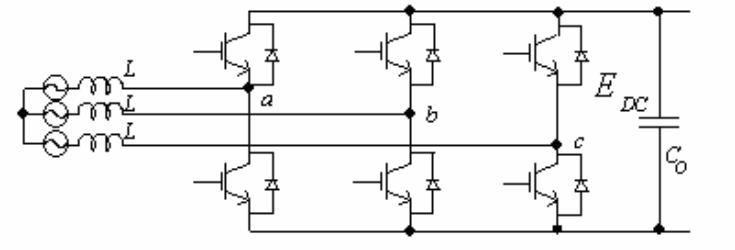

Fig. 4: *Regenerative front-end converter.*

5. BROWN OUT AND POWER DOWN PROTECTION

Complex mechanical structure of a production machine can be damaged in case of collisions or the lack of control. In case of an interruption of the main power supply, the accelerated masses may proceed moving by inertia, and eventually crash, damaging the tools, moulds, or make other damage. As a precaution, the servo motors are frequently equipped with brakes. The motor brakes can be used as a safety measure. Though, their braking action is not controllable, and they cannot make the system stop along a predefined trajectory. Rather abrupt, the use of mechanical brakes should be avoided whenever possible.

When the powerdown event happens with the system masses running, their kinetic energy can be used as the energy source. Controlled braking is possible with the servo motors operating as generators, and with the kinetic energy being fed back into the intermediate circuit through the power converter / inverter. As long as the control section is properly supplied, the system can be driven down to a full stop, running along any predefined trajectory, hence avoiding any collision or other mechanical threat. In order to provide continued auxiliary power supply, the SMPS module should have the possibility to use the DC-bus (intermediate) voltage in all cases when the mains voltage is too low.

6. TEXTILE INDUSTRY

Textile machines generally feed or use hundreds of threads (500-1000). Traditional textile machines make use of a single controllable electric drive, with hundreds of thread-feeders coupled to the main drive by means of belts or frictional couplings. This prevented tension control of individual threads. Nowadays, there is a pressing need to use low power (50-100W) controlled induction motor drives for each of the thread-feeders. With a total power of 50 – 100 kW, textile machines power management require novel power electronics solutions. Due to an extraordinary high number of individual drives, the textile machine require low cost, robust and reliable electric drives with slow, but reliable communication channels. Having the cost reduction as the primary goal, significant research resources are assigned to development of simple converter topologies, new types of electric motors and algorithms for the sensorless speed control.

Among other requirements, electric drives in textile machines are expected to be environmentally friendly; low thermal, acoustic and electromagnetic emissions are forced by government regulations and international standards. The level of the electromagnetic interference strongly depends on the power section layout and might be improved by the introduction of newly developed power switches with spatially distributed lifetime control (CAL). At the same time, the cost reduction of the power switches would give a strong incentive to a more frequent use of electronic controlled drives in textile machine applications.

Power semiconductors are used within the drive converter for accurate control of the energy flow between the power source (i.e. the mains) and the motor. They have extremely short response times and low dissipation. The dramatic developments in IC technology, particularly during the last ten years, have made possible the design of modern, self-protected components, with simple, “low loss” drive characteristics, wide dynamic control range, switching power levels up to the megawatt range, and a direct interface to microelectronic systems.

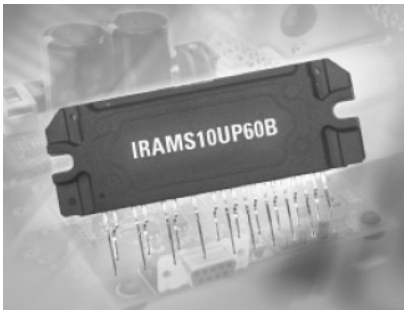

Fig. 5: *The Intelligent Power Module with integrated power devices and control electronics. IRAMS device interfaces directly to 3.3V and 5V processors.*

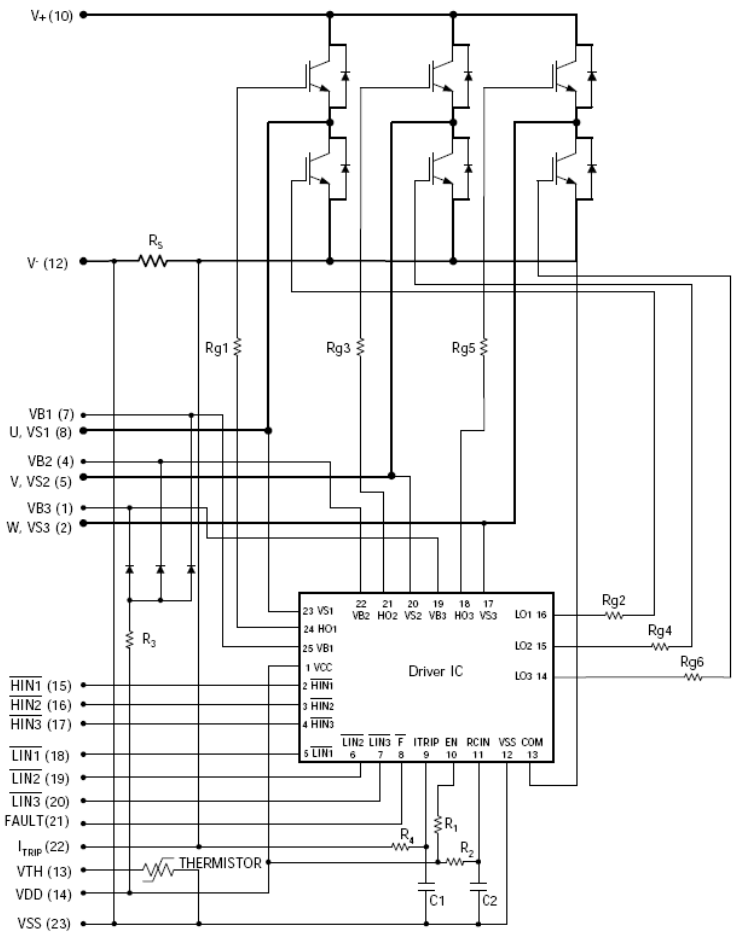

Fig. 6: *Internal schematics of IRAMS Intelligent Power Module.*

In Figs. 5 and 6, IRAMS intelligent power module is presented. It houses almost all of the power electronics and control electronics required to supply and control an induction motor. Device is made by IR, and it interfaces directly to most DSP and RISC controllers. It is of interest to compare the component cost of an inverter made with the IPM and the cost of the equivalent inverter build by using traditional components. The rated power of 1HP was taken as the design example. The intelligent 3-phase module comprises 6 IGBT power switches with associated power diodes, the internal gate drivers and the thermistor. Using the data of Table I, one calculates the total component price as equal to USD 15.095. Traditional bridge converter requires six IGBTs, six fast diodes, one thermistor and three IGBT drivers (one per leg). From Table I the total component cost is USD 14.6313. The comparison shows that the converter with the IPM is, in terms of the component cost, insignificantly more expensive (USD 0.4637 or 3.17%). However, it is obvious that the reduction in the manufacturing cost is more than likely to offset this component price difference. Discrete design requires individual handling, assembly, cooling, fixing and soldering for each of the semiconductor power switches.

Commonly adopted way of supplying 500-1000 inverters within a textile machine is the use of a 3-phase transformer with 3x400V 50Hz delta-connected primary winding, and with star-connected secondary winding having 3 x 220V 50 Hz between the terminals. The inverters are having topology given in Fig. 7. Being single-phase load, the inverters are wired to 3x220V 50Hz supply alternatively, in an attempt to equalize average loading of individual phases

Table I - Component prices for 1hp inverter (reference: www.Digikey.com).

Description	Code	Quantity	Unit price (USD)
3-phase IGBT VSI 6-pack module; integrated drivers & thermistor	IRAMS06UP60A-ND	1,000	10.625
IGBT with anti-parallel diode	IRG4BC10UD	10,000	1.2
Thermistor	KTY135, SOT-23	1,000	0.417
IGBT (no diode)	IRG4BC10U, IRG4BC10U-ND	10,000	0.98305
Fast diode	RS3JB-13	3,000	0.351
Driver, one IGBT pair	IR210STR	2,500	2.07

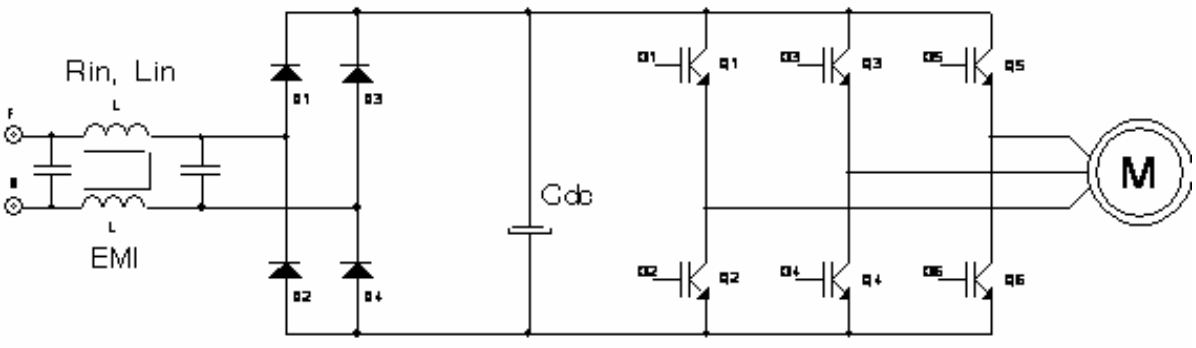

Fig. 7: *Single-phase supplied inverter with the 3-phase output.*

With a diode rectifier at the front end, the converter in Fig. 7 draws a non-sinusoidal, distorted current from the 50Hz mains. The input current waveform is given in Fig. 8. Considering a low rated power of the drive (50-100W in textile machines), the line current distortion caused by a single inverter is not significant. The problem arises from the fact that there are 500-1000 units within each textile machine, having a total rated power of roughly 100 kVA. At this point, low frequency harmonics produced by a passive frond-end converter cannot be tolerated. Harmonic limits for Class A and Class D equipment, according to EN 61000-3-2 is given in Fig. 9. These cannot be met with a passive front-end and P_{nom}>1 HP. Therefore, the power converters such as the one in Fig. 7 should be equipped with active power factor corrector.

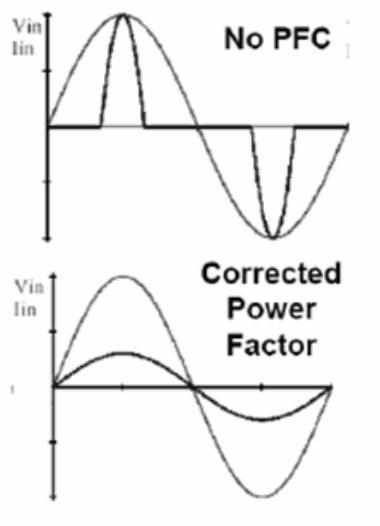

Fig. 8: *Power factor correction.*

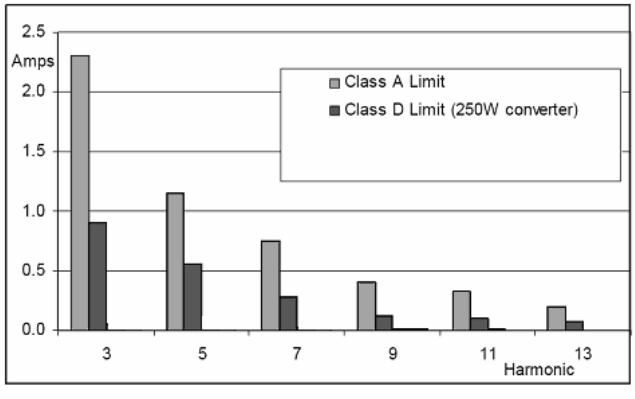

Fig. 9: *Harmonic limits for Class A and Class D equipment.*

In low cost, textile-application induction motor drives, the current sensing becomes a cost sensitive issue. Traditional Hall-effect current sensors, used in high performance drives are too bulky and too costly for a 50W-100W converter that should stay within the cost boundaries of 20-30 EUR. In Fig. 10, the usage of PCB-mount magnetic resistive bridge is illustrated. The stator current flows through the PCB traces below the bridge. Magnetic field caused by the stator current circulation causes a variation of the resistance within the bridge. Subsequently, desired analog signal, proportional to the stator current is derived. Allegro Microsystems manufactured first commercial PCB-mount current sensor for cost-sensitive applications (Fig. 11). It is an open-loop Hall-effect device with the performance quite compatible with the requirements imposed by 50-100W textile drives.

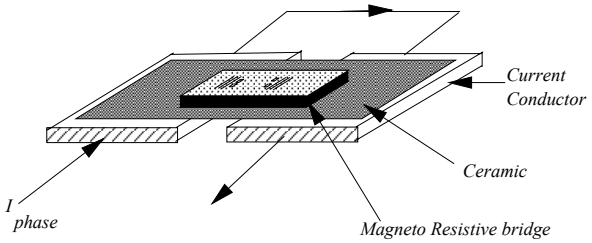

Fig. 10: *Usage of mageto-resistive bridge in current sensing.*

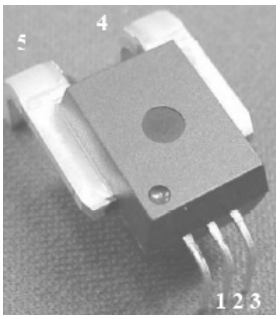

Fig. 11: *Allegro Microsystem ACS750 current sensor for PCB mounting.*

7. LARGE POWER

Large power AC drives are found in rolling mills, petroleum industry, water supply and many other applications where the rated power exceeds 300 kW and the nominal stator voltage falling into the medium voltage range (2300, 4160 or 6600 V). The main problem in this class of electric drives is the design of controlled three phase variable frequency source in the megawatt range. Until recently, the variable frequency, medium voltage drives were not available due to the absence of high

voltage semiconductor power switches. The need for the economic use of energy, miniaturization of electrical systems, and reactive power compensation have been the motives for the revolutionary development of high voltage, high current power semiconductors. For their high power rating, Gate turn off thyristors (GTO) are considered the main switching device for the construction of multi-level high power three phase inverters. The power losses occurring in the GTO at turnoff limit the GTO's normal operating voltage to the range from 30 to 40% of the breakdown voltage, thus limiting the dc-link voltage of a conventional GTO inverter to 1500-2500 V. High-power inverters with dc-link voltage up to 4000 V and existing GTO's cannot be made with conventional six-switch topology. Several converter configurations for the realization of a large capacity inverter with more than 4000 V dc-link voltage are possible. One of them is the six-switch configuration with each of the switching elements being made out of several series connected GTO's. However, the direct series connection method of GTO's has the problem of blocking voltage unbalance during turn-off transient, due to the different turn-off characteristics of each device. Whenever additional equipment is used to overcome this problem, the overall system becomes more complex and expensive. Besides the circuit complexity, a limited switching frequency of GTO's causes large harmonic components of the output voltage and current. Split DC-link voltage three-level converter topologies configurations are being developed for the large capacity inverters, capable of solving the above mentioned problems. Appreciable research effort is devoted to switching rules for a multilevel inverter capable of reducing the commutation stress while maintaining at the same time an acceptable ripple amplitude and the spectral content of the output current.

8. LINEAR ELECTRIC SERVO MOTORS

The power converters for linear AC drives do not differ in topology with respect to their counterparts supplying rotary servo actuators. Though, the reactive power of linear AC motors is higher, and their N/A ratio is less favorable when compared to conventional servo motors.

Most of the operations of an automated production machine involve linear translation of machine parts, work pieces and tools. On the other hand, common electric motors are rotary electromechanical converters producing the torque at the output shaft. Transmission mechanisms such as the rack and pinion, ball screw and gear systems convert the rotary into linear motion. Dry friction, backlash, elastic coupling and the torsional resonance intrinsic to all the rotary – to – linear transducers severely limit the servo loop bandwidth.

Relatively large rotational masses constrain the peak acceleration of the system. On the other hand, large equivalent inertia filters out the torque ripple and the quantization excited +/- 1 LSB torque chatter, alleviating in such a way the tracking error. Imperfection of the transmission mechanism may be eliminated by the application of direct drive concept with linear electric motors. As the tolls are coupled directly to the motor moving parts, the problems of mechanical resonance exist no more. The absence of rotational masses results in a much larger peak acceleration of the overall system, while the ratio between the peak driving force and the friction increases several time when compared to a servo axis with a rotational actuator.

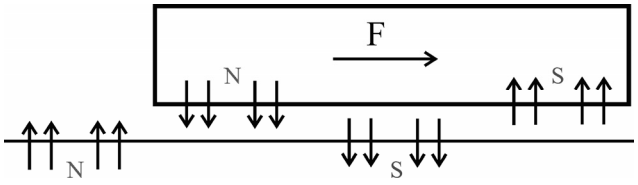

Fig. 12: *Linear electrical actuator – principles of operation.*

Contemporary linear motors exhibit the top speed of 3-5 m/s and offer the positioning accuracy down to 1 □m. Exceptionally low inertia stresses the torque ripple and the chatter related problems. Due to the motor imperfection and the finite resolution of the sensors, the driving force exhibits (the same way as the driving torque of a rotational servo motor) high frequency oscillations – the chatter – with an amplitude of 1-3 LSB. The smaller the inertia, the larger the speed and position fluctuations caused by the jitter in the driving force. Dissipativity based approaches to the servo loop synthesis permit significant reduction of the chattering problems, but do not solve completely the torque/force ripple problems. For this reason, the force ripple minimization is one of the main design requirements for linear electric servo actuators.

Modern linear motors are mostly asynchronous or synchronous permanent magnet motors. They have magnetic, hydrostatic or the air bearings. The stiffness coefficient of linear motors (200 N/m) is much better than the stiffness of the fluid power actuators (50 N/m). It is possible to move the weights above 50 kg and attain the driving forces up to 2000 N. Low equivalent inertia of motion control systems employing linear motors results in a speed loop bandwidth of 130-200 Hz and the peak acceleration well above 100 m/s^2.

When designing the power converters for linear AC drives, similar design rules apply, and the only difference is an elevated reactive power and higher stator currents.

9. CONCLUSION

Power converters in motion control systems are accountable for converting the electric energy obtained from the primary source and adjusting the frequency and the amplitude of the output voltages and currents. The output quantities are suited according to the needs of the electric servo motor. The elements of motion control systems, and in particular the power electronic units became commodity products, their cost becoming one of the main issues. At the same time, the energy efficiency, a higher peak-to-rated power ratio, the energy quality and the regenerative braking imposed new standards to power converter topologies and solutions.

This article outlines the impact of recent trends in motion control systems on the power converter topologies used in electric drives. Both high volume, low performance applications and the cutting edge applications are pointed out, including as well the insight into most recent power electronics products and solutions, offered by leading PE manufacturers. It is found that the recent trends in motion control system and introduction of low power, electronic controlled drives in textile machines and similar applications deeply affect the topology of power electronic devices and create the need for new PE solutions. New drive applications require the drive power converters with a higher peak-to-

RMS ratio, much longer life time and storage time, and built-in safety features such as the anti-free-wheeling. Power factor correction and regenerative braking becomes common requirement, while the proper thermal management becomes main competitive feature. Although with a mature technology and the basic problems already solved, power converters for electrical drives are still in the intense development phase. Numerous control problems and the problems of energy conversion yet need to be solved. The said problems will attract the attention of many young engineers world-wide at Universities, research laboratories and companies involved in controlled electrical drives development and production.

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FLYBACK CONVERTER - PRACTICAL REALISATION IN THE TUITION PURPOSE

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Abstract: *The purpose of this project was the analysis, the application of a chosen integrated solution for controller and the realization of the Flyback converter. The paper gives all needed terms, the basic algorithm of the components sizing and the characteristic diagrams. The software tools are shown, which are used to affirm mathematical estimate. Finally, the measures were performed and the results that were obtained are represented and analysed.*

Keywords: *Flyback Converter, Feedback Coupling, Primary Clamp*

1. INTRODUCTION

Flyback converters have a remarkably low number of components compared to other switch mode power supplies (SMPSs) and they also have the advantage that several isolated output voltages can be regulated by one control circuit. Flyback converters are used in most of mains supplied electronic devices with low power consumption. There are many different types of integrated solutions for realization of Flyback converter. One of them, based on TopSwitch integrated circuit, with high level of integration irrespective of the number of outputs, was practically realised.

The paper is organised as follows. In the *second chapter* principles of operation of the Flyback converter are described with basic expressions for the dimensioning of the components. *Third chapter* shows realisation of the converter based on TOPSwitch integrated circuit and possible options for configuration of feedback coupling. Simplified design flow of Flyback converter is given in the *fourth chapter*. In the *fifth chapter,* the issues concerning primary clamp circuit are given attention. In the *sixth chapter* the results of the measurements obtained from the developed converter are presented and the conclusion is given in the *seventh chapter.*

2. FLYBACK CONVERTER

Electrical circuit of the Flyback converter is shown in Figure 1 and Figure 2 show the voltages and currents in the circuit. There V_{in} is the input voltage which is connected to primary side of transformer through N-channel power mosfet. When mosfet is on, during t_1, transformer primary voltage *V1* is equal to the input voltage V_{in} which causes the increase of transformer primary current I_P. Secondary current I_2 equals zero, as the rectified diode is blocked. The energy is accumulated in the primary inductance. Then after switching off the mosfet at T-t_1 it is transformed onto the output capacitance. The relation between the primary ripple current I_R and the maximum primary current I_P, defines the factor of waveform K_{RP}, which has the value between 0 and 1 in continuous mode, and equals 1 in discontinuous mode, as shown in Figure 3. Besides electrical isolation, the transformer enables adjustment of the output voltage level. The flyback's transformer must have an air gap in order to accumulate the energy.

The converter has only one magnetic component - transformer, and a small number of additional elements. Thanks to that, the device is less expensive than other SMPS topologies. The converter uses this advantage at powers below 100W and for output currents below 10A. Since the transformer always operates just in the first quadrant of B-H its characteristic, for output power above 100W it becomes inefficient comparing to other topologies (eg. *push-pull*, *bridge* etc). Flyback converter can be realized with multiple outputs (Fig. 1), by adding extra secondary windings, where a good cross regulation can be expected.

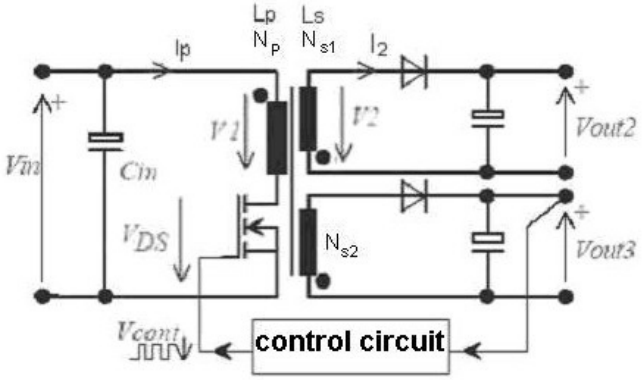

Fig. 1: *Flyback converter for several output voltages.*

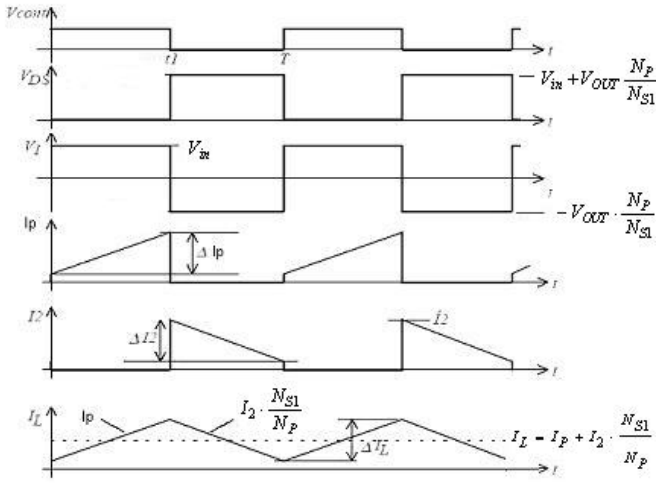

Fig. 2: *Voltages and currents at the Flyback converter.*

From figure 2 expressions for voltage transmission ratio, drain-source voltage and maximum needed peak inverse voltage rectifier diode can be obtained:

$$V_{OUTx} = V_{in} \times \frac{N_{Sx}}{N_P} \times \frac{t_1}{T - t_1} \tag{1}$$

$$V_{DS} = V_{in} + V_{OUTx} \times \frac{N_P}{N_{Sx}} \tag{2}$$

$$PIV_{Sx} = V_{Sx} + (V_{MAX} \times \frac{N_{Sx}}{N_P}) \tag{3}$$

where PIV_{Sx} is maximum peak inverse voltage, V_{Sx} is one of the output voltages, N_{Sx} is the number of secondary turns, N_P is the number of primary turns and V_{MAX} is maximum DC input voltage (typically 375VDC).

The choice of rectifier diodes hugely determines the total level of converter efficiency and quality of variable's waveforms in the circuit. Therefore it is recommended to use ultra fast Schottkey diodes.

Maximum of primary current is calculated as:

$$I_P = \frac{I_{AVG}}{\left(1 - \frac{K_{RP}}{2}\right) \times \frac{t_{1MAX}}{T}} \quad (4)$$

where I_{AVG} stands for average primary current of diode bridge, which can be calculated from the necessary output power.

Primary RMS current I_{RMS} can be expressed through maximum primary current and K_{RP} factor:

$$I_{RMS} = I_P \times \sqrt{\frac{t_{1MAX}}{T} \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1\right)} \quad (5)$$

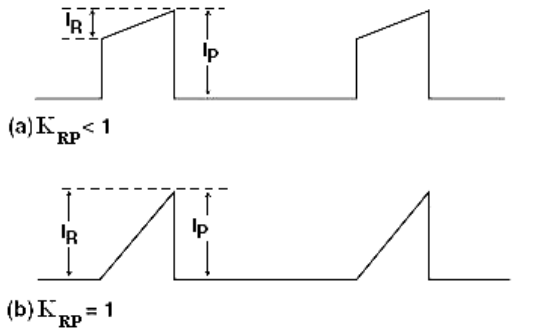

Fig. 3: *Relationship of primary ripple current I_R and primary peak current I_P.*

3. FLYBACK CONVERTER REALISED WITH „*TOP SWITCH*" CIRCUIT

TOPSwitch circuit is integrated component which is specially designed to operate Flyback converters. It is based on voltage mode control. TOPSwitch integrates the high voltage power mosfet, PWM control, fault protection and other control circuitry onto a single CMOS chip. Many functions are integrated to reduce system cost and improve design flexibility, performance and energy efficiency: soft start, 132kHz switching frequency (automatically reduced at light load), frequency jittering for lower EMI, wider DC_{MAX}, hysteric thermal shutdown. In the process of constructing of the device, the control circuit is unchangeable, irrespective off output parameters. The choice of feedback coupling can influence achieved stability of output voltages with load variation. TOPSwitch uses the bias winding of the transformer to derive information about the regulated secondary output. There are three topologies of feedback circuits which are shown in Figs. 5, 6 and 7. The figures show the main output winding $N_{S1,}$ the voltage of which is directly regulated, and secondary bias winding N_{SB}. Additional secondary windings are not shown. They are usually not connected to the feedback circuit [2].

Fig. 5 represents basic feedback topology. Diode and capacitor constitute rectifier circuit which provides bias voltage V_B. Control circuit adjusts period of on-time t_1, to bring V_B to the level of *5,7V*. Therefore, transmission ratio between one output secondary winding and bias winding is determined by:

$$V_{OUTx} = \frac{N_{Sx}}{N_{SB}} \cdot 5{,}7V \; . \quad (7)$$

In the second topology of feedback circuit, shown in Fig. 6, bias voltage secures polarization of the optocoupler. Optocoupler is used for transmitting current level which is in proportion with regulated output voltage, and is determined by Zener diode voltage and series resistance R_B. Control input current I_C is now:

$$I_C = \frac{V_{OUTx} - V_{OC} - V_{ZD}}{R_B} \cdot CTR \quad (8)$$

where V_{OC} is forward voltage of the optocoupler's LED *(typically 1.2V)*, V_{ZD} is Zener diode voltage and *CTR* is current transfer ratio factor. Duty cycle *D* is defined as the ratio of on-time t_1 to switching period *T, (D=t_1/T)*. In stationary state, *D* can have values from *0,02* to *0,7*. For chosen operating point of *D* (eg. *D=0,35*), from transmission characteristic of the TopSwitch control circuit, shown in Fig. 4, the corresponding control input current value I_C in stationary condition can be read and then needed value for R_B calculated from (8) [3].

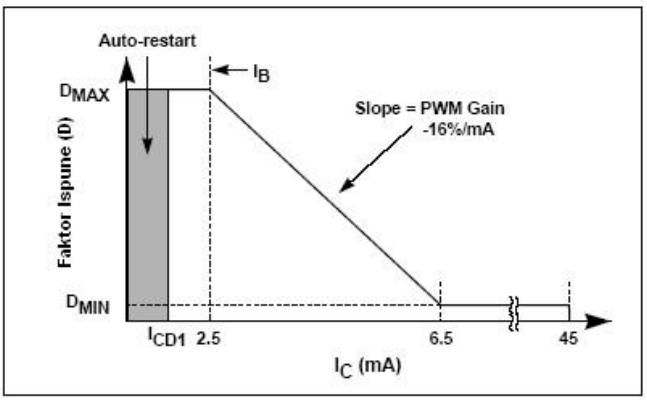

Fig. 4: *Relationship of Duty cycle to CONTROL Pin Current.*

In the third topology, with shunt regulator *TL431,* output voltage is determinate by resistance R_1 which is connected to control input of *TL431* (9). Namely, the converter circuit behaves as a part of feedback coupling of the regulator, so that operating point of optocoupler is dynamically adjusted.

$$V_{OUTx} = \frac{2{,}5V \cdot R_1}{10k} + 2{,}5V \quad (9)$$

As earlier mentioned, with selection of feedback coupling it is possible to influence the stability of output voltages with load variation. Table 1 [1] shows typical values of the deviation of regulated (main) output voltage of the converter and the values of other output voltages which are indirectly regulated. Topology of *TL437* shunt regulator, evidently provides the maximum stability of the main output voltage as well as other output voltages, that is, the best cross regulation. In the subsequent chapters of the paper, the given data will be compared with the obtained measurement results.

Table 1 - Output specification based on feedback coupling

Feedback Circuit	Output Regulation	
	Output (main)	*Other outputs*
Basic	± 10%	More than ± 10%
Opto/Zener	± 5%	Less than ± 10%
Opto/TL431	± 5%	More than ± 10%

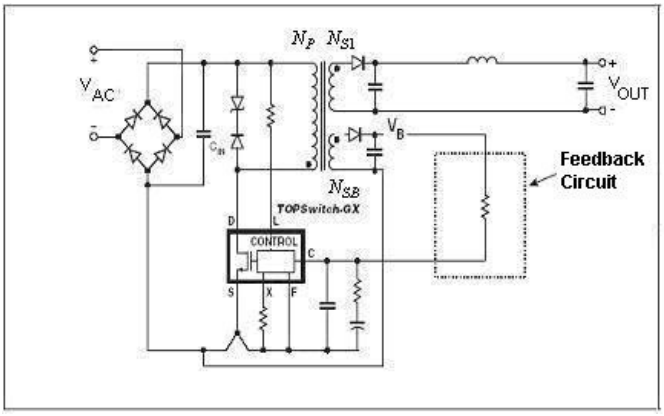

Fig. 5: *Basic Feedback Circuit.*

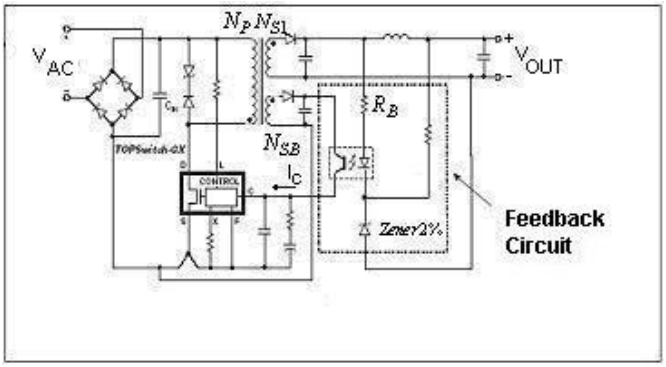

Fig. 6: *Opto/Zener Feedback Circuit.*

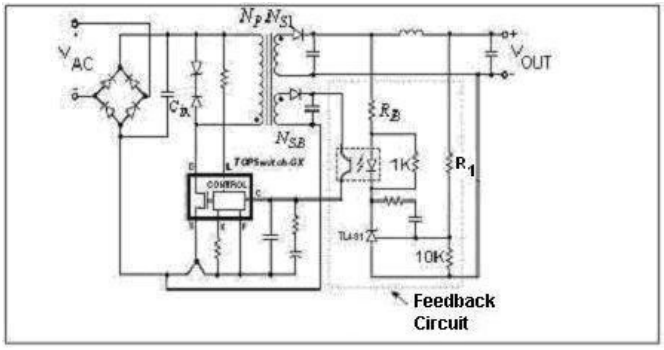

Fig. 7: *Opto/TL431 Feedback Circuit.*

4. CALCULATION OF THE CONVERTER PARAMETERS

Designing of the isolated DC/DC converter is an iterative process with many variables, which can be represented as design flow chart, as shown in Fig. 8. The first step is to determine the input requirements, like the value of the input voltage, output voltages, the load at each output, converter operating mode defined by current waveform factor K_{RP}, and the feedback circuit topology.

Transformer accumulates energy from the source, while the switch is on, in it's inductance L_P which determines shape of current I_P and K_{RP} (10). Average value of I_P, $I_{P(AV)}$, can be determined based on the data from output power P_O, and K_{RP} is input parameter of algorithm.

$$L_P = \frac{10^6 \times P_O}{I_{P(AV)}^2 \times K_{RP} \times \left(1 - \frac{K_{RP}}{2}\right) \times f_S}. \quad (10)$$

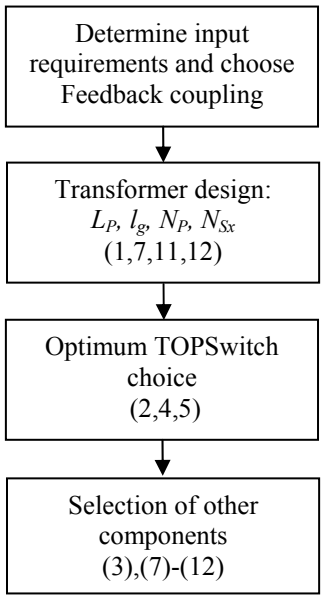

Fig. 8: *Flyback converter - Design Flow Chart.*

The number of windings on the transformer primary can be determined from expression (11), where B_{MAX} is the maximum value of the magnetic core inductance B, which for the ferrite materials equals *0,3T*, and A_e is core effective cross sectional area.

$$N_P = \frac{L_P \cdot I_P}{B_{MAX} \cdot A_e} \quad (11)$$

Based on the value of duty cycle in nominal operating point, the on-state time t_1 of the mosfet can be determined and the number of windings of each secondary N_{Sx} can be calculated from (1). Gap length l_g can be determined from (12), where A_L is ungapped core effective inductance.

$$l_g = 4\pi \times 10^{-7} \times A_e \times \left(\frac{N_P^2}{L_P} - \frac{1}{A_L}\right) \quad (12)$$

Choice of the TOPSwitch component depends on the mosfet's maximum voltage level (2), and the primary current (4) and (5). Finally, the rectifier diodes should be chosen, where the basic parameter is peak inverse voltage *PIV*, from (3), and feedback couple elements, which depend on the chosen topology (7)-(12).

Power Integrations, the TOPSwitch manufacturer, recommends the use of PIExpert which implements the design methodology and also includes a knowledge base and optimisation feature for making key design choices (Fig. 9).

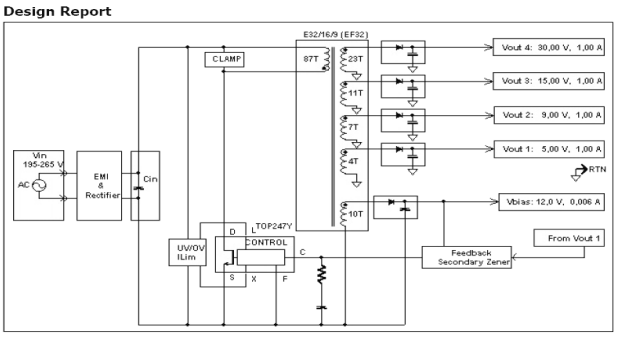

Fig. 9: *PIExpert-Design report.*

5. PRIMARY CLAMP

A Zener primary clamp, used to limit the voltage spike caused by leakage inductance, is assumed to provide a constant clamping level of 200 V. Practical implementation may require a parallel RC network to limit Zener dissipation.

One of the solutions as can been seen in Fig. 10, represents the combination of *RCD* clamp and Zener diode ZD_{CL}. The value of resistance R_{CL} and capacity C_{CL} are dictated by switching frequency where it is advisable to follow recommendations of the manufacturer [4].

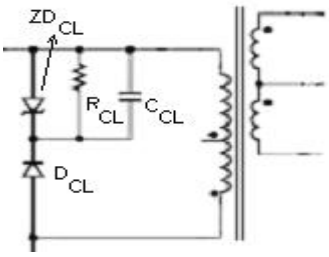

Fig. 10: *Primary Clamp Circuit*

On the other hand, selection of the Zener diode should be carefully adjusted to voltage levels in the circuit. Figure 11 shows the example of selection Zener diode V_{ZD} for input voltage maximum level of $V_{inMAX}=375V$ and output voltage which is translated on primary of transformer $(N_P \cdot V_{OUTx})/N_{Sx}=135V$. It is necessary to include the increase of the voltage owing to diode's temperature rise V_{ZDMAX}, and then diode recovery voltage, so that the appropriate margin is assured below breakdown voltage BV_{DSS}.

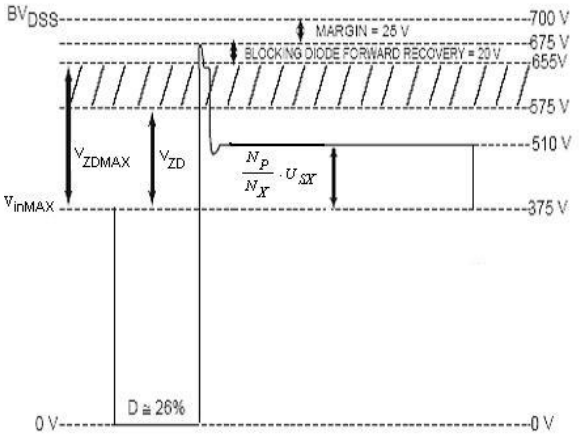

Fig. 11: Reflected Voltage V_{OR} and Clamp Zener Voltage V_{CLO}.

6. TEST RESULTS

In order to verify the design procedure, the prototype with TOPSwitch integrated circuit was realized, as shown in Fig. 12. The device is supplied through rectified network voltage, and at the output has four voltage levels: V_{OUT1}=5V, V_{OUT2}=9V, V_{OUT3}=15V i V_{OUT4}=30V, with maximum load on each output of 1A. The main output is V_{OUT1}, from which feedback coupling is taken. By using the algorithm for calculation of circuit parameters the selected TOPSwitch was *247Y* and the transformer core *E32/16/9(EF32)* [5].

The test results for output voltage stability are presented in Table 2. The data with different feedback coupling topologies are measured and corresponding results are given. Thereby, in the first experiment, load on output V_{OUT1} is changed from minimum (*0,4A*) to maximum value (*1A*), while other outputs are minimum loaded (*0,4A*). In the second experiment, V_{OUT1} is maximum loaded 1A, load on V_{OUT2} is changed, and V_{OUT3} and V_{OUT4} bare minimum load. Then, in the third experiment, V_{OUT1} and V_{OUT2} have maximum load, load on V_{OUT3} is changed, and V_{OUT4} was minimum loaded. Finally, V_{OUT1}, V_{OUT2} and V_{OUT3} bare maximum load and V_{OUT4} is changed until maximum value. The measured results show typical values of output voltage variation due to load changes. It is also shown that the topology with Zener diode has better stability at lover load values, while usage of *TL431* gives better cross regulation for higher load values.

Table 2 - Output voltage stability for load variation

	load variation on V_{OUT1}(5V)	
Type	*OPTO/ZENER*	*OPTO/TL431*
V_{OUT1}	0,8%	0,2%
V_{OUT2}	0,1%	0,1%
V_{OUT3}	0,1%	1,34%
V_{OUT4}	0,33%	0,67%
	load variation on V_{OUT2}(9V)	
Type	*OPTO/ZENER*	*OPTO/TL431*
V_{OUT1}	0,15%	0,2%
V_{OUT2}	1,12%	2,22%
V_{OUT3}	0,2%	0,2%
V_{OUT4}	0,3%	0,3%
	load variation V_{OUT3}(15V)	
Type	*OPTO/ZENER*	*OPTO/TL431*
V_{OUT1}	0,3%	0,35%
V_{OUT2}	0,3%	0,4%
V_{OUT3}	0,66%	1,33%
V_{OUT4}	0,7%	0,33%
	load variation on V_{OUT4}(30V)	
Type	*OPTO/ZENER*	*OPTO/TL431*
V_{OUT1}	1%	2%
V_{OUT2}	1,11%	0,5%
V_{OUT3}	0,67%	0,8%
V_{OUT4}	4,99%	1,34%

Figs. 13, 14 and 15 show the drain-source, V_{DS}, and the output voltage waveforms. In Figure 13 we can see that the primary clamp successfully limits the voltage spike caused by the leakage inductance. Waveforms of the output voltages

V_{OUT1} and V_{OUT4}, shown in Figs. 14 and 15 respectively, indicate the appearance of pronounced oscillations at switching instants. By using fast rectifier diodes, much better performance can be achieved. Figs. 16 and 17 show the output voltage at start up. Soft start functionality is often useful to avoid a high output voltage overshoot during power supply turn on.

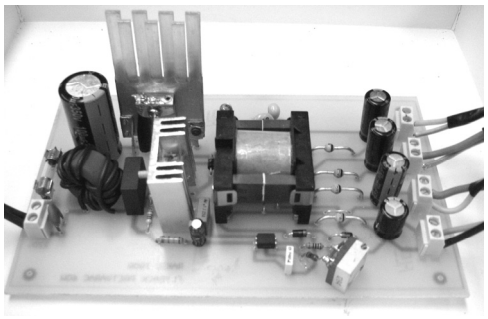

Fig. 12: *Flyback converter prototype.*

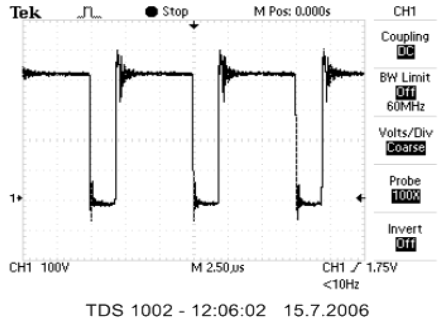

Fig. 13: *Voltage V_{DS} – all outputs maximum loaded.*

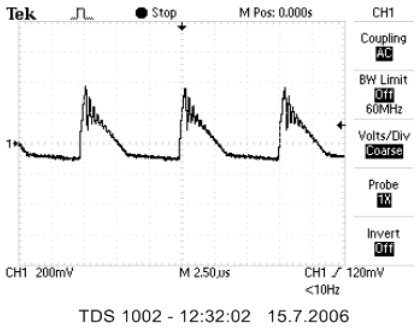

Fig. 14: *Waveform of V_{OUT1} at maximum load – other outputs are minimally loaded (discontinuous mode of operation).*

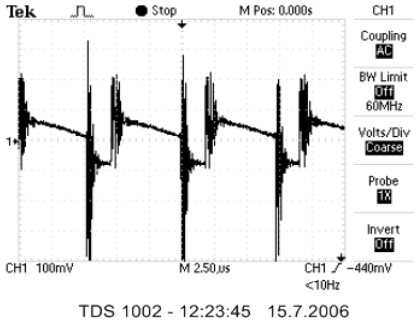

Fig. 15: *Waveform of V_{OUT4} – all outputs maximum loaded (continuous mode of operation).*

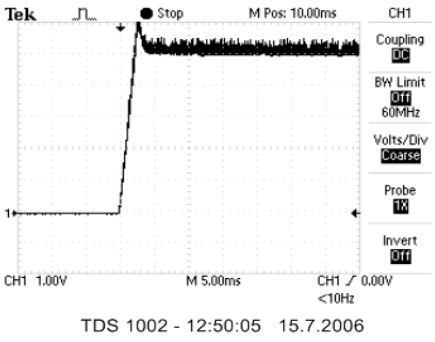

Fig. 16: *V_{OUT1} at start up at maximum load– other outputs are minimally loaded.*

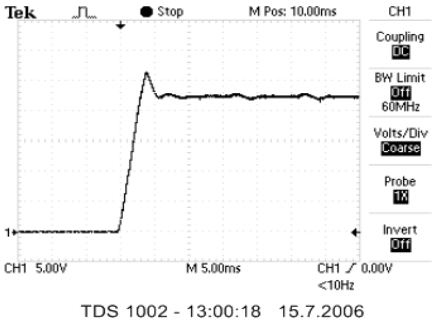

Fig. 17: *V_{OUT4} start – all outputs maximum loaded.*

7. CONCLUSION

In this paper the implementation of an integrated solution for the control of the Flyback converter was analysed where, among the available integrated circuits, TOPSwitch was chosen. It simplifies the device structure by reducing the number of its external components and incorporates additional features such as protection, soft start etc. Also the detailed procedure for sizing of the converter components is shown where special attention is given to the transformer construction. In order to verify the design procedure, the device is realized according to recommendation of the manufacturer. Finally, the measurement results were presented which are in accordance with typical values. However, unacceptably high output voltage oscillations during switching instants, indicate the necessity of using high performance rectifier diodes.

8. REFERENCES

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COMPACT ARCHITECTURE OF DIGITAL DECIMATION FILTERS FOR SOLID-STATE ENERGY METER

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Abstract: *This paper presents the architecture of decimation filters used at the output of A/D converters in three-phase solid-state energy meter. The filter implementation uses a new compact form of Multiplier and Accumulator (MAC) architecture combined with Time Division Multiplexing (TDM). This implementation enables significant savings in chip area. The presented architectures are coded in VHDL, verified by simulations and synthesized using AMI CMOS 0.35um standard cells library. Besides, areas of the decimation filters implemented using this architecture are compared to the areas of the filters implemented in the fabricated single-phase chip prototype.*

Keywords: *Decimation filter, Energy measurement, MAC architecture, FIR filter design*

1. INTRODUCTION

Solid-state energy meter is used for measuring of active and reactive energy using instantaneous values of voltage and current [1]. Fig. 1 presents corresponding block diagram of the chip. It consists of three main units: analog unit containing band-gap voltage reference, A/D converter based on ΣΔ modulators, digital decimation filters block and DSP block that performs all necessary calculations.

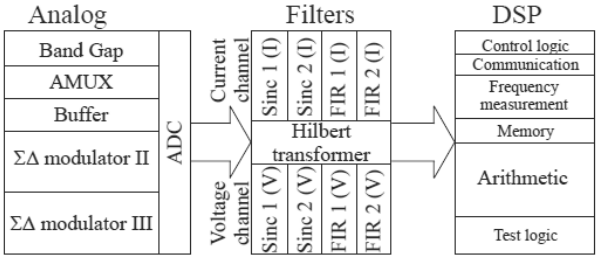

Fig. 1: *Solid-state energy meter block diagram.*

ΣΔ modulators are implemented using oversampling technique with sampling frequency of 524.288 kHz. This frequency is 128 times higher than operating frequency of the DSP block. This enables 1-bit A/D converter implementation in voltage channel while A/D converter in current channel is implemented as MASH architecture [1] with 3-bit signal at the output.

Decimation filters in voltage and current channel remove noise at high frequencies and reduce sampling frequency from 524.288 kHz to 4.096 kHz. The decimation factor of 128 is achieved in four filter sections with decimation factors 8-4-2-2. The first two sections are Sinc filters, while the last two sections are half-band FIR filters (Fig. 2) [2]. Hilbert transformer implemented as half-band FIR filter [3] shifts phase of voltage signal for 90° . This enables using the same hardware for active and reactive power calculation.

DSP block processes digital signals generated at the output of decimation filters and Hilbert transformer and calculates all quantities required by the project specification [1]. Besides, it contains modules that control data flow within the chip, communication modules, memory for storing measured and calculated values and test logic.

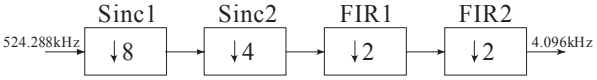

Fig. 2: *Architecture of decimation filters chain.*

The following section briefly describes the digital filters implementation used in prototyped single-phase chip. The third section introduces modification of MAC architecture in order to improve its performances and achieve additional reduction in chip area. Such improved MAC architecture is called *compact* MAC architecture. The fourth section presents filter block architecture for three-phase chip based on time division multiplexing. The paper concludes with a comparison between results of simulation and synthesis obtained for filters in single and three-phase chip.

2. FILTER BLOCK ARCHITECTURE FOR SINGLE-PHASE SOLID-STATE ENERGY METER

As Fig. 2 shows, the first two sections of decimation filter are realized as Sinc filters with decimation factor 8 and 4, respectively. Amplitude response of this filter corresponds to the function $\mathrm{Sinc}(x)=(\sin x)/x$. Sinc filter with frequency reduction ratio of N is a linear system that calculates mean value of at least N input samples. The implementation of these filters is very simple. The deviation in amplitude response at lower frequencies which Sinc filter introduces can be corrected using an appropriate FIR filter.

Comb architecture with all coefficients equal one enables the simplest implementation of Sinc function that does not require multipliers.

The order of Sinc filter, k, ($\mathrm{Sinc}^k(x) = (\mathrm{Sinc}(x))^k$) should be bigger for at least one than the order of ΔΣ modulator before it [2].

Figure 3 shows the architecture of Sinc^3 filter implemented as cascade connection of three accumulators and three differentiators [2]. This filter is the first Sinc filter in the voltage channel. Since the order of ΔΣ modulator in voltage channel is 2, the filter order is 3. The accumulators operate at oversampling frequency of appropriate ΣΔ modulator, while the differentiators operate at N times lower clock frequency, where N is the decimation ratio. As a result, the filter generates mean value of N samples at the output. Minimal output word length is determined by: (i) input word length, (ii) filter order and (iii) decimation ratio. Since the Sinc filter in Fig. 3 has the decimation ratio N=8, clock frequencies for accumulators and differentiators in this filter are clk_a = 524.288 kHz and $clk_d = clk_a / 8$ = 65.536 kHz.

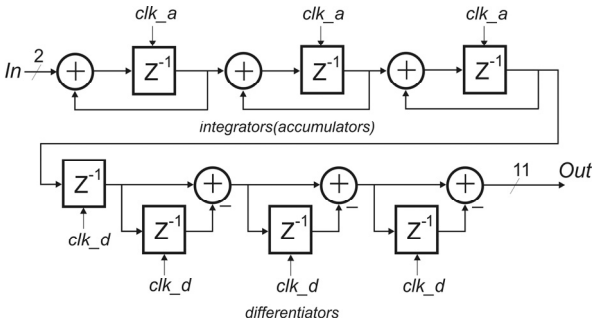

Fig. 3: *The architecture of the first Sinc[3] filter in voltage channel.*

The second part of the decimator chain contains two FIR filters. Decimation factor for each FIR filter in voltage and current channel is 2. Both filters are half-band, in order to simplify their hardware implementation. It enables to generate filters with symmetrical coefficients $h(i) = h(N-1-i)$ (i=0,...,N), N is the filter order, where all odd coefficients equal zero. Fig. 4 shows the structure of such FIR filters.

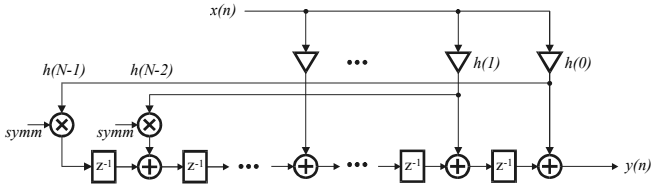

Fig. 4: *Half-band FIR filter structure.*

The first FIR filter corrects distortion in amplitude response caused by Sinc filter. Moreover, this filter provides appropriate out of band attenuation.

Hardware implementation of FIR filter coefficients is based on CSD (Canonical Signed Digit) representation. Such architecture does not require multipliers. The multiplication is implemented using bit shifting and adders. Due to CSD form, the number of addition and subtraction operations is minimal. The architecture provides low power consumption, high speed and simple implementation [2].

Hilbert transformer is implemented as a FIR filter with CSD coefficients [3], as well. In order to compensate for the delay that it introduces, the voltage and current signal at the output of FIR filters should pass through all-pass filters (Fig. 5). All-pass filters are implemented as an array of (N-1)/2 = 15 registers, where N is the number of taps in Hilbert transformer (N=31).

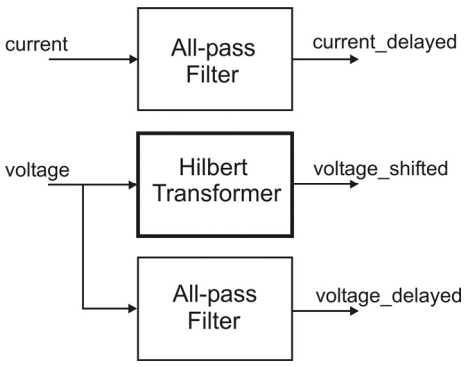

Fig. 5: *Hilbert transformer and all-pass filters.*

Fig. 6 shows the layout of the single-phase solid-state energy meter chip. The filter block containing Sinc filters, FIR filters and Hilbert transformer is outlined in rectangle.

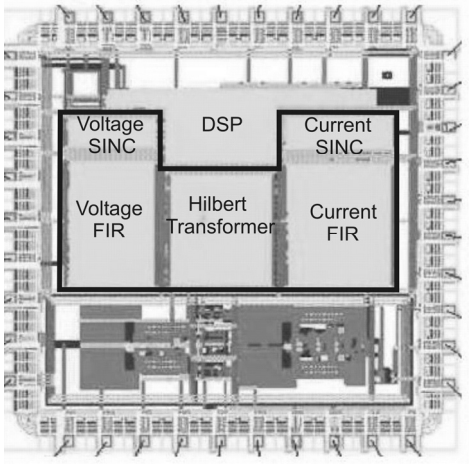

Fig. 6: *The layout of single-phase solid-state energy meter prototype chip.*

Table 1 gives the area for every block in digital part of the chip expressed in number of NAND gates. These values represent the results after synthesis using program *Ambit Build Gates*, which is the part of *Cadence* IC design package [8], and AMI CMOS 0.35um technology library.

As Fig. 6 shows, filter block occupies the biggest area in the chip. From the data given in Table 1, one can calculate that filter block contains 68% of the digital part of the chip. FIR filters and Hilbert transformer, as one of biggest blocks, together contain 58% of the digital part.

Having in mind that chip area directly influences the cost of its fabrication, it is very important to design a chip with the smallest area. One good design solution for FIR filters that does not require high sampling frequencies is MAC (Multiplier and Accumulator) architecture [5],[6]. Compact MAC architecture that is presented in this paper introduces a number of improvements in this architecture relating to area, dissipation and efficiency. It enables significant savings in area, especially having in mind filters required for three-phase energy meter.

Table 1 - The area of digital blocks in the single-phase chip after synthesis

Block	*The area in number of NAND gates*
Voltage SINC	2296
Current SINC	3265
Voltage FIR	10006
Current FIR	11704
Hilbert transformer	10286
DSP	17673
Total	55230

3. COMPACT MAC ARCHITECTURE

FIR filters with MAC architecture use the following method to calculate output sample.

The pairs *coefficient/corresponding_input_signal-_sample* represent inputs to a multiplier. Product of multiplying is written into accumulator where it is added to the product of the previous pair. The calculation is over when the product of the last pair is written into the accumulator. Then the result from the accumulator is loaded into the output register, accumulator resets, and the complete calculation cycle repeats.

Registers implemented using standard flip-flops can store input samples of the filter. However, such solution causes significant overhead in the chip area.

In order to improve the ratio area-speed-dissipation, compact MAC architecture implements the following techniques:

- RAM macrocells are used instead of registers
- Gated clock signals reduce dissipation
- Modified Booth algorithm reduces the number of clocks necessary for multiplication
- Overlapping technique is used in order to speed up output sample calculation

These techniques contribute to reduction in the chip area and dissipation and improve speed.

Implementation of Hilbert transformer and FIR filters using compact MAC architecture for single-phase energy meter chip is described in [5] and [6]. It is important to note that used RAM macrocells of 64x24 bits are bigger than it is necessary.Table 2 compares the area of the filters with CSD coefficients to the area of the filters with compact MAC architecture.

Table 2 - The comparison of decimation FIR filter areas implemented in CSD and compact MAC architecture after synthesis

Architecture	*Area in number of NAND gates*		
	Voltage FIR	Current FIR	Hilbert
CSD	10006	11704	10286
Compact MAC	4285	4784	5690

4. FILTER BLOCK ARCHITECTURE FOR THREE-PHASE SOLID-STATE ENERGY METER

Prototyped solid-state energy meter measures electrical energy consumption in single-phase systems. In order to apply it in three-phase systems, it is necessary to make certain modifications. The simplest solution for digital filter block is to replicate all modules in it three times, once for each phase. However, having in mind that the area of three-phase chip should be as small as possible, this solution is not acceptable.

Time Division Multiplexing (TDM) technique appears to be a promising solution. When applied to digital filters in three-phase chip design, it resulted in significant savings in the chip area. This technique provides multiple uses of some filter resources. Therefore, it is implemented in Sinc filters, as well as in FIR filters and Hilbert transformer with compact MAC architecture.

Fig. 7 shows Sinc filters chain for voltage channel in the three-phase energy meter. Counter generates the *select* signal for multiplexer which successively passes input voltage samples for phases S, R, and T with rate of 524.288 kHz. After processing in Sinc filters with decimation factors 8 and 4, respectively (removing of noise, increase in number of bits and reduction of sampling rate), samples are written into output registers clocked by frequency of 524.288 kHz / 8 / 4 = 16.384 kHz.

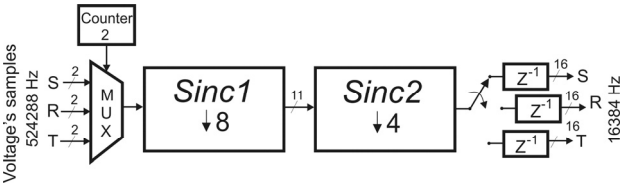

Fig. 7: *Three-phase Sinc filters in voltage channel.*

Fig. 8 shows the architecture of the first Sinc^3 filter in voltage channel. Accumulators and differentiators contain three registers to store samples relating to S, R, and T phases. The number of arithmetic blocks (adders and subtractors) is the same as for the filter in the single-phase chip shown in Fig. 3. This is also the case for other Sinc filters. Such architecture provides significant savings in the area comparing to the solution with replication of all filters.

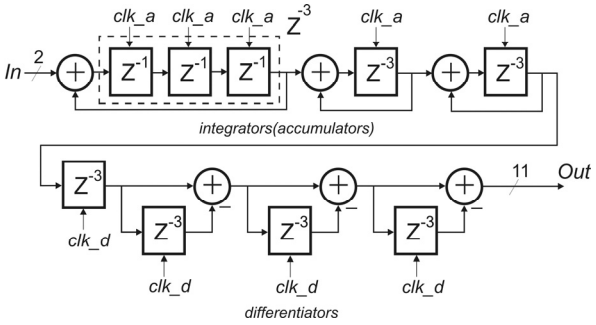

Fig. 8: *Architecture of the first Sinc^3 filter in voltage channel.*

However, the clocking becomes a little bit more complex. In order to achieve the same processing speed as in the case of single-phase filter, clock frequencies of accumulator and differentiator should be at least three times higher. Fig. 9 shows the waveforms of clock signals for accumulators (*clk_a*) and differentiators (*clk_d*).

Gating the clock signal *clk_2* with frequency of 4 x 524.288 kHz = 2,097.152 kHz, generates clock signals *clk_a* and *clk_d*. The frequency of *clk_2* is four times higher than the frequency of input signal that is 524.288 kHz. Since the basic frequency in the chip is 4.096x1024 = 4,194.304 kHz, the clock *clk_2* can be easily generated by dividing this frequency by 2.

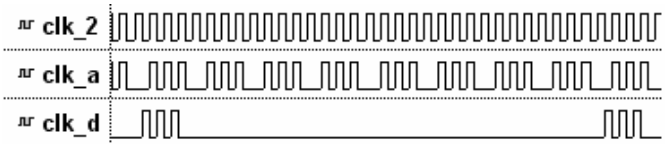

Fig. 9: *Waveform of clock signals clk_2, clk_a, clk_d.*

Compact MAC architecture for three-phase FIR filters and Hilbert transformer is based on *controller*/*datapath*

structure. It will be briefly explained on an example of FIR filters design in voltage channel. Responses of these filters for all three phases referred as S, R, and T are described by the following equations:

$$y_{v1}(n) = \sum_{k=0}^{2} h_{v1}(2k)\left[x_{v1}(n-2k) + x_{v1}(n-10+2k)\right] + h_{v1}(5)x_{v1}(n-5) \quad (1)$$

$$y_{v2}(n) = \sum_{k=0}^{7} h_{v2}(2k+1)\left[x_{v2}(n-(2k+1)) + x_{v2}(n-32+(2k+1))\right] + h_{v2}(16)x_{v2}(n-16) \quad (2)$$

Where h_{v1} and h_{v2} are filter coefficients, x_{v1} and x_{v2} are input signal samples, and y_{v1} and y_{v2} are output signal samples.

Fig. 10 shows block diagram of the filter datapath. It consists of the following modules:

- Input registers for storing samples from Sinc filter outputs
- Three 64x24 SRAM memory cells for storing filter input samples x_{v1} and x_{v2} for phases S, R and T,
- Registers *Reg_sym1* and *Reg_sym2* for storing samples relating to symmetric coefficients which adder *Adder_sym* sums.
- ROM memory for storing filter coefficients
- Booth multiplier with accumulator (MAC unit)
- Multiplexers *MUX_1* and *MUX_2* to control data flow
- Output registers for storing output samples y_{v1} and y_{v2} for phases S, R, and T.

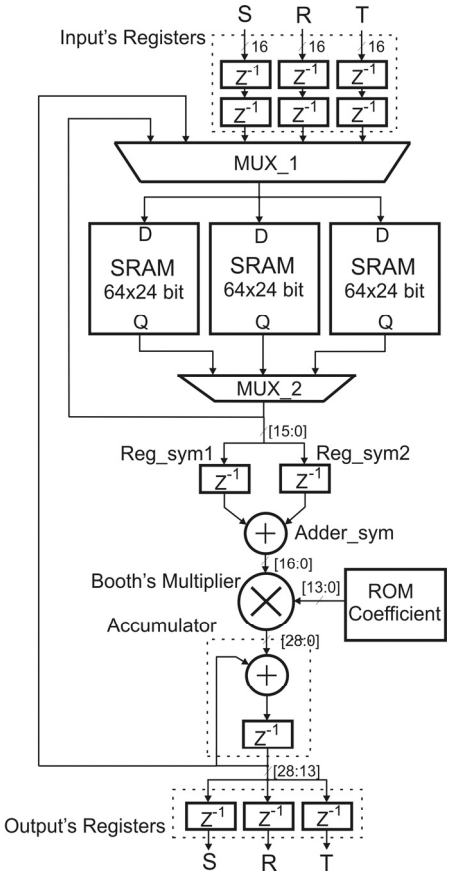

Fig. 10: *Datapath block diagram for FIR filters in voltage channel.*

Control unit implemented as an FSM of Moor type controls the work of the datapath. It contains 2-bit counter that generates the mode in which the control unit works, i.e. samples of which phase are filtered at the moment. States of the counter are: "00" (state *IDLE*), "01" (phase S), "10" (phase R) and "11" (phase T). Fig. 11 shows simplified state diagram of the control unit.

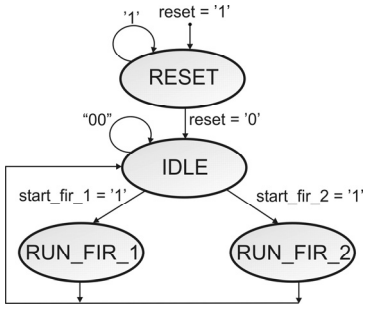

Fig. 11: *Simplified state diagram of the control unit.*

The clock of the control unit is 4.096x1024 kHz. At system startup it is necessary to reset the control unit (*reset = '1'*). From *RESET* state it goes to *IDLE* state when reset signal is inactive. In *IDLE* state the control unit waits for activation of signals *start_fir_1* or *start_fir_2* with frequencies of 8.192 kHz and 4.096 kHz, respectively.

When *start_fir_1* = '1', the control unit goes into complex state *RUN_FIR_1* in which it generates control signals necessary for functioning of the first FIR filter represented by Eq. (1). When *start_fir_2* = '1', the control unit goes into complex state *RUN_FIR_2* in which it generates control signals necessary for functioning of the second FIR filter represented by Eq.(2)

Fig. 12 shows more detailed state diagram of the control unit.

At the beginning of the state *RUN_FIR_1* it is necessary to transfer input samples of phases S, R, and T from the input registers (Fig. 10) into memory cells at addresses '0' and '1' (state *Store*).

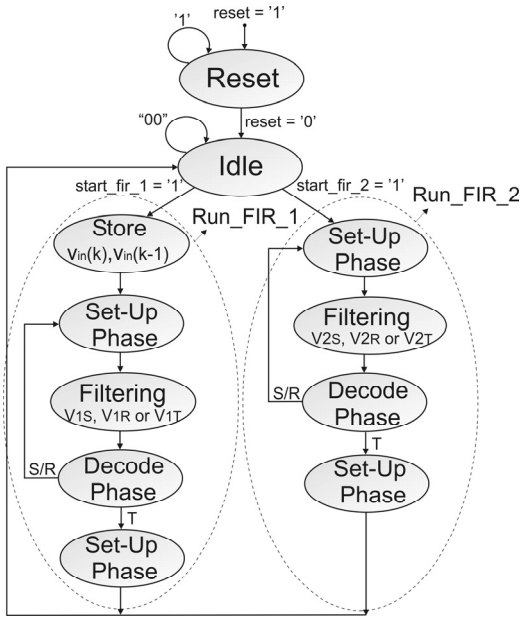

Fig. 12: *Detailed state diagram of the control unit.*

In state *Set-Up Phase* the counter is incremented ("00" → "01") which indicates the control unit that in the next state *Filtering* the datapath should filter samples of S phase. In state *Filtering* output sample is calculated according to Eq. (1). Simultaneously (overlapping technique), the content of memory locations shifts, implementing the delay operation (multiplication by z^{-1}). At the end of the state *Filtering,* calculated samples are stored into appropriate memory locations. Consequently, the control unit goes into state *Decode_Phase* in which the control unit decides (depending on which phase is filtered) if it goes to filtering of the next (R or T) phase, or into state *IDLE* (if filtering of all phases is finished). The control unit then goes into state *Set-Up Phase* in which the counter is incremented. The same operations are performed in state *RUN_FIR_2*. In this state, state *Store* does not exist, because appropriate samples are already in the memories.

Modified Booth algorithm, gated clock signals and overlapping technique are implemented as explained in [6].

5. SIMULATION AND SYNTHESIS RESULTS

Functionality of VHDL digital filter models is verified by *Active HDL* simulator [7]. For each digital filter appropriate test bench containing input and clock signals is written. Fig. 13 shows waveforms of signals *Voltage_S*, *Voltage_R, Voltage_T*, *Current_S, Current_R* and *Current_T* generated in simulations. These signals in time domain have the sinusoidal shape as "analog" signals, but in fact they are values of 16-bit (*Voltage*) and 21-bit (*Current*) output signals. The phase shift between signals is 120°.

After verification of the simulation results, VHDL models of filters are imported into the program for logical synthesis *Build Gates*, which is the part of *Cadence* IC design package.

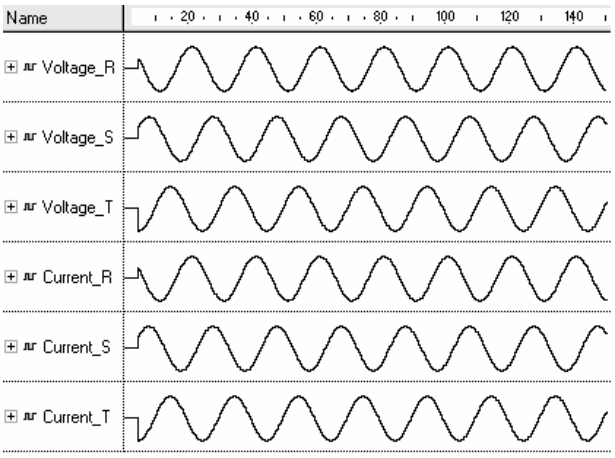

Fig. 13: *Filter simulation results.*

The filters are synthesized using standard cells library AMI Semiconductors CMOS 0.35um C035M-D [9]. Table 3 compares the areas of single-phase CSD and three-phase compact MAC Hilbert transformer, as well as Sinc and FIR filters in voltage (SINC_V and FIR_V) and current channels (SINC_C and FIR_C).

As it can be seen in Table 3, areas of three-phase FIR filters are smaller than areas of single-phase filters, which are implemented in the energy meter prototype chip.

Table 3 - Areas of single-phase and three-phase digital filters

Architecture	*Area in number of NAND gates*					
	FIR_V	FIR_C	SINC_V	SINC_C	Hilbert	Total
CSD (single phase)	10006	11704	2296	3265	10286	37557
Compact MAC (3 phase)	7977	8531	4295	7243	9984	38030

If we compare values of the total area (Sinc + FIR filters + Hilbert transformer), it can be concluded that the total area of three-phase filters is just 1.26% bigger than the area of single-phase filters.

6. CONCLUSION

This paper presents the architecture of digital decimation filters for three-phase solid-state energy meter chip. It uses time division signal multiplexing and compact MAC architecture in order to reduce big area of digital filters in the current single-phase prototype chip. Filters are synthesized using standard cells library AMI Semiconductors CMOS 0.35um. The filters designed in this way occupy only 1.26% bigger area than the filters in the single-phase chip.

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TOP-DOWN DESIGN METHODOLOGY FOR ΔΣ MODULATORS IN A/D APPLICATIONS

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Abstract: *This paper presents top-down design methodology of ADC based on ΔΣ modulators (DSM). The described flow starts from behavioral level and accomplishes with layout and prototyping. As an example the second-order DSM ADC is designed using Alcatel AMIS CMOS 0.35 μm technology. In order to verify design methodology, to measure performance and to detect and correct errors, a fabricated prototype is tested. Measured results are in good agreement with behavioral simulation.*

Keywords: *Top-down design methodology, ΔΣ ADC.*

1. INTRODUCTION

The main advantage of using oversampling delta- sigma modulators in integrated high-resolution analog-to-digital converters (ADC) is great relaxation for the analog component limitations. Delta-sigma modulators (DSM) employ coarse quantization enclosed in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is easy to shape the quantization noise with filters within the feedback loops and to shift most of the noise power out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio.

Oversampling delta-sigma converters are tolerant to imprecision in analog components but require increased complexity of digital part. Another advantage of delta-sigma converters is that they simplify the requirements for analog anti-aliasing filters in ADCs and smoothing filters in DACs. Furthermore, a sample-and-hold predecessor is usually not required at the input of the oversampling ADC. Therefore, they have become popular in recent years especially for medium to low speed applications such as high fidelity digital audio, digital telephony, and instrumentation. Future applications in digital video and digital radar systems are imminent as faster technologies become available.

This paper is organized as follows: the following Section 2 describes oversampling and noise-shaping technique. Section 3 describes architectures of the ΔΣ modulators. A method for behavioral simulation of architecture implementation, design describtion of the proposed second-order modulator and testing of the implemented second-order ΔΣ modulator is presented in Section 5.

2. OVERSAMPLING

Digital modulators relay on amplitude quantization and sampling in time. Periodic sampling at rates more than twice higher of signal bandwidth need not introduce distortion, but quantization does. A quantizer can be modeled with adding the quantization error e(n) to the input signal x(n) in order to generate output signal y(n), i.e., y(n) = x(n)+e(n), where n refers to the n-th sample [1]. The quantization error is the difference between the input and output values, which is bounded by $\pm\Delta/2$, where Δ equals the difference between two adjacent quantization levels, i.e., 1 LSB. The error e(n) is completely defined by the input x(n), but if x(n) is very active, e(n) can be approximated as an independent random number uniformly distributed between $\pm\Delta/2$. Thus one can treat the quantization error as white noise e with power defined by:

$$P_{\mathrm{e}} = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 \mathbf{d}e = \frac{\Delta^2}{12} \tag{1}$$

and it is independent on the sampling frequency, f_{S}. Assuming, the spectral density of e as a constant over frequency and that all of its power folds into the frequency band $\pm f_{\mathrm{S}}/2$, then the spectral density of the sampled noise is given by (2).

$$E(f) = \sqrt{\frac{P_{\mathrm{e}}}{f_{\mathrm{s}}}} = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_{\mathrm{s}}}}\,. \tag{2}$$

Oversampling occurs when the sampling rate f_{S} of the signal band limited to f_0, is larger than Nyquist frequency of $f_N = 2f_0$. The oversampling ratio is defined as $OSR \equiv \frac{f_{\mathrm{S}}}{2f_0}$.

After quantization the signals of interest are distributed below f_0 while the noise is spread over the entire spectrum. Therefore it is useful to filter the output signal according to (3).

$$H(f) = \begin{cases} 1 & |f| \le f_0 \\ 0 & f_0 \le |f| < f_{\mathrm{s}} \end{cases}. \tag{3}$$

This filter eliminates quantization noise (together with undesired signal images) greater than f_0. Simultaneously the in-band signal power remains as the original, while the quantization noise power is reduced to

$$P_{\mathrm{e}}' = \int_{-f_{\mathrm{s}}/2}^{f_{\mathrm{s}}/2} E^2(f)\left|H(f)\right|^2 \mathbf{d}f = \int_{-f_0}^{f_0} E^2(f)\mathbf{d}f = \frac{2f_0}{f_{\mathrm{s}}}P_{\mathrm{e}} = \frac{P_{\mathrm{e}}}{OSR}. \tag{4}$$

Therefore, each doubling of OSR (i.e., sampling at twice the rate) decreases the in-band noise power by one-half or, equivalently, 3 dB. Simultaneously, according to Eq. 1, it increases the resolution by only 0.5 bits.

2.1 Noise-Shaping Oversampling ΔΣ Modulation

A more efficient oversampling quantizer is the noise-shaped DSM shown in Fig. 1 [1]. Although most ΔΣ converters utilize 1-bit quantizers (i.e., only two output levels) due to the inherent linearity between two levels, a general discussion may be addressed on multilevel quantizers. Analysis based on the linear model shown in Fig. 2, gives signal transfer function, STF(z), and noise transfer function, NTF(z), as follows:

$$S_{TF}(z)=\frac{Y(z)}{X(z)}=\frac{H(z)}{1+H(z)}, \quad (5)$$

$$N_{TF}(z)=\frac{Y(z)}{E(z)}=\frac{1}{1+H(z)}, \quad (6)$$

where *Y(z), X(z)* and *E(z)* represent z-domain equivalents of discrete signals *y(n), x(n)* and *e(n)*, respectively.

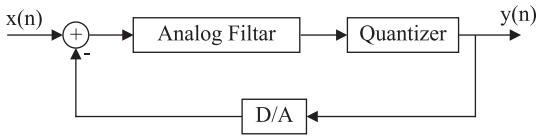

Fig. 1: *ΔΣ Modulator.*

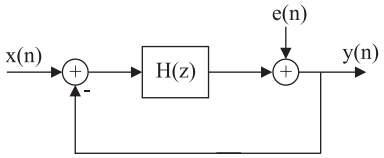

Fig. 2: *Linear model of ΔΣ modulator.*

Note that the zeros of NTF(z) will be equal to the poles of H(z). In other words, when H(z) goes to infinity, NTF(z) will go to zero.

According to Eq. 5 and Eq. 6 it is obvious that the output signal can be written as combination of the input signal and the noise as:

$$Y(z)=S_{TF}(z)X(z)+N_{TF}(z)E(z). \quad (7)$$

Useful noise-shaping requires to diminish NTF(z) and set STF(z) near unity within the bandwidth. Thus, the quantization noise is reduced over the signal bandwidth while the signal stays largely unaffected. Eventually, additional low-pass digital filters can remove the out-of-band noise.

3. ARCHITECTURES OF THE ΔΣ MODULATORS

The world of DSM can be roughly divided into the following groups:

- single-bit single-stage low-order designs,
- single-bit single-stage high-order designs,
- multi-stage cascaded designs with feedforward error cancellation, and
- multibit noise shapers.

The first and second order DSMs belongs to the first category as long as 1-bit quantizers are used. They have guaranteed stability [1], small restriction on input range and simple circuit design. However, they cannot achieve high SNR with low-to-medium oversampling ratios.

3.1 Higher-Order Single-Stage ΔΣ Converters

Generally, any arbitrary higher-order loop filter can be realized using cascade structure like the one in Fig. 3.

When a modulator has *L* loops and *N*-bit quantizer and is not overloaded, linear analysis [2] shows that the dynamic range of the modulator is:

$$DR(dB)=10\log\left(\frac{3}{2}\frac{2L+1}{\pi^{2L}}OSR^{2L+1}\left(2^{N}-1\right)^{2}\right). \quad (8)$$

Dynamic range increases by 3(2L-1) dB for every doubling of OSR when 1-bit quantizer is used, providing (L- 1/2) extra bits of resolution. However, modulator becomes unstable for loop filters of order greater than two. It is revealed in [1] that higher equivalent quantizer gain improves stability. To ensure finite output signal, the maximum input must be restricted to low values. In practice, the loop filter has to be carefully designed and the stability may be signal dependent.

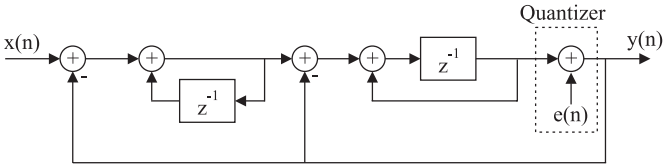

Fig. 3: *Second order ΔΣ modulator.*

3.2 Multi-stage (Cascade) ΔΣ Converters

An alternative structure to realize higher-order noise-shaping converters, which is free of the stability problems associated with the higher-order single-stage converters described above, is the multi-stage or cascade architecture shown in Fig. 4 [1].

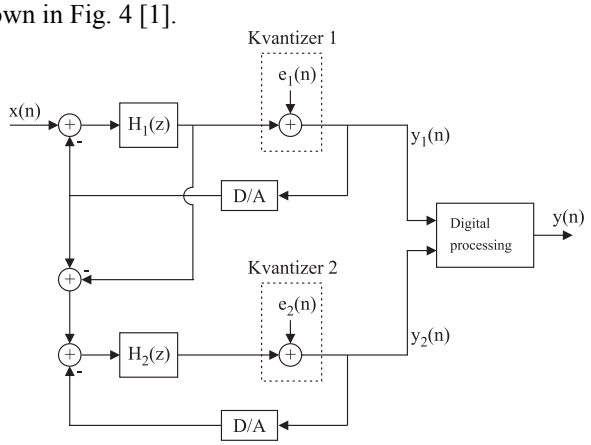

Fig. 4: *Model of cascaded modulator.*

The overall ΔΣ modulator consists of a cascade of several lower order single-loop modulators, each with its own quantizer. Each single-loop modulator in the cascade converts the quantization error from the preceding modulator. The errors of all but the last single-loop modulator are then digitally canceled. The guaranteed stability is achieved by using first- and/or second-order loops in a feedforward (as opposed to feedback) configuration.

It should be mentioned here that a major disadvantage of the cascaded structure is that the exact cancellation of the error e_1(n) (ref. to Fig. 4) requires accurate matching of transfer functions $H_1(z)$ and $H_2(z)$. If these conditions are not exactly satisfied, then unfiltered or poorly filtered noise due to e_1(n) will leak into the output data *y*(n), and the SNR rolls-off.

3.3 Multi-bit ΔΣ Converters

As mentioned before, one-bit DSM employ a 1-bit internal DAC with inherent linearity that does not require precision component matching. This relaxes requirement for analog components and increases attractiveness for modern VLSI technologies. According to Eq. 8 one can easily realize that employing multibit quantizers in the modulators can significantly increase SNR. This increase does not depend on OSR and the order of modulator. Equivalently, the multibit ΔΣ coder can achieve resolution comparable to that of a single-bit modulator at a lower sample rate, which is a

considerable advantage in applications requiring high bandwidth (like digital video). Simultaneously, it implies the lower clock rate and, therefore, decreased power consumption of digital circuitry.

Finally, the multibit quantizer is a better approximation to a linear amplifier than a single-bit one. Consequently, the stability properties are better as well as the agreement between the behavior predicted by linear theory and the actual performance.

The multibit internal ADC must be a parallel (flash) type circuit, since stability and noise cancellation allow only one clock period for conversion. On the other hand, the ADC nonlinearity merely increases the quantization noise, and should be suppressed by the noise shaping process. In contrary, any nonlinearity of the internal feedback DAC will directly affect the output signal. This can be seen from the analysis of the linear model [1] shown in Fig. 5, where a(n) represents the errors caused by the deviation of the quantizer thresholds from their ideal values (i.e., ADC nonlinearity) and d(n) represents the errors caused by internal DAC nonlinearity.

Proper noise shaping requires large H(z) gain at low frequencies. Therefore, both a(n) and e(n) are reduced by it when referred back to the input x(n). However, d(n) still resides in the feedback path, so that the ultimate linearity of y(n) is not better than the linearity of the N-bit internal DAC.

Table I summarize advantages and disadvantages of presented topologies.

Depending of imposed requirements (bandwidth, SNR, dynamic range, maximum clock frequency) the architecture should be chosen. According to Eq. 8, the dynamic range of a DSM operating at a given oversampling ratio may be extended by increasing the order of noise shaping loop L or by increasing the quantizer resolution N. Effectiveness of increasing the order of noise shaping is significantly diminished as the oversampling ratio decrease. Oppositely, the effectiveness of increasing the quantizer resolution is independent on the oversampling ratio. Every additional bit of quantizer, increases the dynamic range typically by 6 dB. Due to DAC linearity requirements number of bits at quantizer output is limited to 3-5. The full dynamic range predicted by Eq. 8 can be achieved for L>2 by cascading several first–order or second-order modulator stages. In practice, the dependence on achieving precise noise shaping, limits the number of cascaded stages to 3. One should choose the proper value for *OSR* considering the bandwidth, maximum clock frequency and power consumption.

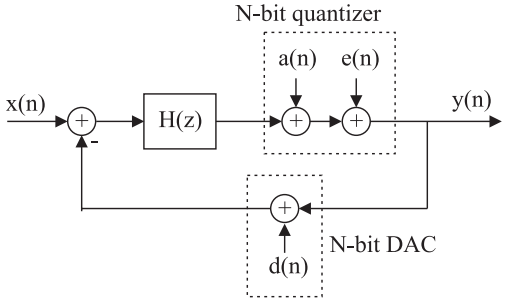

Fig. 5: *Simplified linear model of multibit ΔΣ modulator with included nonlinearity errors.*

The choices for NTF are n^{th}-order pure differentiator, Butterworth high-pass, inverse Chebyshev etc.

After architecture is chosen, the next step is to made choice between a switched-capacitor (SC) and a conventional active-RC (continuous-time) design. In general, most integrated circuit (IC) implementations of ΔΣ ADCs use SC circuits, whereas most system-level or hybrid implementations use active-RC circuits. The comparison between these types given in Table II explains reasons for such choice.

4. EXAMPLE OF ADC DESIGN

The entire design methodology will be illustrated on an example of ADC with the following specifications:

- Signal bandwidth is from DC to 2048 Hz,
- maximum input signal is 500 mVpp,
- maximum clock frequency is 4194304Hz,
- required SNR is 60 dB,
- standard CMOS 0,35μm is available.

Table I - Comparison of modulator architectures [1]

Modulator type	*Advantages*	*Disadvantages*
Low-order single-loop single-bit	*Guaranteed stability.* *Simple loop filter design.* *Input range may use almost the full range of 1's densities.*	*Low SNR (except for high OSR).* *More prone to idling tones (dither may help).*
High-order single-loop single-bit	*High SNR for modest OSR.* *Less prone to idling tones.* *Simple circuit design.*	*Difficult loop filter design.* *Stability is signal dependent.* *Maximum input range must be restricted to ensure stability.*
Multiloop cascade	*High SNR for modest OSR.* *Stability guaranteed.* *Maximum input range almost equal to the full range of 1's densities.*	*Requires near-perfect matching between analog and digital differentiator.*
Multibit	*High SNR for fairly low OSR.* *Stability much easier to achieve for high-order loops.*	*Imperfect matching of levels (in D/A half of quantizer) results in imperfect dc transfer function (integral nonlinearity errors).* *Decimation filter must allow for multibit input.* *More complex circuit design.*

Table II - Comparison of SC and RC modulator realizations, [1]

Circuit style	*Advantages*	*Disadvantages*
Switched capacitor	*Easily simulated.* *Compatible with VLSI CMOS process.* *Insensitive to clock jitter as long as full settling occurs.* *Insensitive to exact shape of op-amp settling waveform as long as full settling occurs.* *Pole-zero locations are set by capacitor ratios, which are highly accurate.*	*Large capacitor required for high SNR (*KT/C *noise limit).* *SC circuits are true samplers, potentially causing aliasing of out-of-band noise. They are thus more prone to picking up digital noise.* *Large spike currents drawn by capacitors are hard to drive from external sources (RC isolation circuits required).*
Continuous time	*Easy to breadboard.* *Less prone to pick up digital noise (no true input samplers are used).* *Easy to drive from external sources; no SC current pulses.* *SNR is not limited by capacitor size.*	*Not compatible with a simple CMOS process. Needs large capacitors, linear high-values resistors, low-noise op-amps.* *Accurate RC time constants not possible for monolithic designs without laser trimming.* *SNR degraded by nonideal comparator feedback signal.* *Sensitive to jitter, noise, and switching characteristic of 1-bit feedback waveform.* *Loop filter does not scale with clock frequency.* *Op-amp must always remain linear. It is not just the settled value that counts.* *Discrete-time simulations more difficult.*

Considering signal bandwidth and possible sampling rates it is easy to conclude that the maximum *OSR* value is 1024. However, this would imply high degree decimation filter and, therefore, OSR = 128 look as reasonable choice. It is quite logical to start considerations with the simplest i.e. 1-bit quantizer.

Initial calculations based on Eq. 8 show that first-order modulator gives dynamic range of 59 dB. It is good practice to have same margin during design and therefore the second-order modulator imposes as the proper choice.

For implementation in CMOS technology, SC configuration is natural [3].

4.1 Behavioral simulation

Simulation at behavioral level is the following design step. Writing the code for simulating ΔΣ modulators is a fairly simple task, particularly for discrete-time implementations. There are several software programs available for simulating DSM.

Verification of the chosen architecture is done using *Matlab Simulink* environment [4]. Ideal modulator output spectrum for a sinusoidal input signal of 97 Hz and amplitude of 125mV is shown in Fig. 6.

The analog circuit block cannot precisely perform their ideal function, so most of modulator nonidealities must be taken into account. Such are sampling jitter, *kT/C* noise, and operational amplifier parameters (white noise, finite dc gain, finite bandwidth, slew rate and saturation voltages). Only the first integrator needs to be simulated with nonidealities, since noise shaping does not attenuate their effects.

Simulink model used to simulate nonidealities is shown in Fig. 7 [5]. Only white noise is considered, while flicker noise and dc offset are neglected, because the first integrator has correlated double sampling [6]. Output spectrum obtained from simulation data for the sinusoidal input signal of 97 Hz and amplitude of 125mV of the modulator with modeled nonidealities is shown in Fig. 8.

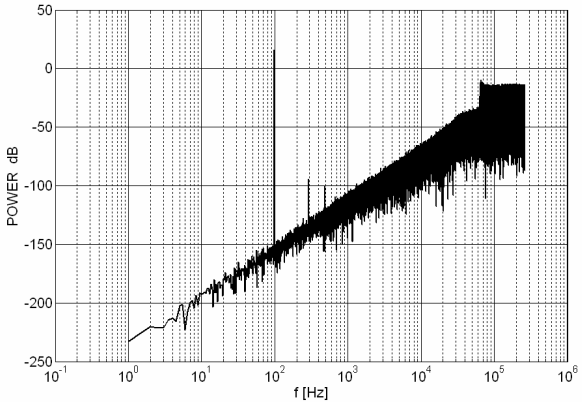

Fig. 6: *Output PSD of ideal modulator.*

4.2 Circuit design

After verification at behavioral level, the design is ready for transistor level implementation.

The operational amplifier used in integrators is the most critical element of the modulator. Behavioral simulation with nonidealities indicates that a slew rate of 4 V/μs, GBW of 2.5 MHz is sufficient to meet performance objectives. Since the comparator can be designed to be quite fast, the settling speed of the integrator ultimately limits the achievable sampling rate of the modulator, even if complete settling is not required. The need for high speed, together with a relatively modest gain requirement of 60 dB to suppress harmonic distortion, encouraged the use of the folded-cascode operational amplifier [7].

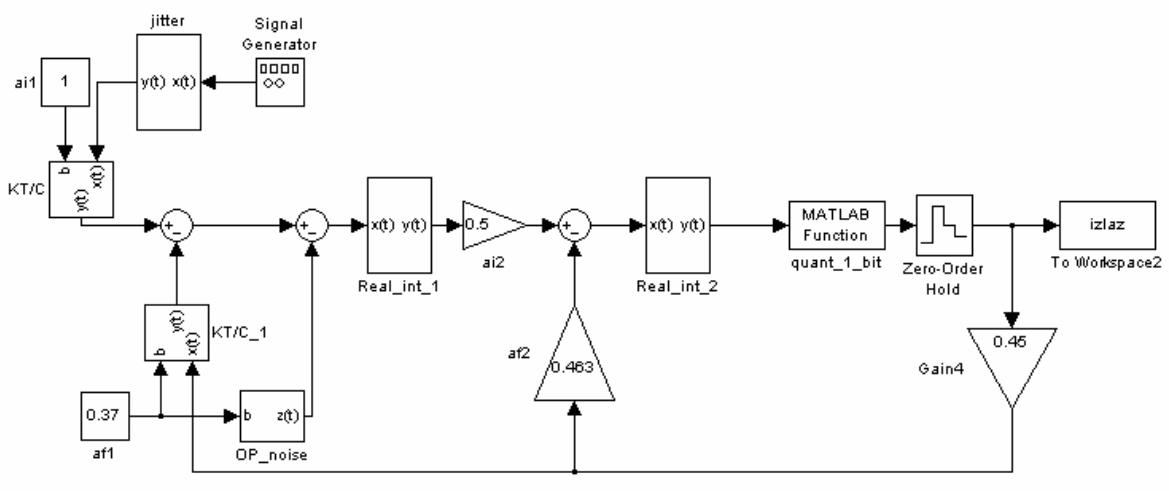

Fig. 7: *Simulink model of the second-order modulator.*

The common-mode levels in the fully differentially amplifier are set by the common-mode feedback (CMFB) circuit.

A wide-swing cascode current mirror bias circuit provides the bias voltages [8].

The second major component of the modulator is the comparator. The performance of the modulator is relatively insensitive to the comparator offset and hysteresis since the second order noise shaping attenuates the effects of those impairments. The regenerative latch has been used to implement the comparator [9].

During layout implementation a special attention was paid to the component matching and noise reduction.

After all required analog blocks (operational amplifiers, bandgap reference, switches, capacitors and quantizer) were designed and verified by circuit analysis the design is prepared for layout implementation.

The delta-sigma modulator was designed for fabrication in 0.35-μm CMOS technology. Modulator occupies the area of 0.57 mm^2.

4.3 Measurement

In order to verify design methodology and measure performance of fabricated ADC, a dedicated test set-up is developed. The set-up is shown in Fig. 9.

It consists of PCB with circuit under test, acquisition card NI-6251 [10] which is responsible for analog stimulus generation and digital data acquisition. The card is controlled by *Lab View* software [11]. After acquisition analysis is performed in frequency domain using FFT.

Spectrum obtained after stimulus with amplitude of 500 mVpp differential sine-wave signal and frequency of 97 Hz, applied to ADC input is shown in Fig. 10. Fig. 11 presents the power spectrum of output signal acquired from the second order delta-sigma modulator. In order to verify design methodology the same input signal is used as stimuli for behavioral simulation of the delta-sigma modulator. Fig. 12 illustrates the corresponding power spectrum. Obviously, behavioral model matches well to measured results.

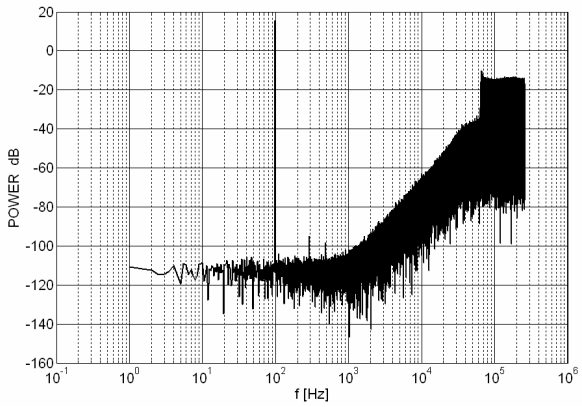

Fig. 8: *Output PSD of DSM from Fig. 7 with nonidealities.*

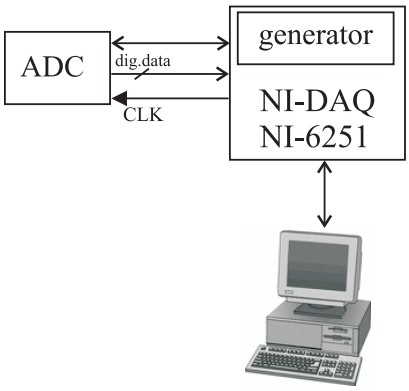

Fig. 9: *ADC test-up.*

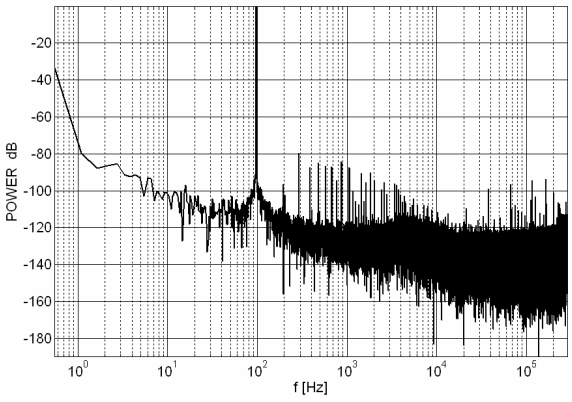

Fig. 10: *Input PSD of acquired data.*

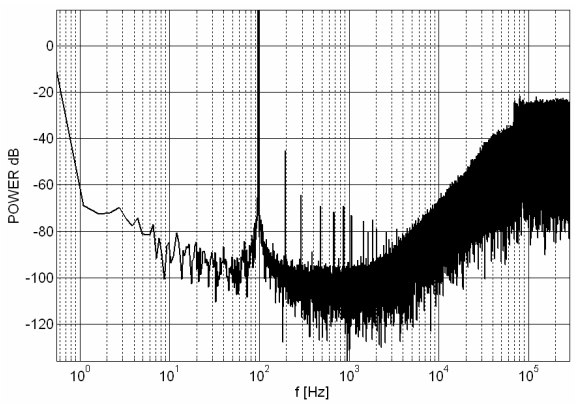

Fig. 11: *Output PSD of measured signal.*

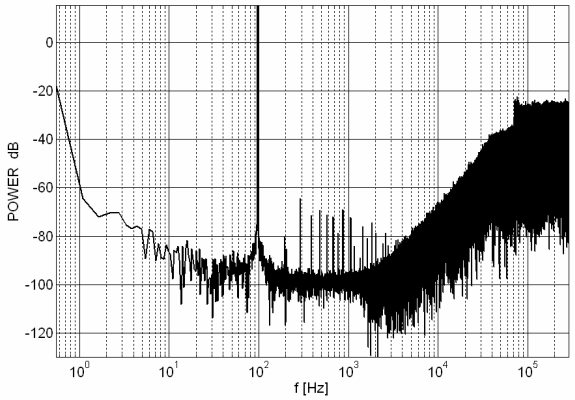

Fig. 12: *Output PSD from behavioral simulation.*

5. CONCLUSION

This paper presented methodology for design of ADC based on DSM. Second-order ΔΣ is realized in SC technique. Circuit is implemented in Alcatel AMIS 0.35 μm technology. ADC occupies 0.57 mm^2. To verify design methodology, prototyped ADC is tested and results shows good matching between behavioral and measured results.

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THERMOVISION AS THE RELIABLE CONTROL MEASURMENT SYSTEM OF ENERGETIC EFFICIENCY IN INDUSTRY

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Abstract: *This work deals with the possibility of a contemporary thermovision system application in producing plenary energetic balance in a industrial company. A modern optical thermovision system of high resolution has been used. Verification of the suggested control-measuring method was done in the factory of inner tyres production "Tigar"-Babusnica.*

Keywords: *Thermovision, Energetic efficiency, Measuring, Industry.*

1. INTRODUCTION

Temperature measuring in thermovision systems is based on the detection of the energy of rays (with wave length of 0.7μm to 14μm), emitted by all objects in nature whose temperature is above the absolute zero. Rays which are proportional to temperatures of objects get moderated into pictures or thermographs, whose relative temperature differences are demonstrated by the colour palette or in shades of grey [1].

The way of non-contact temperature measuring as well as insufficient sensitivity of infrared sensors, applied in these systems have influenced that only two separate atmospheric windows get used in practice because of the specific earth atmosphere spectral transmission. These two have been emphasized in literature, the first, as the field of middle wave infrared rays (MWIR) of 2μm to 5μm with matching silicium optics, and the second, as the field of long wave infrared rays (LWIR) of 8μm to 14μm with matching germanium optics. For those two applications adequate families of infrared sensors have been developed which are used as receptive detectors of rays in thermovision systems. In practice, the LWIR thermovision sensoring systems have shown their advantages and possibilities for wide application in various economy fields.

2. BASIC FEATURES OF THERMOVISION SYSTEMS

When there has to be a choice of a certain thermovision system, as one of its very important features is which detecting technology is used. Two basic methods of detecting are widely used in all systems: scanning and the matrix scheme of the detector in focal plane array (FPA) [1].

Thermovision systems based on scanning which is considered as an earlier method use only one detector combined with two-dimensional opto-mechanic scanning system.

FPA is a new technology in which a lot of mini sensors (pixels) in the form of matrix are placed in FPA of an objective. A thermovision picture is formed by a successive reading of the pixels, applying different methods and digital circuits electronics. Thermovision systems with this scanning technology are much more expensive, but at the same time they are much more compact, more flexible and more precise, too [2].

Temperature measuring done by applying the thermovision systems belong to the category of complex measuring methods. Besides the basic characteristic infrared rays (marked by 1 in fig. 1) emitted by the given object, there appear three unwanted types of radiation when measuring is in the question. In figure 1, those rays are shown as those which get reflected from the surface of the given object, or from the surfaces of the surrounding objects which can be spanned by the given measuring system objective (marked by 2), and it seems to be radiation of the objects behind the measuring system reciprocal to the transitivity of the measured object (marked by 3) as well as the characteristic radiation of the air beam (shown by the broken line) [3].

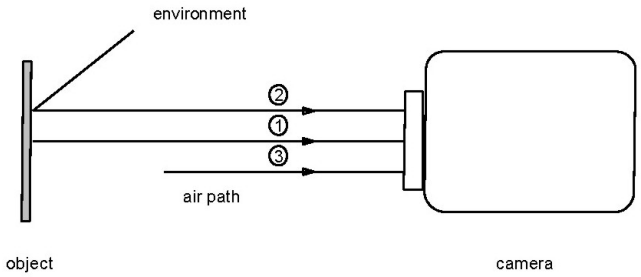
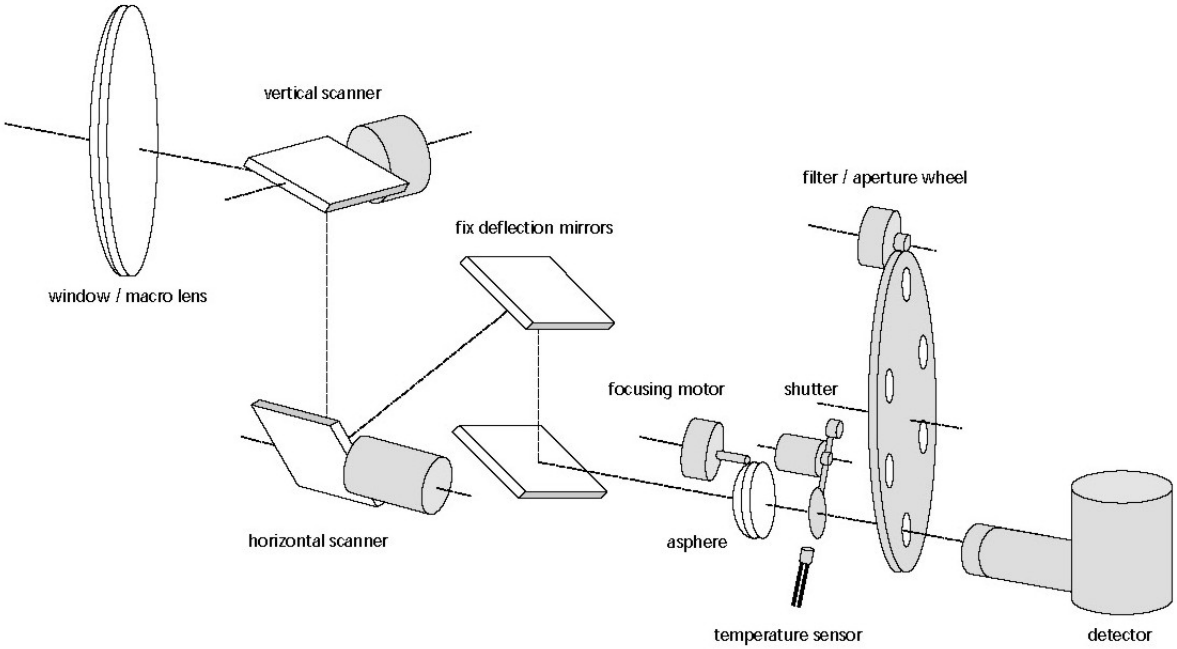


Fig. 1: *The possible mistakes during non-contact temperature measuring.*

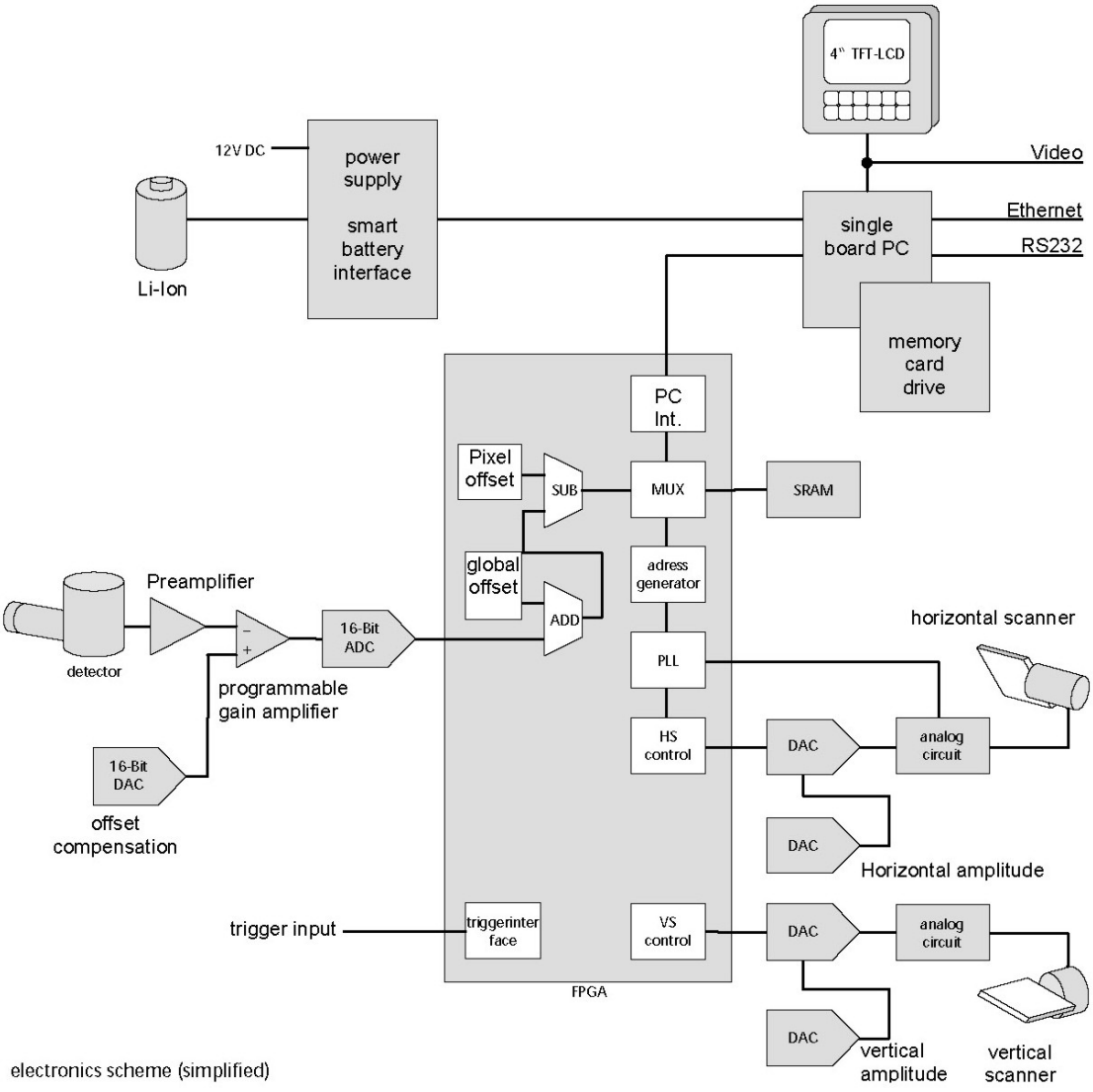
Since the total of radiation is the sum of the basic rays of a basic measured object, reflected and transmitting radiation, as well as characteristic radiation of an air beam, the quality of temperature measuring systems mostly depends on applied software. The software has to make calibration diagrams modification or on the applied analytical formulas for temperature definition. It is suggested that a measuring system automatically defines and records certain correcting parameters, or at least to enable some parameters modification in the course of measuring (the distance of a measured object, an emission factor, ambient temperature, etc).

In the real conditions, the precision of the thermovision temperature measuring gets worse as the ambient temperature reduces (especially if it's below 0°C). It goes especially in cases when measuring objects are under the sun radiation influence or under some other artificial light sources, or when measuring is done under inconvenient outdoor conditions, i.e. windy weather, smoke and gases presence, or the presence of some transparent obstacles on the measuring way (e.g. windows made of glass, poly-bicarbonate or acryl, etc.).

Out of all types of non-contact temperature measuring, the thermovision systems offer more options because they provide creating two-dimensional picture with the resolution similar to those of a TV set. The measure results are given in digital recording which is found to be very good for memorizing and data processing.



(*a*)



(*b*)

Fig. 2: *(a) Principle of thermovision camera scanning, (b) Basic feature scheme of the camera Varioscan 3021*ST.

Basically, all thermovision systems consist of the same parts: optic system, detector, electronical device, the calcualtor and visualizator. Figure 2 presents scanning principle and a basic feature scheme of the used Varioscan camera.

The optic system is the most expensive part of the camera because it has systems of lens on *Ge* and *Si* bases , depending on the chosen spectral span of TV camera functioning.

Fast development in the sensor technology production for the last years of the 20th century has put aside the use of cameras with quant detectors and mechanical scanning systems, making that way cameras with matrix detector, which is placed in the focal plane array (FPA), more used.

The latest technology of censor production enables matrix detectors to be used as censor elements non-cooled microbolometres or quant censors, 640x480 pixels tick and of 25μm in size.

All other parts of the newest thermovision camera are made in the purpose of using the most advanced components and function principles within real time, at which the quality of the thermovision picture matches the quality of a standard TV picture. Introducing adequate multibit A/D and D/A converters, high temperature sensitivity is obtained.

3. EXPERIMENT

Thermovision systems offer a wide application in economy fields [4, 5]. This part of the work presents the results after applying the thermovision system Varioscan 3021 produced by "Jenoptik" from Germany. The Thermovision Laboratory of the Electronic Faculty of Nis, in cooperation with the Mechanical Faculty of Nis, carried out the project of energy balance check in industrial companyes. It was based on the specific application in the "Tigar" MH programme of inner tyres in Babusnica, so the main characteristics of the thermovision systems application were determined, i. e. the system has been claimed to be a reliable controlling and measuring system [6].

Figure 3 shows the scheme of the 4 different functional areas on which the application of the newest systems has produced excellent results.

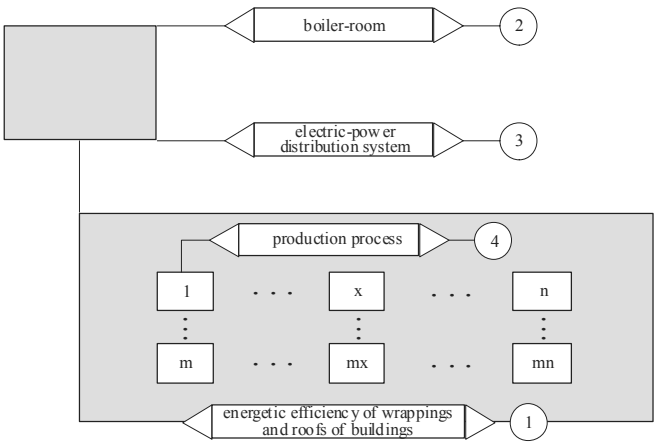


Fig. 3: *Functional areas of the application of a thermovision system.*

The first field (1) presents the importance analysis of the heat loss through the walls, outer openings, as well as roofs of various industrial objects within one industrial company [7].

Thermovision recording of the given objects provides fast and efficient input data collection for a consequent laboratory analysis, using some available PC programme, which is good for calculating heat losses of building and object coverings, while the given software has to be in accordance with the technical conditions of the European Standards SIST EN 832.

The second area (2) presents the thermo visioned system for production, distribution and use of hot water (i.e. vapour) with a special use of a boiler. Figure 4 shows the thermovision record and appearance of the front part of the boiler, whose vapour is used for technological process in the production and heating the objects.

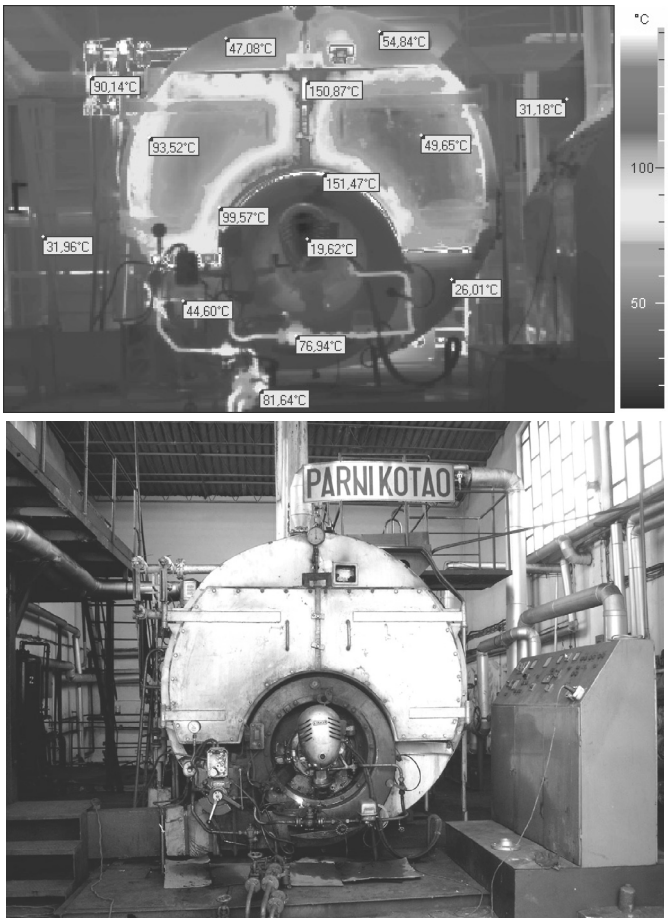


Fig. 4: *Thermovision/photo record of the front part of a boiler.*

Thermovision recording provides the efficient detection of the velave status, possible damage on tube isolation, present status of isolating surfaces on the boiler, as well as the proper functioning of a water cooling tower.

The third area (3) there was done thermovision check of the electricity distribution system. The efficiency of the thermovision check can be seen well in figure 5 which shows a switchboard with a detected anomaly active in one phase of charging (overheating of a safety device at temperature of 74.41°C).

The fourth (4) functional area shows the thermovision/photo recording as related to the production process (fig. 6). After consulting the experts in various fields some production line segments were defined. Thermovision/photo recording of the defined segments and the consequent analysis of the temperature profiles/ranges could optimize and embetter the production process.

Fig. 5: *Thermovision/photo record of a switchboard.*

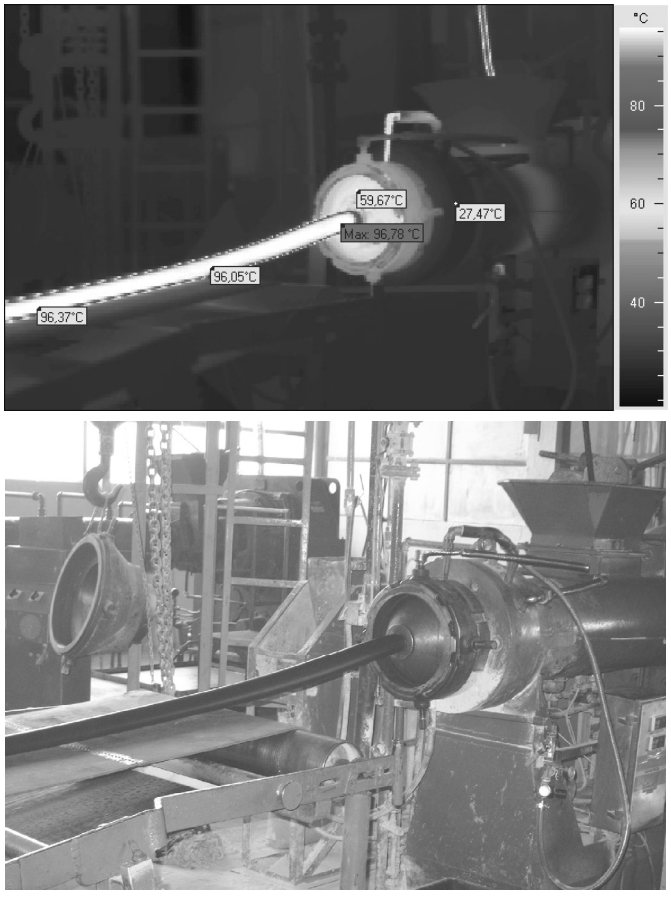


Fig. 6: *Thermovision/photo record of a machine for inner tyres production.*

The thermovision system, used in optimizing production process has to possess, besides necessary technical features, a convenient implemented software. The Varioscan 3021ST camera's software enables it to have a large number of optional functions.

The analysis of the processes mutually dependent on temperature (chemical, productive, technological, etc), which understands temperature as an important parametre, needs a thermovision system which can also have automatic functioning. This gives possibilities for pictures memorizing according to the given initial (starting) time and the matching time period during which the temperature status of a process is recorded. This function offers a possibility to follow the status of the process within a longer period of time. Time period is defined in such a way that optimal output data, show the nature and certain principality of the very process.

4. PLENARY ENERGY BALANCE

In nowadays industrial companies in developed countries, as well as in the countries in transition, the tendency exists to gain the control over energy usage, i.e. to enable an industrial company to identify and apply certain steps for reducing energy usage by using systems with various techniques.

The basic task of a management of an industrial company is to provide an energy usage control system, defining a programme of energy use, forming a team of experts, following characteristic parametres, accepting convenient suggestions, as well as doing a financing analysis.

The first step is to do a plenary energy balance which will be in fact an estimation of current energy usage of an industrial company or some of its premises; it will be done by using existing written records as well as by measuring some parametres within relatively short period of time at the characteristic points chosen in advance.

The plenary energy balance reflects which investment at a low and middle level could reduce significantly energy usage per product unit, so that energy usage reduce can be gained and paid out within a predefined period of time.

This programme realization understands a team of experts involvement which will be a continuous dealing with energy efficiency, defining regular and planned activities in reasonable energy usage, as well as defining ways of following characteristic parametres, etc.

The basic parametre which represents energy (or some other power resources) usage which is in the function of production process span shows a current status and it has to be compared to those in other similar industrial companies of developed countries. According to an overall analysis some steps get done for saving energy after some detailed reasearch and testing, necessary measuring, and using better monitoring of energy usage have been done. The final objective is to make the energy usage parameters reach those in the global energy usage standards, as well as to make production process more stable.

5. EXPECTED RESULTS

The main objective of this study is to implement a new thermovision method into an initial phase of working on plenary energy balances in industrial companies. A plenary energy balance is an immediate preview of energy usage of an industrial company or some of its premises based on the

available documents and a short-time measuring and checking in an industrial company, so the thermovision appears to be a very reliable device for checking, which enables analysts to get quite good results. Depending on set objectives, good results of this method application have been shown in the following fields:

- Energy efficiency improvement in industrial premises, as well as in buildings with thermovision detection devices, overall construction of heat losses, and production of adequate cards;
- Detecting potentially harmful elements in the systems of secondary net of remote control heating, or in the systems for vapour distribution used in technological processes and data base forming, based on thermovision method (Fig. 7);
- Optimal check of thechnological processes in the purpose of production process stability;
- Efficient detecting of potentially harmful elements in the systems for electricity supply and introducing periodical thermovision control devices for energy control and distribution.

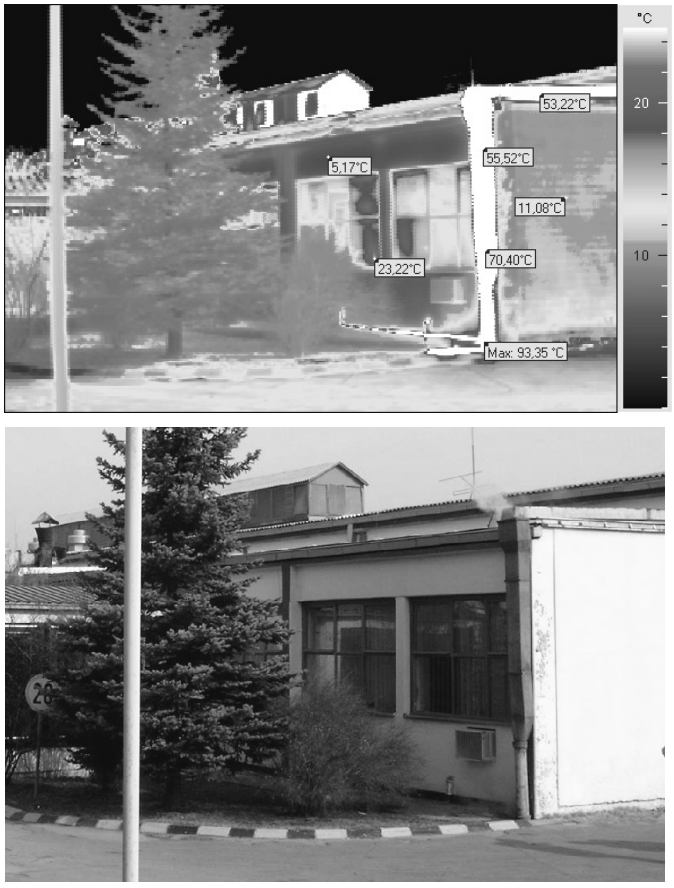


Fig. 7: *Thermovision/photo record of a building with losses in vapour distribution.*

6. CONCLUSION

A plenary energy balance shows in which of the investments of a low and middle level energy usage can be reduced in industrial companies. The thermovision method application in an initial phase of a plenary energy balance significantly reduces the measuring period as well as the time necessary for checking out at chosen points in industrial companies. A characteristic example shows four functionally connected areas on which the thermovision system has become dominant, enabling contemporary observing of current measuring parametres, while a forthcoming analysis of data and measuring results provide all necessary elements fo energy balance achievement.

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12-CHANNEL PC-BASED ELECTROCARDIOGRAPH

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Abstract: *PC-based 12-channel electrocardiograph for the stress and resting test is considered in this paper. It consists of an external module connected to the PC over the USB port and the Scope software application that runs under Windows XP OS. The module doesn't need battery or external 220V power supply since it gets 5V DC power supply directly from PC through the USB port. So, if notebook computer is used, this ECG diagnosis system becomes portable.*

Keywords: *Electrocardiograph, ECG amplifier concept.*

1. INTRODUCTION

An electrocardiogram (ECG) is the recording of electrical activity generated on body surface by the heart. Pathological changes and events in heart activity are detectable in electrocardiogram in advance - before they show some visual harmful effect [5]. ECG signal, in form of voltage potential, is collected by conductive skin electrodes placed at designated locations on human body [2]. The signal is characterized by a recurrent wave sequence labeled by successive letters of alphabet (P, Q, R, S, T and U), given in Fig.1.

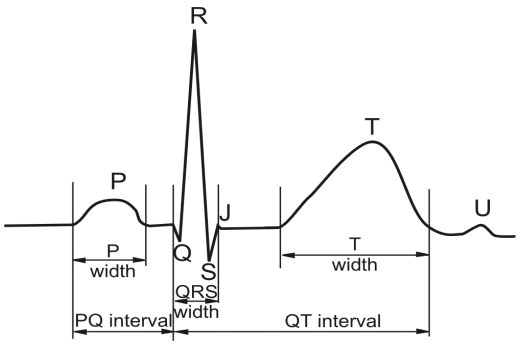

Fig.1: *Typical ECG wave with relevant features.*

The ECG signal shape and the time intervals (P width, PQ interval, QRS width, QT interval, ST-segment level and slope, etc, Fig.1) are significant for electrocardiographic diagnosis. Disorders in electrocardiogram reflects the fault heart functioning. But, these disorders often occur sporadically and cannot be seen in short term recording. They can appear in situations when patients are under some kind of physical or mental stress. Therefore, it is mandatory to perform ECG signals recording during the stress test.

PC-based 12-channel electrocardiograph for the stress and resting test is considered onward in this paper. Its concept is described first, and the circuitry that performs the analog-to-digital conversion, digital filtering and data streaming to the PC over USB are discussed after that. The associated new-developed software program named *Scope* is described also. Finally, the overall system functioning and use facilities are discussed.

2. ECG-PC 6/12B CONCEPT

ECG PC 6/12B is the 12-channel electrocardiograph for resting and exercise testing. Interfaced to the PC, ECG-PC 6/12b can record, display, archive, present and analyze ECG recordings. The ECG PC 6/12B system consists of external module connected to the PC through the USB port, and the *Scope* software application that runs under Windows XP operating system.

The module collects the voltage potential signals from patients skin over conductive electrodes. The standard 12 ECG leads (D1, D2, D3, aVR, aVL, aVF, V1, V2, V3, V4, V5 and V6) requuire 10 electrodes placed at designated points on the human body. Four of them (named R, L, F and N shown in Fig.2) are placed on the arms and legs and other six on the chest (Fig.3) [1].

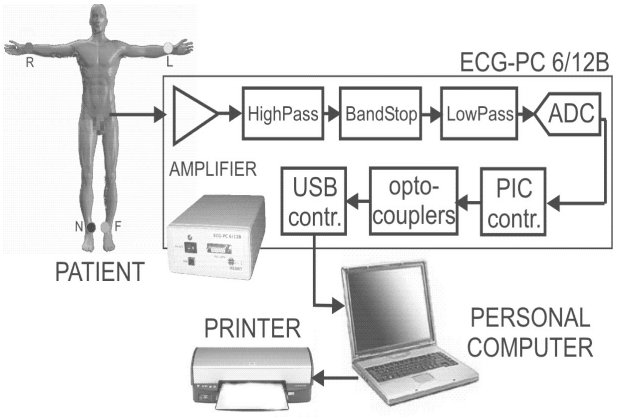

Fig.2: *Block diagram of ECG-PC 6/12B.*

The simplified block diagram of the ECG recording system is shown in Fig.2. Signals received from the electrodes are buffered and connected to the inputs of resistor network inside the module. Resistor network provides 12 ECG lead signals on its outputs - D1, D2, D3, aVR, aVL, aVF, V1, V2, V3, V4, V5 and V6. Besides, the resistor network provides the common-mode signal (the R, L, and F average signal) on one of its outputs. It is amplified by inverting amplifier and then connected to the neutral electrode N (shown in Fig.2). This applies an inverted version of common-mode interference to the patient's right leg, with the aim of cancelling the interference.

The module amplifies and filters the ECG leads signals. After analog-to-digital conversion has been completed, the microprocessor (part of this module) further processes the data in digital domain and then send the data to the USB controller.

The *Scope* software application receives the data sent over USB and displays the ECG signals on the PC monitor. Application has many advanced features of recording and analizing the ECG signals that will be further described in detail.

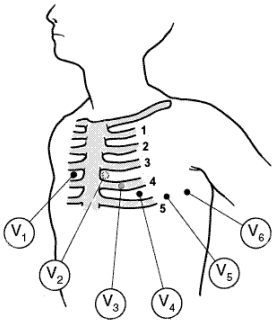

Fig.3: *Positions for electrode placement on the chest.*

3. ANALOG AMPLIFIER CIRCUIT CONCEPT

The analog part of the system must deal with extremely weak signals ranging from several μV up to 5mV. The useful bandwidth of ECG signals is 0.05Hz – 100Hz [1].

The ECG signal is combined with significant DC component which is several hundred times greater than the amplitude of ECG signal [2]. The DC component is caused by the contact between the electrode and patients skin and have to be eliminated with high-pass filters[5].

Beside DC component, ECG signals can be corrupted by various kind of noise [5]:

- power-line interference: 50Hz pickup and harmonics from power mains that are several tens times greater than useful signal;
- patent's respiration, motion artifacts and electrode contact noise cause variable resistance between the electrode and the skin that generates the fault beseline drift of ECG signals;
- muscle contraction adds fault signals that are mixed with the ECG signals. Frequency band of muscle contraction signals is a subpart of a band of ECG signals;
- electromagnetic interference from other electronic devices.

The main characteristics of ECG analog amplifiers can be sumarized as follows:

- frequency band at 3dB from 0.05Hz to 100Hz with the first-order high pass filter [1],[3],
- tolerance of DC input voltages (the level depending on type of the electrode),
- overall gain in range 200-1000 (46dB-60dB) with the maximal input signal of ± 5mV without output stage saturation [1],[3],
- differential input impedance is greater than 5MΩ in the entire frequency band [3],
- common mode rejection ratio CMMR> 80dB.

The analog signal processing chain (Fig.4) for one ECG signal lead amplification consists of three analog signal processing stages: front-end amplifier circuit with embedded high-pass filter, analog 50Hz band-stop filter, and back-end non-inverting analog amplifier circuit with low-pass filter. The total signal gain of amplifier is chosen to be 500.

The simplified block diagram of the first stage amplifier circuit is shown in Fig. 5. The differential input signal is buffered and then filtered by the first order high-pass filter consisting of resistors R1 and capacitor C1 [3]. The high pass filter cut-off frequency is chosen to be 0.05Hz.

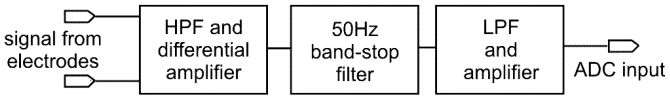

Fig.4: *Analog signal processing chain.*

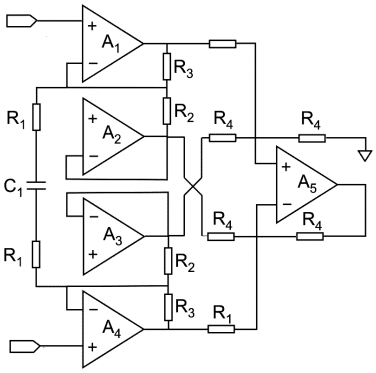

Fig.5: *The front-end amplifier circuit concept.*

The A1 and A2 amplifiers take one half of the differential input AC signal each and form the first amplifier [3]. The A3 and A4 amplifiers take the other half of the differential input AC signal and form the second amplifier. The gain of two differential amplifiers is given by following expression:

$$A_d = 1 + \frac{R3}{R1 \| R2} \quad (1)$$

The last stage of front-end amplifier circuit (consisting of A5 operational amplifier and resistors R4) is unity gain adder/subtractor circuit [3].

The front-end circuit amplifies both the ECG signal and 50Hz signal that is several times greater then ECG signal. To avoid amplifier output saturation, signal gain of the front end circuit (Ad) is chosen to be only 200. The A3, A4 and A5 operational amplifiers are selected to have low offset voltage, and A1 and A2 to have high gain-bandwidth product.

ECG derived from the skin surface bears frequency components up to a maximum frequency of 100Hz but the most of spectrum is concentrated below 40Hz. Therefore, 50Hz band-stop filter from the second stage (block given in Fig.4) has minimal influence on ECG signal shape. The second stage stop-band filter has unity gain.

The amplifier's third stage is non-inverting amplifier and low pass filter with cut-off frequency of 100Hz. The gain inside the pass band of the third stage is set to 2.5.

The analog circuitry is made of operational amplifiers and passive components (resistors and capacitors). Operational amplifiers are low power with 5V single supply.

The measured common mode rejection of analog signal processing chain ratio is nearly 100 dB.

4. DIGITAL SIGNAL PROCESSING

Analog signals are sampled with the frequency of 250Hz which is more than enough for ECG signal monitoring purpose [5]. AD conversion was performed by the converter with 12 analog inputs.

ADC provides 12-bit data resolution on its output. After AD conversion, digital samples are brought to the input of microcontroller. The serial communication block of the microcontroller transmits serial data.

Digital isolation is necessary for data transmission to the PC. The optocoupler with enough high transmission rate is chosen as digital isolator. Optocoupler's high maximal isolation voltage of 5000V satisfies the patient safety standards. Over its output, microcontroller provides serial data that come to the optocoupler's input. After digital isolation, data is fed to the input of FT232 chip, an RS232 to USB converter IC. USB data is then sent to the PC.

The power supply for the ECG PC 6/12B module is brought from PC over USB port. Not only the digital signals but also the power supply had to be isolated.

The patient safety standards demand the protection against the voltage difference between power mains (personal computer supply) and patient should be at least 4000V [1]. Therefore, DC-DC converter with the isolation voltage of 5200V is used for power supply isolation. It receives 5V input voltage from USB and provides 9V on its output. Isolated 5V supply, derived after the linear voltage regulator, is connected to the power supply inputs of analog and digital circuits of the ECG PC 6/12B module.

The total power dissipation of the analog and digital circuits inside the ECG PC 6/12B is 0.35W. The circuit consumes from USB port the current of approximately 70mA at 5V power supply voltage.

5. SCOPE APPLICATION

The software application named *Scope* is a comprehensive high-end application for both resting and stress cardiac testing. It runs under Windows operating system and has user-friendly graphical interface. Scope has been developed in Microsoft Visual C++.NET 2003 which provides the dynamic software development environment for creating Microsoft Windows–based and Microsoft .NET–based applications, dynamic Web applications, and XML Web services using the C++ object programming language [8].

Scope application provides plenty of useful features for recording and analyzing the ECG signals. The electrocardiogram is available on PC monitor. The doctor (program user), can use printer connected to PC to print recordings and analysis results. Also, the *Scope* provides database for ECG recordings storing. The complete resting and exercise test recordings and other useful information can be easily retrieved from database and shown on PC monitor. Also, the recordings can be sent over the internet in form of JPEG picture. *Scope* is designed to be simple and intuitive, and, because of this, ECG-PC 6/12B can be used immediately with minimal operator training. Main benefits of the Scope are:

- simple one key operation with dedicated icons and functions,
- records 12-channel electrocardiogram during both resting and exercise test and displays it on PC monitor in real-time,
- controls the whole exercise test process and sends commands over RS232 PC interface to digitally controlled bicycles and treadmills,
- ECG reports are printed by the printer that uses A4 paper format,
- data management system offers the ability to store unlimited number of recordings with full analysis.

The user interface for resting test is shown in Figures 6 and 7. ECG signals are displayed on the left side in the main window of the application. The amplitude of ECG waves in the main window can be determined by comparing with the grid made of horizontal and vertical lines. The distance between two consecutive grid lines corresponds to actual size of 5mm.

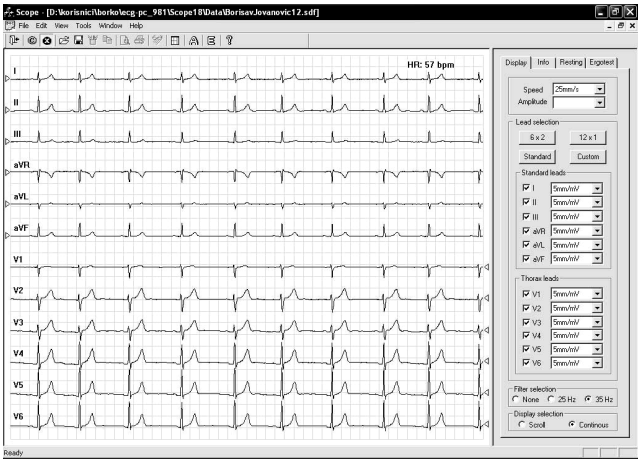

Fig. 6: *User interface during the resting test.*

In the main window, ECG signals drawing can be divided into one or two columns. When displayed in one column (Fig.6), the user of program can choose one of three possible values for time-base sensitivity 25mm/s, 50mm/s or 100mm/s corresponding to 10s, 5s or 2s time interval shown in one line on the screen. In the other option, shown in Fig. 7, time-base sensitivity values 25mm/s, 50mm/s or 100mm/s corresponds to time intervals 5s, 2s and 1s. The time-base value of 25mm/s is most frequently used; the other two values are useful for detailed signal analysis.

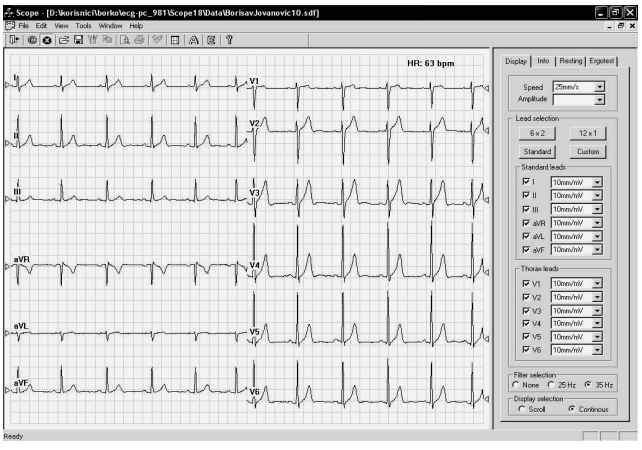

Fig.7: *User interface during the resting test.*

The size sensitivity of ECG signals can be set to one of three values 5mm/mV, 10mm/mV and 20mm/mV. The selected sensitivity can be applied to the all signals on the screen or to the only particular one specified by the user. Beside setting the sensitivities of time-base and size, the user can turn on and off particular leads and therefore setup the screen in his/her own manner.

During the exercise test, the patient rides the ergo-meter bicycle or walks on the treadmill. In the same time, the doctor is watching and analyzing the ECG signals on PC monitor. Usually, the test doesn't last longer than 20 minutes.

At the test beginning, patient is in resting state or runs the test under the minimal load (the ergo-meter bike is set to minimal load, or treadmill speed and elevation are set to minimal values). The load is gradually increased during the test. The test protocol defines the load values for each stage and the time moments when the load changes. At the end of the test, in the resting phase, patient stops riding the bike (or stops walking on treadmill) when the doctor analyzes the patient heart ability to rest. *Scope* supports standard cardiological test protocols for treadmill test: Bruce, Balke, Naughton, Ellestadt, Cooper, etc. Besides, the doctor can define his/her own protocols.

The user interface during the exercise test is shown in Fig.8. In the particular exercise test following ECG leads are chosen: D1, D2, D3, aVR, aVL, aVF and V5.

In the main window, above the ECG signals, the *Scope* provides three diagrams (Fig.8) especially useful to doctors:

- diagram of heart rate and load during the test related to time;
- trend graphs of amplitude and slope of ST segment (the part of the ECG signal relevant for detecting the ischemic heart disease) for leads D2 or V5;
- bar graphs showing the instantaneous values of ST segment amplitude and slope for all selected leads.

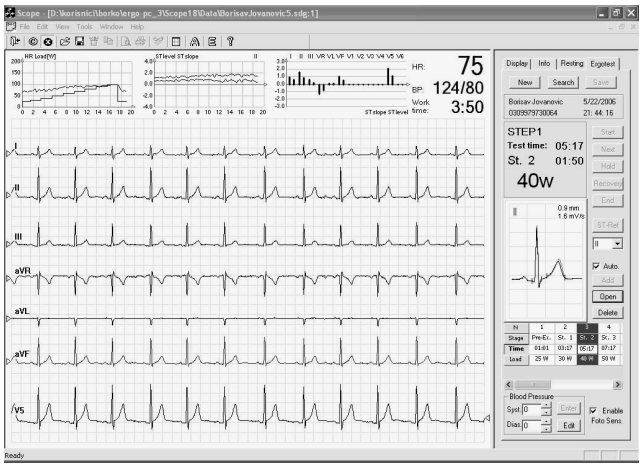

Fig.8: *The Scope application during the exercise test.*

Numerical values for current values of heart rate, blood pressure and time elapsed from the test beginning are showed on the right side, next to the graphs (Fig.8). During the test, blood pressure values are measured by external blood pressure meter and manually entered into application. *Scope* program automatically calculates heart rate values.

The control part of the window on the right side (Fig.8) provides control buttons for:

- searching the database for the desired record,
- storing the currently made record into database,
- test process control (starting, stopping, changing the load levels during the test),
- storing the current event into the exercise record (set of ECG signals currently shown in the main window).

During the exercise test, current signals (of lead D2 and V5) can be compared with the referent ones that are stored at the test beginning. After the test is completed, the program provides:

- trend graphs of heart frequency, load, ST amplitude and slope, table with important information gathered during the test,
- ST measurement results in a graphical format for every lead during the time-flow,
- comparison of average signals for all selected leads for all steps during the exercise test (Fig.9) with ST amplitude and slope values,
- complete ECG recording during the test for D2 and V5 leads.

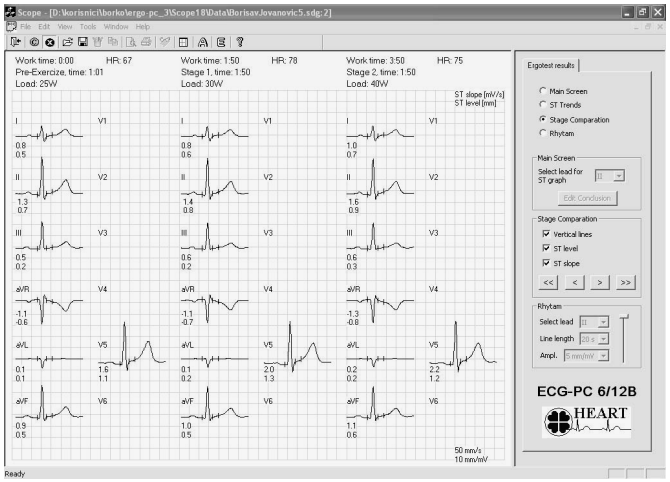

Fig.9: *Exercise test results - Stage comparison***.**

The window showing the analysis results for lead D2 is given in Fig. 10. The signal curve is given on the left side of window. The amplitude sensitivity is 40mm/mV and time base - 200mm/s.

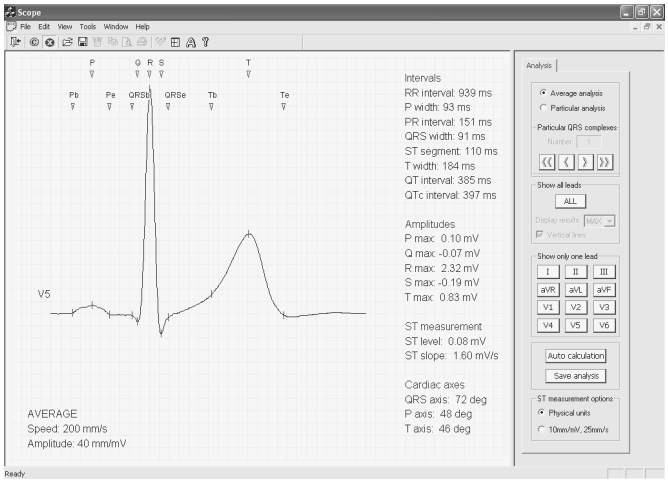

Fig.10: *ECG signal analysis for the lead D2.*

The *Scope* program automatically calculates the following ECG signal parameters:

- RR interval – the average time interval in milliseconds between two consecutive QRS complexes,
- P width – the average duration of P wave in milliseconds (Fig.1),
- PR interval – the average time interval between the beginning of P wave and the beginning of Q wave,
- T width – time interval between T-wave beginning and end (Fig.1),

- QT interval – the average time-interval between Q wave beginning and T wave end (Fig.1),
- QTc interval – normalized QT interval if the heart rate is 60 bpm. As the QT interval depends on heart rate, it is often converted to the normalized QTc. The conversion is according to Bazetts' formula:

$$QT_C = QT\sqrt{\frac{1000}{RR}}, \qquad (2)$$

- amplitudes of waves and peaks of ECG signals: P, Q, R, S and T.

The wave onset and offset vertical lines (for P wave, QRS complex and T wave) and wave peak lines (P, Q, R, S, and T peaks) are placed on the signal line The *Scope* program automatically sets the onset, offset and peak markers and calculates the time intervals and other parameters. Besides, it is possible to manually change the position of those markers. It can be done by moving the cursor line above the marker. All measured parameters are recalculated when cursor is released.

6. CONCLUSION

ECG PC 6/12B is a 12-channel PC-based electrocardiograph for resting and exercise testing. The ECG PC 6/12B system consists of external module connected to the PC through the USB port and the software application named *Scope* that runs under Windows XP OS. The communication between the ECG PC 6/12B module and the personal computer is achieved through the USB port. The module doesn't need battery or external 220V power supply. Instead, it gets 5V DC power supply directly from PC through the USB port. Therefore, installed on notebook computer, ECG diagnosis system becomes portable.

The software *Scope* is a comprehensive high-end application for both resting and stress testing. It has user-friendly graphical interface and many advanced features for recording and analyzing the ECG signals. Also, this software provides database for ECG recordings storing.

The electrocardiogram is presented on PC monitor and recordings and analysis results can be printed by printer connected to the PC. Whole exercise test process is controlled by the *Scope* software. Ergo-meter bicycles and treadmills are digitally controlled over RS232 port of the PC.

The proposed electrocardiograph has been evaluated at the Clinic for Cardiovascular Diseases - Niš, and the Institute for Prevention, Treatment and Rehabilitation of Rheumatic and Cardiovascular Diseases – „Radon" in Niška Banja. The evaluation has been carried out in period from April to September 2006. The algorithms implemented in the *Scope* were especially tested. The results of system testing are obtained using several hundreds different ECG records. The results show that the information about waveform shape is very accurate and useful for ECG classification and cardiac diagnosis. The measurements of clinically important intervals obtained using *Scope* program are comparable in accuracy with those obtained by human experts.

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GRID DATA MANAGEMENT WEB PORTAL

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Abstract: *The Grid Data Management Web Portal enables easy interaction with grid file catalogue using simple Web-based user interface. The paper describes the implementation of this portal and its features that facilitate integration with the other Web-based applications.*

Keywords: *Grid portals, Replica management, Logical file management.*

1. INTRODUCTION

The Grid represents a computing infrastructure which provides a scalable, secure, efficient and coordinated way of finding and accessing distributed resources. The resources can be storage devices, computational resources or any other device witch we can access and control over the network: telescopes, medical equipment etc. The coordinated access over shared distributed resources requires defining of the access rules and policies under which sharing occurs. The set of individuals and/or institutions defined by such rules and sharing some common interest form the virtual organization (VO). The grid users gain the rights to access the grid resources by becoming members of the virtual organizations.

The grid infrastructure consists of the following core elements:

The **User Interface** (UI) represents user's access point to grid services. The user connected to the UI can manage jobs running on the grid, perform data management operations, find information about available resources etc. The user can also develop the applications using the APIs provided on the UI.

The **Computing Element** (CE) has the queue of received user jobs. Every CE has Worker Nodes (WN) and a Local Job Management System (LJMS). The jobs from the queue are sent to WNs for the execution and the LJMS decides which WN should execute the job. The Storage Element provides the uniform interface for accessing storage devices. The SE enables copying replicas from one SE to another, accessing replica's contents and deleting. The replica is identified by its Storage URL (SURL). The File Catalogue maintains the mapping between the logical file names (LFN), their unique identifiers (GUID) and the replicas of logical files stored on SEs. The catalogue enables the user to find files by their logical names and organizes them into logical namespace. This way they don't need to know where the file actually physically resides, the catalogue will find the replicas for them. The Information Service (IS) gathers the information about the described elements of the grid, their state, characteristics and it tracks the statistic about submitted jobs. The Resource Broker (RB) is a scheduler which receives the job submission requests from the UI, looks up for the resources requested by job by querying IS and puts the job into the queue of the chosen CE.

1.1. Data Management on LCG-2

The Web portal described in this paper was developed and tested on LCG-2 middleware so the further description of the Grid services and functionality will refer to this environment. The LCG-2 middleware offers LCG File Catalogue (LFC) witch logically organizes files into a hierarchical namespace similar to classic file systems. Every grid file has its unique identifier – grid unique identifier (GUID) and its logical file name (LFN) mapped to file's GUID. Each logical file has one or more replicas on storage elements which represent physical location where the grid files are stored. The replicas are identified by its storage URL (SURL).

LCG-2 distribution offers CLI (Command Line Interface) data management tools and a few data management APIs for C/C++ and Python programming languages.

1.2. Data Management Web Portal

The data management provided with LCG-2 covers the most of the data management operations needed, but have some disadvantages. The command line interface provided by these tools is cumbersome and requires some time for learning. Some practice is required before a user becomes comfortable with its usage.

Furthermore, some commands can create inconsistency between catalogue entries and their mapping to replicas on storage element. For example, the lcg-uf command removes the entry from the catalogue but leaves file's physical representation on the storage element. Such lower-level command demand users with higher experience.

The access to the commands requires the user to establish the connection to a user interface computer via ssh or similar protocol, have an account on this computer, and have a grid certificate.

This paper describes a Web portal which enables grid data management trough simple and easy to use Web interface. The portal provides the following grid data management functions: directory browsing, copying and registering of new files to the catalogue, file deletion, as well as the replica management operations (download, replication and deleting). The Web portal's appearance and the set of operations offered to the user can be controlled using a configuration file.

The portal offers its users the ability to for manipulate the data on the grid without detailed knowledge about the underlying infrastructure and grid middleware. Its user interface provides an easy and fast way of performing data management operations both to the people who are using the grid for some specific usage related to their area of expertise and for the software developers and administrators, helping them to perform necessary data management operations faster and focus on other aspects of their work.

The portal can be used both as a standalone application or integrated into some existing Web application. It is implemented in Java, but since their interaction is implemented trough web server paradigm, as HTTP sessions, cookies and exchange of variables using HTTP request parameters, the integration is possible with the Web applications developed using other technologies, as PHP, ASP, ASP .Net, Perl and so on.

Any information about the available grid resources needed for operation of the Web portal, like obtaining of the list of storage elements is done transparently for the user by querying the IS.

The ability to perform data management from any remote computer using Web browser also solves one of the disadvantages of existing tools provided by LCG-2 which require execution directly from the UI computer using shell commands or low-level grid APIs. The access is possible from any computer with the internet connection and Web browser, without requiring installation of any additional software. On the other side, this kind of access demands to build in some security into our Web portal to ensure that only authenticated and authorized users can gain the access to data management operations.

2. SYSTEM ARCHITECTURE AND TECHNOLOGIES

The system consists of the client and server component. The server component is running on the UI while the client component can run on the same computer or any other machine connected to the UI via the network. The client computer needs a JavaScript enabled Web browser. The client/server communication is implemented via HTTP protocol.

The server component consists of the presentation layer and data management layer. The presentation layer communicates with the client, data management layer and also with other, third-party Web components, if the system is integrated with other Web application. The presentation layer also provides authentication and authorization of the clients accessing the server. The diagram displaying the architecture of the server component and the environment in which it runs is displayed in the *Fig. 1*. The white-colored blocks represent parts of server component, while the grey ones represent the remainder of the environment.

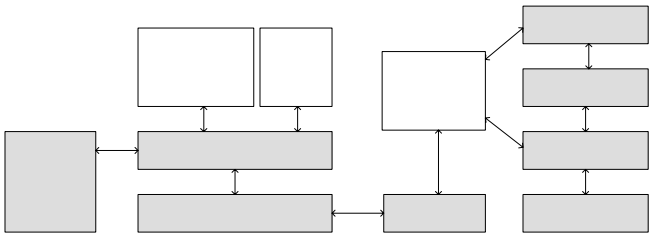

Fig. 1: *The architecture of server component.*

The presentation layer is implemented using Java Servlet/JSP technology. This technology is chosen because it provides an easy way of developing functionality needed for presentation layer, like acquiring of HTTP request parameters and upload and download functionality, simple management the appearance of user interface and good performance. Using this technology, the functionality provided by the system can be easily expanded using some of many available Java APIs and object oriented programming paradigm. Another important aspect of Java technology is its full portability as well as the large number of freely available high-quality integrated development environments.

Data management layer is implemented is developed using Java and C programming languages. At the time when the portal was developed there was no Java data management API for LFC - only available APIs were for C/C++ and Python. The data management layer therefore provides an interface implemented in Java witch communicates with presentation layer, while its implementation wraps LFC and LCG_UTIL C/C++ APIs via Java Native Interface. The LFC API is used for catalogue interaction and the LFC_UTIL API for file and replica management.

The client communicates with the server via HTTP protocol. The client component is run from the Web browser and displays the server's replies to user's requests. The client also implements parts of file upload and download functionality. The client executes Java Script that is used to validate users' requests and provides some error handling eliminating unnecessary network traffic between client and server and filtering server requests. The client can be run in any Java Script enabled browser, independently from the underlying operating system.

The presentation and data management layer of the server are implemented by Java packages webPortal and dataManagement. The dataManagement package implements grid data management functionality, while the webPortal package encapsulates the functionality of the presentation layer: saving of required temporary user data during session, authentication and authorization control, processing of portal configuration, communication via HTTP request parameters and interface to the dataManagement package. The grid package groups all the packages developed for running on a grid infrastructure. *Fig. 2* is a UML class diagram of the package dataManagement. *Fig. 3* is a UML class diagram of the package webPortal, while *Fig. 4* contains the class diagrams of the package webPortal.itemActions. The UML component diagram of the system is shown in *Fig. 5*.

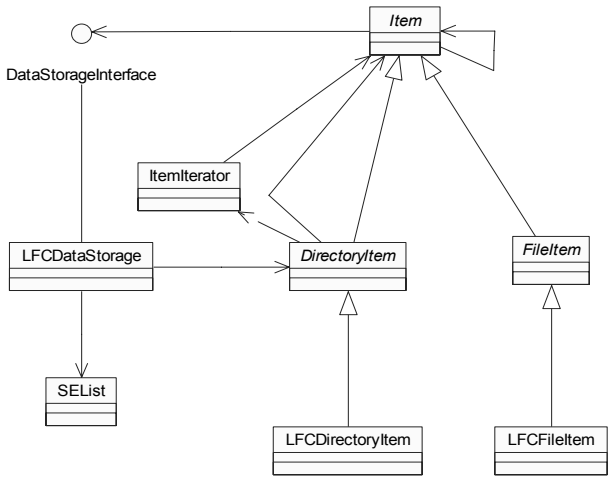

Fig. 2: *Class diagram of package dataManagement.*

3. SYSTEM USAGE

The tree key pages of the Web user interface are Data Management page used for browsing the grid catalogue and file selection, File Details page for the detailed information about the selected grid file and related data management actions, and Upload page for copying of files from the user's local file system and their transfer and registration on the grid.

When user comes to the portal, the Login page requesting authentication is displayed. After successful sign on, the user's identity is the kept for the duration of the web session. The details of implemented authentication and authorization will be discussed later.

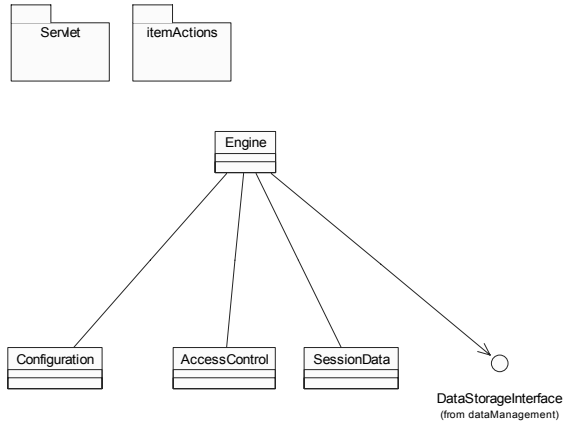

Fig. 3: *Class diagram of package webPortal.*

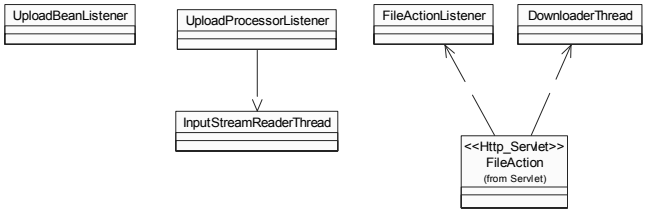

Fig. 4: *Class diagram of package webPortal.itemActions.*

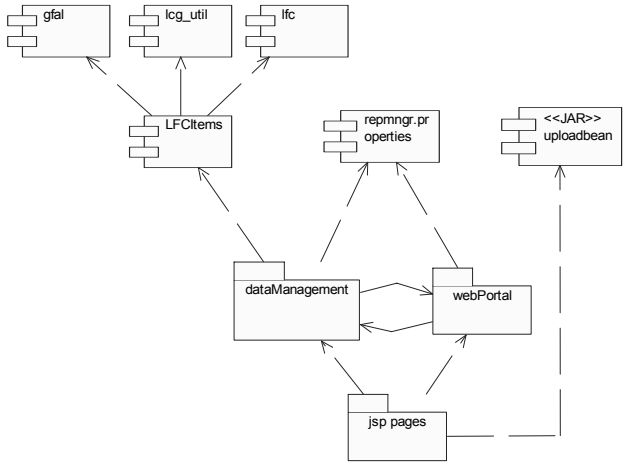

Fig. 5: *Component diagram.*

Data Management page consists of the main menu in the upper left part of the screen, the tree pane used for displaying grid catalogue structure and directory browsing, and the current folder contents, where files and subdirectories within the current directory are listed. The appearance and navigation options of this page are defined within configuration properties, while their availability also depends on user access permissions. The look of File Details page is shown in *Fig. 6*.

The main menu is displayed on every page and contains Data Management and Upload items for quick access to these pages, and the item Info leading to a page with information about the portal, its authors and usage. An optional custom menu item can be added by setting its title and link properties in portal configuration. The *Fig. 6* shows the File Details page with added custom menu item "Working Set".

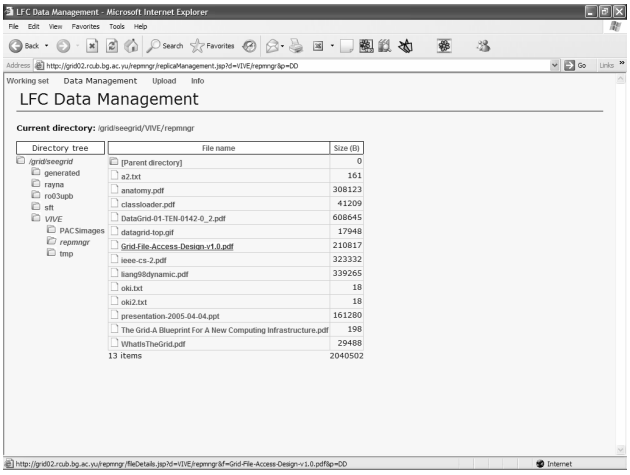

Fig. 6: *Data Management page.*

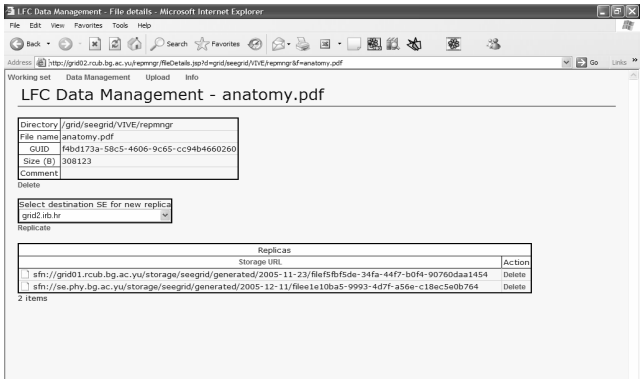

Fig. 7: *File Details page.*

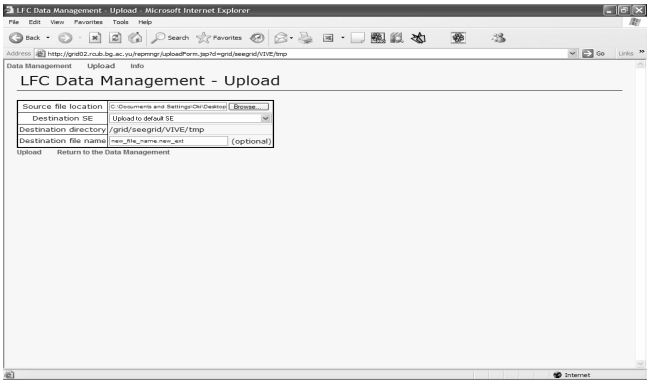

Fig. 8: *Upload page.*

File Details page shows the details of data management actions that can be performed both the selected logical file and its replicas (Fig. 7).

The actions that can be performed on the logical file are download (which opens the dialogue for saving or opening the file in user's Web browser), deletion of all file replicas, deletion of single replica, and file replication to a selected SE.

The actions that can be performed on a replica are downloading to the client computer and replica deletion. If replica deletion fails, the user is offered to unregister the replica from the catalogue without removing it from the SE. This option is only meant to be used for replicas that cannot be removed from SE due to some error.

The Upload page is used to upload files from the client's local file system to the grid and register them in the LFC catalogue. The page consists of main menu and the upload

form for selection of file to be uploaded, destination SE where a replica is to be created, and the logical grid directory and file name to be used when registering the file.

The upload functionality supports optional additional file processing after upload. The uploading and registering of a file to the grid has two phases: uploading of the file from the client computer to a temporary location on the UI, and copying and registering of the temporary UI file to the grid. The user can use the portal configuration to specify that the file on UI should be processed by a custom script or executable program. If the processing ends successfully, the resulting file will be sent to grid instead of original one. If the processor exits with an error, the content of its *stdout* and *stderr* streams and executed command are shown to user through the Web interface so that he/she can find the cause of error.

The authentication and authorization mechanism used by portal has two layers: the one using security infrastructure of underlying grid middleware and the other at the Web application level.

Every LCG-2 user, host and service has a X.509 certificate. During every transaction, both sides are mutually identified using these certificates. Since the portal is executed on an application server and uses Java VM, every data management operation request from the portal users will be mapped to the Linux user corresponding to the application server. This user needs to have a valid proxy certificate in the order for data management operations to work.

The users' names and passwords for accessing the portal are stored in its configuration (properties) file. When the user tries to access the portal for the first time in during the HTTP session, he/she must authenticate by providing a username and password. After successful login, the user information is stored until the end of the session. This portal-level access control can be disabled in portal configuration. This option is useful if the portal is integrated with some other web-based application, inheriting its authentication and authorization mechanism.

The set of data management operations offered to user can be also defined by using the portal configuration parameters. For example, using upload functionality can be forbidden to some user or user access can be constraint to the specific set of directories.

3.1. Configuring the portal for integration with other Web applications

The portal's appearance and some aspects of its functionality can be defined using the configuration file. The adjustment of its configuration can be very useful if the portal should be used integrated into some other Web application.

The Web front end of the portal uses cascading style sheets (css) defined in a corresponding file. This enables us to easily modify its appearance.

The data management operations can be also executed by sending the HTTP request with the correct set of parameters to the portal. For example, to delete the file we would send the HTTP request containing the target file name and data management operation type.

The HTTP request parameter can be also used to choose the portal's configuration file to use when processing the request. This enables us to use different configuration on the same instance of the Web portal and to dynamically switch its configuration.

4. CONCLUSION

The ability to manipulate data on the grid using the Web based user interface gives the users an easy and fast way of performing required data management operations even for the users who don't have high level of experience in using this infrastructure.

The thin Web client enables the user to perform data management operations on the grid from any computer with the internet connection and Web browser, without requiring installation of any additional software.

The developed Java data management API uses the advantages of the object oriented programming paradigm, offers high level of portability, easy code refactoring and reuse. The API can be easily integrated into existing programming systems written in Java or it can speed up grid application development by providing them with data management functionality.

The Java data management API provides the interface to the data management operations and its implementation for the interaction with the LFC catalogue. By writing another implementation of the provided interface the API can be expanded to support other grid catalogues or even other versions of the grid middleware.

The ability to configure the appearance of the Web portal, choose the set of data management operations offered to user and request data management operation via HTTP interface makes the integration with other Web applications easy. The concept of the upload processor gives us the possibility to expand basic upload functionality.

4.1. Planned improvements and long term goals

The long term goal of the project would be to implement the Web portal supporting full grid data management functionality covering both the simple operations and the complex ones like recursive directory copying. The portal should have high level of portability, supporting more grid middleware projects and hardware architectures. The portal should also be highly flexible and configurable to support easy integration and to meet user's needs.

Planned improvements include further development of the Java data management API by adding additional data management operations and by its integration with the data management APIs provided by new versions of the grid middleware. For example, the API can be integrated with FTS API, used for reliable scheduled transfer of replicas.

The Java data management API should also have more precise error information, explaining the cause of the operation failure, for example: "communication error", "invalid credentials", etc.

The list of available storage elements is currently stored in a file and the user has to manually perform the updates. This list should be obtained automatically by querying the IS. This functionality is already supported by the newer versions of the Java data management API but the support is needed by the presentation layer of the portal.

The authentication and authorization mechanism of the portal should fully rely on the underlying grid security infrastructure. The users should be authenticated and authorized using their proxy certificate. The user should also be able to create and destroy his/her proxy certificate from the Web portal by entering the pass phrase.

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SOFTWARE BASED GSM NETWORK CALL PERFORMANCE INDICATOR

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Abstract: *The practically realized technical solution of software for monitoring and measurement of traffic quality on signalization connections, based on signalization number 7 (SS7) and ISUP protocol, between of two gateway nodes of the Mobile switch and the Telecom transition switch in Banja Luka is described in the paper. The goal of the solution is to resolve by own resources the problem for monitoring of services quality, key indicators of network performances, monitoring of network by traffic directions and time, and alarming in cases when the service quality drops under predefined level. The solution is based on PC platform and standard software tools. The need and importance for solution of monitoring and indication of service quality in mobile GSM network is pointed out first. Then the practical solution of given software-based indicator of traffic performances in mobile GSM network is described in more details. Some results obtained by using of described indicator are also shown.*

Keywords: *GSM, KPI, Call Performance, PostgreSQL, Java*

1. INTRODUCTION

GSM networks in phase 2G+ consist of access network part with base station subsystem (BSS) and base station controler (BSC) and central switching part (core network). Switching subsystem is divided into circiut switching subsystem (voice and standard ISDN services) and packet switching subsystem (GPRS subsystem). Other subsystems (as IN, SMS, MMS) are connected to core network [1,2].

Statistics measurements are sufficient for network planing and for global overview of traffic in network. However, for network surveillance in real time it is needed system for monitoring signaling system number 7 (SS7) [1,2]. SS7 monitoring system enables to survey quality of service (QoS), gives possibility for troubleshooting and for traceing of call flows (call trace for one certain call or mass call trace). Monitoring system for SS7 signaling network covers all interfaces and protocols in GSM network. System is collecting signaling messages from all interfaces by passive metod and after that performs decoding of messages and store decoded signaling data in database. Many applications (Call Trace, Protocol Analysis etc.) are using decoded signaling data from database. Also there is possibility for development of new applications on the existing platform. This possibility is used here for developing of application software for analytical processing of data previously collected and decoded on aquisition system, so called Key Performance Indicator (KPI) for certain traffic case. It is used SS7 monitoring system MasterQuest for monitoring and observation. [3]. It consist of hardwer part (aquisition system and system for data storage) and software part (Oracle database, applications software, web server, etc). Architecture of the system is shown in Fig. 1.

In Fig. 2 it is shown principal scheme of connection between mobile gateway switches (MSC) and international PSTN exchange, with marked points of aquisition of signaling data. VLR (visitors location register) is dinamic database with date of all visitor subsribers in this MSC/VLR area. HLR (home location register) is database of home PLMN subscribers (own subscribers) .

Each traffic case (eg. call from mobile to PSTN) that is happend on measurement points (Fig. 2) is described by record ISUP CDR (CDR – Call Data Record). Every such record consists of more fields that describe traffic event (eg. time of event, calling party number, called party number, call duration, signaling paths, etc) [3]).

Data from aquisition servers that describe traffic event between MSCs and international exchanges are stored in database of aquisition system. Every 5 minutes aquisition system generates csv text files this with data, and this data are interface for developing third party applications.

That generated file is source of data for additional processing and for new applications on existing system. Acess to acquisition MasterQuest server with data is possible and performed with ftp protocol which is used for file transfer into our software subsystem for SS7 monitoring.

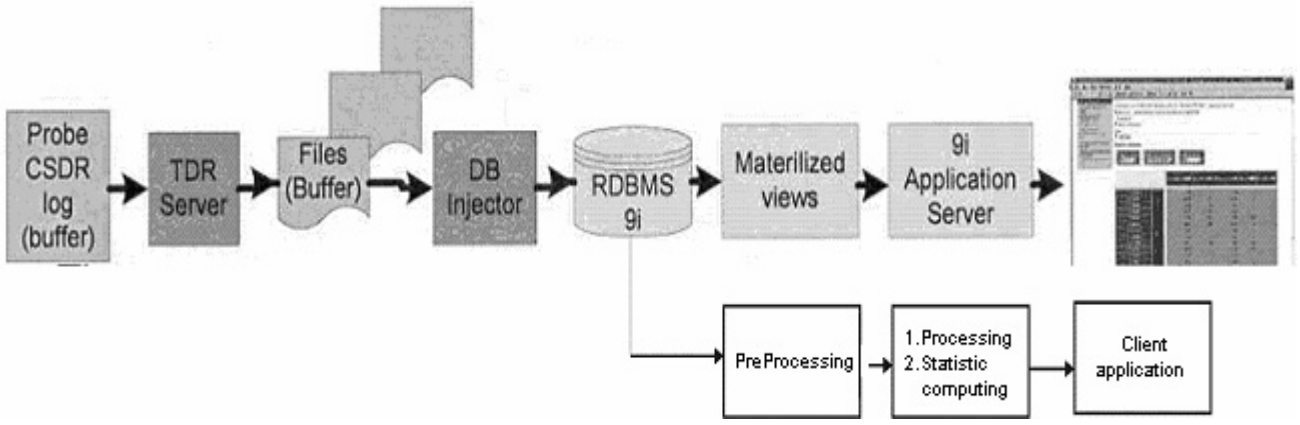

Fig. 1: *Acquisition system architecture with marked of additional KPI module.*

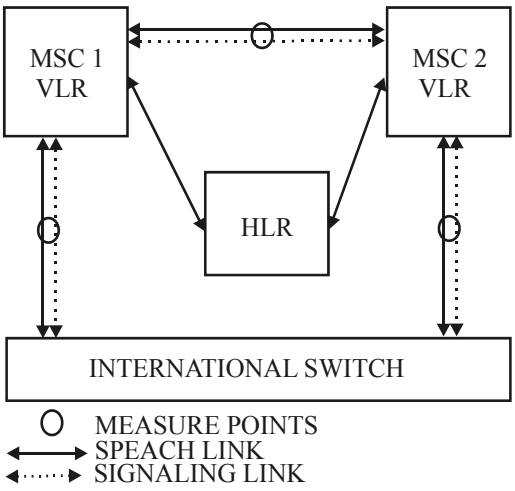

Fig. 2: *Basic network infrastructure diagram with main network signaling and speech wiring and measurement points.*

2. SOLUTION DESCRIPTION

Software subsystem that was practical developed is functionaly divided into two parts: database and subsystem for backend data processing, and user graphic interface.

Database and subsystem for backend processing of data consists of database, server procedures on database and batch data processing which is under control of operating system on server. Within the scope of this part also exist archiving of files with report definitions, system configuration files, etc.

Graphical User Interface is client application developed as J2SE desktop application [4]. This solution contains all functions that are concerning with display, printout, process management, alarm definition, archive searching with results and initiating of action. Also this part is responsible for administration user accounts, update of index and define of user accounts. Practicaly obtained desktop of user graphic interface for realized application is shown in Fig. 3. In Fig. 3 are shown temporary values of data for choosen call prefix. The system was practicaly developed for local usage, so all texts in panels and reports are given in local (Serbian) language.

2.1 Client application

Client application consist of main menu in what is performed call of respective module, and of forms for presentation of current traffic state.

Basic modul contains presentation of traffic state on choosen prefix pair (Fig.3). This modul gives possibility that for choosen prefix can be monitored real signaling traffic for choosen direction for next parameter:

- Sucessful call No, Unsucessful call No, Total CDR amount and Sucess percentage.
- Conversation time.
- Holding time.

All this data on the form are refreshed automatically. Refreshing period is 3 minutes, and it is possible to decrease on increase this period. Refreshing feature is realized using software threads and is independent for every form.

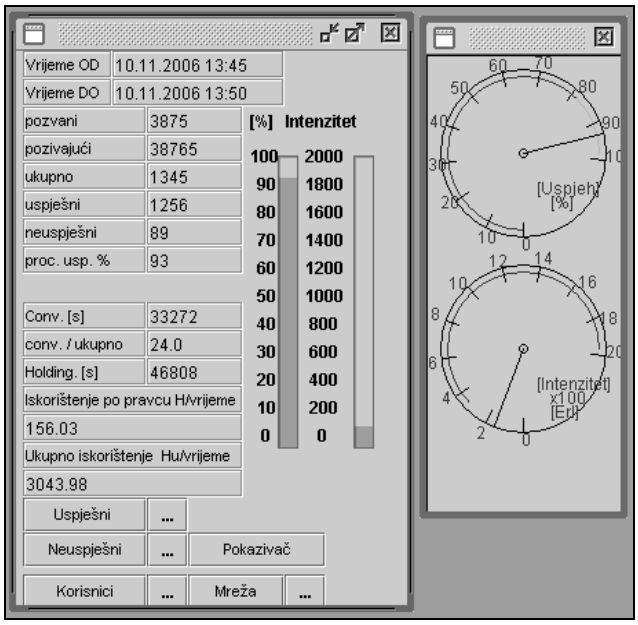

Fig. 3: *Client application panel. Presentation of current traffic information based on chosen prefix direction.*

Client application funcional modules are also:

- Active alarm display module. It is based on alarm level setting and preview form. (Figs. 4, 5 and 6).
- Traffic analyse prewiev module and printing capabilities.
- Administration modules, user permissions, user accounts and security.
- Archived traffic statistic preview module with searching, printing and graphics bar preview capabilities.
- Graphics User interafe settings modules. (look and feel settings)

2.2 Database and background data processing

This part is functionally divided on system for archiving of data together with predefined procedures for data processing and active (batch processing) files for automatic initiation of process on system. Used database is Open Source database PostgreSQL version 8.0.1. [5]. Advantage of this choice is: PostgreSQL is modern database in public ownership (General Public License). It is possible to run that database on Unix-like operating systems and also on Windows 2000 and XP platform. PostgreSQL has procedural language pg/plsql that is made like Oracle PL/SQL language and has many similar matters. All programmers that are familiar with Oracle PL/SQL could easy use pg/plsql for development. In development phase it is used distribution of PostgreSQL for Windows OS. In operational phase it is installed distribution of operating system Fedora Linux that is covered with GPL license, i.e. in public ownership.

This module has more software parts.

Preprocessing program

Preprocessor perform decoding of data in raw file which are not suitable for further processing and change it into format suitable for processing. Preprocessor also performs prefix analyze of calling and call party number.

Result of preprocessing action is preprocessed file with new extension that is stored in directory for preprocessing files as it is described in configuration file.

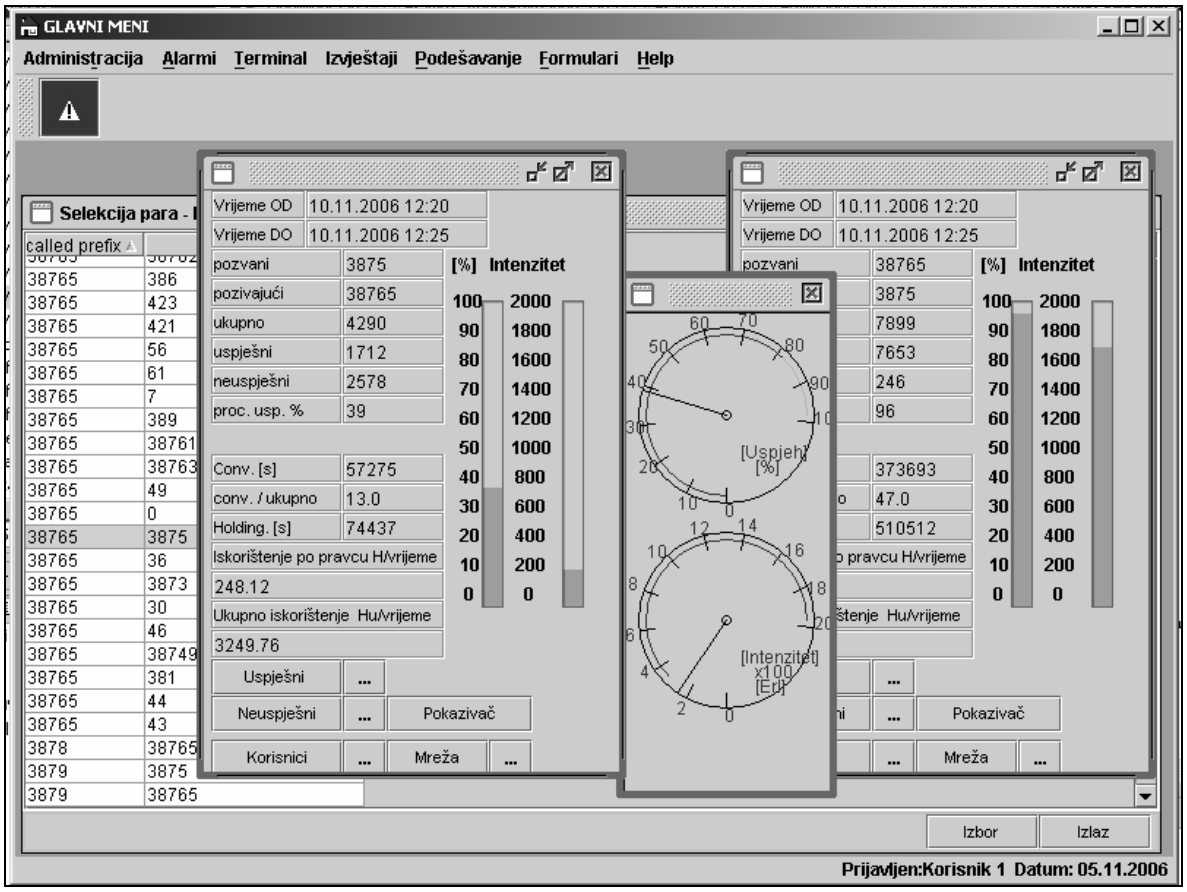

Fig. 4: *Alarm definition preview and handling form.*

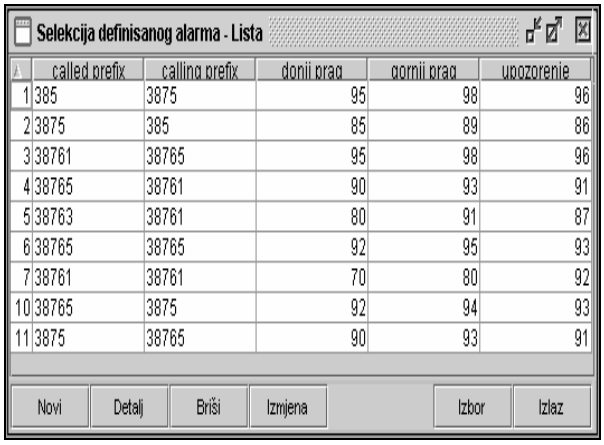

Fig. 5: *Alarm definition preview and handling form.*

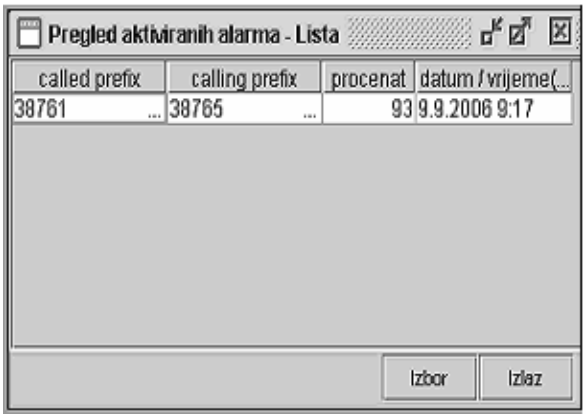

Fig. 6: *Active alarm preview and handling form.*

This program performs function of adjusting row files into files with appropriate format for further processing, i.e. import into database. Source files are coming from MasterQuest server and represent SS7 signaling traffic on point of measurement in system. In this concrete case this is triangle consisted of international PLMN exchange and two gateway MSCs of MOBIS-Telekom Srpske mobile network, and all traffic cases on ISUP protocol on this interfaces are covered. File is standardized in accordance with technical specifications given in [1,2].

Tasks of preprocessor are to perform decoding of data in source file what are not in format suitable for further processing into format adapted for further phases of processing, and to perform prefix analysis of calling and called numerations that are contained in it. As a result of this program it is obtained preprocessed file marked with new extension. The file is put into folder for preprocessed files, as it is defined in file for configuration.

Inside of this phase is practicaly implement error detection in the file and in format of data. All fields inside of record which have some errors are moved into error file, that is on server in folder for batch processing, in accordance with specification from configuration file. In preamble of error file there is line with name of originating file and error code. After preprocessing is performed result is write into control log file of preprocessor. Flow diagram of actions performed during preprocessing is shown in diagram in Fig.7.

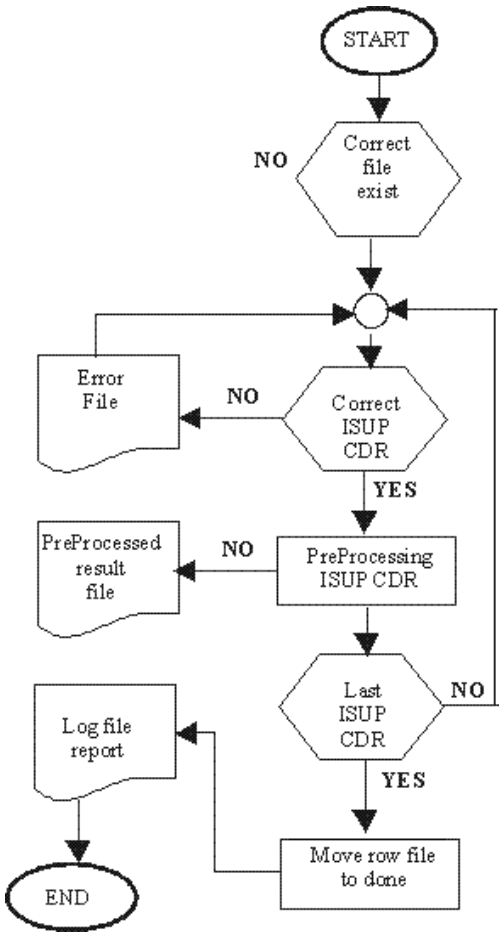

Fig. 7: *Preprocessing action algorithm.*

Processing program

This program imports data from preprocessing unl file into database. Time for processing of the biggest files (about 2 Mb) is around 1 minute. After execution of processing result of processing is written into log file Proc.log. Processed file is moved to directory for processing files following specification in configuration file. Flow diagram of actions performed during processing is shown in Fig.8.

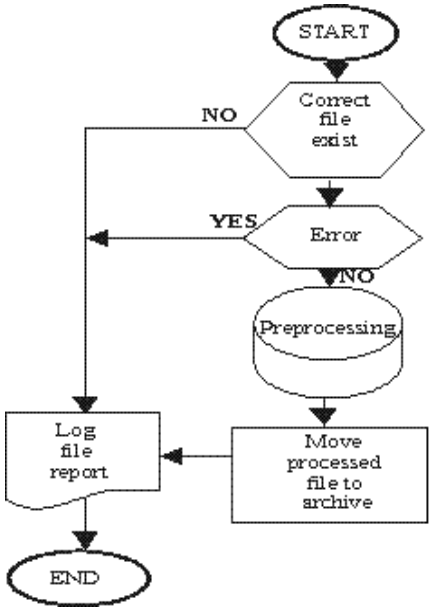

Fig. 8: *Processing action algorithm.*

Generating of statistics results

This program performs loading of tables for archives of statistics results and temporary tables for store of data for display. That process is executed once per day on predefined time on system process of operating system that starts this process.

Mechanism for deleting of data

This program deletes all time expired data. The process is performed once per day in predefined time on system process of operating system that is responsible for starting of this process.

Set of procedure for initiation of action

These procedures are in form of batch files. Operating system initiates batch files. There are four type of batch processing:

- Initiating of ftp transfer of new raw file. This procedure is done every 5 minute.
- Initiating of preprocessing.
- Initiating of processing.
- Initiating of aggregation on long time period.

In following text are denominated obtained capabilities and performances of the system:

- Archive of all daily data on 3 day level for operational use.
- Archive of all aggregated data on daily, monthly and annual level. Period of saving aggregated data on system is from one month to one year depending of data type.
- User-friendly display of actual analytic data.
- Form type list for set query on table of imported CDR with detailed CDR.
- Opening temporary index tables on level of array that are in CDR tables.
- Form type list for display and search of defined alarms. Enter of new alarm, change and delete of existing alarms.
- Menu for generating reports.
- Export of generating reports in basic file formats (pdf, Excell,..)
- Mechanism for deleting of data from database after planing time interval for saving data expire
- List for display of analitic data with possibility for searching data.
- Possibility of generating adaptive alarms which could be activated on change of state in aggregated data.

Backup of data is performed on database level with using scripts for activation.

Output results

There are two types for display output data that are realised in the program. First type is diplay direct from form which is implemented inside of program. Second type is via generated reports for display and print.

Reports are divided per type of information. First group consists of key performance indicators of network. This type sould be presented in pseudoreal time with possibility to set up parameters of query (type of calling or called prefix, time interval, etc). Second group consists of call statistics to certain destinations taking into consideration call originating, time of call setup, call duration and release cause (data are aggregated on hour and daily level). Some examples of practicaly generated reports are shown in Figs. 9, 10 and 11.

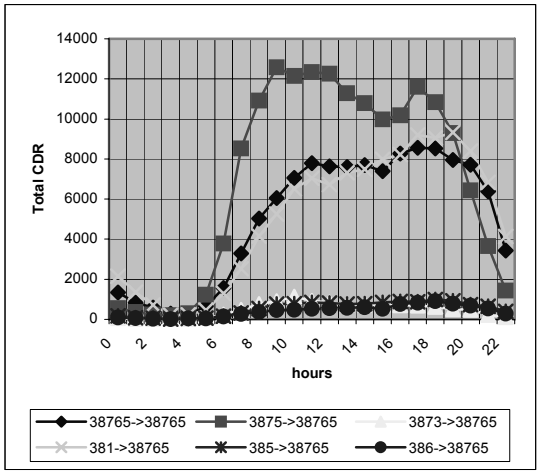

Fig. 9: *Comparative diagram of successful calls distribution.*

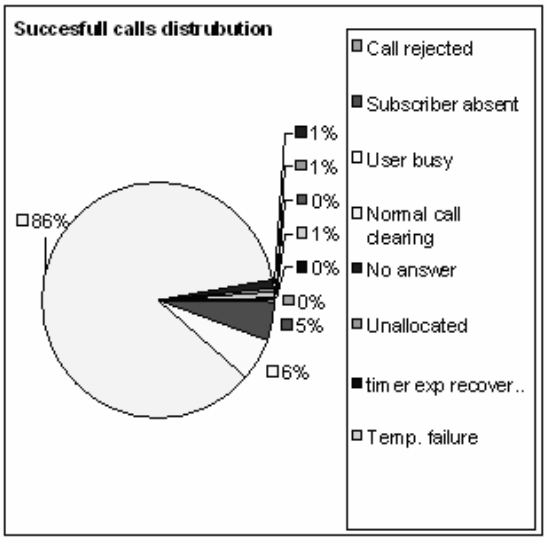

Fig.10: *Graphics diagram of successful calls distribution (similar one for unsuccessful calls).*

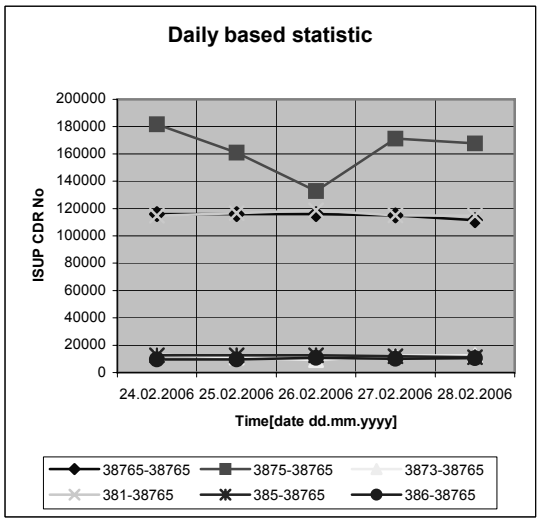

Fig. 11: *Comparative diagram of daily-based statistics.*

For practical realisation of described system it ware used next appropriate hardware and software platforms and appropriate database and develpoment tools.

Hardware and operating sistem platform:
Siemens – Fujitsu Primergy server

- Processor P3 1 GHz, dual, RAM 512 Mb DDR SDRAM, PC 3200, HDD 40 Gb SCSI hard discs RAID 5 architecture
- OS Fedora Linux Core 4

Database and development tools:

- PostgreSQL rdbms 8.1.1 [5]
- Java Desktop Apl. for client application and batch processing. (J2SE 1.5) [4]
- Oracle JDeveloper 10g, Java develop environment
- Jasper Reports, Report generator [6].

Open Reports, develop environment for generating of reports.

3. CONCLUSIONS

Described software key performance indicator (KPI) in GSM network is practicaly realized and it is in operational function from June 2006. Results obtained from real network and with real traffic cases are very good and useful for network surveilance and troubleshooting in pseudoreal time conditions and for every day operation and maintenance jobs. Goals that ware set up in begining of system development are completely reached in practice. Whole project was realized with own resources and without any additional investments.

With this solution is achieved possibility to generate listing of traffic events that ware generated on signaling level. It includes successful and unsuccessful calls and events. This is new possibility that is not covered with classic billing records that have not included unsuccessful traffic events that are important considerable for measuring and monitoring in telecommunications. Also, this solution in a way is solved some of problems of maintenance. It is open for eventual future additional development.

Possibilities for further development and upgrade of this solution are first of all conected with verification of billing files and upgrade of system with new reports on traffic quality (measurement of number of very short conversation duration calls, for example less than 10 sec, and very long duration calls, for example more than 30 minutes). That would be very useful for marketing purposes, giving possibility for detailed analysis and creating new strategies, subscriber user groups, traffic models and tariffing models.

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TAKE BACK CONCEPTS AND END-OF-LIFE MANAGEMENT OF POWER ELECTRICAL COMPONENTS

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Vančo Litovski, Faculty of Electronic Engineering, Niš, Serbia

Abstract: *Electrical equipment became the most frequent product at all and, accordingly, from the sustainability point of view, they are the most hasardeous ones. Recycling materials and components that constitute the nonfunctional and obsolete electrical devices become the most secure and cheapest strategy of managing at their end-of-life. In that way, puting-away of power electrical devices offers new oportunities in reuse of row materials and components, and effectively protects the environment. In the same time, substantial reduction of cost related to disposal are avoided. In this paper we consider the power electrical components as environmetal risk and review the take back procedures in order to get the ones that will be most convenient for application in local communities.*

Keywords: *End-of-life, componets, power electronic.*

1. INTRODUCTION

Obsolete electrical equipment represent hasardeous waste being risky for the environment and human helth. If disposed without processing they become a threat. The European Union (EU) and its member states have concerns about the disposal of solid wastes due to limited space available for landfills. In the year 1999, the European Commission produced a Directive according to which demands are set that in the year of 2015 the amount of domestic hard waste is to be reduced to only 35% comparing with the amount disposed in 1995 [1]. By 2001 restriction on discharge of liquid waste, explosives, corrosives, oxidizers, flammables and infectios human and animal waste will be baned.

Having all these in mind, effective management of the end-of-life of a electrical equipment, becomes an important social and business activity that encompasses take-back, dismantling, recycling, reuse, neutralization of toxic materials and disposal of the rest in a sustainable manner. Among these activities, crucial part is the collecting-back or take-back in societies and communities where no stringent regulations and environment protective tradition exists. Organization of the service and share of responsibilities are of crucial importance. Here we consider the case where no recycling exists at all. This, however, by no means makes the take back senseless. Collecting the hazardous waste is the first step that, we think, will get the picture of the problem and press towards successful recycling and safe disposal.

In the next we consider the problem of take-back first. Than we go trough existing praxis including an overview of the status in Serbia. Finaly we consider take-back schemes and discuss structure and applicability.

2. TAKE-BACK OF ELECTRICAL EQUIPMENT

The awareness of the problems stated above by the whole society and specially by governemental institutions, we consider, is of paramount inportance for setting up of solutions. Among these the take-back is of greatest importance originating from the fact that it needs participation of several subjects generally not connected among themselves and being not interested to do something for the solution. The municipal and governemental authorities are, accordingly, expected to play the fundamental role in the subject. In the next we will go through these considerations in more details.

2.1 Who is responsible

There are different oppinion on who is the most responsible in the take back scheme including the activities that are following it in the end-of-life management of the electrical and electronic products. The European Union considers the electrical equipment production industry responsible for supporting this activity in several respects. First, it is expected that sustainable design of electrical products to be implemented in order to avoid hasards at the end-of-life. Having this in mind it puts the financial responsibility on the producers. They are expected to manage the end-of-life including reuse of components and materials. Technologies of recycling are expected to be developed in the design phase of the product. It is expected the price of this activities to rise the production costs for about 1 to 3% of the retail prices of the electrical and electronic products comparing with avoiding any recycling and reuse.

Extended Producer Responsibility (EPR)

The concept of Extended Producer Responsibility (EPR) [2] is based on considerations that the responsibility, that the waste generated during the production processes could be taken care of in a proper way, from an environmental and resource-saving point of view, should primarily be of the manufacturer. Before the manufacturing of a product is commenced it should be known how the waste which is a result of the production process should be treated, as well as how the product should be taken care of when discarded.

This concept was first introduced in Sweden in 1979 and was related to aluminium cans for single-serve beer and soft drinks. It is estimated that, thanks to the requirements of this legislations, more than 90% of these products are taken back when obsolete.

While there are many definitions of EPR, it is generally described as a pollution prevention policy that focuses on product systems rather than production facilities. Thus responsibility for product is broadened beyond the emissions and effluents generated by the extraction or manufacturing processes to the management of the product once it is discarded.

The ultimate goal of EPR is sustainable development through environmentally responsible product development and product recovery. The following basic types of EPR may be recognized:

- *Liability* - producer is responsible for environmental damage caused by the product in question
- *Economic responsibility* - producer covers all or part of costs for collection, recycling or final disposal of products he manufacturers, and may charge a special fee

- *Physical responsibility* - manufacturer is involved in physical management of the products or of the effect of the products. This can range from merely developing the necessary technology, to managing the total "take back" system for collecting or disposing of products he has manufactured for which he may charge a fee
- *Ownership* - producers assumes both physical and economic responsibility
- *Informative responsibility* - producer is responsible for providing information on the product or its effects at various stages of its life cycle.

It is important to note that take-back schemes generally combine both economic and physical responsibility.

In order to ERP to be implemented there are three categories of policy instruments that can be initiated by government to encourage product responsibility.

- *Regulatory Instruments:* mandatory take-back; minimum recycled content standards; secondary materials utilization rate requirements; rates and dates; energy-efficiency standards; disposal bans and restrictions; materials bans and restrictions; and product bans and restrictions.
- *Economic Instruments:* advance disposal fees; virgin materials taxes; removing subsidies for virgin materials; deposit/refund systems; and environmentally preferable products procurement.
- *Informative Instruments:* seal-of-approval types of environmental labelling (Green Seal, Blue Angel); environmental information labelling (energy efficiency, Chlorofluorocarbon (CFC) use, recycled content); product hazard warnings; product durability labelling.

3. SOME EXEMPLES OF MANAGING AT THE END-OF-LIFE

3.1 Fluorescent lamp

Over the past few years, state and federal regulations in the USA concerning fluorescent lamp disposal have become increasingly complex, affecting a wide range of US businesses. Fluorescent lamps and high intensity discharge lamps contain a small quantity of mercury. Concerns over mercury releases to the air and water are driving stricter disposal regulations.

Mercury is an essential ingredient for most energy efficient lamps. Fluorescent lamps and High Intensity Discharge (HID) lamps are the two most common types of lamps that utilize mercury. Fluorescent lamps provide lighting for most schools, office buildings, and stores. HID lamps, which include mercury-vapor, metal halide, and high-pressure sodium lamps, are used for street lights, floodlights, and industrial lighting.

A typical fluorescent lamp is composed of a phosphor-coated glass tube with electrodes located at either end. The tube contains mercury, of which only a very small amount is in vapor form. When a voltage is applied, the electrodes energize the mercury vapor, causing it to emit ultraviolet (UV) energy. The phosphor coating absorbs the UV energy, causing the phosphor to fluoresce and emit visible light. Without the mercury vapor to produce UV energy, there would be no light.

A four-foot fluorescent lamp has an average rated life of at least 20,000 hours. To achieve this long life, lamps must contain a specific quantity of mercury. The amount of mercury required is very small, typically measured in milligrams, and varies by lamp type, date of manufacture, manufacturing plant, and manufacturer.

If lamp life is shortened, more lamps must be purchased to achieve the same length of service, and the number of lamps that generators must dispose will increase.

Based on a 1999 NEMA (The National Electrical Manufacturers Association) [3] survey, the average four-foot fluorescent lamp contains about 11.6 milligrams (mg) of mercury. This number has been steadily declining over the last 15 years as lamp manufacturers work to reduce mercury content to the minimum amount technically feasible without reducing lamp life, as depicted in Fig. 1. According to data from the U.S. Department of the Interior, the lighting industry has reduced its use of mercury from 57 tons in 1984 to 32 tons in 1997. This represents almost a 50% reduction in mercury usage despite increasing use of mercury containing lamps. The average four-foot lamp today contains over 75% less mercury than the same lamp would have contained in 1985. Because of the significant energy savings, however, using high efficiency fluorescent lamps to replace incandescent lamps or older fluorescent lamps results in additional net reduction in mercury emissions.

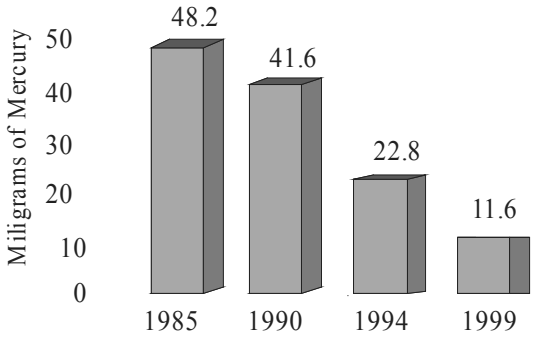

Fig. 1: *Mercury contained in four-foot fluorescent lamp - industry average.*

From the other side, mercury is a common pollutant emitted from power plants burning coal, oil, or gas. As we see in Fig.2 [4], Hg from fluorescent lamp disposal is small compared to the Hg released from power generation required to operate the lamp. Accordingly, incandescent lamps contain no mercury but result in the highest Hg emissions. For many years, EPA considered mercury-containing lamps to be ordinary municipal solid waste that generators would dispose of along with everyday garbage. In 1990, EPA revised the test it uses to identify a hazardous waste (the Toxicity Characteristic Leaching Procedure or “TCLP” test). Under this new test, many spent mercury-containing lamps failed and were classified as hazardous waste.

3.2 Transformer

Recent surveys indicate that the average age of utility power transformers exceeds 30 years. Managing the life-cycle of these critical assets requires monitoring the factors that cause transformer damage. Excessive heat and mechanical stress during through faults on transformers are recognized as the two major causes of damage. New technology in transformer protection relays provides for both thermal and through-fault monitoring. Many electric utilities and large industrial, commercial and institutional owners of medium and large power transformers are beginning to develop their own "Life Cycle Transformer Management" programs [5].

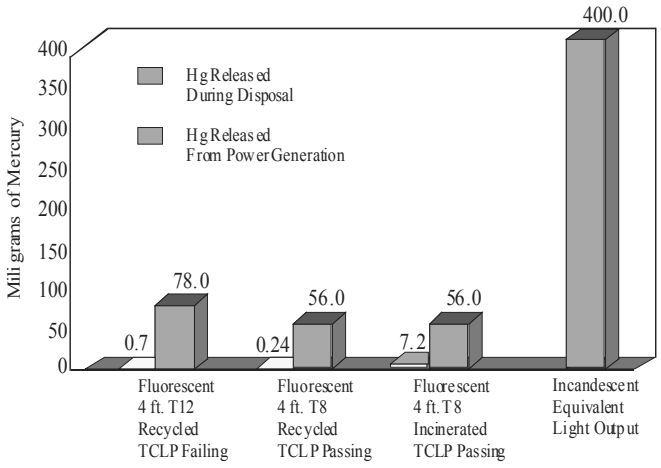

Fig. 2: *Lifetime Hg emissions.*

Measurable indicators of transformer serviceability include electrical load; top-oil, hottest-spot, and ambient temperatures; fault history; and dissolved gas analysis. Utilities that use these indicators can make intelligent profit/risk decisions and plan optimal transformer loading and maintenance.

The best way to protect and extend the life of transformers is to collect information such as load and fault current as well as top-oil or hottest-spot temperatures, and receive notification when a value has reached a preset level. Logically combining these quantities can help predict or anticipate an alarm condition, and keeping a record of these measurements provides a more complete picture of the transformer's insulation condition.

The challenge is providing a means to collect this information without creating a massive new system requiring its own maintenance and cost structure. Protective relays that are permanently connected to the transformer current (and possibly temperature inputs) have memory and recording capability, and have logical decision making capacity, can be the beginning of a comprehensive "life management" system for transformers.

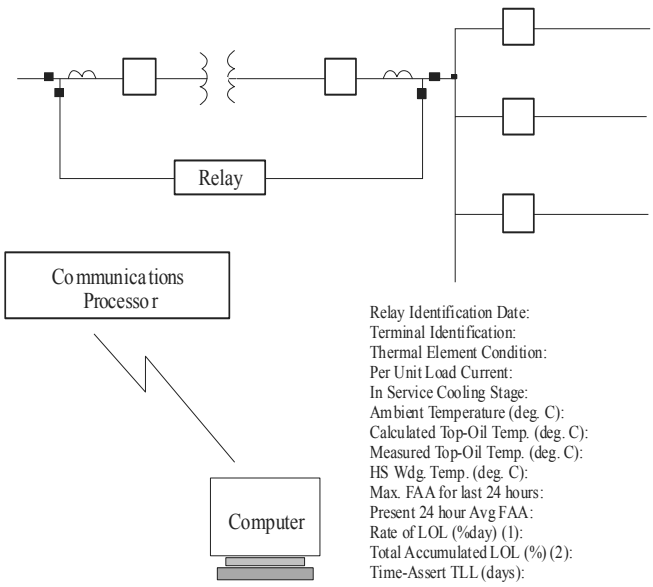

Fig. 3: *Using a communications processor to send a formatted report.*

It is not enough that data on overall loss of life exist inside a relay. It must be transmitted to a person who can use the information to improve decision-making and better manage the transformer asset. The simplest way to send data is to assign an alarm contact to a certain loss-of life level. The problem is that this takes away the additional intelligence that may be available, as discussed in previous sections. Using a communications processor to send a complete report to a responsible engineer is a way to send more useful information (Fig. 3).

With more complete information, the engineer can assess the degree of risk associated with continuing with the transformer in service under the same conditions or performing maintenance. Combining multiple reports-such as thermal, through-fault, and online dissolved gas analysis- can give the best view of the conditions within the transformer.

4. THE STATE-OF-THE ART IN SERBIA

There are many reasons why the situation related to e-waste management in Serbia is different comparing to the developed world. First of all, the absolute quantity of the obsolete (and non-obsolete) equipment and appliances is smaller. Then, thanks to lower leaving standards again, the criteria for an equipment to be pronounced obsolete are less restrictive. In other words, the life of the equipment is extended beyond usually expectations. From the other side, however, the uncontrolled import of used equipment being almost at end of life in the period just after the NATO Campaign in 1999 against Serbia, led to practical shortening the average life time of electrical and electronic equipment in Serbia. To prevent further negative trends on April 19. 2004. [6] governmental restrictions were imposed on the import of used computers, for example. For now, that is the only effective measure aimed to reduction of E-waste.

Note that, to our knowledge, there are no demanufacturing facilities for electronic equipment in Serbia. Furthermore, there is no awareness of the importance of the problem and the need for emergent solutions.

A specific aspect should be considered when discussing the subject of take-back of components and devices not produced in Serbia. Accordingly no EPR is applicable. The EPR have to target different subjects. Among them we recognize the importers and the government.

The wholesale importers of electrical equipment in Serbia may be seen as producers being the one that first have the product. They are the only ones having direct contact to the original producer. Having in mind that, however, the possibility to force the real producer to take back (import) the obsolete device is negligible, we come to the conclusion that the importer is the only one to be targeted by the EPR.

Of course, the Government while issuing import licenses is to share the responsibility with the importer. At this moment, to our knowledge, the following measures are planned to be implemented by the Serbian Government [6]:

- Creating an action plan for management of the e-waste according to the EU regulations.
- Prevention of waste production by implementation of cleaner production, reduction of dangerous properties of the waste and introduction of European standards for reduction toxic substances (such as heavy metals, for example). Encouraging the recycling. Introduction of methods and tools for evaluation of the

environmental indicators and evaluation of the life cycle of electronic products.
- Establishment of a complete scheme and a system for e-waste management from the moment of take back until disposal.
- Establishment of an information system describing the e-waste.
- Development and implementation of economical instruments (such as subventions, taxes and similar) for encouraging proper waste management and preventing waste generation and improper disposal.

Note that no take-back strategy is mentioned. It is our opinion that take-back is a crucial step for the start of any treatment and, accordingly, much more attention should be paid to this activity by the Government. Here, not only regulations but concrete actions for implementation of the regulations are expected to be undertaken.

5. TAKE-BACK PROGRAMS

Here we will try to make a short overview of the implementation of existing take-back concepts in the USA and in Europe, to look for the experience accumulated, to make comparisons, and try to get conclusions and recommendations applicable to domestic circumstances.

According to [7] the following are to be the prerequisites and needed action for a successful take-back campaign:
- Identify a common format for data collection for materials and cost;
- Evaluate and aggregate existing collection and demanufacturing materials and cost data sets;
- Identify common opportunities and barriers for different collection and transportation models;
- Define the advantages and disadvantages of different collection and transportation models;
- Identify commodities that are most viable economically (positive revenue) for collection and
- demanufacturing;
- Identify successful motivators and strategies for marketing collection events;
- Identify key issues and motivators for various groups that have or may participate in electronic
- equipment collection including consumers, local government officials, small businesses, recyclers,
- demanufacturers, shippers, etc.;
- Identify data gaps and infrastructure needs to increase residential participation; and
- Analyze what motivates the public to participate in collection events.

5.1 One of the possible take back schemes

The EU's approach, known as EPR in policy circles, creates incentives for manufacturers to reduce the environmental impacts of high-tech products throughout their life cycle. Instead of issuing regulation for an industry in constant flux, the EU has set clear goals for electrical and electronic products collection and recycling and has given the industry flexibility in how it meets them. Rather than trying to make law catch up with technology, the EU is making the technologists catch up with the code.

The first European Union directive on e-waste, requires producers to take responsibility for the entire life cycle of their products. By 2005, companies will either have to take back products directly from consumers or fund independent collectors to do so. Waste that was generated prior to the enactment date will be the responsibility of all existing companies, in proportion to their market share. Future waste is to be the individual responsibility of each company, thereby creating an incentive to redesign products for easier and safer recycling and disposal. No e-waste will be allowed in municipal waste streams. The public will be able to return e-waste without charge.

The second directive phases out the use of key toxic materials by 2006, including lead, mercury, cadmium, hexavalent chromium, and the brominated flame retardants (polybrominated diphenyl ether) PBDE and (polybrominated biphenyl) PBB.

Intensive research was supported in order to evaluate different models for implementation of various phases of e-waste management [7].

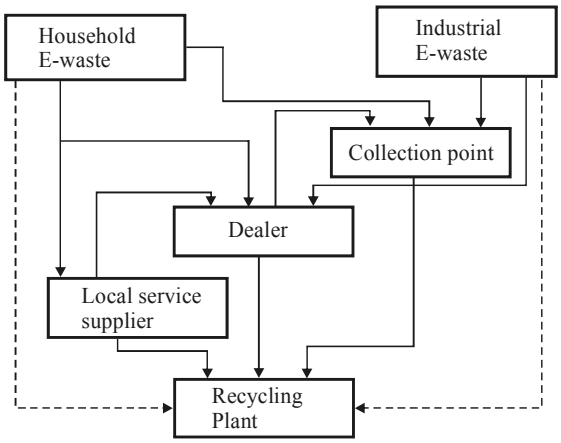

Fig. 4: *Collection system of E-waste.*

Fig. 4 depicts one of the possible take back schemes advised in [8]. The hart of the system is the so called collection point. It is accessible directly by both households and industrial product users. In the same time, however, the equipment dealer has access to it. It is not a simple matter to decide who is to be the owner of the Collection point. Should it be the dealer, the municipality or an independent proprietor? Note that Collection point is necessary if refurbishing, dismantling and other reuse intended activities are expected. Accordingly, for products supposed to be of no use an opportunity to be transported directly to recycling plant is allowed.

The implementation of any scheme as well as the one depicted in Fig. 4, to our opinion, asks for at least tree actors besides the governmental/municipal participation. These, would be the organizer, the Collection point and the Recycling plant. No such actors are sought in Serbia at the moment. That may become a serious obstacle for implementation of any such scheme.

6. CONCLUSIONS

The importance of the organization of take-back of electronic and electrical equipment as a crucial step in creating condition for implementation of recycling technology is considered. We consider some power electrical components as environmetal risk and review the take back procedures in order to get the ones that will be most convenient for application in local communities.

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INSTRUCTION FOR AUTHORS

Name of the author/s, Affiliation/s

Abstract: *Short instruction for authors is presented in this paper. Works that are to be printed in the review "Electronics" should be typed according to this instruction.*
Keywords: *Review Electronics, Faculty of Electrical Engineering in Banjaluka, Instruction for authors.*

1. INTRODUCTION

In the review "Electronics", we publish the scientific and professional works from different fields of electronics in the broadest sense like: automatics, telecommunications, computer techniques, power engineering, nuclear and medical electronics, analysis and synthesis of electronic circuits and systems, new technologies and materials in electronics etc. In addition to the scientific and professional works, we present new products, new books, B. Sc., M. Sc. and Ph.D. theses.

In order to enable the unification of the technical arrangement of the works, to simplify the printing of the review "ELECTRONICS", we are giving this instruction for the authors of the works to be published in this professional paper.

2. TECHNICAL DETAILS

2.1. Submitting the papers

The works are to be delivered to the editor of the review by the E-mail (elektronika@etfbl.net) or on floppy (or CD) by post mail to the address of the Faculty of Electrical Engineering (Elektrotehnicki fakultet, Patre 5, 78000 Banja Luka, Republic of Srpska, Bosnia and Herzegovina).

2.2. Typing details

The work has to be typed on the paper A4 format, 8.27" width and 11.69" height (21.0x29.7 cm), upper margin of 1" (2.54 cm) and lower margin of 0,59" (1,5 cm), left and right margins of 1,57" (2 cm) and 0,39" (1cm) (mirrored margins). The header and footer are 0,5" (1.27cm) and 57" (2 cm). The work has to be written in English language. Our suggestion to the authors is to make their works on a PC using the word processor MS WORD 97/2000, and for the figures to use the graphic program CorelDraw, if the graphs are not going from the original programs, i.e., from the programs received (like MATLAB).

The title of the work shall be written on the first page, in bold and 12 pt. size. Also, on the first page, moved for one line spacing from title, the author's name together with the name of his institution shall be printed in the letter size (10pt, *Italic)*. The remaining parts of the manuscript shall be done in two columns with 0.5cm distance. The work shall be typed with line spacing 1 (Single) and size not less than 10 pt (like as this instruction). After the title of the work and the name of the author/s, a short content in English language follows, written in italics. The subtitles in the text shall be written in bold, capital letters of the size as in the text (not less than 10 pt.). Each work shall, at the beginning, comprise a subtitle INTRODUCTION, and, at the end, the subtitles CONCLUSION and BIBLIOGRAPHY / REFERENCES.

The operators and size marks that do not use numerical values, shall be written in common letters. The size marks that can use numerical values shall be written in italics. The equations shall be written in one column with right edge numeration. If the breaking of equations or figures is desired, those may be placed over both columns.

Illustrations (tables, figures, graphs etc.) may be wider than one column if necessary. Above a table there shall be a title, for instance: Table 2. *The experimental measuring results.* The same applies to figures and graphs but the accompanying text comes underneath the figure of graphs, for instance: Fig.3: *Equivalent circuit diagram...*

The work should not be finished at the beginning of a page. If the last manuscript page is not full, the columns on that page should be made even. Number of pages should not go over 6.

3. CONCLUSION

This short instruction is presented in order to enable the unification of technical arrangement of the works.

4. REFERENCES

At the end of work, the used literature shall be listed in order as used in the text. The literature in the text, shall be enclosed in square brackets, for instance: ...in [2] is shown ...

ELECTRONICS, Vol. 10, No. 2, December 2006.

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