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Guest Editorial

THE 15h International Symposium on Power Electronics - Ee 2009 was held in Novi Sad from October 28-30, 2009. It was co-organized by Power Electronic Society (Serbia) located in Novi Sad, Faculty of Technical Sciences from Novi Sad, Institute "Nikola Tesla" from Belgrade and The Novi Sad Fair.

IEEE Serbia & Montenegro Section and IEEE Joint Chapter IES/IAS/PELS, Serbian Academy of Science and Art (SANU), Ministry of Science and Technological Development of Republic of Serbia, Provincial Secretariat for Science and Technological Development of AP Vojvodina and Engineering Chamber of Serbia sponsored it.

This significant event, dating back to 1973, showed constant interest of researchers, university professors, engineers, manufacturers, students and other experts in the field of Power Electronics and related disciplines. It is well known by its abbreviation Ee, which signifies "Energetska elektronika" (Power electronics in Serbian) and where capital letter "E" resembles to energy, power and strength, while lower letter "e" signifies low power, control and regulation.

The first gathering of the Ee, was held in Belgrade in 1973 with 47 presented papers from all over ex- Yugoslavia. Next conferences were in Belgrade in 1975, with 50 papers, in Zagreb in 1978, with 94 papers, in Sarajevo in 1981 with 95 papers, Ljubljana in 1984 with 104 papers, in Subotica in 1986, with 126 papers and in Belgrade in 1988, with 109 papers. After a long pause, due to unfortunate events in ex-YU, Power Electronics has been revived in Novi Sad. It has re-started in 1995 as a symposium in collaboration with the Novi Sad Fair, as an event during the traditional International Fair on Electronics and Informatics, with 79 papers. Next symposiums were held in Novi Sad in 1997, with 98 papers and in 1999, with 82 papers.

Significant participation of foreign authors resulted in upgrade of the symposium into International one, which in Novi Sad in 2001 gathered 107 papers, in 2003 101 papers, in 2005 93 papers, in 2007 101 papers and in 2009 105 papers.

The Ee 2009 International Symposium presented the papers from various institutions of 19 countries (Bosnia & Herzegovina, Bulgaria, Canada, Croatia, Czech Republic, France, Germany, Iran, Italy, Republic of Macedonia, Montenegro, Netherlands, Poland, Romania, Serbia, Spain, Switzerland, United Kingdom and USA) and gathered more than 200 participants. All papers were published in electronic form (CD-ROM), containing facts about Power Electronics Society, as well as complete bibliography from all symposiums on Power Electronics (1973-2009).

The symposium highlighted the problems and practical or virtual solution in many fields. Seven topics were put forward: Power Converters, Electrical Drives, Electrical Machines, Control & Measurement in Power Engineering, Power Electronics in Telecommuni-cations, Power Quality and Renewable Energy Sources.

The 15th International Symposium on Power Electronics continued the best practice of introducing a new topic – this time it was Renewable Energy Sources. For the 5th time the student's competition "Hardware & Software 2009" was organized. The novelty is special edition of the past proceedings of Power Electronics Symposiums in the period of 10 years, from 1997 to 2007. That provided significant insight into development in the field of Power Electronics at the turn of the Millennium, during the past decade and an important overview for the new authors and symposium participants.

The selected papers presented in this issue give an overview of the best contributions of the Ee2009. The first 5 papers were the invited ones. The first presents a historical look on the major power electronics component – thyristor, which is now in its sixth decade. The second is giving power electronics application in electrical automotive industry, the most propulsive one at the moment. The third is presenting for the first time the new real-time digital simulation tool for rapid development of power electronics systems. The forth and the fifth ones represents ecological consideration and improvements in energy efficiency, the topics of great interest, too. The remaining 16 papers represent the most interesting contributions of all topics, the state-of-the-art of power electronics in many world well known research institutions.

The selection of the papers is the guest-editor's choice and only one of several possible. We would like to emphasize our thanks to the authors and all participants of the Ee2009.

We would also like to invite all readers of the »Electronics« journal to take active participation by submitting the papers or attending the next 16th International Symposium on Power Electronics - Ee 2011, which will be organized in NOVI SAD, SERBIA in November, 2011 (http://www.dee.uns.ac.rs)

Guest Editor:
Prof. Vladimir Katić, Ph.D.
Chairman of the Program Committee

Short Biography of the Guest Editor

Vladimir Katić is a Professor and Vice-Dean in the Faculty of Technical Sciences at the University of Novi Sad, Novi Sad, Serbia. He joined the Department of Power, Electronics, and Telecommunication Engineering, Faculty of Technical Sciences, University of Novi Sad, in 1978. He has been Head of the Power Electronics and Converters Group, since 1992. From 1993 to 1998, he was the Director of the Institute of Power, Electronics and Telecommunication Engineering and, since 1998 he has been the Vice-Dean of the Faculty of Technical Sciences. He established the Laboratory for Power Electronics in 1991 and the Laboratory for Renewable & Distributed Electrical Energy Sources in 2007.

The main areas of scientific interest and research of Prof. Katić are power quality, power electronics converters, renewable energy sources (wind and solar) and standardization in electrical engineering.

Prof. Katic is a Senior Member of the IEEE, the Chair of the IEEE Serbia and Montenegro Section, the Chairman of the IEEE Joint Chapter of the Industrial Electronics/Power Electronics/Industry Applications Societies in Novi Sad, a Founder and the President of the Power Electronic Society of Serbia, a Member of the Presidency of National Society of ETRAN, a Member of CIGRE (Paris), an Observer Member in the SC C4 of CIGRE (Paris), a Member of National Commitee of CIGRE (Serbia), and a Founder and a Member of the Executive Board of National Committee of CIRED.

He is the author of Electric Power Quality—Harmonics (Novi Sad, Serbia: Univ. of Novi Sad, 2002, Eng. Monograph Series 6), Microprocessor Application in Power Engineering —Laboratory Practice (Novi Sad, Serbia: Univ. of Novi Sad, 2006, Univ. Textbook Series 149), Power Electronics — Laboratory Practice (Novi Sad, Serbia: Univ. of Novi Sad, 2000, Univ. Textbook Series 124), Power Electronics—Worked Problems (Novi Sad, Serbia: Univ. of Novi Sad, 1998, Univ. Textbook Series 66), and the Editor of Modern Aspects of Power Engineering (Novi Sad, Serbia: FTN—Inst. of Power and Electron. Eng., 1995). He has published over 350 papers, and participated or was the main researcher in 54 national and international R&D projects.

He is in the Editorial Boards of International Journal on Electrical Engineering Education (U.K.), International Journal of Power and Energy Systems (USA-Canada-CH), Advances in Electrical and Computer Engineering (Romania), Electronics Journal (BIH), Engineering-Electrical Engineering (Serbia) and was a Member of Program or Steering Committees of more than 50 International Conferences around the World. He chaired numerous international and national conferences, on which biannual International Symposium on Power Electronics – Ee is well known.

The Sixth Decade of the Thyristor

Goce L. Arsov and Slobodan Mirčevski

***Abstract*—The invention of the Silicon Controlled Rectifier (SCR) in the late 1950s, today known as thyristor has led to the revolution in the control of electric power, i.e. in the field of power electronics. At present, about 70% of electric power is consumed by the process of power electronic equipments, and it is expected to grow up in the future. This paper is dedicated to the 50th anniversary of the thyristor. The first part of the paper is dealing with the history and the second with the evolution from SCR to IGCT and ETO and the main characteristics of several members of the thyristor family.**

***Index Terms*—Silicon Controlled Rectifier (SCR), thyristor, triac.**

I. Introduction

TODAY, it is inconceivable to think of living in a society without electricity. In today's modern society, almost everything runs on electrical power. The need for power processing is obvious.

Power Electronics, as an enabling technology is becoming more and more important and is the basis for many industrial processes, for the rational use of the energy, for new technologies in individual and mass transportation, areas that are rapidly growing requiring new concepts in order to fulfill cost, reliability and miniaturization. The impact of power electronics is perhaps equally striking in terms of our environment. Power electronics systems are expected to control up to 80 percent of all electricity used in USA by the year 2010 [1]. The fast development in power electronics was triggered by the invention of the thyristor, in 1957, or Silicon Controlled Rectifier (SCR) as called in that time.

The IEEE Dictionary defines SCR as "an alternative name for the reverse blocking triode thyristor". It is a four layer, three-terminal, solid-state device that controls current flow. It is made from single crystal, high-purity silicon (semiconductor) material. A *p*-type layer acts as an anode and an *n*-type layer acts as a cathode; the *p*-type layer closer to the cathode functions as a gate. It is a solid-state functional equivalent for the older gas-discharge or mercury-arc controlled rectifier known as thyratron.

In 1957 the three-terminal *p-n-p-n* device was introduced by GE as the Silicon controlled rectifier (SCR, later thyristor). This device became very soon the dominant control device in the power industry. The early history of this work (1954–1960), including the shorted-emitter and symmetrical switch (TRIAC), is described in the paper. The early work proved the need to employ, besides the basic vertical *p-n-p-n* layering, lateral *p-n* patterning and the use of the lateral geometry for three-terminal operation, shorted emitters, symmetrical switches (TRIACs), regenerative gate operation, and ultimately gate-turn-off switches.

Once the SCR came onto the world stage, many people in various places played important roles in further developing it into the revolutionary device that it became. However, the name SCR was not the one chosen by GE for the device but rather some at GE chose the name "silicon controlled rectifier" or SCR. In July 1959, Westinghouse announced a solid-state controlled rectifier called "trinistor". By 1966, L. F. Stringer [2] and L. R. Tresino used the name thyristor. Some in Europe adopted the name thyristor more quickly than others elsewhere. This was partly due to IEC TC47 formed in 1960. It was several years before the name thyristor became universally accepted.

Early on, many people misjudged the role that the SCR would ultimately play. They considered it as being a tiny device capable of only a small power rating similar to the transistor. Power transistors were being developed at several places, but even a husky one was capable of controlling only 37 W compared with the 2-kW capacity of SCRs. The key missed by many people was the switching nature of SCRs, rather than the continuous-current mode of the transistor. The fast switching behavior of SCRs reduced the power loss that was dissipated into the rectifier device.

The prototype SCRs available in 1957 worked at 300 V and up to 7 A. The diameter of the junction was 3 mm, and the price was 60 USD each. The amount of control power required to trigger individual devices was about 15 mW.

Today we deal with whole family of thyristor based devices starting with classic SCR up to new complex devices with turn-off capabilities (IGCT [3] and ETO-Thyristors [4], [5]).

II. Brief Historical Evolution of Power Electronics

Officially, power electronics was born in 1901 by the invention of glass-bulb mercury-arc rectifier by Peter Cooper Hewitt of USA [6]. Then, it went through the eras of gas tube electronics in the 1930s and saturable core magnetic amplifiers in the 1940s. Hot cathode thyratron was introduced in 1926 and the ignitron rectifier in 1933. Power electronics applications began to spread and in 1930 the New York

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Subway installs grid-controlled mercury-arc rectifier (3 MW) for DC drive. Then, in 1931 the German railways introduces mercury-arc cycloconverter for universal motor traction drive. In 1934 thyratron cycloconverter (synchronous motor 400 hp) was installed in Logan power station as a first variable frequency drive.

The present era of solid-state power electronics started with the introduction of thyristor or silicon controlled rectifier (SCR). Bell laboratories of USA published the historical paper on *p-n-p-n* triggering transistor in 1956 [7] of Moll (Fig. 1) et. al., and then, GE commercially introduced the thyristor in 1958. Since then, there has been a vast expansion of the technology with the research and development radiating in different directions as shown in the Fig. 2.

III. The Invention of the SCR

The invention of the bipolar transistor at BTL (1948) became a great stimulus for further investigation in semiconductor components in order to replace the bulky electronic tubes (vacuum, gas etc.) with much smaller and more efficient devices based on semiconductor technology.

Fig. 1. John L. Moll.

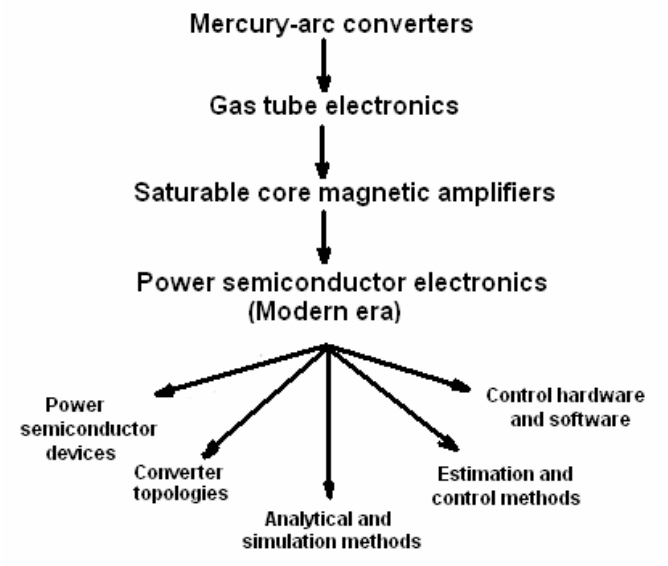


Fig. 2. Historical evolution of power electronics [8].

The Silicon Controlled Rectifier (SCR) or Thyristor was proposed by William Shockley in 1950. It was theoretically described in several papers by J. J. Ebers [9] and especially by J. L. Moll [7] and others at Bell Telephone Laboratories (BTL). In 1956 the SCR was developed by power engineers at General Electric (G.E.) led by Gordon Hall. The commercial version was developed in 1958 by G. E.'s Frank W. "Bill" Gutzwiller (Fig. 3).

The idea of the *p-n-p-n* switch was simulated by a circuit model, the Ebers' model [9], which is the center part of Fig. 3 between *A*(+) at the bottom and *B*(−) at the top. The idea of a *p-n-p-n* switch was that a *p-n-p* transistor (bottom) is driving an *n-p-n* (top) and, in turn, the *n-p-n* is driving the *p-n-p*. The collector of one, either one, drives the base of the other. This is guaranteed to yield instability. When the voltage from *A* to *B* reaches avalanche breakdown of the "*n-p*" diode (center of Fig. 4) and sufficient current flows in emitter shunt resistors R_1 and R_2 to bias on the emitters, the sum of α_{PNP} and α_{NPN} approaches unity, and to maintain current continuity switching occurs to low voltage. The two collectors switch from reverse to forward voltage, and to the "on" state of the *A-B* switch, which, of course, is still not a *p-n-p-n* switch in a single "slab" of *Si*. The question was: could such a switch be built, and would it, indeed, work?

In early autumn 1954, J. M. Goldey, from MIT, and Nick Holonyak Jr. (Fig. 5), from Bardeen's laboratory – Urbana, joined John Moll's BTL group with the specific task of constructing a Si *p–n–p–n* switch, that potentially could compete with a two terminal gas tube designed to be used, perhaps in large numbers, as a telephone crosspoint switch [10].

Not knowing, in the beginning (1954), the role of traps (defects) in governing the injection efficiency of Si *p-n* junctions, they followed pretty much Jim Ebers' two-transistor model for the proposed *p-n-p-n* switch [9]. For test reasons, multiple terminal structures with resistive paths were planned, including if necessary external resistors, to provide shunt leakage and variable bias at the *p-n-p-n* emitters, just as suggested in Fig. 4 by the five components stacked vertically from *A* to *B* (+ to -) within the diamond-shaped rectifier bridge. At avalanche breakdown of the center *n–p* collector

Fig. 3. Frank "Bill" Gutzwiller.

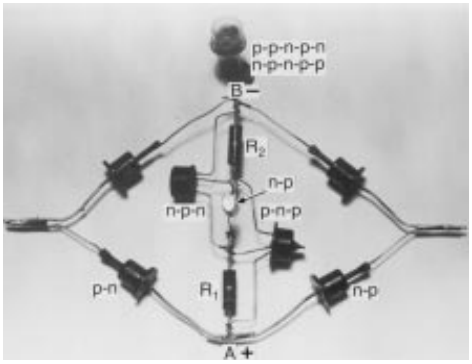


Fig. 4. Circuit model of a p-n-p-n switch made at GE [9].

Fig. 5. Nick Holonyak Jr.

junction (in the circuit model the diode at the center of Fig. 4) a result shunt current provides emitter bias and forces the device to switch from high reverse bias (voltage) to low forward bias to maintain continuity of current, all a consequence of [9]. This is the key to the switch operation, the alpha sum approaching unity (and thus the need to switch).

Based on these ideas, they built relatively quickly (1954–1955) three and even four terminal Si *p-n-p-n* switches. At that time they were pleasantly surprised to find that the we didn't need shunt leakage or resistors around the emitter junctions (as in Fig. 4) are not needed because of the saturable traps inherent in the junctions [9]. Simultaneously (1954–55) their colleague from BTL, Mort Prince was observing and independently confirming the effect of defects (traps) on the injection behavior (*I-V* characteristics) of diffused junction Si rectifiers [11]. Because of the traps in the junction transition region, at lower current levels the diffused Si rectifiers, as well as the two emitters of the *p-n-p-n* switch, behaved essentially as *p-i-n* [12], and not *p–n* junctions. Not only a new device but also a new technology was introduced. In 1955 in BTL three forms of Si *p-n-p-n* switch were proposed (Fig. 6). The switch shown in Fig. 6b later (at GE in 1957) became the Silicon controlled rectifier.

The SCR became a huge success for General Electric. It was reported in the business press by Business Week in their December 28th edition headlined *New way to Change AC to DC*. Commercial SCR were on the market in early 1958 [14] and Bill Gutzwiller was responsible for their technical and promotional support.

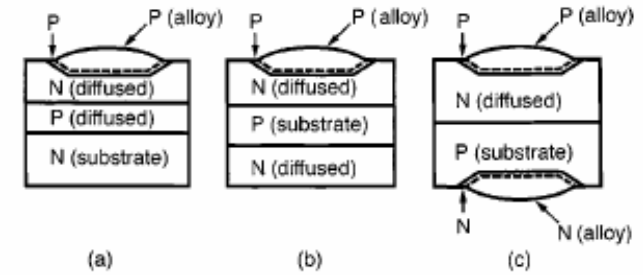


Fig. 6. Schematic cross sections [10] of three forms of Si p-n-p-n switches made at Bell Telephone Laboratories (BTL) in 1955. The switch shown in (b) became the Si controlled rectifier (SCR) at GE in 1957.

The demonstration of a SCR prototype from 1957 is shown in Fig. 7.

In the Spring of 1958, at a meeting in Syracuse, Holonyak and Aldrich were asked to develop a full wave controllable switch which could operate down to low forward voltages [15]. After the meeting Holonyak and Aldrich stayed on and devised a solution. Their prototype was made from a parent N-type wafer in a single diffusion step using gallium and phosphorus simultaneously Fig. 8.

Aldrich and Holonyak developed and described several bidirectional *p-n-p-n* devices having two, three, and more terminals. These devices utilized the "shorted emitter," an innovation of theirs which not only made single-chip bidirectional *p-n-p-n* devices possible, but also led to improvements in the characteristics of unidirectional devices (such as SCR's) [17].

The shorted-emitter did more than make possible the symmetrical (ac) switch. It made it possible to set, by design, a

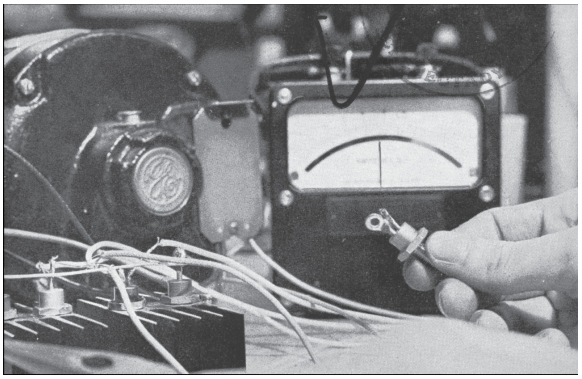


Fig. 7. Demonstration of prototype SCR in 1957 [13].

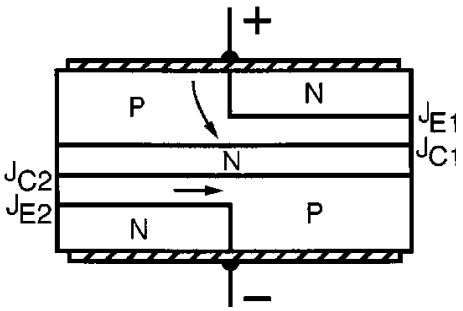


Fig. 8. Schematic cross section of a shorted-emitter symmetrical switch (DIAC) that in either polarity operates as a p-n-p-n switch [16].

certain current level before a *p-n-p-n* device switched, i.e. before the emitters became functional and thus $\alpha_{PNP} + \alpha_{NPN} \rightarrow 1$.

Adding to the structure a control electrode they obtained a controllable device called TRIAC (Triode alternating current switch). The first commercial Triacs were the *SC40* and *SC45*, rated 6 amperes and 10 amperes.

The thyristor era has begun.

IV. The Thyristor Evolution

From the invention of the thyristor up to present day's the power electronics has been continuing its growth centering on inverter and converters as its key system topologies. This has been accelerated by several evolutionary changes and breakthroughs achieved in the areas of power semiconductor device physics and process technology. The evolution of power electronics was directly related to the evolution of power electronics devices. The later can be categorized into four generations. The first generation spanning around 17 years, when thyristor-type devices dominated, is defined as the thyristor era. In the second generation, lasting about 10 years, self-controlled power devices (BJTs, power MOSFETs, and GTOs) appeared along with power ICs, microprocessors and ASIC chips. In the third generation, the most dominant power device, the IGBT, was introduced and became an important part in power electronics history. In addition, SITs, Intelligent power modules (IPMs), and powerful DSPs appeared. Finally, in the current or fourth generation, new devices, such as IGCTs, ETOs, cool MOSs and converters in integrated form as power electronic building block (PEBB) were introduced. The new materials are investigated and the technology is moving towards Silicon Carbide Devices.

The comparison of the characteristics of some power semiconductor devices with the year of their appearance is given in Table I.

Today the SCR family consists of:

- Thyristor (SCR);
- ASCR — Asymmetrical SCR;
- RCT — Reverse Conducting Thyristor;
- LASCR — Light Activated SCR (or LTT — Light triggered thyristor);
- DIAC & SIDAC — Both forms of trigger devices;
- BOD — Breakover Diode or Diode Thyristor (A gateless thyristor triggered by avalanche current);
- TRIAC — Triode for Alternating Current (A bidirectional switching device);
- BRT — Base Resistance Controlled Thyristor;
- SITh — Static Induction Thyristor (or FCTh — Field Controlled Thyristor) containing a gate structure that can shut down anode current flow;
- LASS — Light Activated Semiconducting Switch;
- GTO — Gate Turn-Off thyristor;
- MCT — MOS Controlled Thyristor (has two additional FET structures for on/off control);
- IGCT — Integrated Gate Commutated Thyristor;
- ETO — Emitter Turn-Off Thyristor.

The last four are thyristors with forced turn-off capabilities.

Until the appearance of the IGCT the main disadvantage of the thyristor was its incapability to be turned off by control signal. The GTO, invented in 1962, had high voltage drop in conducting state and needed very high turn-off gate current. As a result of intensive work, in 1996 and 1998 two new components, capable to turn off at any time, appeared. In 1983 the IGBT was introduced, but it suffers from limited voltage and current capabilities and high on-state voltage. The integrated gate turn-off thyristor (IGCT) appeared in 1996, and emitter turn-off thyristor (ETO), combining the best performance characteristics of IGBT and IGCT, appeared in 1998. Some of their characteristics are presented in Table I. Both components are using the unity-gain turn-off condition [18].

The key to achieve a hard-driven or unity-gain turn-off condition lies in the gate current commutation rate. A rate as high as 6 kA/μs is required for 4-kA turn-off [18]. The method to achieve this condition, used in IGCT, is to hold the gate loop inductance low enough (3 nH) so that a DC gate voltage less than the breakdown voltage of the gate–cathode junction (18 to 22 V) can generate a slew rate of 6 kA/μs. On the other hand the method used to achieve unity gain in the ETO thyristor is to insert an additional switch in series with the cathode of the GTO.

The key disadvantage of the IGCT approach (Fig. 9a) is the high cost associated with the low-inductance housing design

TABLE I
Comparison of Power Semiconductor Devices [19], [20], [21]

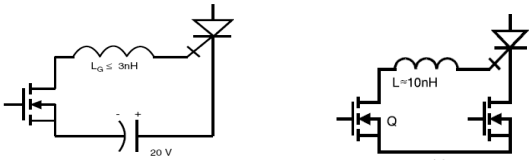
Device type	Year made available	Rated voltage	Rated current	Rated frequency	Rated power	Forward voltage
Thyristor (SCR)	1957	7 kV	3.5 kA	500 Hz	100's MW	1.5–2.5 V
Triac	1958	1 kV	100 A	500 Hz	100's kW	1.5–2 V
GTO	1962	4.5 kV	3 kA	2 kHz	10's MW	3–4 V
BJT (Darlington)	1960 s	1.2 kV	800 A	10 kHz	1 MW	1.5–3 V
MOSFET	1976	500V	50 A	1MHz	100 kW	3–4 V
IGBT	1983	1.2 kV	400 A	20 kHz	100's kW	3–4 V
SIT	1985	1.2 kV	300 A	100 kHz	10's kW	10–20 V
SITH	1988	1.5 kV	300 A	10 kHz	10's kW	2–4 V
MCT	1988	3 kV	2 kA	20–100 kHz	10's MW	1–2 V
IGCT	1996	6 kV	4 kA	1 kHz	100's MW	1.5–3 V
ETO	1998	6 kV	5 kA	2 kHz	100's MW	1–2.5 V

for the GTO and the low inductance and high current design for the gate driver.

Because of the use of hybrid approach based on conventional GTO, ETO devices (Fig. 9b) have clear advantages in terms of forward voltage drop, cost and gate drive power requirement over IGCTs. ETO devices also have two other advantages when compared with the IGCT. One is its feasibility of having a forward biased safe-operating area (FBSOA), and the other is its simplicity in overcurrent protection. Some comparative diagrams for the IGBT, IGCT and ETO's characteristics are given in Fig. 10.

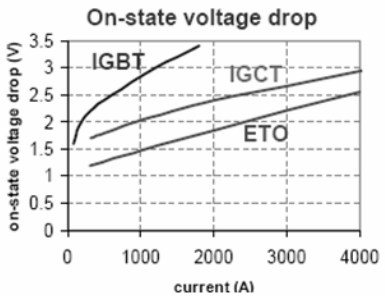
V. Comments and Conclusions

The power semiconductor devices discussed thus far are exclusively based on silicon material. Silicon has enjoyed a monopoly for a long period of time in both power and microelectronic devices, and this will remain so in the near future. However, new types of materials, such as gallium arsenide, silicon carbide, and diamond (in synthetic thin-film form), show tremendous promise for future generations of devices. SiC devices are particularly interesting for high-voltage, high-power applications because of their large band gap, high carrier mobility, and high electrical and thermal conductivities compared to silicon material. These properties permit devices with higher power capability, higher switching frequency, lower conduction drop, higher junction temperature. However, processing and fabrication of these materials are difficult and expensive. Most of the power devices based on SiC have been tried successfully in the laboratory. SiC-based power MOSFETS with *Tj* up to 350°C appear particularly interesting as replacements for medium-power silicon IGBTS in the future. Today, SiC-based high-voltage Schottky diodes (300–1700 V, 2–10 A) with close to a 1-V drop and negligible leakage and recovery currents are commercially available.

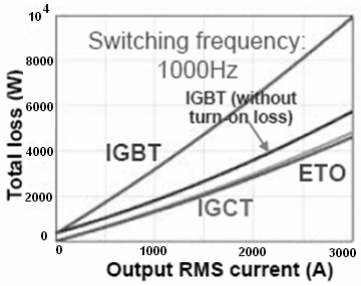


(a) (b)

Fig. 9. Circuit representation: (a) IGCT, (b) ETO [18].



(a)



(b)

Fig. 10. Comparisons of the device's (a) on-state voltage drop, (b) total losses in a PWM voltage source converter with sinusoid output [19].

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Semiconductor Solutions for Automotive AC Drives

Dušan Graovac, Benno Köppl, Frank Auer, and Michael Scheffer

***Abstract*—This paper gives an overview of the semiconductor solutions for the 3-phase automotive drives systems as based on the technologies existing today. The special attention is given to micro-hybrid systems, since they represent the most challenging application on low-voltage board net. The application requirements will be discussed and mapped directly into semiconductor requirements. An outlook in the future is given as well.**

***Index Terms*—Power electronics, automotive, semiconductors, drives.**

I. Introduction

CURRENT CO_2 discussion and the need for higher efficiency lead to the significantly growing market share of the hybrid automotive systems. One of the significant agenda points are so called micro-hybrid cars. In those cars the alternator is used also as a starter and the braking energy, or at least some part of it, is recuperated to the battery. The micro-hybrid (starter-alternator) systems are easy to integrate into the existing cars, since they can operate on the 14 V board net. Mild- and full-hybrids are high-voltage systems, based on IGBTs, while the micro-hybrids are low voltage systems based on power MOSFETs. The overview of hybrid technologies is given in Fig. 1. Table I shows an overview of AC drives on a classical 14 V board-net with their typical power and current requirements. The highest powers, apart from micro-hybrid, are required for electric and electro-hydraulic power steering (EPS & EHPS).

The aim of this paper is to give an overview of the semiconductor solutions for the automotive AC drives as based on the technologies existing today. The special attention will be given to micro-hybrid systems, since they represent the most challenging application on low-voltage board net. The application requirements will be discussed and mapped directly into semiconductor requirements. An outlook in the future will be given as well.

Since the micro-hybrid application is the ultimate challenge on low voltage power semiconductors in terms of need for high current, low power losses and the low voltage drop on the semiconductors, a special attention will be given to MOSFET technology. A comparison between planar and trench technologies for automotive power MOSFETs with their advantages and disadvantages will be shown. Further accent will be stressed on packaging of the discrete MOSFETs and on the solutions based on power modules. Bonding options based on Power Bond Technology for high current MOSFETs will be presented for discrete MOSFETs mounted on insulated metal substrate will be given, as well as the power module solutions. Reliability of the power module solutions, together with some failure modes will also be provided.

In order to achieve desired switching and steady state characteristics of the MOSFET, high performance bridge drivers are necessary and will thus be discussed. To complete the system picture, possible solutions for micro controller as well as the sensors and the communication devices will be presented.

System demonstrator for 3- and 6-phase alternator is presented, together with experimental results.

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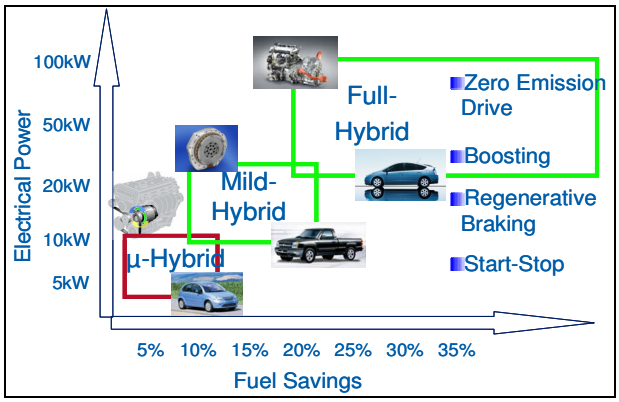

Fig. 1. Overview of hybrid automotive technologies.

TABLE I
Overview of Automotive AC Drives

EHPS	1 kW, 100 A peak
EPS	1.5 kW, 140 A peak
Water Pump	300 W – 1 kW
Fuel Pump	200 – 300 W
Clutch/Gearbox	peak currents up to 70 A
Engine Cooling Fan	400 W – 1 kW
HVAC Fan	250 – 450 W
Starter-Alternator	3 – 4 kW, High Currents

II. Application Overview

An overview of all start-stop systems (including micro-hybrids), together with different system voltages and required features is given in Fig. 2. A simplified block diagram of a belt driven starter-alternator ECU is shown in Fig. 3. It consists of the electric machine, 3-phase inverter with power MOSFETs and a bridge driver, micro-controller for motor control during both starting and generation mode, H-Bridge for excitation control, position/velocity/ sensor and current/voltage sensors.

The electric motor used is usually a classical claw-pole motor (Lundell alternator). It is a wound field synchronous machine with a three-phase (or six phase) stator, and a claw pole rotor structure where the claw poles close around a field winding. The field winding is supplied from the stator via slip rings. The rotor time-constant is rather high (~100 ms) and can cause both high amplitude and long load dumps, if not properly controlled and quickly de-energized. The reduction of the load dump is the reason for using the H-bridge in excitation control.

The most important task in alternator mode of operation is to maximize the efficiency of the electrical energy generation. Fig. 4 shows a typical split between individual power losses in alternator. Modern generators have typical efficiency of $\eta \approx 70\%$. It can be seen that the diodes in the rectifier bridge cause 38% of generator losses. Exchanging them with MOSFET leads to increased efficiency.

During starting of the engine, it is necessary to provide the required ICE start-up torque. The typical alternator torque/speed characteristics are given in Fig. 5 together with excitation currents needed to achieve a maximum torque at given speed.

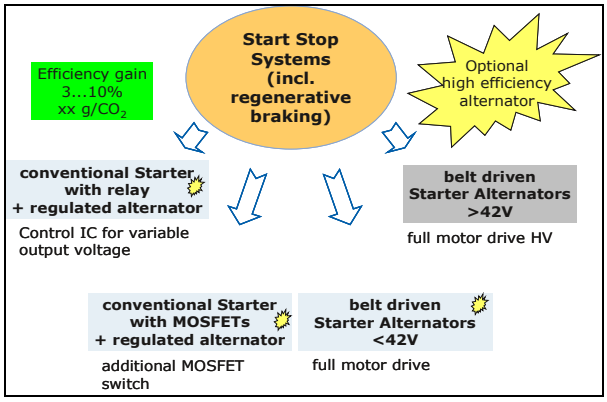

Fig. 2. An overview of the start-stop systems.

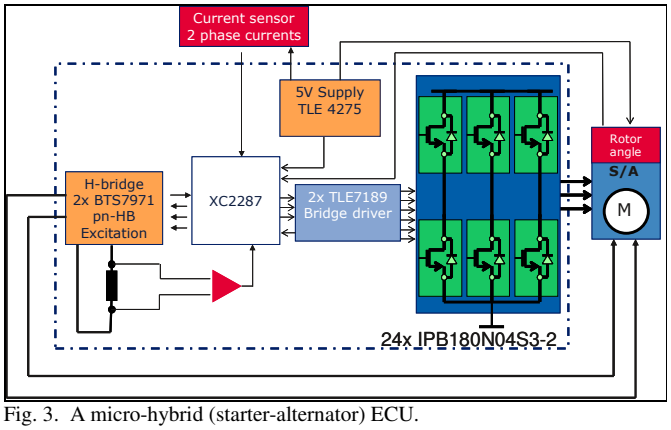

Fig. 3. A micro-hybrid (starter-alternator) ECU.

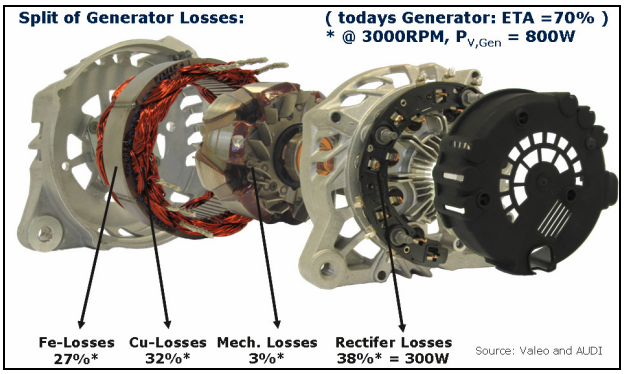

Fig. 4. Alternator losses split (source: Valeo and Audi).

The MOSFETs in inverter have to drive high currents (up to 600A) with a minimum power loss and are driven by a 3-Phase Driver IC which is controlled by a µC which generates the PWM/SVM patterns. The whole system is controlled by engine management ECU via LIN interface.

III. Application Requirements for Power MOSFETs and Driver IC

The hardest requirements in a micro-hybrid system are set for power MOSFETs. Very high currents (600 A) and the need for low voltage drop and high efficiency require very low Rdson value and also a large chip area which is needed for placement of the bonding wires. Such large chip area could have a negative influence on both the gate-charge (important for the bridge driver current capability) and gate-to-drain charge (important for the minimization of the switching losses). An overview of the requirements on power MOSFET is given in Fig. 6. Modern low voltage MOSFETs are based on trench cell concepts. Advantage of a trench technology over a planar technology is the capability for much lower area specific on state resistances on chip level. This improvement is based mainly on the reduced channel resistance and on higher cell density. The performance difference as based on figure of merit (FOM=Rdson*Qg or Qgd or Qsw) comparison between classical trench and the IFX trench technology is given in Fig. 8. The IFX trench concept, compared to the classical trench, enables further reduction in Rdson, gate-to-drain

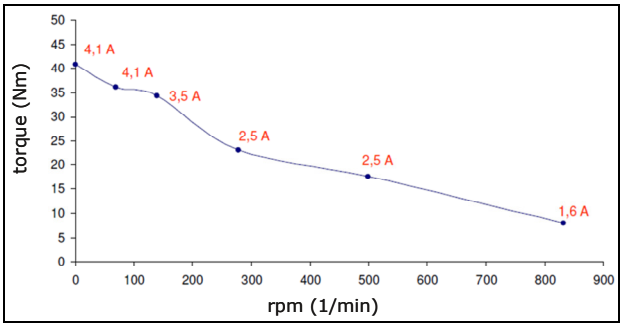

Fig. 5. Alternator characteristics during starting (source: BMW).

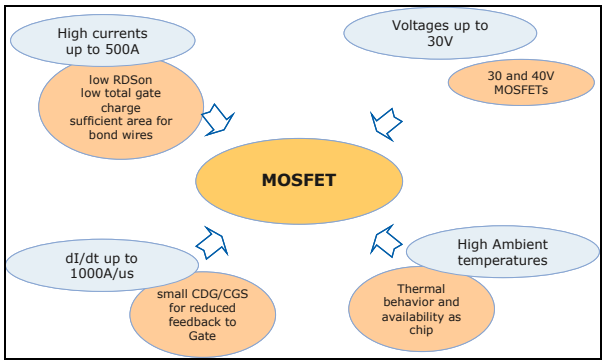

Fig. 6. Power MOSFET requirements.

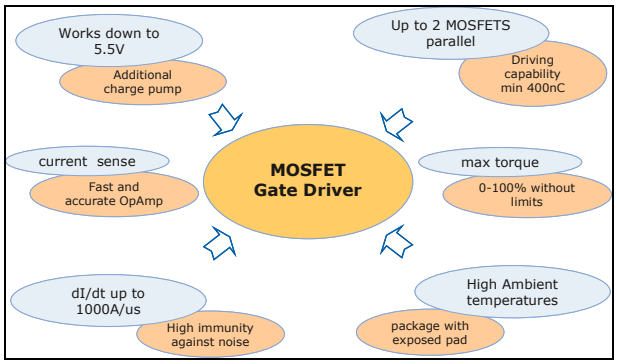

Fig. 7. Bridge driver requirements.

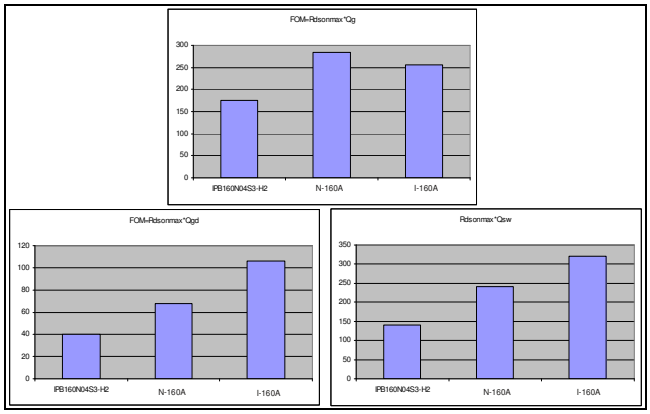

Fig. 8. FOM comparison between classical Trench and Infineon Trench technology.

charges, gate resistance and is more robust against the parasitic turn-on as triggered with high du/dt transients.

The driver IC is the interface between the µC and the MOSFETs. As the µC delivers the control signals, the Driver IC level-shifts, amplifies, and buffers the control signals to provide the necessary gate charge for the power stage. In addition, the driver IC incorporates protection functions and functions to reduce the external part count and cost. It also incorporates circuitry that allows operation at very low battery voltages or other extreme application conditions. The set of requirements of the micro-hybrid application on driver IC are given in Fig. 5. In addition to that it should be noted that the overcurrent, shoot-through, under-voltage and over voltage protection are necessary.

In order to achieve high currents using standard 7-pin D2PAK (packages), a PowerBondTM bonding technology is used. PowerBondTM was developed to respond to the increasing demand of current needs in high power applications. It also contributes to lower overall package resistance. This is especially important for new power MOSFET technologies. Today the package resistance is about 20% of the total MOSFET resistance. The other 80% are the chip contribution. In the near future with further decreasing of the specific on-resistances of a power MOSFET, the package share would be easily 50% without further development in assembly technology. Depending on the bonding configuration the current rating of a MOSFET is limited either by the chip itself or by the bonding wires, since the hottest temperature on the bonding wire has to be limited to 200°C. The reason is not the bonding wire itself, but the mold compound. In usual molding compounds decomposition occurs if temperature exceeds about 220°C. This temperature limit restricts the permissible current. This approach enabled achieving of a true 180 A DC current capability of a D2PAK. The bonding consists of 4x500 µm bond wires (Fig. 9) with the package resistance reduced to 0.3 mΩ only.

IV. Systems Demonstrator and Experimental Results

The system, which block-diagram was shown above in Fig. 3 is a starter-alternator prototype, which can start the internal combustion engine and once the engine is running, also act as a classical alternator with AC/DC converter using active rectification with power MOSFETs instead of the diodes. Such a system has a very high efficiency compared to the diode rectification in classical alternator solutions. The efficiency of the complete system, including generator, in AC/DC mode is improved for at least 6%. With modifications at the alternator itself efficiency improvements of more than 10% are realistic. The other significant advantage is the increase of the available generator current at low speed of around 40% (the exact amount is dependent on the alternator design). The 3-phase demonstrator platform is given in Fig. 9 and its 6-phase counterpart in Fig. 10.

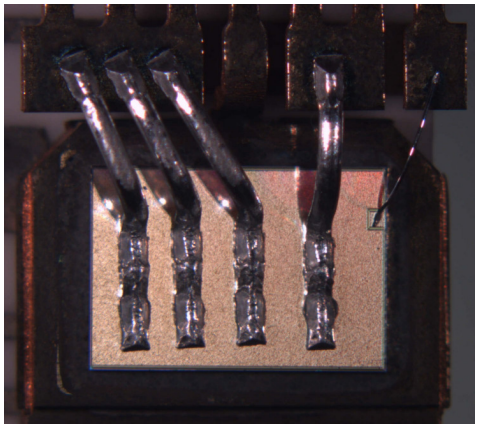

Fig. 9. FOM comparison between classical Trench and Infineon Trench technology.

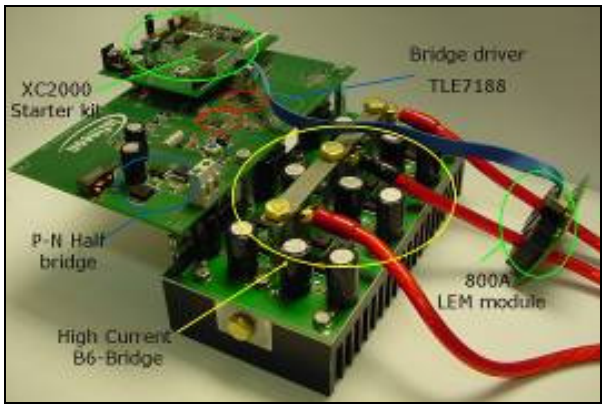

Fig. 10. 3-phase system demonstrator.

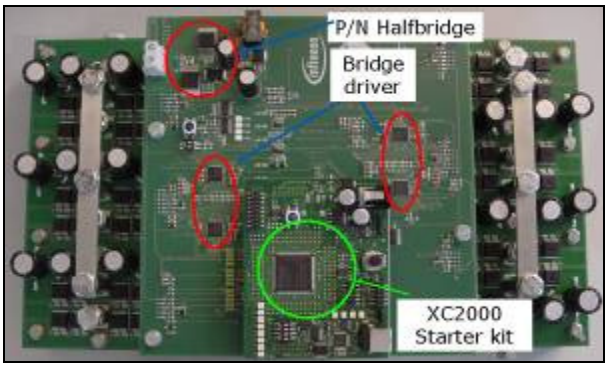

Fig. 11. 6-phase system demonstrator.

The control concept during starting mode of operation is shown in the Fig. 12. It is based on field oriented control of a Lundell alternator. The required velocity or torque profile is converted into q-axis current component, whereas the required flux is mainly driven by the excitation winding, supplied by the DC/DC converter. However, if a stronger magnetisation is required, an additional d-current component can be generated. To minimize the power losses in MOSFET inverter during start-up, a minimum loss space vector modulation with 30° shift (MLSV_30) has been implemented. It reduces the switching losses to 50% as compared with classical space vector modulation.

During alternator mode of operation, it is important both to switch on the appropriate MOSFET, according to conduction sequence and also to minimize the load dump. For the purpose of load-dump minimization a two-fold concept is used:

- DC/DC H-Bridge of fast de-excitation of the machine.
- Implementation of the zero voltage vector on the alternator (short-circuiting of the windings) for the periods of time when fast de-excitation alone is not enough.

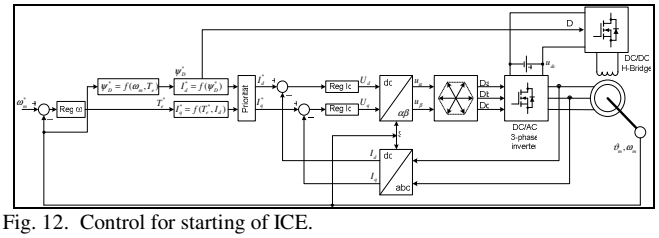

Fig. 12. Control for starting of ICE.

Based on the previous considerations, the following results were obtained:

Two examples of the MLSV_30 (with fixed and random carrier frequency) PWM during starting mode are given in Figs. 13 and 14. First trace (yellow) is the phase to phase voltage with 10 V/div, second trace (magenta) is phase current with 150 A/div, and third trace (purple) is the magnitude current spectrum, while the fourth trace (brown) is the magnitude voltage spectrum. For the spectra, the frequency axis resolution is 7.81 kHz/div.

The alternator mode of operation is illustrated in Figs. 15–17. Fig. 15 shows the board-net (alternator after rectification) voltage and current when an active (MOSFET) rectification is used.

It can be seen that over a whole speed range of interest the voltage is kept constant and a current margin is high. This current margin, or the availability of the board net current, is especially important at low speeds. Table I illustrates the superiority of the active converter compared to the passive one, i.e. at 1500 rpm and nominal load, 50% more current is available. Fig. 16 shows a comparison of power losses between passive and active rectification. The energy savings with active rectification are significant over the whole current range.

Finally, Fig. 17 illustrates a load dump behavior of the proposed alternator control in a so called “loss of battery” situation. It can be seen that when dumping the 100 A load, the

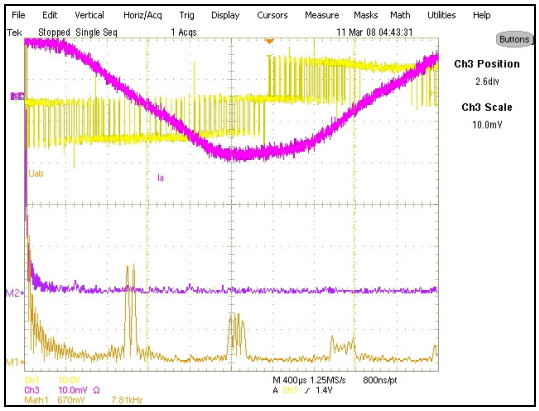

Fig. 13. MLSV_30, M = 1.

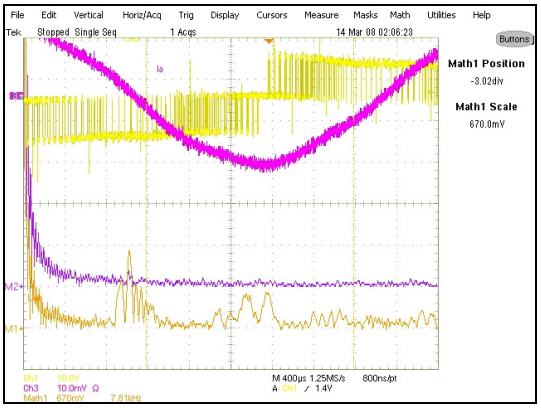

Fig. 14. MLSV_30, M = 1, variable pulse rate.

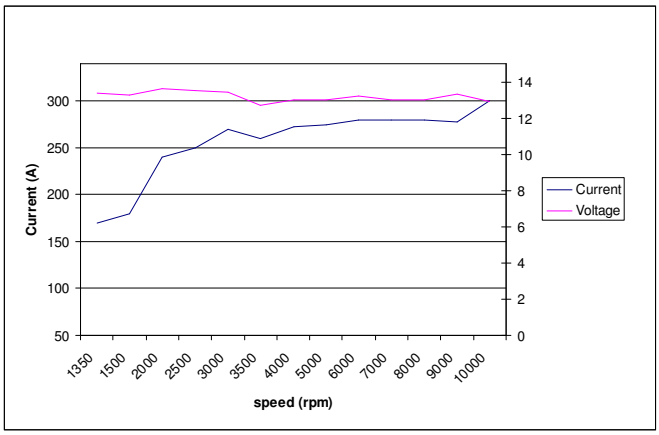

Fig. 15. Current margin with active rectification.

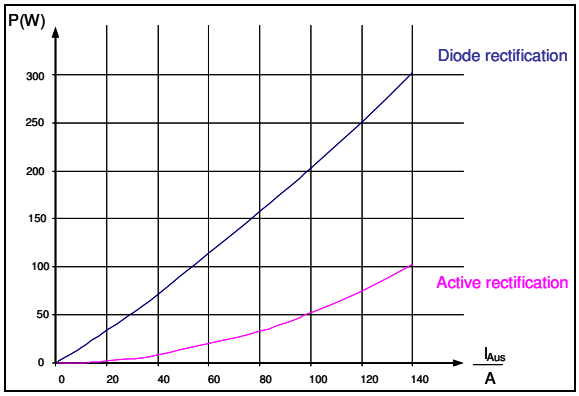

Fig. 16. Efficiency comparison.

TABLE II
AVAILABLE BOARD NET CURRENT AT LOW SPEED

U=13,5 V	Active (MOSFET)	Passive (Diode)
Speed (rpm)	1500	1500
Load	100 %	100 %
Current (A)	180 A	125 A

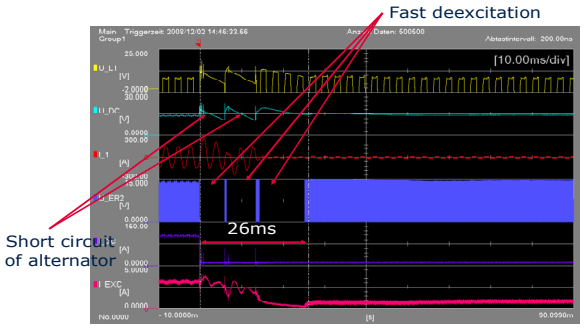

Fig. 17. Load dump with fast de-excitation and zero vector (short circuit).

overvoltage peak remains below 25 V and has a very short duration of below 5 ms. Compared with classical load dump condition, which vary between 32 V and 45 V for 400 ms, this concept bring significant advantage for the voltage classes of semiconductor components used in all automotive subsystems connected directly to board net.

V. PACKAGING AND INTERCONNECTION OPTIONS, QUALITY AND RELIABILITY OF POWER MODULES

Semiconductor devices in the micro-hybrid application are placed in the engine compartment with an additional goal of integrating both the power electronics part as well as the control circuitry into the alternator. Thus, they have to deal with both severe temperature cycles and high junction temperatures. ECU has to withstand 600.000 ICE starts over 17 years without failure, together with additional thousands of operating hours in generator mode. These requirements are summarized in Fig. 18.

Although it is possible to design an ECU based on discrete MOSFETs mounted on IMS (insulated metal substrate), as done previously with the system demonstrator, very high current and power densities, integration in the generator housing and reliability/life time requirements can only be achieved using the power module with a ceramic substrate (DCB – direct copper bonding). Fig. 19 shows a typical cross-section of an IGBT power module, as well known from industrial or railway applications: semiconductor chips (MOSFETs or IGBTs/Diodes) are soldered on a ceramic substrate and the DCB is soldered to the base plate. This classical build-up of a power module is, from automotive point of view, bulky and expensive for micro hybrid vehicles. For that reason, power modules without a base plate are often used in automotive applications. One module of this type is shown in Fig. 20.

Thermal advantages of ceramic substrate over discrete

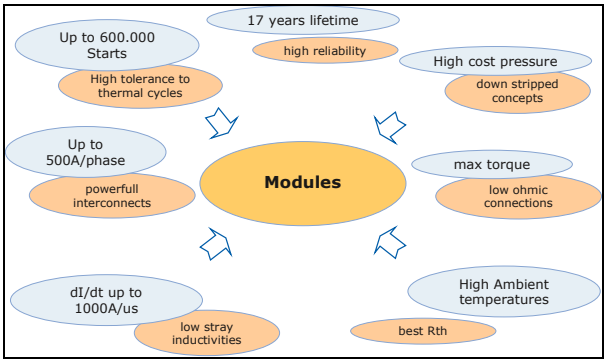

Fig. 18. Power module requirements.

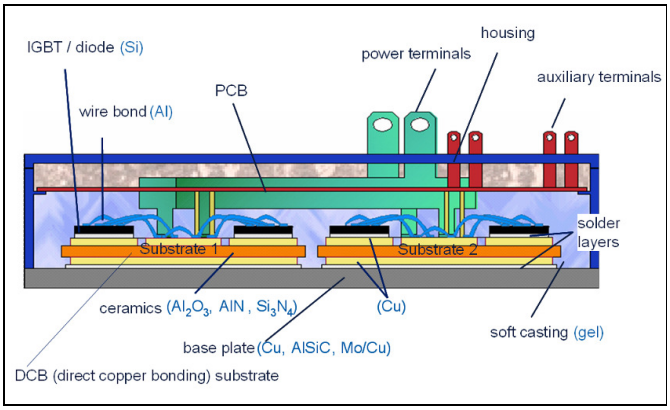

Fig. 19. Classical power module cross-section.

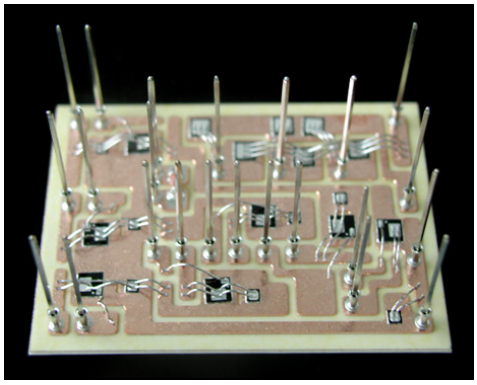

Fig. 20. Module without a base plate.

components mounted on IMS are illustrated in Fig. 21, which shows the thermal resistance (Rth) dependence on the chip area for. Compared are IMS with AL_2O_3 and AlN DCB. It can be seen that DCB offers lower Rth by the factor of 2-4.

To withstand high electrical and thermo-mechanical stress, interconnections inside the power module have to be as strong as possible. Fig. 22 shows the failure mechanisms for standard modules due to thermal load changes. These are:

- Bond wire lift-off
- Delamination of the upper side copper layer
- Solder cracks.

The main cause of these failures is different heating of the individual areas/layers and the different thermal expansion coefficients of the materials used in the inside the power

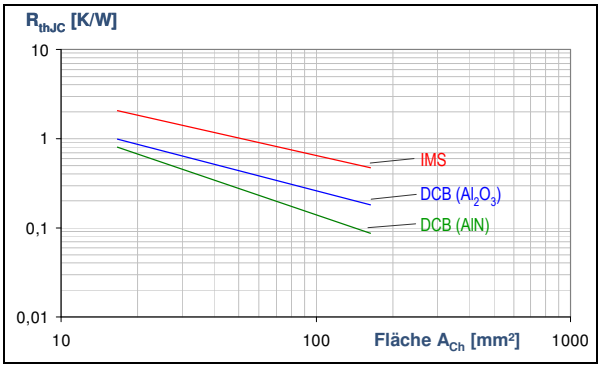

Fig. 21. Rth comparison between IMS and DCB.

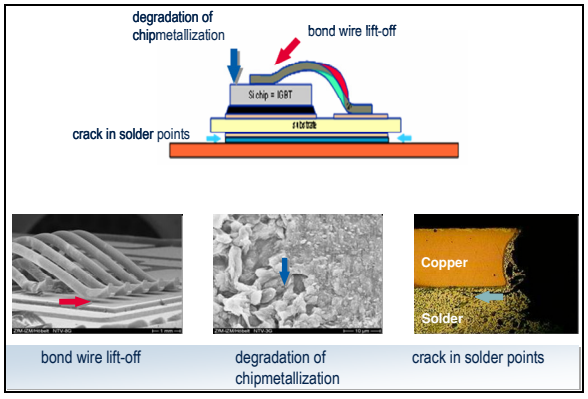

Fig. 22. Failure mechanisms in power modules.

module. This also shows the importance of the proper material choice for the module life time. The different expansion coefficients for different materials are given in Fig. 23. It can be seen that the ceramic substrate materials are much better match to silicon expansion coefficient, as compared to copper, which is a main leadframe material for the discrete components.

VI. Future Outlook

In the power MOSFET technology, further minimization of both Rdson and charges is expected together with the increase in temperature capability. Changing the maximum allowable junction temperature of the power semiconductor will directly change the thermal stress on the interconnection of the chip surface. A typical wear out effect at the chip surface is the wire bond lift off. To test this interconnection power cycling tests are performed. The number of cycles that a device survives is related to the temperature swing, the maximum temperature and the slopes. For the introduction of a maximum junction temperature of 175°C the wire bonding process has already been improved from standard wire bonding to the IFX new generation wire bonding. For future designs results of the low temperature joining process are promising. As can be seen in Fig. 15 the tests were still ongoing after 70000 cycles with a temperature swing of 130°C.

Further innovation comes from the field of sensors. In the development, there is a rotor position sensor based on iGMR (integrated giant magneto resistance) technology. Compared to AMR (anisotropic magneto resistive) sensors, iGMR sensors have incorporated not only position measurement but signal processing, diagnostics and a calibration as well. It enables high precision position measurement over 360°C and requires a very small mounting space. Also, the multi functional alternator control IC with A/D converter and digital control logic (similar to LIN-VDA-Regulator IC) is very promising.

VII. Conclusion

This paper gave a detailed overview of the semiconductor solutions for the micro-hybrid vehicles, especially for the belt

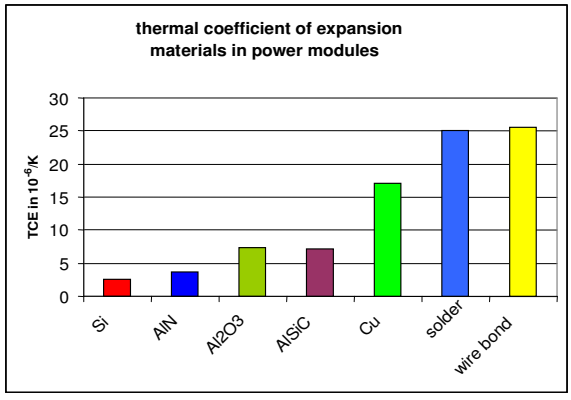

Fig. 23. Thermal coefficients for different materials.

driven starter alternators. The application requirements were given and mapped into semiconductor requirements. Special attention was given to power MOSFETs technologies, power modules and driver circuitry.

System demonstrator for 3-phase and 6-phase systems with the appropriate control design was presented, together with a load-dump minimization concept. The experimental results based on 3-phase system, confirm the validity of the semiconductor concepts presented in the paper.

It was shown that existing semiconductor devices existing today are already able to fulfill the application requirements and allow for first designs. The MOSFET module technology reaches the required lifetime level dependent on the choice of material. An outlook in the future was given as well.

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Real-Time Digital Simulation: Enabling Rapid Development of Power Electronics

Ivan Čelanović, Pierre Haessig, Eric Carroll, Vladimir Katić, and Nikola Čelanović

***Abstract*—In this paper, we present the Typhoon Real Time Digital Simulation (T-RTDS) platform for high-power electronic systems, the fastest simulation platform of its kind. T-RTDS is based on novel simulation algorithms and proprietary high-throughput low-latency processor architecture. This approach enables simulation with a 1 μs time-step, including input/output (I/O) latency. As a case study, we present modeling, simulation and experimental results for a system comprising a rectifier, an inverter, an output filter and a load. In addition, we demonstrate the T-RTDS capabilities for testing and verification of control hardware and software for various operating conditions.**

***Index Terms*—Power electronics, real-time, simulation, testing, hardware in the loop, controls.**

I. Introduction

POWER electronics is one of the key enabling infrastructural technologies that promises to deliver up to 30% electric energy savings [1]. It is a technology that allows energy savings across all aspects of conversion of primary energy into electricity and electricity into useful work. Furthermore, power electronics is one of the instrumental technologies in the effort to reach 20% renewable energy generation by the year 2020.

In order for power electronics to reach its full potential, cost, reliability, and performance must be significantly improved. Improvements need to address long design cycles, lack of standardization, and reliability problems due to labor-intensive manufacturing, testing, and verification. In addition, performance and flexibility need to be significantly enhanced by means of standardization and automation of control software and hardware tools (e.g., automatic code generation, automatic code verification).

Typhoon RTDS has developed a novel digital platform for design and testing of high-power electronics. This technology, based on what we believe is the world's fastest real-time digital simulator platform for power electronics, is enabled by a new approach to system description/algorithms and a proprietary high-throughput low-latency digital processor architecture tailored to those algorithms.

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II. A Bit of a History

Almost eighty five years ago MIT engineers lead by Prof Vannevar Bush started a revolution in scientific computing and simulation tools with the invention of what came to be known as the *Differential Analyzer* [2]. The search for advanced analysis tools — motivated by the need to understand the dynamics of power transmission networks — resulted in development of the first analog computer ("Differential Analyzer") capable of solving differential equations in real time: arguably the world's most important computer until the end of the Second World War. Since those days, many technologies had been developed to enable real-time simulation of dynamic systems. However, the power electronics industry today still largely relies on analog simulators (low-voltage/low-power versions of real converters) and in some cases on digital simulation technologies that were designed for continuous dynamic systems with relatively slow time constants.

With the advent of T-RTDS technology, real-time simulation in power electronics will radically change, because it is a tool designed to help power electronic engineers reinvent the design and testing of power electronics and for the first time, allow flexible real-time measurement and control — with extremely high fidelity — of prototype systems that can be redesigned, refined or tuned for increased reliability and efficiency.

III. Hardware Finally Gets into the "Power Electronics Loop"

Real-time digital simulation makes it possible to replace a physical system with a computer model for the design and testing purposes. This concept is illustrated in Fig.1 where a detailed model of a power electronics controlled wind turbine is simulated on the *T-RTDS* platform. The *T-RTDS* simulation interacts with a real physical controller via a fast input/output in *real-time*. From the controller perspective there is no difference between the physical system and its real-time simulation. Indeed, the controller (and here we mean also the

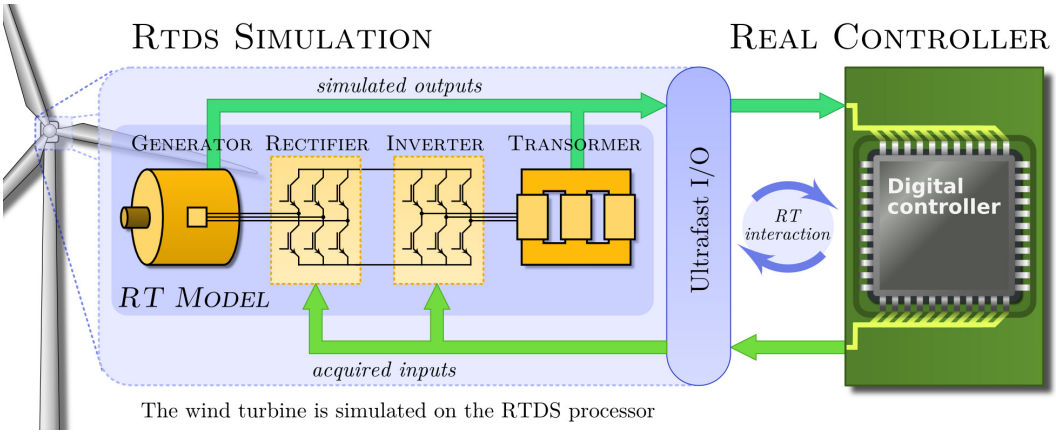

Fig. 1. Block diagram of a wind turbine real-time simulation. RTDS simulation interacts in real time with real controller.

high speed part of the controller which includes the modulator and the protection functions) "feels" that it is controlling a real physical system.

Real-time digital simulation as a means of testing control systems is not a new idea [3]. For example, the aerospace industry has been using it since software became a safety-critical component of flight control systems. The automotive industry is another example where real-time digital simulations have become an invaluable design and testing tool.

There are four compelling reasons for using real time hardware in the loop simulation that can be summarized as:

- reduction of development cycle,
- demand to extensively test control hardware and software in order to meet safety and quality requirements,
- the need to prevent costly failures, and
- increased availability of hardware in the loop components.

Indeed, real-time digital simulation has been a central tool for aerospace and automotive control and systems design engineers. However, real time hardware in the loop digital simulators are still rare in power electronics industry, and one may wonder why is that the case?

Power electronics systems control the flow of electric power by means of *fast* switching actions. In other words they belong to a class of hybrid systems called switched dynamic systems which can be represented with a set of discrete states and their associated continuous dynamics. Depending on external controls and internal state variables, they switch between different continuous descriptions. Combination of high-frequency switching actions and fast continuous dynamics makes such systems hard to simulate in real time using current technology.

To illustrate this point consider a variable speed wind turbine generator example from Fig. 1 where power flow and turbine speed are controlled with a four-quadrant rectifier-inverter operating at a switching frequency of several kHz [4]. In order to simulate this system in real-time with good fidelity a simulation time step on the order of 1 µs which accounts for both latency and computation time is needed. This is almost two orders of magnitude improvement when compared to today's 50 µs time step of commercially available digital hardware in the loop systems.

A. *Benefits of a High-Speed Low-Latency T-RTDS Platform*

T-RTDS platform simulates all the time critical parts of the wind-turbine system (and other power electronics systems) with the simulation time step and latency of 1µs. This performance requires formidable parallel processing power, specially formulated power electronics models and algorithms suitable for parallel execution, a very fast digital input/output interface with low-latency and sophisticated high throughput software for data analysis and processing.

T-RTDS technology is geared for power electronics developers in the following areas:

- control hardware design, testing and tuning,
- control software testing and verification,
- fault response and recovery testing,
- testing against regulatory standards,
- education, and
- service and maintenance.

Industries that we expect to be early adopters and that are to profit the most from this approach are:

- renewable energy: wind and solar,
- transportation (automotive, traction, and aerospace),
- power generation, and
- industry automation.

IV. The T-RTDS Platform Description

T-RTDS platform supports 1µs simulation time step thus enabling high-fidelity real time simulations. Simulation algorithms are based on fixed time step integration algorithms. The T-RTDS platform is based on our innovation in three key areas from Fig. 2:

- minimal circuit description
- proprietary compiler and
- processor architecture tailored for low latency implementation of the minimal circuit description.

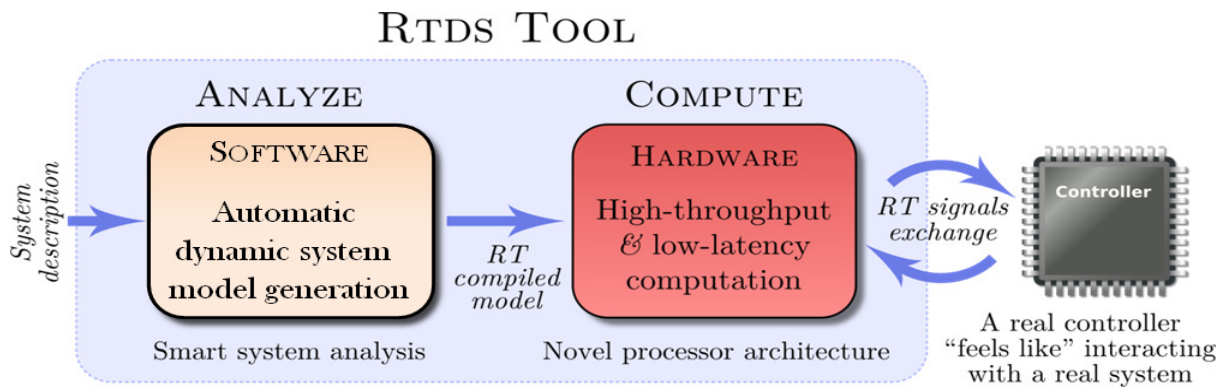

Fig. 2. The RTDS platform architecture depicts the relationship between software and hardware components. Their symbiotic design is the foundation enabling real-time operation where software compiles a model that is specifically tailored for execution on our custom processor.

A. T-RTDS Modeling Approach

To achieve "hard" real time digital simulation of switched dynamic systems we have developed algorithms that use ideal models of the switches and generate a minimal representation of power electronics systems. Indeed, combination of ideal switches and minimal dynamic system representation enables completely *deterministic* simulation time step, which is the key to real-time simulation. None of the circuit/system simulation algorithms available, to the best of our knowledge, provide completely deterministic time execution for switched dynamic systems such as power electronics systems.

B. Available RTDS Architectures

Commercially available real-time simulation hardware platforms are based on standard of the shelf processors for computing and field programmable gate arrays (FPGA) for input/output interfaces [5]. This traditional approach offers cost effective and flexible solutions down to 50 µs simulation steps.

One of the biggest problems when using standard processors for real time digital simulation is their inherent latency. Latency can be defined as the time delay between an event at the input of the RTDS and the corresponding reaction of the RTDS at the output. Most of the standard processors indeed have large throughput but also large latency simply because they tend to achieve the throughput with the use of architectures with long pipelines.

Table I shows peak floating-point performances of current state of the art processing platforms. At first glance all the platforms considered easily satisfy the requirements for real time simulation of power electronics circuits. However, most general purpose processors sustained computing performance for I/O intensive algorithms can drop way below the peak performance.

On the other hand, latest commercially available FPGA platforms [6] offer lower latency high bandwidth interface to the x86 CPUs using either FSB (Intel) or Hypertransport (AMD) interface. It is also shown that an IBM Cell processor can establish a high-bandwidth interface to an FPGA using FlexIO interface developed by Rambus [7]. With these newly developed interfacing capabilities, communication latency between the processing element and the external world is significantly reduced. The problem is that the mentioned platforms are expensive, are not commercially available and lack software support. In addition, loop-back latencies are still in the order of 10 µs.

TABLE I
PROCESSING PLATFORM PERFORMANCE COMPARISON

	General purpose processors		GPU	FPGA
Processing platform	Cell PowerXCell 8i	Intel Core2 QX9775	Nvidia GTX 295	Virtex5 VSX240T
GFLOPS (single)	≈ 200	≈ 50	≈ 2000	≈ 192
GFLOPS (double)	≈ 100	≈ 25	≈ 200	≈ 68
Fastest interface	FlexIO	FSB	PCIe	Custom

Another approach is to perform all the computation on an FPGA device [8]. Today's FPGA devices offer the comparable peak computing power to the state of the art general purpose processors even though they operate at order of magnitude slower clock speed. When it comes to computation efficiency with I/O intensive algorithms the FPGA technology is a clear winner. The programmable structure of an FPGA allows application optimized solutions resulting in a sustained performance close to the peak performance [8]. Fig. 3 illustrates the performance space of standard off the shelf processors compared to our custom processor in terms of latency vs. processing power given in giga floating point operations per second (GFLOPS). While in terms of processing speed T-RTDS algorithms require relatively modest GFLOPS number, the latency requirement our processor satisfies is almost two orders of magnitude better than what can be achieved with standard processors and holds the key to real time digital simulation of power electronics systems.

C. T-RTDS Architecture

Earlier work on FPGA based RTDS implementation was mostly based on implementing custom hardware models [5]. That way the hardware architecture of the system is customized for each instance of the problem and results in highly optimized digital simulator at the cost of flexibility and model development time.

This work on the other hand proposes an architecture that is general enough to cover a wide variety of power electronic

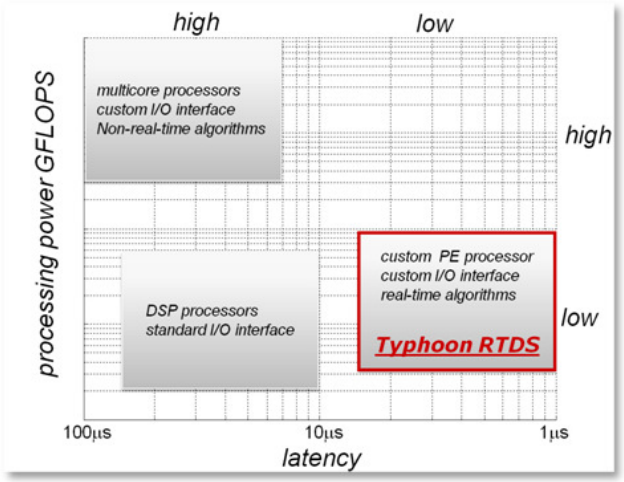

Fig. 3. Processing power vs. latency graph for standard processors and our RTDS processor.

models and is at the same time as high performing as the dedicated solutions. In addition, it is platform independent in the sense that it does not count on the flexibility of the FPGA technology and can later be migrated to ASIC for an additional tenfold reduction in simulation time step and latency.

D. *High-Speed Input/Output Interface*

Because there are no standard interfaces available for power electronics controllers their interface to RTDS almost always has to be custom made. Combining the glue logic and a processing engine in a programmable structure of an FPGA device allows the loop-back latency in the order of 1 µs which is the key advantage of this technology for RTDS application.

V. A Case Study: Variable Speed Drive System

To demonstrate our RTDS modeling and simulation process we have simulated a rectifier-inverter-filter system from Fig. 4. A SimPowerSystem (SPS) toolbox is used as a graphic user interface to specify a model that is simulated in real time on our processor platform. The model consists of single phase diode rectifier (four ideal diodes), three phase voltage source inverter, eight energy storage elements (inductors and capacitors) and five resistors.

After the schematic is specified in SimPowerSystems a netlist file is created. In the subsequent steps netlist is used as an input to T-RTDS compiler which generates a set of state space equations which are part of the minimal dynamic system representation. Once the minimal system representation is complete compiler generates a final binary file that is ready to be loaded into T-RTDS processor. Compiler generated processor code guarantees "hard" real-time with 1 µs execution time.

To benchmark the accuracy of our simulation approach based on ideal switches and minimal dynamic system representation we compared the results of our T RTDS simulation (instead of running it on hardware, for ease of comparison, we were emulating our platform in software) with SimPowerSystem, a commercially available simulation toolbox for Matlab. Results of simulation (DC link voltage, line to line load voltage, and DC link current) are shown in Fig. 5. The difference in simulation results between the two approaches is shown with red traces magnified by one thousand. Although T-RTDS (green) and SimPowerSystem (blue) curves overlap almost ideally slight differences can be observed at switching transitions because T-RTDS approach uses ideal switches while SimPowerSystem approach relies on numerical snubers. As a result, unlike other simulation tools, T-RTDS algorithms with ideal switches exhibits clean, oscillation free transitions between switching states under all operating conditions.

VI. Summary and Conclusions

We presented a new real time digital simulation platform for high-power power electronics systems. It simulates power electronics systems with 1 µs sampling time and latency and is based on innovation in: minimal circuit representation, compiler and proprietary processor architecture tailored for low latency implementation of the minimal circuit description.

These three components enable T-RTDS to guarantee 1 µs latency for a broad selection of power electronics topologies and systems.

As for the technology adoption rate we believe that power electronics industry will follow the footsteps of both automotive and aerospace industries and that tools like T-RTDS will play a decisive role in this transformation. The ease of design, testing and verification of both control hardware and software that T-RTDS platform brings hold promise for enormous time savings during the development and testing of power electronics systems, increased reliability, and improved performance. In addition, educational and training benefits of RTDS should not be neglected. Our platform brings a true emulator performance, until recently available only in the high power laboratories, to the desktop thus enabling safe and fully realistic training of engineers, technicians, maintenance staff, users and power electronics students on intricate aspects of developing, using, commissioning and debugging high-power power electronics systems.

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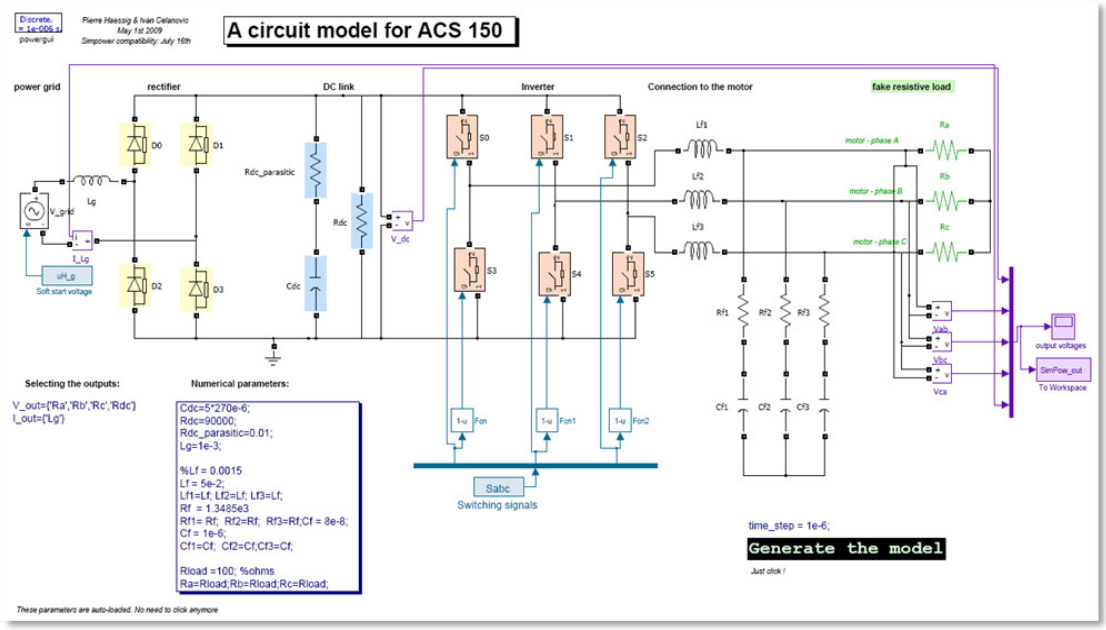

Fig. 4. Parametrized SimPowerSystem model of grid connected single-phase rectifier feeding three-phase voltage source inverter with output filter and resistive load.

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Current Trends in Power Electronic Devices in Ecological Equipment

Slobodan Vukosavić

***Abstract*—Emerging technologies for removing pollutants from waste gasses, released by industry and power plants, provide the means for removing COx, Nox, sulfur and fine dust particles. These technologies impose very stringent requirements on the power supply. The choice of the high-voltage supply can play an important role in the optimization of electrostatic precipitators. Widely discussed, the environmental pollution problems are the outcome of the world wide increase in energy consumption and industrial growth. The overall amount of waste gasses has increased, including the emission of fine, 1–50 μm particles, particularly harmful and being a well known health risk. Therefore, both large industrial sites and the power plants require dust cleaning equipment and on-line pollution control. Automated control is required for the equipment to operate on its own, without the need for a continuous operator intervention. Control goals include the need to meet the environmental regulations, keeping at the same time the power losses and the overall energy consumption under control, in order to reach the energy efficiency goals. In this article, an overview of electric filter performance problems is discussed, and the summary of available technologies and solutions is outlined. Experimental data is obtained from TE Morava, Svilajnac, where concurrent tests have been performed with conventional, 50 Hz power supply, and with high frequency power supply.**

***Index Terms*—Electrostatic precipitation, waste gasses, pollution control, electro filters, power plants.**

I. Introduction

CONTEPMPORARY dust cleaning equipment comprises electrostatic precipitators (ESP), forcing the waste gas to flow between large electrode plates, exposed to pulsating DC voltages of several tens of kV. Exposure to high strength electric field charges dust particles and they migrate towards the collecting plate, which is the positive one, and in most cases grounded. The other, negative electrode is attached to the negative supply rail of the controllable DC voltage source. The electrode surface is barbed and equipped with appropriate protruding spikes, responsible for an enhanced ionization. The migration of the charged dust particles takes place due to the electric forces exerted by the field. The drift velocity of the particles and their collection efficiency largely depend on the gas speed and the eventual turbulent flow. To enhance the filtering, the ESP comprise several (up to 8) series connected sections, wherein the output gas from the previous section becomes the input to the next. In such cases, the subsequent section may collect the dust particles that were properly ionized within the previous section, but were not collected due to an insufficient particle drift and/or too large speed of the gas stream.

In an attempt to enhance the ionization, drift speed and filtering, the voltage between electrodes can be increased. Though, along with the voltage increase, corona effects do pass into arcing. The electric arc within the filter effectively short circuits the power source and results in large currents and mass ionization. Following the arcing, the filter should be kept off the power source for several tens of milliseconds in order to allow for the ionized gasses to evacuate. Otherwise, at the reconnection without the de-ionization interval, the filter won't be able to withstand the reconnected voltage and will fall into arcing and short circuit again.

University of Belgrade and INT EE Institute developed and deployed the ESP controller [4] which integrated and coordinates control and monitoring of ESP process, rapping process, rappers, heaters and hoppers, enhancing the ESP performance and energy efficiency.

Basic features include integration of voltage control and rapping, and adaptive intermittent power supply for improved collection efficiency. Time-based and spectral analysis of voltages and currents helps the estimation of the dust layer thickness and resistivity, relevant for the voltage and rapping control. Adaptive rapping with simultaneous voltage profiling helps clean the electrodes and reduces particles re-entrance. Control is customized for input, middle and output zones of the ESP. Pre-arcing state detection based on the spectral analysis helps adjusting the operating regime so as to maximize the corona current without an excessive number of actual sparks. Back corona detection mechanism provides the input to the intermittent power supply, adjusting the dwell-intervals and relax-intervals in such way so as to optimize the collection efficiency. Controller provides internal data logging, providing the energy meter in [kWh] and the overall emissions meter in [mg/Nm^3 × h]. Controls can be set to provide desired number of arcings per minute, to maximize the cleaning efficiency disregarding the energy consumption, or to keep the emissions on the legal threshold, saving on the power consumption.

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II. Coordinated Voltage and Rapping

Keeping track of the key variables of the ESP units installed in TENT A1 and A4 since their installation, it has been found that the key requirement for the filtering efficiency is the proper operation of the input zone. The input zone of the ESP collects major part of the flying ashes weight. Collected particles are mostly of a larger diameter. Roughly speaking, the input zone collects the particles with D > 10-20 μm, accounting for more than 80% of the overall weight. Flue gas exiting the input zones caries small particles (D<10 μm) to middle zones.

Low sulfur coals in Serbia are highly resistive. Thick layers of the collected dust are highly resistive. Therefore, the spatial electric current (*electric wind*) causes significant voltage drop within the dust layer. As a consequence, resulting electric field keeps the dust sticky and presses the dust layers against the collection plates. In such conditions, rapping does not provide for the complete cleansing of the plate, and it has to be repeated more frequently. On the other hand, frequent rapping contributes to mechanical wear of the filter and increases the particle re-entrance into the gas stream.

A. Solution: Adaptive Rapping with Simultaneous Voltage Control

ESP controller [4] tracks the voltage and current waveforms during the ON pulses of the intermittent power supply, as well as during the OFF intervals. Their time change and spectral characteristics comprise sufficient information for determining the thickness of the dust layer. Hence, the rapping can be performed when really needed, avoiding in such way the unnecessary rapping instances, inherent to conventional, pre-programmed rapping sequences.

Prior to rapping, the last OFF interval of the intermittent power supply is extended, in order to relax space charges and have the dust layers ready to be detached from the plates.

As the rapping of the input zone collection plates begins, certain small voltage is re-applied, in order to reduce the particle re-entrance into the gas stream during the rapping interval.

Whenever mechanical construction of the filter allows, the rapping hammers hitting individual plates should be phase shifted, in order to avoid simultaneous rapping of all the plates at the same instant.

B. Resistivity and the Rapping Frequency

There is no fixed threshold for the dust layer thickness that will trigger the rapping. Namely, the ESP unit increases the rapping frequency in cases when the dust resistivity increases. This is done in order to increase the overall efficiency of the filter.

In cases with an increased resistivity, the plates withstand more or less the same voltage as they do with the normal resistivity of the dust. Yet, the spatial current (*electric wind*) is reduced, and the current density drops significantly below desirable 1 mA/m^2. Any attempt to increase the current by increasing the voltage results in sparking. When the input zone operates in such condition, collection is notably reduced, and vast quantity of dust passes in the subsequent sections, compromising the overall efficiency.

In order to alleviate the queer consequences, the rapping frequency is increased, giving in turn a reduced average thickness of the dust layers.

C. Hopper Control

The outcome of the ESP intermittent power supply is an increased quantity of dust collected in the input zones. At the same time, adaptive rapping with simultaneous voltage control provides for rather even surfaces and uniform thickness of the dust layers. All these consequences are positive, yet, there is one aspect that needs particular attention. Adaptive rapping and intermittent control do increase the quantity of ashes falling into the hopper during one single rapping session. Therefore, it is suggested the hopper be equipped with adequate number of sensors, securing a proper and timely operation of the dust removal system.

If the above measures are not fulfilled, there is an increased risk of the hopper getting full, which dramatically increases re-entrance of the collected particles into the gas stream. In some cases, even short circuits between the plates have been noted, with the short circuit current passing through the top dust layers of the over-spilling hopper.

III. Voltage Control in Middle and Output Zones

Majority of particles collected in the middle and the output zones are small particles, with the diameter D < 10 μm. When collected into the dust layer, residing on the collection plates, these small particles result in elevated resistance, which may exceed the resistance of the input-zone dust by an order of magnitude. The root cause for this is plane fact that most of the resistance, encountered by the *electric wind* current, passing through the dust, comes from the need for the charges to pass from one particle to another. Overall effect of highly resistive dust layers include back-corona, phenomenon which includes localized internal arcing with the dust layers and local heating, resulting in a number of craters, erupting the pre-heated dust back into the gas stream. Non-uniform *electric wind* and non-uniform electric field focuses toward the craters, jeopardizing the collection efficiency, annihilating the corona effects of the emission plates, and resulting in a very high re-entrance of the particles.

Solution

ESP relieves the back corona effects by the adaptive intermittent control and the proper rapping. Intermittent power supply provides the relax intervals with no voltage, their duration being several tens of milliseconds. These intervals proved to be an adequate prevention of back-corona effect. The ON dwell interval, wherein the proper voltage is applied between the electrodes ranges from several tens to several hundreds of milliseconds. With an increased resistivity of the ashes, the *electric wind* and electric field, initially

homogenous, tends to deteriorate and focus towards hot spots that are being formed within the dust layer. Continued, uninterrupted power supply would give a rise to forming the craters. On the other hand, brief OFF intervals are used to relax the hot spots and insure a homogenous field at the beginning of the next ON pulse.

Although the relaxation OFF state proved useful in fighting the back corona, its extensive use over prolonged intervals of time reduces the average current density and hence, the collection efficiency. Therefore, duration of ON and OFF intervals has to be adjusted on-line, in order to suite to the best possible extent the operating regime and filtering goals.

ETF2005 controller utilizes DSP technology to decode and identify the signs of the back corona within the voltage and current waveforms. The current spectrum during the ON dwells and the voltage waveform during the relax-OFF intervals comprise sufficient information for the on-line adjustments of the intermittent power supply.

A. *Rapping of the Output Zone*

The particles re-entering the gas stream during rapping of the output zones cannot be collected further on, and they make part of the final emission, ending in the chimney.

Solution

The rapping frequency of this zone is reduced to the indispensable minimum. The need for the rapping in this zone is detected through ESP algorithm for detecting the thickness of the dust layers. When the rapping command is generated for the output zone, all and any other rapping processes are postponed, in order to avoid simultaneous rapping of the output zone and other zones. In such way, the adverse consequences of the output zone rapping are minimized.

B. *Rapping of the Emission Electrodes*

Collection efficiency relies on the abundance of ions, generated by negative corona on the emission electrodes. These electrodes get dusty as well, yet to a much lower extent. Though, even a small veil of dust increases the radius of the electrode curvature, reduces the peak values of the electric field, and diminishes the overall corona and current. Therefore, proper rapping of the emission plates proves an essential role.

Solution

Analysis of the voltage and current waveforms provides for the indication of the emission electrodes status. The need for rapping is detected and scheduled. In most cases, emission electrodes are to be rapped more frequently than the collection plates. Rapping of the emission plates contributes only a small amount of particles re-entering the gas stream. Therefore, their rapping can be made more frequent and suited to the actual needs. The rapping does increase the number of sparks per minute. Therefore, whenever possible, the rapping of emission electrodes coincides with the rapping of collection plates.

IV. HIGH FREQUENCY ESP UNITS

Conventional 50 Hz design had been predominant solution for controlling the particulate emission from large electrostatic precipitators. Although capable to reach removal efficiencies up to 99.8%, 50 Hz design suffers a number of drawbacks, leading to poor energy efficiency, very large size of electrode plates, and it cannot compete with the high frequency HFESP. Resulting voltages and currents obtained with conventional ESP units are presented in Fig. 1. Essentially, the plates are supplied with rectified 50 Hz waveform. Therefore, the voltage pulsates at a pace of 100 Hz, passing quickly the crest value and falling down into dale. Hence, the time interval when the instantaneous voltage is close to the breakdown value, leading to a rich ionization and efficient precipitation, is very short. In brief, the ESP filters only at the peaks of the voltage crest, while operating idle in between the two 10ms spaced crests.

With conventional 50 Hz design, the output DC current is discontinuous, depending on the thyristor firing angle. The input line current is therefore distorted and lagging. As a consequence, the input power factor is very poor, with a high harmonic distortion in the mains supply. Reactive and apparent power are very large, with $\cos(\varphi) < 0.65$, whilst power factor $\lambda = P/S < 0.5$. On the other hand, the HFESP high frequency supply has diode rectifier in input stage with $\cos(\varphi)$ above 0.95 and power factor above 0.75.

During the intermittent operation of conventional 50 Hz system, the ESP pulsations reflect directly to the main 6kV/0.4kV transformer, supplying the whole ESP; as the system does not have any intermediate filters or intermediate DC-link. Low frequency (3–10 Hz) pulsations introduce a flicker, mechanical stress and audible noise. These problems are resolved with HFESP, by adopting a 3-phase rectifier, turning the 3x400 V, 50 Hz main supply into a stable DC-link voltage, followed by a 10–20 kHz IGBT H-bridge.

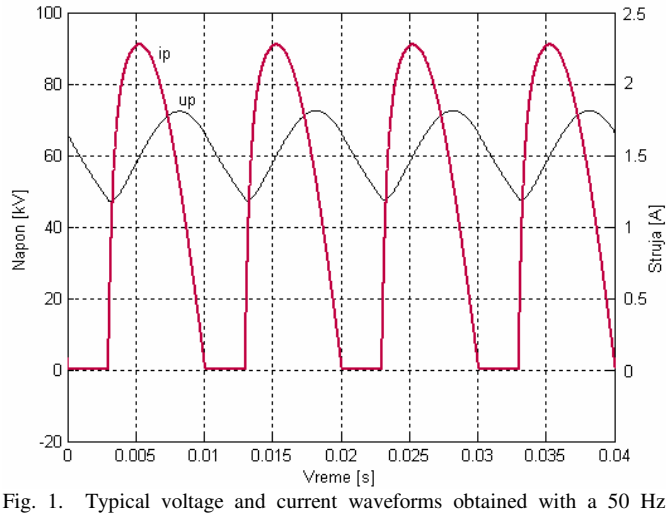

Fig. 1. Typical voltage and current waveforms obtained with a 50 Hz supplied, SCR driven ESP.

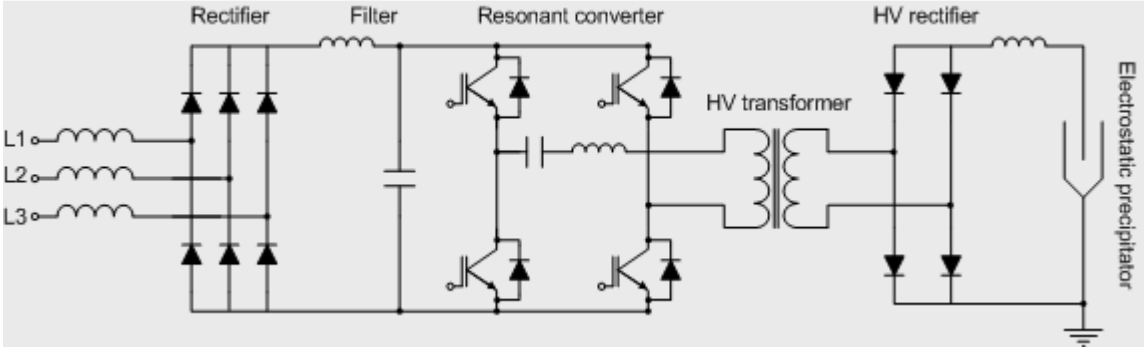

Fig. 2. High frequency ESP supply.

The efficiency of the precipitation can be increased by providing the power supply which keeps the voltage closer to the breakdown threshold over longer time intervals. With f = 10 kHz supply of the transformer, the rectified pulses at the output would be spaced 50 μs. In such case, due to a finite capacitance of the plates and the associated low pass filtering, the voltage across the plate would be almost ripple-free, without any significant crests and deeps. As a consequence, it would be possible to control the plate voltage more accurately, and keep it next to the breakdown level almost at all times.

In Fig. 3, simplified electrical schematic of the high frequency ESP supply is shown. It comprises:

- Three phase diode rectifier,
- IGBT H bridge,
- High frequency – high voltage transformer,
- High voltage, high frequency diode rectifier,
- Digital Voltage, rapping and heating Controller & Integrated PLC.

HFESP (high frequency ESP power supply and control) require a lower size and weight of electrodes, offers significant energy savings, prevents back corona, brings up a very fast reaction to flashover, results in a much higher high power factor, and has a transformer/rectifier set several times smaller and lighter compared to traditional 50 Hz design. Compared to conventional 50 Hz power supply, the HFESP package offers a significant weight and size reduction. For the ratings of 75 kV and 1000 mA, the weight of the complete system is some 300 kg, which can be installed directly on ESP roof. Notice at this point that the 50 Hz transformer only weighs over 1500 kg.

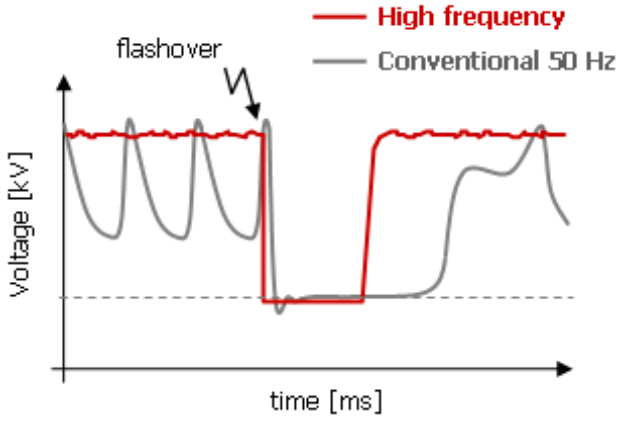

Fig. 3. HFESP reaction to the flashover.

Development and deployment of HFESP units rated 1000 mA and 2000 mA is performed at the Department of Electrical Engineering, University of Belgrade. Key element of any ESP is the proper control, allowing for the proper corona control, sufficient ionization, and the suppression of the back corona effect. Digital Voltage Controller represents the most important component of the HFESP device. It is developed on the bases of the last generation Digital Signal Processors, and comprises the proprietary adaptive algorithm of voltage control, tested at major Serbian thermal power plants and confirmed a superior particle filtering and energy efficiency performance.

Controller has a number of operating modes. One of them is the adaptive-intermittent mode of power supply. Result is energy saving and improved collection efficiency. This algorithm eliminates the back corona risks, and re-entry of collected particles. Due to adaptive algorithm of intermittent power supply, digital Voltage Controller maintains the emission under required 50 mg/Nm^3, reducing at the same time the power losses and the power consumption.

With the power supply no longer dependent on the mains frequency, the response time of the system will be shortened by an order of magnitude. The HFESP reacts in hundreds of microseconds, and it quickly minimizes the adverse effects of flashover, such as the short circuit current spikes, massive ionization, and a significant de-ionization time. As a consequence, the HFESP-controller precipitator can operate much closer to the breakdown voltage, with a very low incidence of flashover, increasing thus the particle filtering. With the HFESP high frequency supply, reaction time is below 500 μs. Conventional 50 Hz supply has the reaction time of 10 ms or more. Result is a significant improvement of precipitator performances in terms of energy saving and improving the collection efficiency.

Very fast microprocessors can provide real time parameter estimation of the DC-current spectrum, which allows back corona detection, estimation of the dust layer thickness, early corona detection and prevention of arcing. Hence, de-ionization intervals are rarely used, and the precipitation efficiency increases. DC-current spectrum content is detected through the parameter spectral estimation, leading to an ease in

detecting the corona phases. At the same time, this eliminates the need for the operator to adjust the references manually in cases when the coal/fuel parameters change during the operation.

For the maximum efficiency of particle collection, the ESP needs to operate as close to the breakdown potential as possible. With the highest voltage feasible and the maximum electric field, the collection efficiency improves. The collection efficiency is proportional to the square of the applied voltage.

With conventional 50 Hz system, the breakdown occurs at the crest of rectified sinusoidal voltage half-wave. Thus, amplitude of half-wave should not cross breakdown voltage. The mean voltage is lower (maximum mean value is $2/\pi \cdot U_{max}$). Therefore, the average of the squared voltage at the ESP is roughly twice lower than the breakdown voltage squared. On the other hand, the HFESP can control the voltage with a minimum voltage ripple, keeping it close to the breakdown level where needed. Hence, as a rough estimate, the HFESP offers the high voltage on the electrodes which has the average square value twice larger than the one encountered with a 50 Hz system.

High frequency power supply has a negligible ripple, below 1%, and the mean value of voltage can achieve 98.5% of U_{max}.

V. Conclusion

From the above analysis, we conclude that the HFESP bring considerable advantage in terms of cost, precipitation efficiency, energy efficiency and weight over the conventional ESP systems, based on 50 Hz SCR control. In brief, the HFESP approach results in:

- High collection efficiency
- Significant energy savings
- High power factor
- Much lower size and weight of electrodes
- Suppression of back corona
- Early corona detection, analysis and flashover suppression
- Fast recovery from arcing and a scarce needs for power down intervals
- Flexibility and modularity.

ESP controller implemented at TENT-A offers an improved collection of fine particles, improves the energy efficiency of the ESP, benefits on coordinated control of the ESP voltage, rapping and distributed heating, includes the spectrum based flashover suppression and the back corona elimination, and comprises the adaptation mechanism with respect to the fuel parameters.

Although there has been an increasing awareness of the atmospheric pollution, the tendency to limit uncontrolled emissions from all sources has become larger. Enacted legislation is continuously reviewed and is becoming more stringent.

The new control technology for electrostatic precipitators, developed at the University of Belgrade, minimizes the atmospheric pollution problem and offers a number of side benefits. The package includes the hardware and software bases for this new ESP control technology process.

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Efficiency Optimization Methods in Low-Power High-Frequency Digitally Controlled SMPS

Aleksandar Prodić

***Abstract*—This paper gives a review of several power efficiency optimization techniques that are utilizing advantages of emerging digital control in high frequency switch-mode power supplies (SMPS), processing power from a fraction of watt to several hundreds of watts. Loss mechanisms in semiconductor components are briefly reviewed and the related principles of on-line efficiency optimization through power stage segmentation and gate voltage variation presented. Practical implementations of such methods utilizing load prediction or data extraction from a digital control loop are shown. The benefits of the presented efficiency methods are verified through experimental results, showing efficiency improvements, ranging from 2% to 30%, depending on the load conditions.**

***Index Terms*—Low-power SMPS, efficiency optimization digital control.**

I. Introduction

In low-power SMPS supplying mobile devices, computers, as well as numerous other applications, digital controllers have emerged as an attractive alternative to traditionally used analog systems. The digital control offers flexibility and possibility for implementation of advanced control and power management techniques improving systems flexibility, dynamics, reliability, and power processing efficiency.

In here, the focus is on the techniques for improving the shape of the power processing efficiency curve by minimizing semiconductor losses. Conventional SMPS are usually designed to be the most efficient at the optimal operating point, defined for a specific load conditions. As a result their efficiency curve is not flat and at, certain loads, reduces to drastically low values. This presents a serious issue in modern low power systems, where the loads are frequently changing over a wide range. To minimize this problem, systems operating in two or three distinctive modes, and often combining switch mode and linear power supplies, have been developed [1]. In these systems, at medium and heavy loads the SMPS operating in continuous-conduction mode is usually utilized. At light loads, the SMPS operates in the discontinuous conduction mode, regulated through pulse-frequency modulation, and at very light loads the liner supply usually takes over. These 3-mode systems demonstrate a significant improvement of the efficiency curve over single-mode SMPS, but still have relatively large regions where the efficiency is poor.

This paper shows a set of digital-control based methods for further elevating the low efficiency regions and obtaining flatter efficiency curves. The following section briefly reviews sources of losses in low-power SMPS. In this paper, the emphasis is on the losses caused by semiconductor components that can be minimized through a design of power stage and controller, which in low-power SMPS are usually on-chip integrated and in the designer's control. In view of that, basic principles of efficiency optimization and implementation challenges are described. Sections III to V review several practical implementations of the efficiency optimization systems. In Section VI conclusions and a general comparison of the methods are given.

II. Sources of Semiconductor Losses and Principles of Optimization

Fig. 1 shows a general block diagram of a low-power dc-dc converter highlighting various sources of losses. In this SMPS, semiconductor losses are not only caused by the power switching components and gate drives but also by the power consumption of the controller itself. Due to low amounts of the processed power, in some cases, the consumption of the controller is comparable to the total amount of processed power significantly affecting the overall system efficiency. Also, in the case when a wide bandwidth current sensing circuit is used, such as in current programmed (CPM) mode

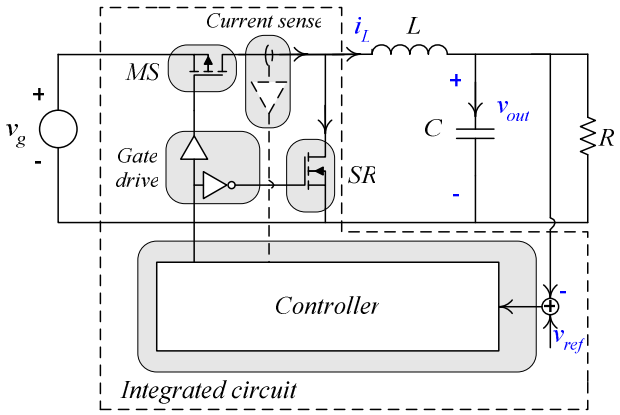

Fig. 1. A low-power dc-dc buck-based SMPS with highlighted sources of emiconductor losses (grey shaded areas).

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controllers the losses of the current sensing circuit can also be significant. Hence, a control circuit for improving efficiency needs to be implemented in a practical way, both in terms of the hardware complexity and the power consumption.

To review the task that a controller with efficiency optimization needs to complete, we can analyze the losses of power switching components.

Fig. 2 and equations (1) to (3) describe the sources of losses associated with the operation of the N MOSFET power transistor.

The losses of the gate drive circuit, P_{gate}, can be approximate as [2]:

$$P_{gate} = V_{gate} Q_g f_s \tag{1}$$

where V_{gate} is the gate supply voltage, Q_g is total gate charge seen by the driver, which is proportional to the transistor area, and $f_s = 1/T_s$ is the switching frequency of the converter.

The conduction losses of the transistor can be described as [2]:

$$P_{cond} = i_{rms}^2 R_{ds} \tag{2}$$

where

$$R_{ds} \approx \frac{R_{ds\_o}}{K(V_g - V_{th})}, \tag{3}$$

in (3), V_{th} is the threshold voltage of the transistor, and K is a construction constant that, for a given length, determined by the brake down voltage, is inversely proportional to the transistor area.

It can be seen that both conduction and switching losses, depend on the transistor's sizing and the gate supply voltage. Ideally, in order to maximize the efficiency, the optimizing controller needs to change one or both of these two parameters, such that, for any given operating condition, the sum of P_{cond} and P_{gate} is minimal. Accordingly, the efficiency optimization methods that, generally, can be categorized in dynamic power stage segmentation and gate voltage variation based have been developed.

In segmentation based methods, the complete power stage or just semiconductor switches are divided into parallel segments and, depending on the load conditions, the number of active segments is changed in time. Gate voltage variation based methods dynamically change V_g to achieve the same effect.

From the previous discussion the task of the optimizing controller can be recognized. It usually needs to "recognize" operating condition in the circuit and, accordingly, reconfigures the power stage and/or adjust gate drive voltage, such that the losses are minimized.

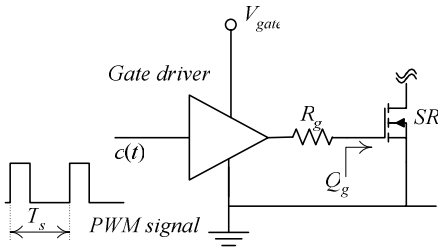

Fig. 2. N-MOS transistor and gate drive circuit.

III. Single Phase Current Programmed Mode Controller with Optimization

In the current programmed mode controller (CPM) [3] of Fig. 3, information about the load conditions in the circuit is extracted from a control loop and consequently utilized for efficiency optimization.

In this implementation [4], both the segmentation and gate-voltage variations are utilized. It can be seen that the power switches and gate drive circuit are separated into several parallel segments that can be controlled independently. The controller consists of two feedback loops, outer voltage loop implemented in a digital fashion, and the inner current loop that is analog.

The output voltage regulation is performed like in a conventional current programmed mode (CPM) regulator. Based on the difference between the output voltage and the reference, i.e. voltage error $e[n]$, the voltage loop compensator creates a digital signal proportional to the peak inductor current $i_c[n]$. This digital value is then converted to an analog equivalent by a 1-bit Σ-Δ digital-to-analog converter, whose structure is fairly simple.

The efficiency optimization is performed as follows. Based on the value of $i_c[n]$, the segment selector of Fig. 1 changes the mode of SMPS operation between 4 distinctive modes, such that the losses are minimized. The first mode of operation is designed for heavy loads, where the conduction losses are dominant. In this mode all of the power switches are active increasing the total transistor area and minimizing R_{ds} (3) of the power switches. In the second mode, for medium loads, where the switching and conduction losses are comparable, only one or two segments are active. In both of the previous two modes the gate supply voltage is at its maximum minimizing the conduction resistance. The third mode of operation is at light loads, in the region where the switching losses are becoming larger than those due to the conduction. Here, only one segment is active and the gate supply voltage dynamically changes to reduce the contribution of the switching losses at the expense of minor increase in the conduction losses. This change is performed through the gate swing controller and switch capacitor circuit (Fig. 3) providing a set of constant voltage levels. The fourth mode of operation is reserved for even lighter loads. In this mode the gate supply voltage is at the minimum level and the output voltage regulation is done through pulse frequency modulation (PFM). To initiate PFM operation the peak current controlling reference $i_{cnt}[n]$ is set at a value lower than the equivalent of the inductor current ripple. Also, instead of clocking RS latch with an external clock at the switching frequency, in the fourth mode, the latch is clocked by the ADC. As soon as the error signal becomes larger than 1 it produces a clocking signal for

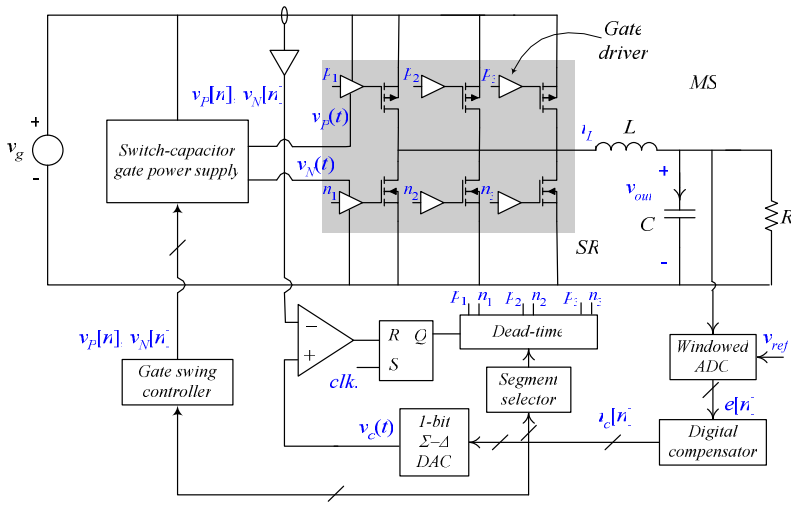

Fig. 3. Mixed-signal current programmed mode controller with efficiency optimization.

the latch.

Fig. 4 shows a comparison of the power processing efficiency between the previously presented system and a conventional CPM controlled SMPS without optimization. It can be seen that the efficiency improvement of this method depends on the operating point and ranges between few percent and more than 30%, at light loads.

It should be noted that, unlike the voltage controlled based methods discussed in the following sections, this method always guarantees that during load transients the SMPS always operates with the proper number of segments for a given instantaneous current. However, this comes at the price of a high gain bandwidth current sensor, which for some very low power high-frequency SMPS is too costly, both in terms of silicon area utilization and power consumption.

IV. Voltage Mode Controllers with Efficiency Optimization

In a typical voltage mode controlled low-power SMPS a current sensing circuit providing information about instantaneous current is usually unavailable. Hence, to obtain information about the current, in the two system presented here estimation is used. In both cases, the structure of the power stage, gate drivers, and the gate swing circuits can be similar to the one shown in Fig. 3.

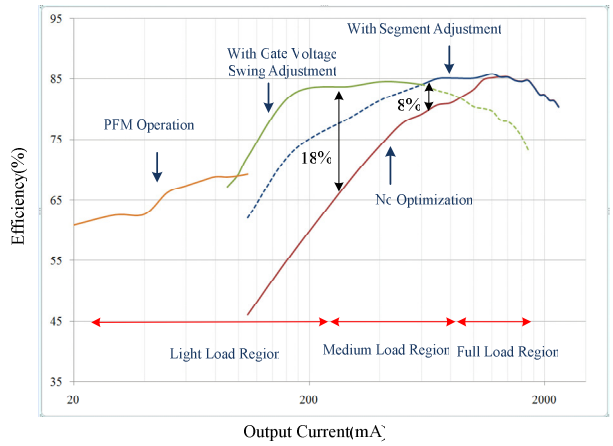

Fig. 4. Power processing efficiency comparison of a 2 A dc-dc buck converter.

A. Duty Ratio Based Optimization

The system of Fig. 5 uses information about duty ratio variation from its ideal value to estimate the load [5], and consequently, adjust the mode operation optimizing efficiency. The controller uses the fact that in a realistic SMPS the duty ratio $d[n]$ varies from its ideal due to the losses in the circuit and is usually proportional to the output load. The calculation of this discrepancy is performed with a slow ADC and an ideal duty ratio calculator, which based on the input and output voltage computes the ideal duty ratio value D_{ideal}, i.e. V_{ref}/V_g for a buck converter.

Since in most dc-dc converter input voltage usually changes slowly it is possible to use a slow and simple ADC. This method is suitable for a crude estimation of the mode of work and steady state operation.

Main limitations of such an efficiency optimization system are low precision of current estimation and a limited bandwidth. The estimation depends on the parasitic resistances and other loss contribution elements that change in time and

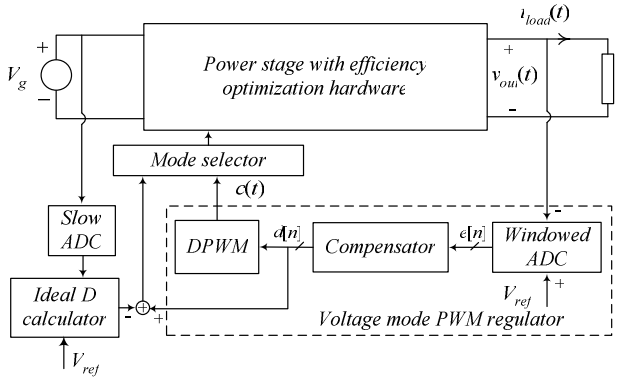

Fig. 5. Duty ratio based optimization system.

depend on the operating conditions. Also, it is highly inaccurate during load transients when, due to the compensator action, the duty ratio changes drastically.

B. Load Communication Based Predictive Efficiency Optimization

Compared to the previously presented method, a significant improvement of the speed and accuracy of the current estimation can be achieved if, to the certain extent, behavior of the load is known. The load predictive optimizer of Fig. 6 is designed for applications where the load depends on a digital data stream $s[n]$ that is fed to it. Examples include modern audio amplifiers [6], video equipment, small motors of portable devices, and other systems processing digital data streams in a predictable fashion. Here, a load predictor emulating transfer function $i_{load}[n]/s[n]$ is added to the conventional voltage loop allowing mode selector to react timely to frequent load changes.

It should be noted that, even thought, this system provides much more accurate current estimation its accuracy is still limited with the accuracy of the model used in the estimator construction.

Drawbacks of the both voltage mode methods presented here are related to a limited speed of the estimation and inaccuracy. Hence, a special attention needs to be devoted to the protection of power stage from current overstress. To eliminate situations where a small number of segments conduct a large current, possibly occurring during load transients, in these methods during each light-to-heavy load change all transistors of the segmented power stage are usually turned on. As a consequence, for highly dynamic loads the voltage mode system might be operating in suboptimal conditions over large time periods.

V. CPM Based Multi-Phase Converter with Logarithmic Current Sharing

In multiphase dc-dc systems the segmentation of the power stage is done such that several converters are operating in parallel. Due to cost constrains, implementation of the system with separate current sensing circuit in each phase is considered impractical

The principle of operation of the system with logarithmic current sharing [7] is described with Fig. 7.

The system consists of N parallel stages and operates on a similar principle as the $R/2R$ digital to analog converter

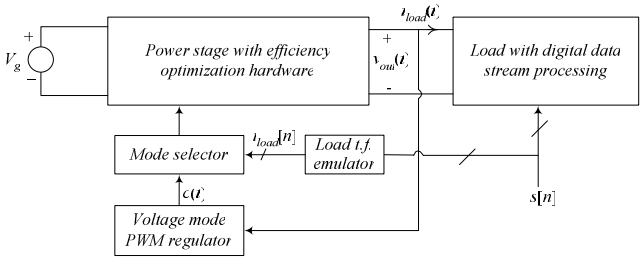

Fig. 6. Load prediction based efficiency optimization system.

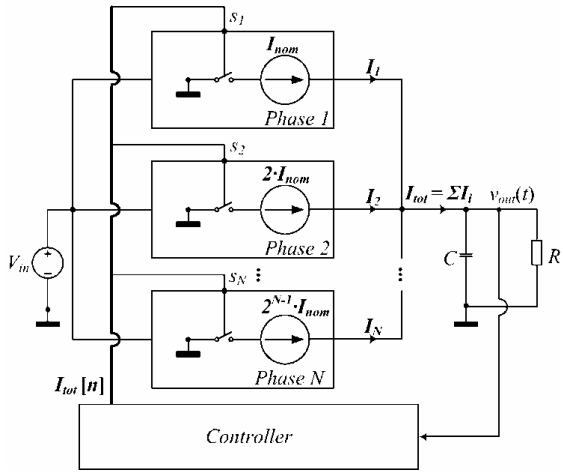

Fig. 7. Multi-phase CPM converter with logarithmic current sharing.

eliminating the need for a large number of current sensing circuits. Its parallel stages have currents that are rated in a binary logarithmic fashion. Each of the converters operates at a fixed peak efficiency point. To maintain the high efficiency over the full range of operation the binary weighted power stages are turned on and off, depending on the load requirement.

Practical implementation of this system is shown in Fig. 8. It can be seen that the controller operates in a similar fashion as the current program mode controller described in Section III. The digital voltage loop again creates a current reference, which is proportional to the load current. This current is formed by directly enabling and disabling binary weighted phases without a need for implementing a current sensor in each of the phases. The states of the phases (active or inactive) are controlled directly, by $i_{cnt}[n]$ signal in the following fashion: Its most significant bit (MSB) is connected to the largest phase, MSB-1 is connected to the second to largest phase, MSB-2 bit controls the second to largest phase, and so on.

In addition to the phases that are only operating in on or off state, with constant current, one phase equal to the smallest on/off phase and operating in an ordinary fashion, with current sensing circuit is added.

This phase provides tight output voltage regulation without the need for a large number of parallel phases. Compared to conventional multi-phase converters, the logarithmic system has a higher and flatter efficiency curve virtually over the full range of operation.

VI. Conclusions

In this paper optimization principles based on power stage segmentation and gate drive voltage variation for low power dc-dc are presented. Several practical implementations of the controllers with efficiency optimization are shown. A brief comparison between voltage and current program mode controlled techniques is given. Benefits and limitation of the methods are also presented.

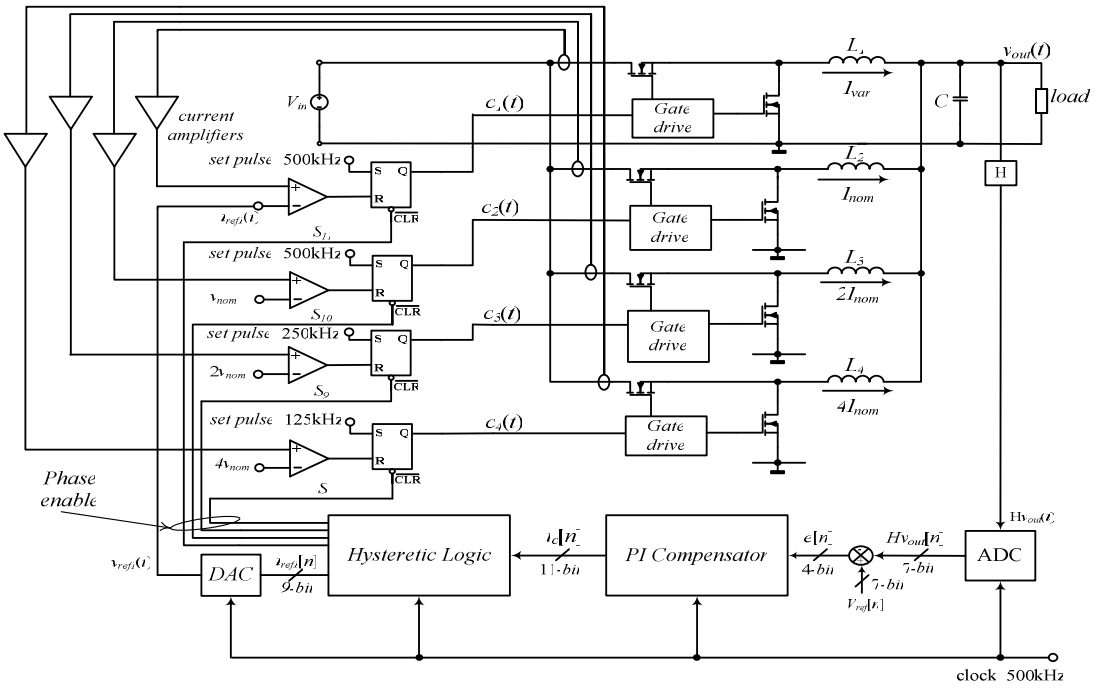

Fig. 8. Practical implementation of the multi-phase system with logarithmic current sharing.

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Experimental Analysis of the Line-Side Interphase Transformer Magnetizing Currents in Three-Phase Output Voltage Type Rectifiers

Dejana Čučak, Predrag Pejović, and Johann W. Kolar

***Abstract*—Magnetizing currents of a line side interphase transformer applied in a three phase twelve pulse voltage output type rectifiers are analyzed. Waveforms of the transformer voltages are derived. It is shown that fluxes of the core limbs contain a significant zero sequence component, resulting in a stray flux and high magnetizing currents. Application of three single phase cores is proposed. The results are experimentally verified.**

***Index Terms*—AC-DC power conversion, converters, harmonic distortion, power conversion harmonics, power quality, rectifiers.**

I. Introduction

A MAGNETIC device applied in the three phase twelve pulse voltage output type rectifier shown in Fig. 1 is analyzed in this paper. The device is designated by a dotted rectangle in Fig. 1, and it is named line side interphase transformer [1]. Three phase rectifiers of the output voltage type are analyzed in [1–4]. They are characterized by simple and robust construction, requiring only passive elements. Analysis of a voltage loaded six pulse rectifier applying sinusoidal approximation is given in [5]. The analysis applies for the continuous conduction mode. In the case resistive losses can be neglected, an exact solution for the rectifier model is presented in [6]. The analyses of [5, 6] are extended for the twelve pulse output voltage type rectifiers in [7]. Experimental verification of the sinusoidal approximation approach is given in [8].

The line-side interphase transformer input voltages v_{Tk}, $k \in \{1, 2, 3\}$, in the continuous conduction mode have twelve-pulse waveforms, obtained as linear combinations of the output voltages v_{Ak} and v_{Bk}. To obtain proper twelve-pulse voltage waveforms, the line-side interphase transformer turns ratio should be set to $p = \left(\sqrt{3}-1\right)/2 \approx 0.366$ [1]. The line-side interphase transformer output currents are i_{Ak} and i_{Bk}, while the input currents are i_k, $k \in \{1, 2, 3\}$.

Goal of this paper is to determine magnetizing currents of the line-side interphase transformer in the continuous conduction mode of the rectifier, and to analyze how does the transformer construction affect the magnetizing currents.

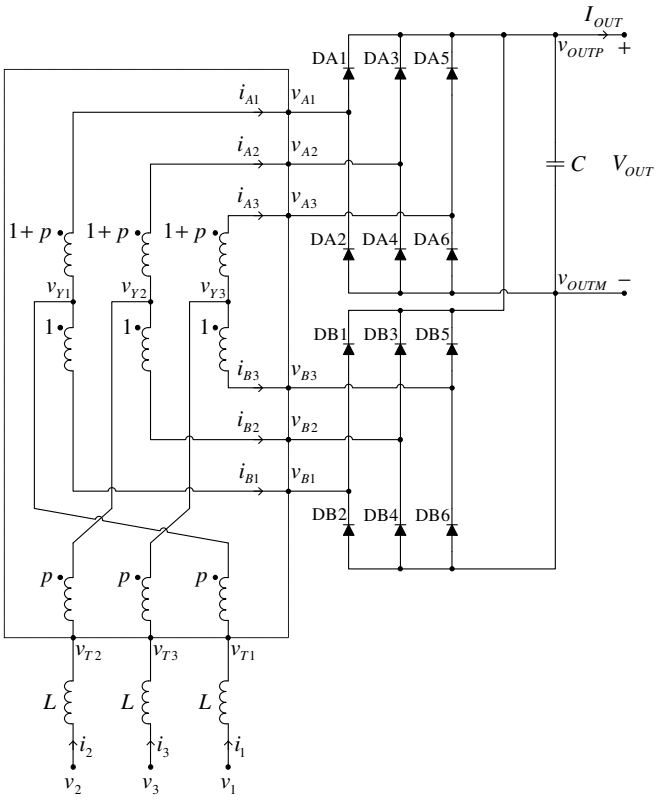

Fig. 1. The rectifier.

II. The Waveforms

It is assumed that the rectifier is supplied by an undistorted symmetrical three phase voltage system

$$v_k = V_m \sin\left(\omega t - (k-1)\frac{2\pi}{3}\right) \tag{1}$$

for $k \in \{1, 2, 3\}$. The voltage system does not contain the zero sequence component since

$$v_1 + v_2 + v_3 = 0\,. \tag{2}$$

The rectifier is connected to the mains as a three wire system, resulting in

$$i_1 + i_2 + i_3 = 0 \tag{3}$$

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according to Kirchhoff's current law. The line side interphase transformer input voltages are given by

$$v_{Tk} = v_k - L\frac{di_k}{dt}. \tag{4}$$

According to (2) and (3), this provides

$$v_{T1} + v_{T2} + v_{T3} = 0 \tag{5}$$

which is used to determine v_{OUTP} and v_{OUTM}.

It is assumed that capacitance of the filtering capacitor is large, resulting in negligible output voltage ripple. In that case, the output voltage

$$V_{OUT} = v_{OUTP} - v_{OUTM} \tag{6}$$

is assumed as constant.

The sinusoidal approximation [7, 8] assumes currents of the inductors as sinusoidal, specified by

$$i_k = I_m \sin\left(\omega t - \phi - (k-1)\frac{2\pi}{3}\right) \tag{7}$$

where I_m is the input current amplitude, and ϕ is the phase lagging of the input currents with regard to corresponding phase voltages. Values for both of the parameters are determined applying the sinusoidal approximation analysis [7, 8].

According to the equations that characterize the line side interphase transformer [7, 8], its output currents are given by

$$i_{Ak} = \frac{\sqrt{3}-1}{\sqrt{2}} I_m \sin\left(\omega t - \phi + \frac{\pi}{12} - (k-1)\frac{2\pi}{3}\right) \tag{8}$$

and

$$i_{Bk} = \frac{\sqrt{3}-1}{\sqrt{2}} I_m \sin\left(\omega t - \phi - \frac{\pi}{12} - (k-1)\frac{2\pi}{3}\right). \tag{9}$$

Waveforms of i_1, i_{A1}, and i_{B1} for $\phi = 45°$ are given in Fig. 2.

Polarity of the line side interphase transformer output currents and determine states of the diodes in the diode bridges as

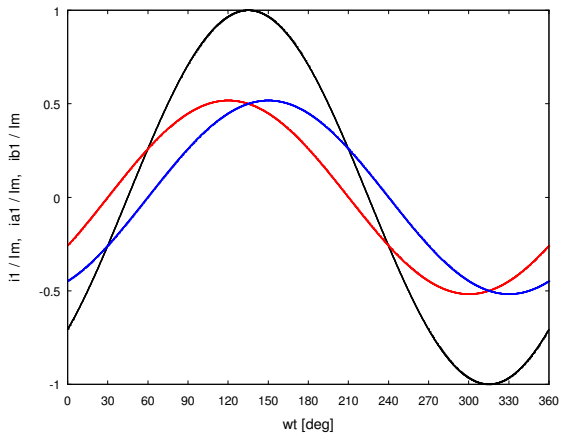

Fig. 2. Waveforms of i_1 (black), i_{A1} (red) and i_{B1} (blue).

$$DA_{2k-1} = \begin{cases} 1, \text{ if } i_{Ak} > 0 \\ 0, \text{ if } i_{Ak} < 0 \end{cases} \tag{10}$$

$$DA_{2k} = \left\{\begin{matrix} 1, \text{ if } i_{Ak} < 0 \\ 0, \text{ if } i_{Ak} > 0 \end{matrix}\right\} = 1 - DA_{2k-1} \tag{11}$$

$$DB_{2k-1} = \begin{cases} 1, \text{ if } i_{Bk} > 0 \\ 0, \text{ if } i_{Bk} < 0 \end{cases} \tag{12}$$

and

$$DB_{2k} = \left\{\begin{matrix} 1, \text{ if } i_{Bk} < 0 \\ 0, \text{ if } i_{Bk} > 0 \end{matrix}\right\} = 1 - DB_{2k-1} \tag{13}$$

for $k \in \{1, 2, 3\}$. At this point, it is convenient to define auxiliary variables that contain numbers of conducting diodes in a certain diode group as

$$DA_{UP} = DA_1 + DA_3 + DA_5 \tag{14}$$

$$DA_{DN} = DA_2 + DA_4 + DA_6 \tag{15}$$

$$DB_{UP} = DB_1 + DB_3 + DB_5 \tag{16}$$

and

$$DB_{DN} = DB_2 + DB_4 + DB_6. \tag{17}$$

In the continuous conduction mode, in each diode bridge and in each time point three diodes are conducting, thus

$$DA_{UP} + DA_{DN} = 3 \tag{18}$$

and

$$DB_{UP} + DB_{DN} = 3. \tag{19}$$

Voltages of the line side interphase transformer output terminals can take only two values, v_{OUTP} and v_{OUTM}, depending on the corresponding output current polarity. In terms of the diode state functions, this is expressed as

$$v_{Ak} = DA_{2k-1} v_{OUTP} + DA_{2k} v_{OUTM} \tag{20}$$

and

$$v_{Bk} = DB_{2k-1} v_{OUTP} + DB_{2k} v_{OUTM}. \tag{21}$$

The line side interphase transformer input voltages are determined by (4) of [8]. Summing up the input terminal voltages and applying (5), the first equation over and is obtained as

$$\begin{aligned} &\left(\left(2-\sqrt{3}\right)DA_{UP} + \left(\sqrt{3}-1\right)DB_{UP}\right)v_{OUTP} + \\ &+ \left(\left(2-\sqrt{3}\right)DA_{DN} + \left(\sqrt{3}-1\right)DB_{DN}\right)v_{OUTM} = 0 \end{aligned} \tag{22}$$

while the second one is

$$V_{OUT} = v_{OUTP} - v_{OUTM}. \tag{23}$$

As already stated, in the continuous conduction mode, in each diode bridge, in each time point, three diodes are conducting. As a consequence of Kirchhoff's current law, all three of the conducting diodes cannot be from the upper diode group (odd indexed), neither from the lower diode group (even indexed), meaning that at least one diode in each group must be conducting. Thus, for the two diode bridges there is a total of four possible combinations for the numbers of conducting diodes, as summarized in Table I. For each of the combinations there is a solution for the rectifier output terminal voltages, as given in Table I. For the input currents assumed by (7), resulting waveforms of the output terminal voltages are given in Fig. 3.

TABLE I
VALUES OF THE RECTIFIER OUTPUT TERMINAL VOLTAGES

DA_{UP}	DB_{UP}	v_{OUTP}	v_{OUTM}
1	1	$\frac{2}{3}V_{OUT}$	$-\frac{1}{3}V_{OUT}$
1	2	$\frac{3-\sqrt{3}}{3}V_{OUT}$	$-\frac{\sqrt{3}}{3}V_{OUT}$
2	1	$\frac{\sqrt{3}}{3}V_{OUT}$	$-\frac{3-\sqrt{3}}{3}V_{OUT}$
2	2	$\frac{1}{3}V_{OUT}$	$-\frac{2}{3}V_{OUT}$

After the rectifier output terminal voltages are known, the line-side interphase transformer output terminal voltages are determined according to (20) and (21), and the resulting waveforms for v_{A1} and v_{B1} are shown in Figs. 4 and 5. The line-side interphase transformer output terminal voltages determine the input terminal voltages according to (4) of [8], and the resulting waveform of v_{T1} is shown in Fig. 6, which is used in [7, 8] to complete the sinusoidal approximation based analysis, taking only fundamental harmonics of v_{Tk} into account.

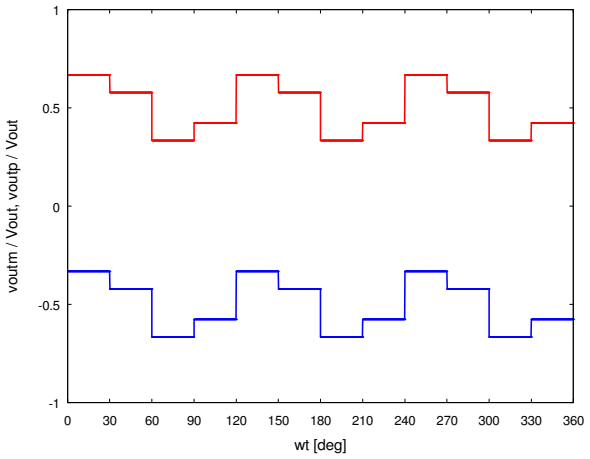

Fig. 3. Waveforms of v_{OUTP} (red) and v_{OUTM} (blue).

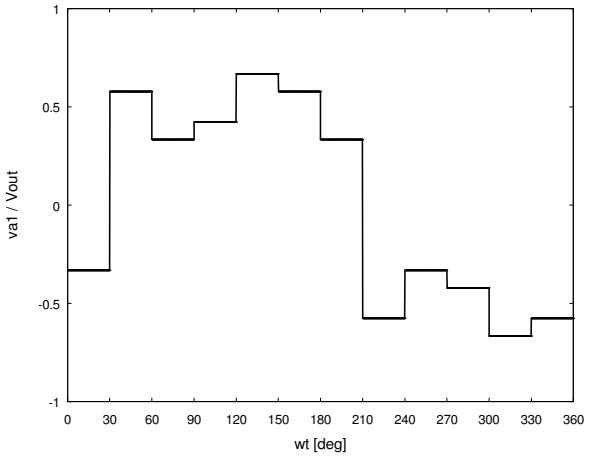

Fig. 4. Waveform of v_{A1}.

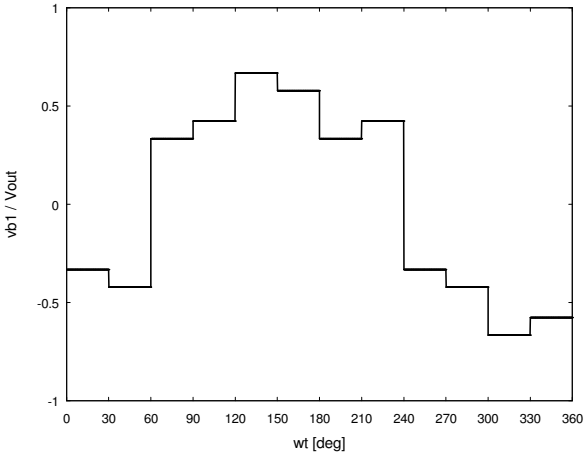

Fig. 5. Waveform of v_{B1}.

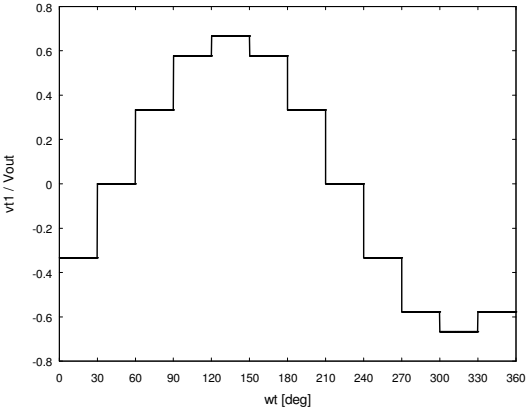

Fig. 6. Waveform of v_{T1}.

III. MAGNETIZING CURRENTS

Let us assume that the line side interphase transformer is wound around a three phase three limb core that can be modeled by an equivalent magnetic circuit shown in Fig. 7. Limb reluctance is represented by R_m, while the leakage air reluctance is represented by R_{m0}. In practice, $R_{m0} >> R_m$. Perfect coupling is assumed. The limb fluxes Φ_k are generated by magnetomotive forces F_k, $k \in \{1, 2, 3\}$. It is assumed that the magnetizing current is associated to the windings with the normalized number of turns equal to 1, actual number of turns being n. Thus, the voltages across the magnetizing windings are

$$v_{Mk} = v_{Yk} - v_{Bk} \tag{24}$$

for $k \in \{1, 2, 3\}$. It is convenient to express the magnetizing voltages in terms of v_{Ak} and v_{Bk} determined by (20) and (21) as

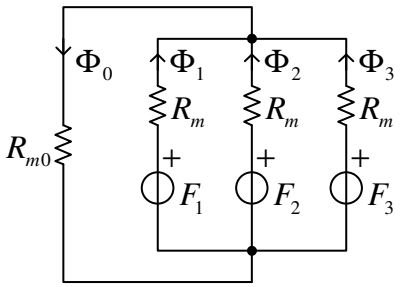

Fig. 7. Equivalent magnetic circuit for the line-side interphase transformer core.

$$v_{Mk} = \frac{v_{Ak} - v_{Bk}}{2 + p}. \tag{25}$$

Voltages across the transformer windings are obtained as time derivatives of the corresponding limb fluxes Φ_k multiplied by the corresponding number of turns of the winding, according to Faraday's law. For the magnetizing windings, this results in

$$v_{Mk} = n\frac{d\Phi_k}{dt}. \tag{26}$$

Waveforms of all three of the magnetizing voltages are depicted in Fig. 8. These waveforms result in the limb fluxes shown in Fig. 9, being determined applying (26). The system of magnetizing voltages contains significant zero-sequence component, shown in Fig. 10.

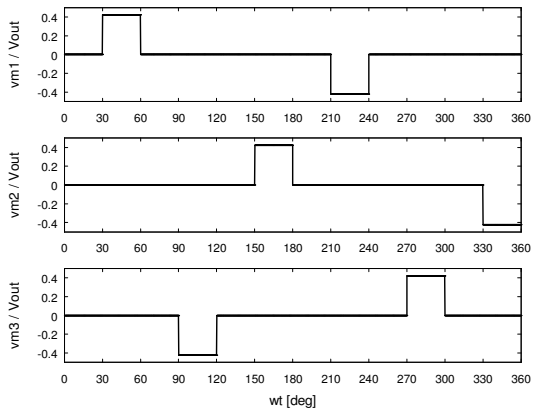

Fig. 8. Voltages across the magnetizing windings.

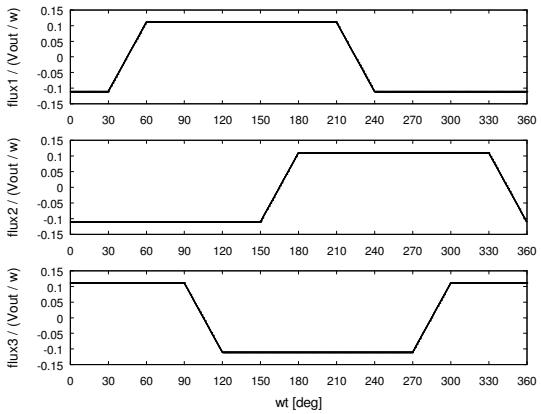

Fig. 9. Waveforms of the limb fluxes.

Conservation of flux yields

$$\Phi_0 = \Phi_1 + \Phi_2 + \Phi_3 \tag{27}$$

resulting in a significant stray flux with the waveform shown in Fig. 11. Since $R_m << R_{m0}$, magnetomotive force drop across R_m reluctances is negligible in comparison to the magnetomotive force drop across R_{m0}. In this manner, the magnetomotive forces required to magnetize the core are obtained as

$$F_1 = F_2 = F_3 = R_{m0}\Phi_0. \tag{28}$$

The magnetomotive forces are obtained as a product of the magnetizing current and the number of turns of the magnetizing winding,

$$F_k = n\, i_{Mk}. \tag{29}$$

Taking the time derivative of (28) yields

$$\frac{dF_k}{dt} = R_{m0}\frac{d\Phi_0}{dt}. \tag{30}$$

Substituting (26), (27) and (29) into (30) provides

$$\frac{di_{Mk}}{dt} = \frac{1}{L_{mzs}}\frac{v_{M1} + v_{M2} + v_{M3}}{3} \tag{31}$$

where

$$L_{mzs} = \frac{n^2}{3R_{m0}} \tag{32}$$

is the zero sequence magnetizing inductance.

According to (31), all three of the magnetizing currents have the same waveform, proportional to the waveform of Φ_0 given in Fig. 11, but with the amplitude equal to

$$I_{m\max} = \frac{\pi}{6\left(3+\sqrt{3}\right)}\frac{R_{m0}}{n}\frac{V_{OUT}}{\omega}. \tag{33}$$

To reduce the magnetizing currents, R_{m0} should be reduced as much as possible. This may be achieved applying five-limb core, core of the shell type, or applying three single-phase cores.

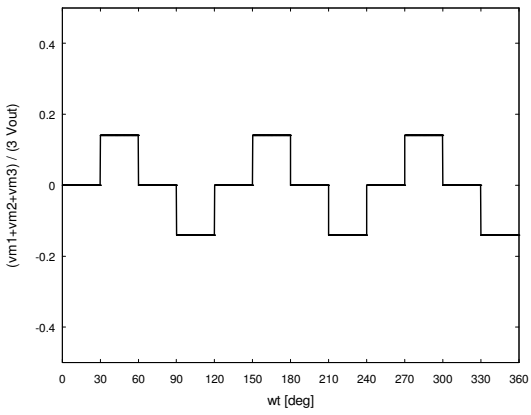

Fig. 10. Zero sequence of the voltages across the magnetizing windings.

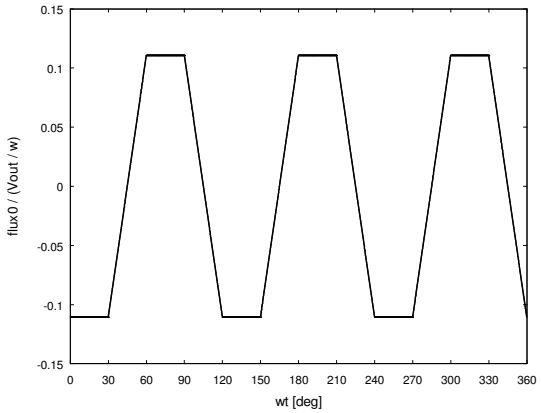

Fig. 11. Waveform of the stray flux.

IV. VA Rating of the Line-Side Interphase Transformer

After the voltages and currents of the line-side interphase transformer are known, its VA rating can be determined. According to [9], in the case three single-phase cores are applied the VA rating of each core is

$$S_{T1} = \frac{6+3\sqrt{2}-\sqrt{6}}{1728}\pi^2 P_{OUT} \approx 4.45\%\ P_{OUT}\,. \tag{34}$$

It should be underlined here that the result of (34) is applicable only if the rectifier is designed to operate at a fixed operating point, i.e. fixed output power. If the operating point varies, the VA rating is higher, since at low output currents the output voltage is high, resulting in increased flux stress on the core, while at high output currents the flux in the core is reduced, but the RMS values of the currents in the line-side interphase transformer windings are increased. Thus, the core should be dimensioned not to saturate at low output currents, while the windings should be dimensioned not to overheat at high output currents. These requirements cause the VA rating to be higher than specified by (34), the increase being dependent on the operating point variation.

Normalized rated power of the inductors is computed according to [9] as

$$S_L = \frac{1}{4}J_m^2 = \frac{\pi^2}{288\left(2-\sqrt{3}\right)}J_{OUT}^2 \tag{35}$$

and it cannot be expressed as a single-variable function of the output power.

V. Experimental Results

To verify the results, two rectifier models were made, one using the line-side interphase transformer with a three-phase core, and the other one with three single-phase cores. The rectifiers were operated with $V_m = 32\ \mathrm{V}$, and the diagrams were recorded at $I_{OUT} = 5\ \mathrm{A}$, where the three-phase core provided $V_{OUT} = 20\ \mathrm{V}$, while the version with single-phase cores provided $V_{OUT} = 27\ \mathrm{V}$, indicating significantly increased efficiency.

Waveforms of i_{A1}, v_{A1}, i_{A2}, and v_{A2} are shown in Fig. 12 for the three-phase core version, while for the single-phase version the same waveforms are given in Fig. 13. The waveforms of v_{A1} and v_{A2} are in agreement with the predictions of Fig. 4, except for the slight curving caused by the resistive voltage drop on the windings, pronounced in the three-phase core version. Currents i_{A1} and i_{A2} are significantly more distorted in the three-phase case in comparison to the single-phase case. Waveforms of $i_{A1}+i_{A2}+i_{A3}$ and $i_{B1}+i_{B2}+i_{B3}$ that contain the waveform of the magnetizing currents, accompanied by the waveforms of v_{M1} and v_{M2} are shown in Figs. 14 (three-phase core version) and 15 (three single-phase cores version). Comparing the waveforms, it is concluded that in the three-phase version the magnetizing currents are reduced for about 27 times, resulting in reduced ringing currents and losses. The waveforms of v_{M1} and v_{M2} are distorted in comparison to the prediction of Fig. 8 for the resistive voltage drop across the windings, not included in the analysis. The distortion is higher in the three-phase case.

Regardless the fact that losses in the transformer windings were not taken into account in the analysis, the idealized analytical approach successfully predicted relevant behavior

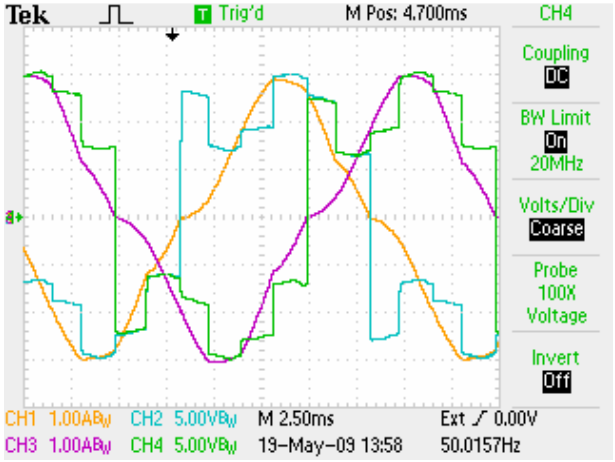

Fig. 12. Waveforms of i_{A1}, v_{A1}, i_{A2} and v_{A2}, three-phase core.

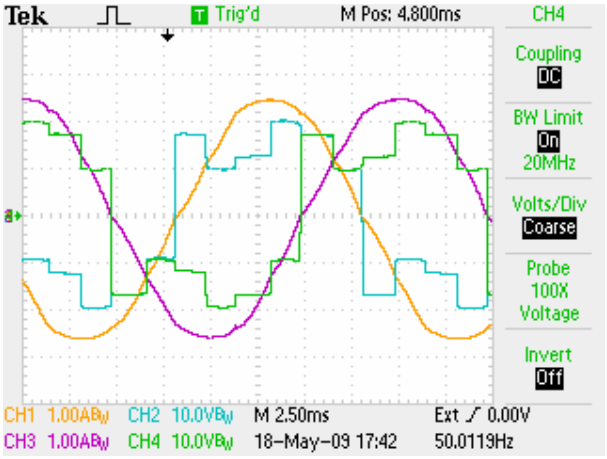

Fig. 13. Waveforms of i_{A1}, v_{A1}, i_{A2} and v_{A2}, three single-phase cores.

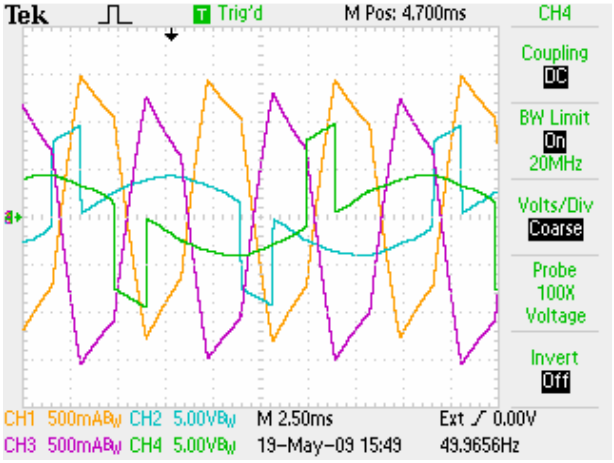

Fig. 14. Waveforms of Σi_A, Σi_B, v_{M1}, v_{M2}, three-phase core.

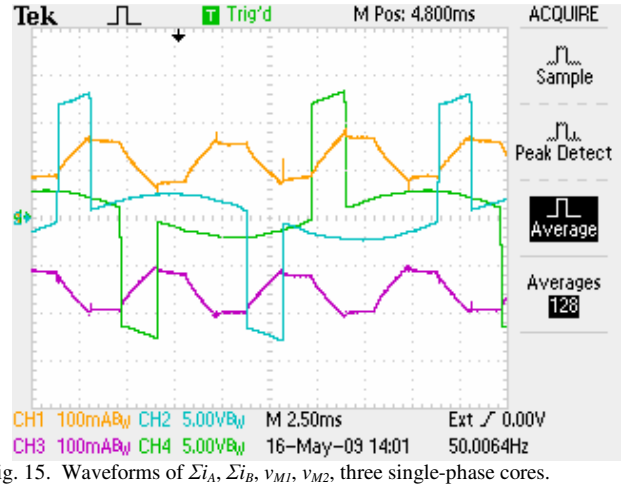

Fig. 15. Waveforms of Σi_A, Σi_B, v_{M1}, v_{M2}, three single-phase cores.

of the converter, including the magnetizing currents.

VI. Conclusions

Magnetizing currents of the line side interphase transformer in a twelve pulse three phase voltage output type rectifier are analyzed in the paper. Waveforms of the transformer voltages are derived assuming sinusoidal input currents and neglecting losses in the rectifier components. Integrating the transformer voltage waveforms, fluxes in the core limbs are determined. It is shown that the fluxes contain a significant zero sequence component, resulting in a stray flux and high magnetizing currents. In the experiment, the magnetizing currents caused ringing zero sequence currents that degraded the rectifier efficiency. To control the stray flux and to reduce the magnetizing currents, either five limb core, shell type core, or three single phase cores should be applied. Application of three single phase cores is experimentally verified as an appropriate solution.

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Comparative Study of Two Multilevel Converters for Envelope Amplifier

Miroslav Vasić, Oscar Garcia, Jesus Angel Oliver, Pedro Alou, Daniel Diaz, and Jose Antonio Cobos

***Abstract*—Modern transmitters usually have to amplify and transmit signals with simultaneous envelope and phase modulation. Due to this property of the transmitted signal, linear power amplifiers (class A, B or AB) are usually used as a solution for the power amplifier stage. These amplifiers have high linearity, but suffer from low efficiency when the transmitted signal has low peak-to-average power ratio. The Kahn envelope elimination and restoration (EER) technique is used to enhance efficiency of RF transmitters, by combining highly efficient, nonlinear RF amplifier (class D or E) with a highly efficient envelope amplifier in order to obtain linear and highly efficient RF amplifier. This paper compares two solutions for the envelope amplifier based on a combination of multilevel converter and linear regulator. The solutions are compared regarding their efficiency, size and weight. Both solutions can reproduce any signal with maximal spectral component of 2 MHz and give instantaneous maximal power of 50 W. The efficiency measurements show that when the signals with low average value are transmitted, the implemented prototypes have up to 20% higher efficiency than linear regulator that is used as a conventional solution.**

***Index Terms*—Power amplifiers, Kahn's technique, envelope amplifiers.**

I. Introduction

IN the modern world of today, the demand for broadband and wireless services is growing on a daily basis. One of direct consequences of this growth is certainly the growth of the networks that have to provide these services and the problem is their energy consumption. Some estimations showed that a 1% of planet's global energy consumption in 2007 was made by telecommunication industry [1]. In [2] is explained that the efficiency of the first generation 3G radio base stations is just few percents, and that the efficiency of the employed power amplifiers is just 6%. The impact of power amplifier's efficiency can be seen in the information that if the power amplifiers could improve its efficiency by 10% the overall efficiency would be raised by 6%.

One of the reasons for very low efficiency of linear power amplifiers is the transmitted signal's statistics. The major part of the transmitted signals have high Peak-to-Average-Power-Ratio (PAPR) and it means that the working point of linear power amplifiers usually is area where they have low efficiency. The Kahn envelope elimination and restoration (EER) technique is used to enhance efficiency of RF transmitter. Fig. 1 shows block diagram of one EER transmitter. This technique combines a highly efficient, but nonlinear RF PA (class D or class E for example) with a highly efficient envelope amplifier to implement high-efficiency linear RF PA [3].

An envelope amplifier based on a multilevel converter in series with a linear regulator is presented in [4]. It is shown that this solution can reproduce 2 MHz sine wave, with low spectral distortion and providing 50 W of instantaneous power. This topology operates at relatively low switching frequency and without additional output filter because the linear regulator filters all the noise and ripple that comes from the multilevel convert.

In this paper two different implementations of this topology are compared regarding its efficiency, complexity, size and possibility of integration.

II. Architecture of the Envelope Amplifier

The topology that is used for the envelope amplifier consists of a multilevel converter in series with a high slew rate linear regulator. The main idea of the solution can be seen in Fig. 2. The multilevel converter has to supply the linear regulator and it has to provide discrete voltage levels that are as close as possible to the output voltage of the envelope amplifier. If this is fulfilled, the power losses on the linear regulator will be minimal, because they are directly proportional to the difference of its input and output voltage. However, in order to guarantee correct work of the linear regulator, the output voltage of the multilevel converter always has to be higher than the output voltage of the linear regulator. Similar solution,

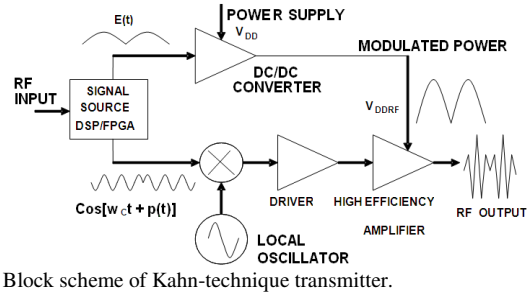

Fig. 1. Block scheme of Kahn-technique transmitter.

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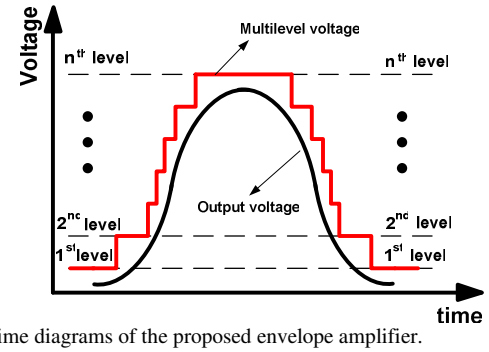

Fig. 2. Time diagrams of the proposed envelope amplifier.

but for lower frequencies and higher power is presented in [5].

There are several possibilities to implement the multilevel converter for this application. The first one, architecture one, is to provide all the voltages that are needed at its output, and then to use a switching network as an analog multiplexer to select each one when it is necessary, Fig. 3. The second solution is to use independent voltage cells that are put in series, and then to generate the output voltage as a combination of its voltages. These cells can be implemented to give just positive voltage (two-level cell, architecture two), or to produce positive and negative voltage (three-level cell, architecture three), Fig. 4.

Due to the independent voltages that have to be produced, it is obvious that it is required to introduce a single-input multiple-outputs stage that will generate all the needed voltages. In the case of the first multilevel solution, the output voltages are the voltage levels that are needed in the system, and they are all referenced to the ground. When the multilevel converter is implemented with two-level and three-level cells, the output voltages should be isolated and referenced to the different grounds. The cell's input voltage does not need to be regulated accurately, because the fine regulation will be done by the linear regulator that is connected in series with the multilevel converter. Additionally, in the case of three-level cell, the cell's input source has to be bidirectional, because, depending on the state of the switches, the source will sink or source the current to the load.

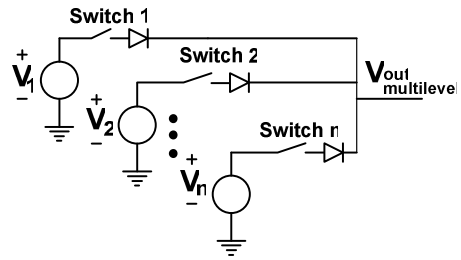

Fig. 3. Multilevel converter realized with independent supplies and analog multiplexer.

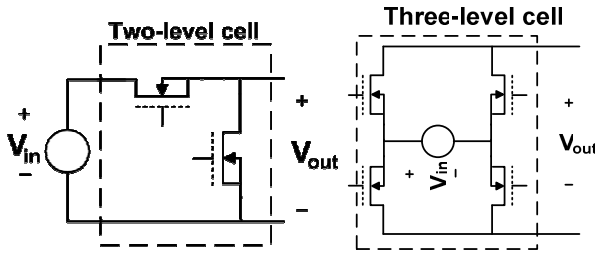

Fig. 4. Voltage cells that could be used as a solution to implement a multilevel converter.

In this paper solutions that employ architectures one and two are compared.

In order to provide fair comparison of two different implementations, both solutions have the same number of levels and the same voltage distribution. The voltage levels are selected in order to maximize overall efficiency and the optimization of the voltage levels is explained in [4].

The envelope amplifiers that have been prototyped have following properties:

- The multilevel converter can reproduce three voltage levels
- The input voltage is 24 V
- The output voltage can be 12 V, 18 V or 24 V

The class E amplifier that is used for transmitter's phase modulation is supplied by the envelope amplifier and it behaves as a resistive load, approximately 12 Ω.

The advantage of this topology is that it provides high dynamics of the output voltage with increased efficiency comparing with linear regulator that is supplied with constant voltage and that its control is very simple and robust. The drawback is that each stage of the system (multiple-output converter, multilevel converter and linear regulator) needs to have very high efficiency, because the total efficiency is the product of individual efficiencies. However, it is still possible to achieve high overall efficiency, as it will be seen later.

III. Implementation of the Architecture One

The multilevel converter for the architecture one is implemented using two converters based on switching capacitor in combination with an analog multiplexer. Both converters have the same topology and divide the input voltage [6], Fig. 5. The first converter is supplied by connecting its input terminals to the ground and 24 V voltage and its 12 V output voltage is referred to the ground. The second converter is supplied by connecting its input terminals between 12 V and 24 V. Its output voltage is 6 V, but this voltage is referred to the 12 V input, therefore, this output is, actually, 18 V output referring it to the ground, Fig. 6. The 24 V input voltage is directly provided to the analog multiplexer. One of the advantages of this solution is high efficiency that can provide

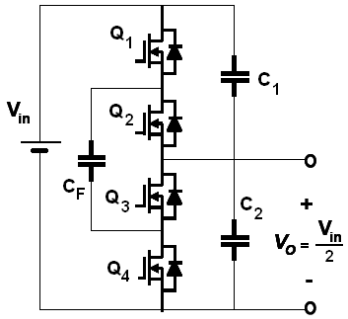

Fig. 5. Voltage divider implemented with switching capacitor converter.

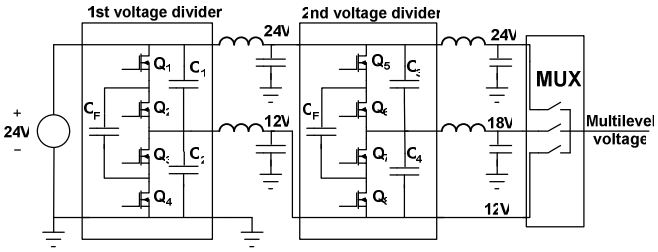

Fig. 6. Block diagram of the multilevel converter for architecture two.

converters based on switching capacitor and that it does not need any huge inductive component, and therefore it can be integrated easily. The disadvantage is that the switching noise or any noise that comes from the input voltage is poorly filtered and this could be a problem for the linear regulator depending on its bandwidth. In order to decrease the propagation of the switching noise to the output and to other system parts, small LC filters are introduced at the outputs of these two converters.

As it is shown in Fig. 3, the analog multiplexer consists of set of switches that are generally realized as a MOSFET in series with a diode. The diode is necessary in order to guarantee that independent voltage sources cannot be short-circuited through MOSFET's parasitic diode. However, in the case of 24 V voltage source only a MOSFET can be used, because there is not any higher voltage source in the system. Similar conclusion can be made in the case of 12 V source where only a diode can be used.

IV. Implementation of the Architecture Two

Fig. 7 shows the block diagram of the implemented envelope amplifier based on architecture two. As it can be seen, a single-input multiple-outputs converter is used to produce several independent voltages that are later combined by using two-level voltage cells.

In the case of the implemented solution in this paper, the single-input multiple-outputs converter is a flyback converter with three outputs. There are two 6 V outputs and one 12 V output. The minimum voltage of the multilevel converter is 12 V and, therefore, only the 6 V outputs are connected to two-level cells.

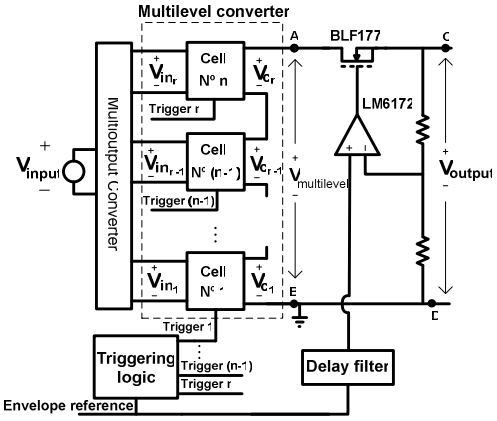

Fig. 7. Block diagram of the implemented architecture.

V. Control of Envelope Amplifier

In both implementations of the envelope amplifier there can be recognized three stages. The first stage is a single-input multiple-output converter that has to provide independent voltages. The second stage applies summation or multiplexing of the independent voltages in order to produce voltage levels needed by the linear regulator. The last stage is the linear regulator that in its output reproduces the voltage needed by the power amplifier.

The first stage works in open loop when it is implemented with switching capacities. The switching frequency can be very low in order to maximize the efficiency of this stage. However, when a flyback converter is used, the first stage is controlled by a voltage feedback from one of flyback's outputs, because all the other outputs will follow the controlled one. The bandwidth of this stage does not have to be high; therefore, the switching frequency of the multiple-outputs flyback can be very low in order to increase its efficiency.

The reference signal that should be reproduced is sent to the analog multiplexer or the multilevel converter through the block named "triggering logic" that consists of simple comparator logic. The each voltage level is activated when the reference signal is higher than a certain value (which is different for each voltage level), Fig. 8. Consequently, the output of the multilevel converter will have discrete levels In the case of the architecture one, the number of levels will depend on the number of the used independent voltage sources and in the case of architecture two on the number of implemented cells. Each cell inside the multilevel converter and each switch inside the analog multiplexer will switch at the maximum frequency of the reference signal. Even more, the dynamic response of the multilevel converter will depend only on the speed of the diodes and MOSFETs that are used inside the switches and cells.

The same reference signal enters in the second stage and in the linear regulator (post regulator). The linear regulator reference has to be synchronized with the output voltage of the multilevel converter in order to guarantee that the system's output voltage (between points C and D, Fig. 7) will be always lower than the output voltage of the multilevel converter (points A and B, Fig. 7) and, therefore, correctly reproduced. Due to the finite time to turn MOSFETs on and off, the output of the multilevel converter is delayed comparing it with the envelope reference, therefore, a delay filter which will compensate this delay is introduced between the reference signal and the linear regulator.

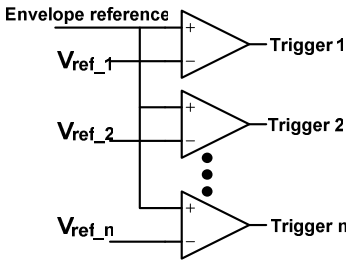

Fig. 8. Comparator logic that is used to control on/off states for each cell/switch of the multilevel converter/analog multiplexer.

VI. Designed System and Experimental Results

In order to compare two proposed architectures two prototypes of envelope amplifier have been made. The specifications for both prototypes are as follows:

- Variable output voltage from 0 V to 23 V
- The maximum instantaneous power is 50 W
- The maximum frequency of the reference signal is 2 MHz.

A. First Prototype

The first envelope amplifier prototype consists of:

- Two converters with switching capacitor (first stage)
  - Input voltage is 24 V
  - Three voltage levels are produced (12, 18 and 24 V)
  - Switching frequency is 100 kHz
  - Floating capacitor is 110 µF
  - The maximum instantaneous power is, approximately, 50 W
- Analog multiplexer (second stage)
- Linear regulator (post regulator).
  - MOSFET BLF177 as the pass element
  - Operational amplifier LM6172 for the feedback.

In Fig. 9, a photograph of the prototype is presented.

Fig. 10 shows the multilevel and system's output voltage in the case of 500 kHz and 2 MHz sine wave. However, whenever the multilevel converter changes its output voltage there is small glitch in the output voltage. The reason is the finite bandwidth of the linear regulator. Step changes of the multilevel's voltage are composed of very high harmonics that are higher than the regulator's bandwidth. Therefore, the linear regulator is not able to react and stabilize the output voltage very well in these moments. In order to make these transitions "softer", with less high spectral components, the resistance in the gates of MOSFETs that form the analog multiplexer is increased. In this way, the MOSFET's transition time is increased, and therefore the switching loss as well, but, the linear regulator can react better and the glitch in the output voltage is almost removed.

B. Second Prototype

The second prototype's specifications are as follows:

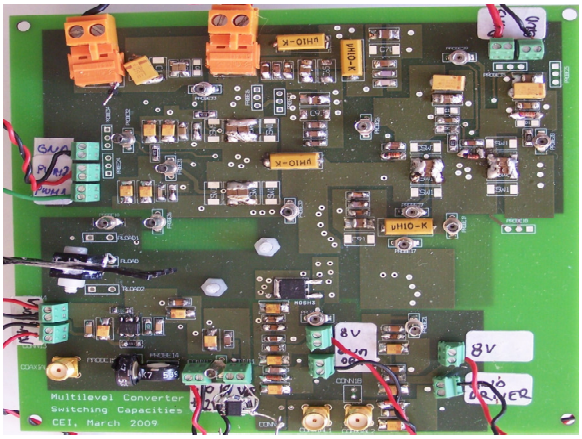

Fig. 9. Photograph of implemented multilevel converter, architecture one.

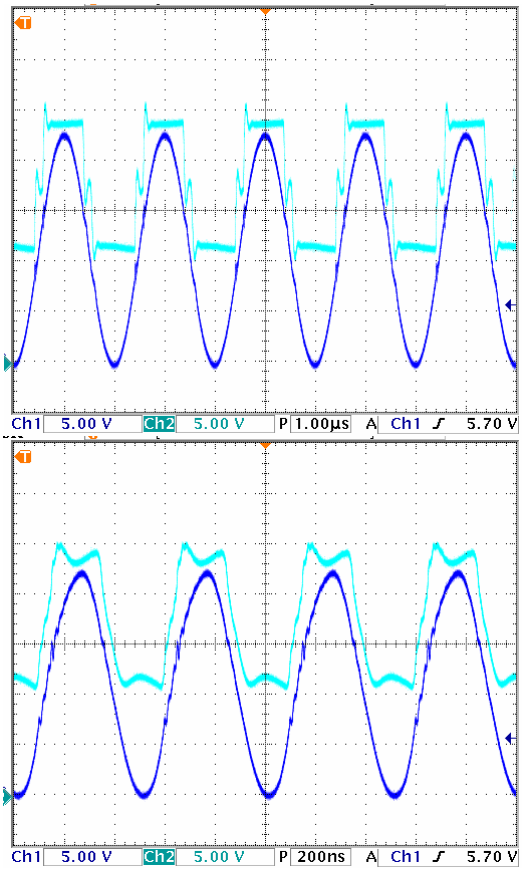

Fig. 10. Waveforms of multilevel (label 1, channel 4) and output voltage (label 2, channel 4) at 500 kHz and 2 MHz.

- single-input multiple-outputs flyback (first stage)
  - Input voltage is 24 V
  - Two 6 V outputs and one 12 V output
  - Switching frequency is 50 kHz
  - The maximum instantaneous power is, approximately, 50 W
- multilevel converter with two two-level cells (second stage)
- linear regulator (post regulator, third stage).
  - MOSFET BLF177 as the pass element
  - Operational amplifier LM6172 for the feedback

In Fig. 11 pictures of the second prototype are shown.

Fig. 12 shows the multilevel and system's output voltage in the case of 500 kHz and 2 MHz sine wave. As in the case of the analog multiplexer, it was necessary to increase the transition time of the MOSFETs that are used in the two-level cells in order to avoid glitches in the output voltage.

C. Efficiency Measurements

The efficiency of the system for both prototypes is measured for different sine waves and the results are summarized in Table I. The measured efficiency is compared with theoretical efficiency of the linear regulator supplied by a constant voltage. Both multilevel solutions have better efficiency than linear regulator when signals with small average value are transmitted, and that is mostly the case when the EER technique is applied. The efficiency of the envelope amplifier is constant (around 43% and 48%, depending on the

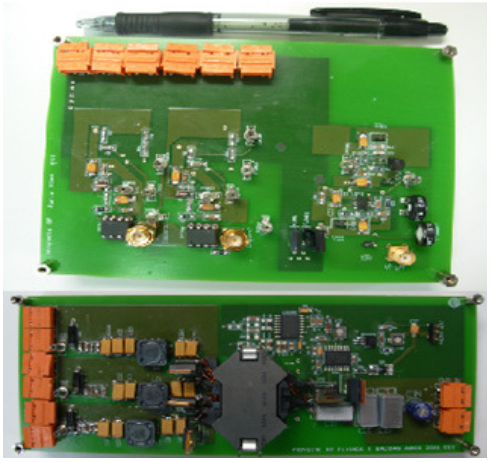

Fig. 11. Photograph of implemented multilevel converter, architecture two.

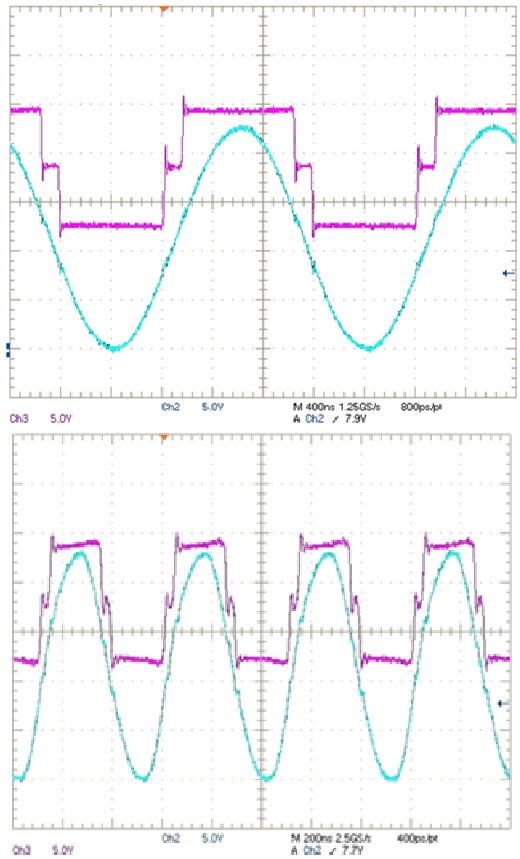

Fig. 12. Waveform of multilevel's output voltage (label 1) and linear regulator's output voltage (label 2) at 500 kHz and 2 MHz.

implementation) when small signals are reproduced, the reason is that only the 12 V cell is active, and there is not any switching losses, only conduction losses, regardless on the frequency of the sine wave. Additionally, the efficiency of the envelope amplifier implemented with switching capacitor is significantly higher than the efficiency of the envelope amplifier that is made by employing a flyback converter.

In Table IIa comparison regarding the size and weight of the realized envelope amplifier is made.

TABLE I

MEASURED EFFICIENCY OF THE IMPLEMENTED ENVELOPE AMPLIFIER FOR DIFFERENT SINE WAVES COMPARED WITH THE THEORETICAL EFFICIENCY OF AN IDEAL LINEAR REGULATOR SUPPLIED BY 23 V

Vsin(V)	Sine wave frequency (MHz)	Measured efficiency of the architecture one	Measured efficiency of the architecture two	Theoretical efficiency of an ideal linear regulator supplied by 23V
0-9	2	48.5%	44.1%	29.3%
5-14	2	59.9%	56.8%	45.9%
0-22.5	2	72.1%	69.8%	73.4%
0-9	0.5	47.9%	43.6%	29.3%
5-14	0.5	61.9%	59.5%	45.9%
0-22.5	0.5	75.7%	71.2%	73.4%

TABLE II

COMPARISON OF THE IMPLEMENTED ENVELOPE AMPLIFIERS REGARDING THEIR SIZE AND WEIGHT

	Architecture one	Architecture two
Weight[g]	215	420
Size[cm^2]	217.5	297

VII. CONCLUSIONS

In this paper two solutions for power supply for EER technique are compared. Both solutions are composed of a multilevel converter that is put in series with a linear regulator. First solution is based on the multilevel converter composed of two switching capacitor converter, and the second solution is based on single-input multiple-output flyback converter. Both prototypes can deliver up to 50 W of instantaneous power and reproduce sine wave up to 2 MHz. The system's efficiency for both solutions has been measured for the various 2 MHz and 0.5 kHz sine waves and compared with the efficiency of the ideal linear regulator. When the sine wave has small average value (what is usually the case in the case of RF amplifier) both envelope amplifiers have better efficiency up to 20% than linear regulator. It is shown that the architecture based on switching capacitor converters has better efficiency up to 4% and it is smaller and lighter. Additionally, this architecture is lighter, smaller and does not need any big inductive component comparing with flyback converter and it can be integrated easily.

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The Dependence of Resistivity on Temperature for Thin Superconductors

Constantin Blaj, Dumitru Toader, and Marian Greconici

***Abstract*—Measurements made on superconducting very thin layers are analysed by modelization using 2D FEM. The electric field distribution is established and can be seen the differences of this distribution during the superconductive transition. The calculation of the temperature variation of the resistivity is made based on measured temperature variation of the resistance, taking into account also the electro kinetic field distribution.**

***Index Terms*—Superconductivity, very thin layers, resistivity measurements.**

I. Introduction

MEASUREMENTS made in liquid nitrogen on YBaCuO samples show the transition of high critical temperature superconductors to the superconductive stage. Very thin samples (60...130 microns thickness), tapes of 5-6 mm width and 50-60 mm length are measured using V-A measurement method. To the samples are soldered electric conductors trough thin drops of silver, in order to assure good electric contacts for the electric measurements. When measuring the voltage and the current, by their ratio, it can be calculated the resistance of a compound resistor. By modelization and using FEM calculation it is analysed how precise the curve representing the variation of the resistance with the temperature fits to the curve showing the variation of the resistivity of the thin superconductor with temperature.

The transition from normal resistor to superconductor it is produced in a 2-3 K temperature interval, as can be seen in the experimental curve presented in Fig. 1. In between the two temperatures, at the beginning at the end of the transition to the superconductive stage (temperatures marked as T_a and T_b) exist the inflexion point of the curve and the temperature corresponding to this point, T_c, can be assumed to be the critical temperature of the superconductive layer.

In Fig. 2 is presented the theoretical curve for variation of the resistivity of the high critical temperature superconductor (curve 1) and the variation of the resistivity of silver (2) in the region of 100…120 K. Between the temperatures T_a and T_b the silver's resistivity has a slight modification, and shall be considered constant in the following calculations [1].

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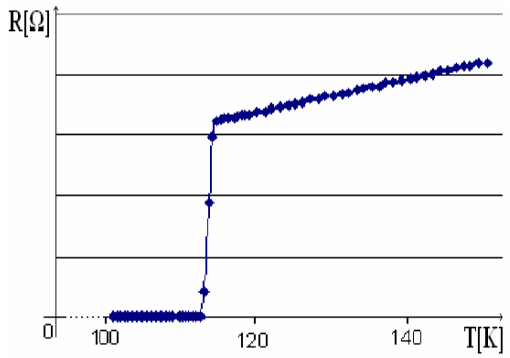

Fig. 1. Resistance of the sample vs. temperature.

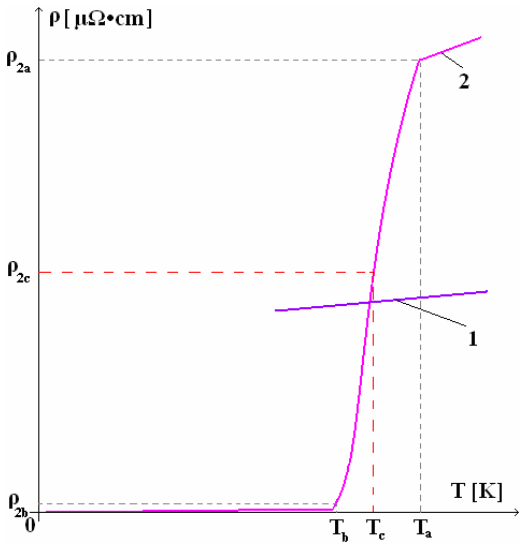

Fig. 2. Resistivity for YbaCuO (2) and silver (1).

II. The Resistance of a Compound Resistor

The thin layer of high critical temperature superconductor, together with the small drops of high conductivity silver, represents a compound resistor [4].

The two silver contacts are very important in size because of the small thickness of the superconductive layer [7].

In Fig. 3 is presented the situations of the measurement with only two contact points. It is not convenient to use the same contacts for injecting the current as well as to measure the voltage difference between them [8]. Some of the inconvenient of using this method shall be presented also in this paper.

The four points measurement method can be used for

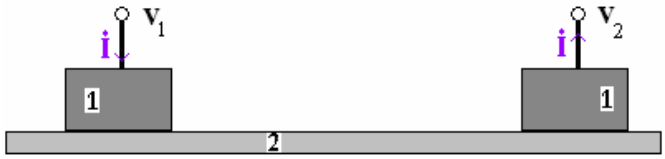

Fig. 3. The two contacts measurement method.

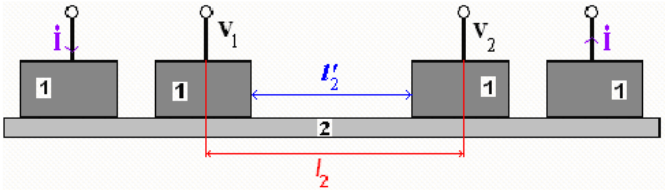

Fig. 4. The four contacts measurement method.

calculating a resistance as the ratio between the voltage measured between two electrodes and the current injected trough other two electrodes

$$R = \frac{V_1 - V_2}{I}. \quad (1)$$

This resistance, in certain conditions, can be accepted as being the resistance of the thin tape of length l_2.

During the transition to the superconductive stage, by decreasing the temperature of the sample immersed in liquid nitrogen, the resistivity of the YBaCuO layer decreases slightly [3] until the T_a temperature. At this temperature the resistivity of silver used for the electric contacts is several times smaller than the resistivity of the tape.

From the temperature T_a descending to T_b the resistivity of the tape decreases abruptly in a few seconds, even if the temperature interval is only of about 2…3 K. The resistivity of the silver can be considered constant in this very narrow temperature interval. At a certain moment, corresponding to a temperature between T_a and T_b, the two resistivities, of the silver and of the tape, are equal one to the other. As the temperature decreases towards T_b the resistivity of the tape becomes smaller and smaller. At T_b the resistivity of silver is several times greater than the resistivity of the tape. After a few seconds the resistivity of the tape is reaching finally the zero value (superconductive stage of the tape) and remains constant even if the decreasing of the temperature goes on.

When the current flows through a compound resistor at the surface separating the two media there are involved some continuity conditions for the electric field.

The distribution of the electric field in this compound resistor modifies significantly during the transition from temperature T_a (when $\rho_1 < \rho_2$) to T_b (when $\rho_1 > \rho_2$).

In Fig. 5, it is shown the continuity of the current density from medium 2 to medium 1, when $\sigma_1 > \sigma_2$ ($\rho_1 < \rho_2$). In Fig. 6,

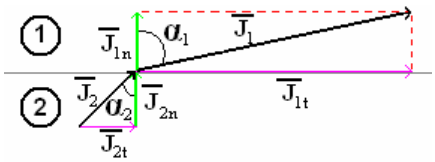

Fig. 5.

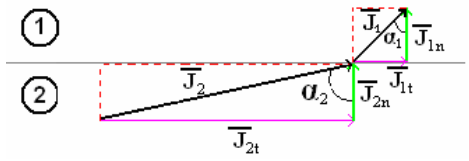

Fig. 6.

it is shown the situation when the resistivity of medium 2 has decreased and became smaller than the resistivity of medium 1 (silver contact).

When the thin layer, medium 2, reaches the superconductive stage the current under the voltage contact has only horizontal component and the current does not enter inside the silver voltage contact, medium 1. This situation is presented in Fig. 7a. Because the current has a finite value inside the layer 2, even if the conductivity $\sigma_2 = \infty$ for temperatures $T < T_b$, this implies that the electric field $E_2 = 0$.

In Fig. 7b is presented the situation under the current injection silver contact. The surface that separates the two media is equipotential surface.

III. The Numeric Modelization of the Compound Resistor

The two measurement methods shown in Figs. 3 and 4 were modelised in 2D FEM, using QField Terra Analysis Student version [5]. For the principle of the method, the 250 nodes are enough to give an image to the students on how measurement results for calculating the electric resistance can be combined with numeric modelisation of the compound resistor. Using both methods the final result (the temperature dependence of the resistivity of a studied material) can be obtained. Also the accuracy of the 4 contacts method is proved by the modelisation also.

As shown in Fig. 2 during the short temperature interval, ($T_a \rightarrow T_b$) the resistivity of the superconducting layer modifies dramatically while the silver's resistivity remains practically the same (we consider it constant in the followings). So, from a situation when the ratio between the resistivities of the two materials is smaller than 1, at the temperature T_a, $k(T_a) = \rho_1(T_a)/\rho_2(T_a) < 1$, by reducing the temperature we pass through a point where the ratio is $k(T) = \rho_1(T)/\rho_2(T) = 1$, and we arrive at temperature T_b where $k(T_b) = \rho_1(T_b)/\rho_2(T_b) >> 1$. Some field distribution representation show the important difference imposed by the variation of the resistivity. Due to symmetry only a half of the model was represented. The representation is made for the situation of the measurement

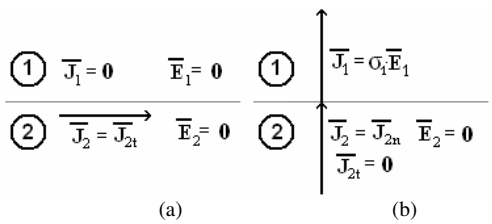

Fig. 7.

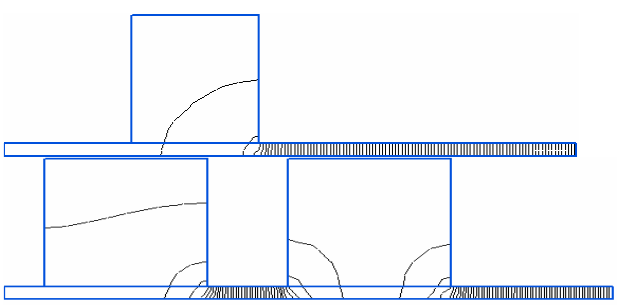

Fig. 8. Representation of the equipotential lines for k=0.2.

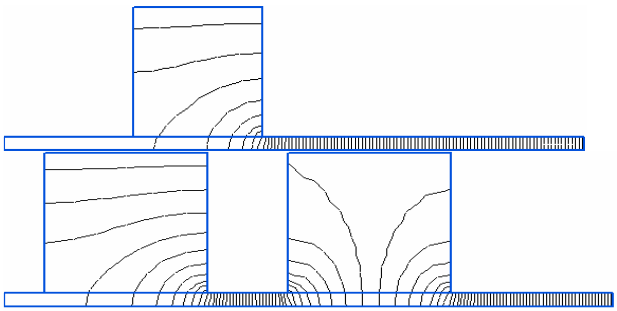

Fig. 9. Representation of the equipotential lines for k=1.

with two contacts as well as with four contacts.

IV. The Calculation of the Resistivity Curve $P_2(T)$

If we assume that the field between the voltage contacts is uniform in each point of the thin layer on the length l_2, the curve of the resistivity is obtained by proportionality from the measured curve of the resistance $R_{ms} = f(T)$.

This is valid for greater values of $k = \rho_1(T)/\rho_2(T)$. For k = 5, situation presented in Fig. 10, we can see that this condition is nearly fulfilled.

If we take as reference the resistance of the sample measured at T_b, one of the last points on the descending resistance curve before reaching the superconductive stage, for this situation $k \approx 50$ and the resistivity can be calculated with (2).

$$\rho_2(T_b) = \frac{R_{ms}(T_b) \cdot S_2}{l_2}. \quad (2)$$

For the analysed sample this value, calculated based on the electric measurements and geometric dimensions of the sample, is $\rho_2(112.75) = 0.102$ nΩ·m.

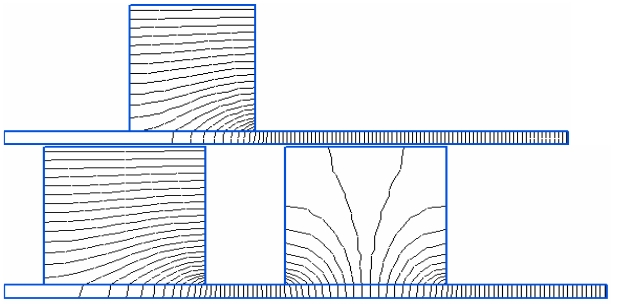

Fig. 10. Representation of the equipotential lines for k=5.

At the same temperature the resistivity of silver is $\rho_{Ag}(112.75) = \rho_2(112.75) \approx 5$ nΩ·m [2].

The relative value of the resistance measured at another temperature, T in the interval (T_b, T_a), is the resistance. R^*_{ms}, and their values are calculated in the third row of Table I.

Starting from the situation corresponding to k = 50, and using the exact dimensions of the sample (including contacts) several numeric modelizations were made. One of the results of modelization is presented in Fig. 11. Based on the symmetry, only half of the compound resistor was modelized.

The resistance is calculated using the field distribution obtained with QField for each modelization (k from 50 to 0.21) and results are in Table II.

$$R_{md} = \frac{2 \cdot \int_m^n \overline{E} \cdot \overline{dl}}{\int_S \overline{J} \cdot \overline{dS}} = \frac{2V_m}{i} \quad (3)$$

$V_n = 0$ and the value of V_m is read from the program.

The current is calculated, using again the program's facilities, by integrating on surface S.

From the measurements (Table I), we have a dependence on temperature of the relative resistance of the sample.

From modelization (Table II) we have a dependence of the resistance of the compound resistor on the resistivity of the thin YBCO layer. The reference value in the two tabs corresponds to the same situation, the calculated one and the modelized one. For this situation which corresponds to a temperature T_a = 112.75 K, the resistivity of YBCO is $\rho_2(112.75) = 0.102$ nΩ·m.

The measured resistance (the relative value) of the compound resistor corresponds to a certain ratio between the resistivity of the silver and the resistivity of the thin YBCO layer. Because was assumed that for the rapid transition to the superconducting stage the resistivity of the silver can be accepted as constant, this means that the relative resistance of the compound resistor is function of the resistivity of the YBCO layer.

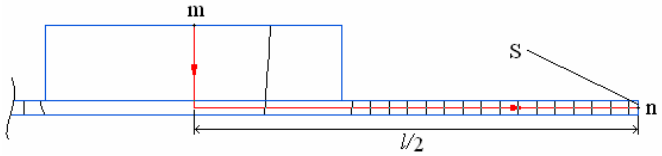

Fig. 11. Modelization of the measured sample.

TABLE I

T [K]	112.75	113.14	113.78	114.24	114.77
R_{ms} [nΩ]	1.074	21.829	99.401	156.17	169.55
R^*_{ms} [-]	1.0	20.325	92.552	145.41	157.87

TABLE II

k	50	5	1	0.5	0.33	0.25	0.21
ρ_2[nΩ·m]	0.1	1	5	10	15	20	24
R^*_{md}[-]	1	8.82	38.2	76.2	107.8	142.4	170

$$R^* = f_1(T) \text{ and } \rho_{2md} = f_2(R^*) \quad (4)$$

Using (5), based on measured R_{ms}, can be obtained the dependence on temperature of the resistivity of YBCO assuming uniform electric field in the layer:

$$\rho_{2ms}(T) = \frac{R_{ms}(T) \cdot S_2}{l_2}. \quad (5)$$

Using relations (4), we obtain the dependence on temperature of the resistivity of the YBCO based on modelization and on the dependence on temperature of the relative resistance of the compound resistor, $\rho_{2md}(T)$. Both of them are presented in Table III.

In graphic representation the variation of the resistivity is presented in Fig. 12. It can be seen that exist a difference between the two calculated resistivities.

V. Conclusions

By the numeric modelization, using QField 2D FEM, the field distribution shows very clearly that the four contact measurement method is much more accurate than the two contact method.

Using the approximation that the electric field inside the thin YBCO layer is uniform, the value of the resistivity results by simple calculation (5), assuming that it is proportional to the resistance calculated from measurements. For very low values of the resistivity of the thin film this is correct, but for medium values and especially for high values of the resistivity this is not correct.

If the resistivity of the silver is much smaller than the resistivity of the YBCO thin layer (at high, "normal", temperatures) the distance l'_2 can be used instead of l_2 and the results would be more accurate. This can be seen from the equipotential field lines represented in Fig. 8.

TABLE III

T [K]	ρ_{md} [nΩ·m]	T [K]	ρ_{ms} [nΩ·m]
112.750	0.1	112.75	0.102
112.906	1.0	113.14	2.079
113.298	5.0	113.78	9.467
113.611	10.0	114.24	14.874
113.916	15.0	114.77	16.148
114.213	20.0	115.36	16.298
114.700	22.0	117.08	16.458
117.982	23.0	118.04	16.698
120.800	24.0	120.14	16.955

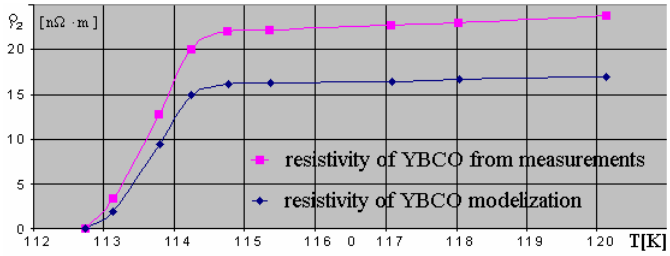

Fig. 12.

But using l'_2 instead of l_2 gives unsatisfying results when the two resisitivities are of the same range and surely shall give incorrect results for the values of the resistivity when the YBCO approaches to the superconducting stage.

By technical point of view the differences between the two curves of the resistivity are not very significant, but if a very accurate numeric modelization is made the result can be a more accurate curve $\rho(T)$.

Some of the authors [6] when presenting results on thin superconducting film give the dimensions of the cross section of the film (width and thickness) and a result as resistance per unit length, R^* [nΩ/m] as function of the temperature, $R^*(T)$.

The critical temperature T_c shows to be in fact a little bit smaller but is not modified in a significant manner by the correction proposed by this paper.

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Short-Term Forecasting of Electricity Load Using Recurrent ANNs

Jelena B. Milojković and Vančo B. Litovski

***Abstract*—One solution to the problem of one-step-ahead prediction of the electricity power consumption in sub-urban areas is proposed. It is based on implementation of artificial neural networks (ANN) that are properly structured for prediction. Architecture named Extended Time Controlled Recurrent (ETCR) ANN is introduced. A proper arrangement of training data is advised. After implementation, promising results were obtained giving, in some instances, predictions with an error less than 1%. In the worst situation observed, the discrepancy between the target and predicted values go as large as 14% what we consider as acceptable and in the same time as an inspiration for further research in improving the method. The method is intended to be integrated into a remote power reading and billing system giving an opportunity to the energy supplier to plan his business. The method proposed implements ANNs that are generally widely known but creates new architecture that is fully original. It is our opinion that it may be implemented with equal success to one-step-ahead prediction of broader class of time series exhibiting inherent quasi-periodical properties.**

***Index Terms*—Electricity load, prediction, artificial neural networks.**

I. Introduction

IN an inspired paper, Prof. Mandel' [1] claims: "Prediction of short time series is a topical problem. Cases where the sample length N is too small for generating statistically reliable variants of prediction are encountered every so often. This form is characteristic of many applied problems of prediction in marketing, politology, investment planning, and other fields." Further he claims: "Statistical analysis suggests that in order to take carefully into account all components the prediction base period should contain several hundreds of units. For periods of several tens of units, satisfactory predictions can be constructed only for the time series representable as the sum of the trend, seasonal, and random components. What is more, these models must have a very limited number of parameters. Series made up by the sum of the trend and the random component sometimes may be predicted for even a smaller base period. Finally, for a prediction base period smaller than some calculated value N_{min}, a more or less satisfactory prediction on the basis of observations is impossible at all, and additional data are required."

Among the fields not mentioned in [1], dealing with really small set of data or „prediction base period", we will discuss here hourly short-term prediction of electricity loads at suburban level or on the level of a low voltage transformer station. In fact, the amount of data available in this case, as depicted in Fig. 1, is large enough to apply any other forecasting method [2]–[5] but looking to the load diagram i.e. hourly load-value curves, we easily recognize that past values of the consumption are not very helpful when short-term prediction is considered. That stands even for data from the previous day and for data from the same day in the previous week. As an illustration of the claim in Fig. 2, we give three load diagrams representing one day consumption of the same load on a) Friday January 31, 2009, b) Thursday January 30, 2009, and c) Friday January 24, 2009. The numerical values are shown in Table I. The power is normalized by a factor of 200 being the turn ratio of the appropriate current transformer in the transformer station. One may notice the similarity of the general shape and the difference in main details confirming the paramount importance of the most recent data for prediction. Accordingly, we propose the problem of prediction of the load value in the next hour (one or two) to be performed as a deterministic prediction based on very short – one day – time series. To help the prediction, however, in an appropriate way, we

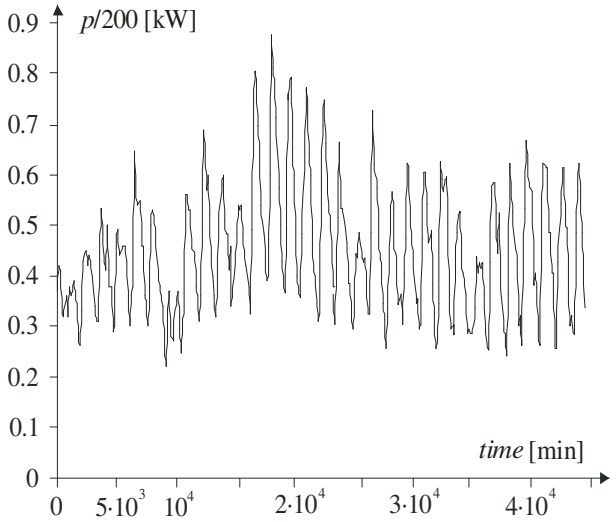

Fig. 1. Average values of hourly consumption at the observed site in January, 2009.

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TABLE I
AVERAGE VALUES OF HOURLY CONSUMPTION (KW) ON THREE DAYS

No.	t (min)	p/200 31.01.09	p/200 30.01.09	p/200 24.01.09
1	0.06	0.40	0.42	0.31
2	146	0.32	0.28	0.32
3	284	0.34	0.27	0.30
4	422	0.30	0.44	0.44
5	561	0.50	0.56	0.50
6	700	0.58	0.63	0.54
7	837	0.64	0.63	0.44
8	977	0.58	0.52	0.42
9	1115	0.50	0.51	0.41
10	1255	0.44	0.44	0.38
11	1393	0.35	0.40	0.31

t=0 at midnight.

introduce past values e.g. loads for the same day but in previous weeks. That is in accordance with existing experience claiming that every day in the week has its own general consumption profile (Murto, 1998).

The idea is reminiscent to the substitution of the simple moving average (SMA) by the exponential moving average (EMA) method for prediction of trend [6]–[7]. The simple moving average is extremely popular among traders, but one argues that the usefulness of the SMA is limited because each point in the data series is equally weighted, regardless of its position in the sequence. It is common opinion that most recent data is more significant than the older and should have a greater influence on the final result.

Having all that in mind we undertook a project of developing an ANN based method that will be convenient for systematic implementation in stationary time series prediction with reduced set of data. Our first results were applied to prediction of environmental as well as technological data and published in [8]–[9]. Our main idea implemented was the following. If one wants to create neural network that may be used for forecasting one should enable this property during ANN's training by proper preparation of the training set. In addition, the ANN used has to have such an architecture to accommodate to the training process for prediction. Following these considerations new forecasting architectures were developed and implemented [8]–[9]. Here, however, we will upgrade one of them and, for the first time, describe its implementation in the field of short term electricity load forecasting.

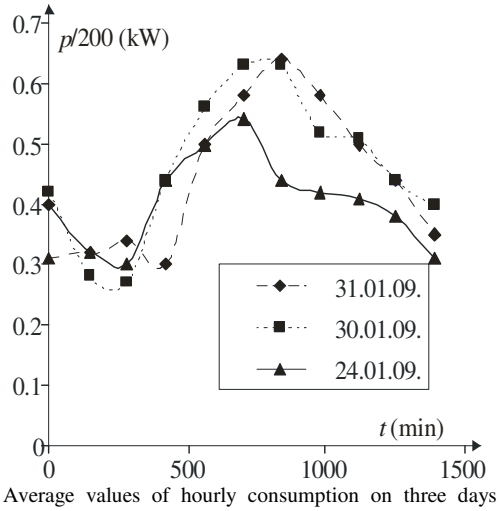

Fig. 2. Average values of hourly consumption on three days (Table I visualized).

The structure of the paper is as follows. After general definitions and statement of the problem we will give a short background related to ANNs application to forecasting. Then we will describe the solution for possible applications of ANNs aimed to the one-step-ahead forecasting task. Finally, short discussion of the results and consideration related to future work will be given.

II. PROBLEM FORMULATION AND SOLUTION

A time series is a number of observations that are taken consecutively in time. A time series that can be predicted precisely is called deterministic, while a time series that has future elements which can be partly determined using previous values, while the exact values cannot be predicted, is said to be stochastic. We are here addressing only deterministic type of time series.

Consider a scalar time series denoted by y_i, $i = 1, 2, \ldots m$. It represents a set of observables of an unknown function $\hat{y} = \hat{f}(t)$, taken at equidistant time instants separated by the interval Δt i.e. $t_{i+1} = t_i + \Delta t$. In the next, we will introduce $h = \Delta t$, for convenience. One-step-ahead forecasting means to find such a function f that will perform the mapping

$$y_{m+1} = f(t_{m+1}) = \hat{y}_{m+1} + \varepsilon \quad (1)$$

where $\hat{y}_{m+1} = \hat{f}(t_{m+1})$ is the desired response, with an acceptable error ε.

The prediction of a time series is synonymous with modeling of the underlying physical or social process responsible for its generation. This is the reason of the difficulty of the task. There have been many attempts to find solution to the problem. Among the classical deterministic methods we may mention the k-nearest-neighbor [10], in which the data series is searched for situations similar to the current one each time a forecast needs to be made. This method asks for periodicity to be exploited that, as already discussed, here may be helpful but not decisively.

In the past decades ANNs have emerged as a technology with a great promise for identifying and modeling data patterns that are not easily discernible by traditional methods. Analysis as to why neural networks are implemented for prediction may be found in [9]. A comprehensive review of ANN use in forecasting may be found in [11]. Among the many successful implementations we may mention [12]. A common feature, however, of the existing application is that they ask for a relatively long time series to become effective. Typically it should be not shorter than 50 data points [11]. This is due to the fact that they all look for periodicity within the data. Very

short time series were treated in [13]. Here additional "nonsample information" was added to the time series in order to get statistical estimation from deterministic data.

In the next, we will first briefly introduce the feed-forward neural networks that will be used as a basic structure for prediction throughout this paper.

The network is depicted in Fig. 3. It has only one hidden layer, which has been proven sufficient for this kind of problem [14]. Indices: "in", "h", and "o", in this figure, stand for input, hidden, and output, respectively. For the set of weights, $w(k,l)$, connecting the input and the hidden layer we have: k=1,2,..., m_{in}, l=1,2,..., m_{h}, while for the set connecting the hidden and output layer we have: k=1,2, ...m_{h}, l=1,2,..., m_{o}. The thresholds are here denoted as $\theta_{x,r}$, r=1,2, …, m_{h} or m_{o}, with x standing for "h" or "o", depending on the layer. The neurons in the input layer are simply distributing the signals, while those in the hidden layer are activated by a sigmoidal (logistic) function. Finally, the neurons in the output layer are activated by a linear function. The learning algorithm used for training is a version of the steepest-descent minimization algorithm [15]. The number of hidden neurons, m_{h}, is of main concern. To get it we applied a procedure that is based on proceedings given in [16].

In prediction of time series, in our case, a set of observables (samples) is given (approximately every two hours or exactly twelve samples per day) meaning that only one input signal is available being the discretized time. According to (1) we are predicting one quantity at a time meaning one output is needed, too. The values of the output are numbers (average power for a period of approximately two hours). To make the forecasting problem numerically feasible we performed transformation in both the time variable and the response. The time was reduced by t_0 so that

$$t = t^* - t_0 . \tag{2}$$

Having in mind that t^* stands for the time (in minutes) during one day, this reduction gives the value of 0 to the time (t_0) related to the first sample. The samples are normalized in the following way

$$y = y^* / M \tag{3}$$

where y^* stands for the current value of the target function and M is a constant (for example M=200, being the turn ratio of the current transformer in the station).

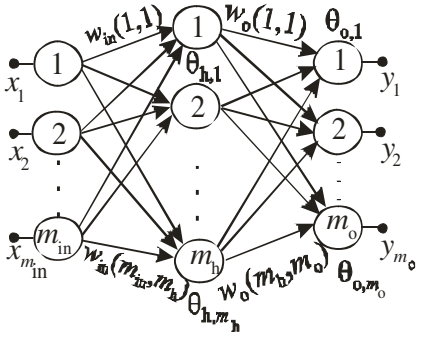

Fig. 3. Fully connected feed-forward neural network with one hidden layer and multiple outputs.

If the architecture depicted in Fig. 3 was to be implemented (with one input and one output terminal) the following series would be learned: (t_i, $f(t_i)$), i=1,..., m). It is our experience [8, 9], however, that such a simple architecture while excellent for interpolation can't extrapolate successfully. That is why we are going for such an architecture that includes more complex sample of input data. In fact, we will here exploit the advantages the k-nearest-neighbor idea and create such an architecture that combines most recent and data periodically dislocated backward in time.

Starting with the basic structure of Fig. 3, in [8] possible solutions were investigated and two new architectures were suggested to be the most convenient for the solution of the forecasting problem based on short prediction base period. Here, the implementation of one of these two architecture will be considered and accomodated to the situation when some additional data is available as mentioned in the introduction. Our intention was to benefit from both: the generalization property of the ANNs and the success of the recurrent architecture.

The first version of this architecture, named *time controlled reccurent* (TCR) was inspired by the time delayed recurrent ANN. It is a recurrent architecture with the time as the only input variable so controlling the predicted value. At the inputs where the output is feed back we introduce signals that are delayed by one sampling interval only.

We extend, now, this architecture so that we allow for the values of the power consumption at instants shifted for one step in future but of the same days in four previous weeks, to control the output. Hence, the term extended will be added. This structure will be referred from now on as the Extended Time Controlled Recurrent (ETCR) architecture. It is depicted in Fig. 4. for a set of chosen parameters. In the case depicted, three samples of previous instants of the given day plus four samples of previous weeks are used in order to create the prediction for a given instant. j stands for the number of samples per day while n is the order number of the week in the time series. In that way the values indexed with n are from the actual week, while the values indexed n-s, s=1,2,3,4, are from the previous weeks. i stands for the i-th sample in the day

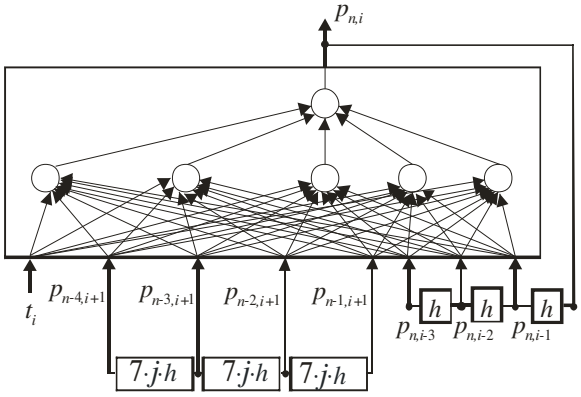

Fig. 4. ETCR (Extended Time Controlled Recurrent) ANN.

selected. Accordingly, for example, $p_{n\text{-}2,2}$ would mean: the second sample for the given day (say Friday) two weeks earlier of the nth week.

Here in fact, the network is learning a series in which the output value, representing the average power consumption for approximately two hours period in a given day of the week, is controlled by the present time and its own previous instances:

$$p_{n,i} = f(t_i, p_{n,i-1}, p_{n,i-2}, p_{n,i-3}, p_{n-1,i+1}, p_{n-2,i+1}, p_{n-3,i+1}, p_{n-4,i+1}), i = 4,...,m, \quad (4)$$

or

$$p_{n,i} = f(t_i, p(t_i - h), p(t_i - 2h), p(t_i - 3h), p(t_i - 7 \cdot j \cdot h + h), p(t_i - 14 \cdot j \cdot h + h), p(t_i - 21 \cdot j \cdot h + h), p(t_i - 28 \cdot j \cdot h + h)), i = 4,...,m. \quad (5)$$

The actual value $p_{n,i}$ is unknown and should be predicted.

In the next we will illustrate the implementation of the method in two phases. First we will select one time instant and show how we do prediction. Then we will implement the method to a complete day and show the effectiveness of the method.

III. Implementation Example

The implementation of the method is conceived so that it should create a prediction for the consumption in the next two hours. Just after the present measurement is finished new training data structure is to be created and training of the ANN lounched. After that the so obtained ANN is to be run with an input vector obtained from the last measurement and prediction is to be obtained. The predicted value is to be added to the consumption log for further processing.

The training data accomodated for training the ETCR network intended to be developed for forecasting the value of the consumption at 07.02 hours in the morning of Friday, January 31, 2009, is depicted in Table II. The location of that point at the consumption curve may be seen from Fig. 5 to be at the second minimim (t=422, note the different time window). The time in Table II is given in minutes so that the forcasting moment is 1523 minutes after the start of the time window. Here n=5 since it is the fifth Friday in the year. Note

TABLE I
Training Data Prepared for the ETCR Method

i	t_i	$p_{n\text{-}1,i+1}$	$p_{n\text{-}2,i+1}$	$p_{n\text{-}3,i+1}$	$p_{n\text{-}4,i+1}$	$p_{n,i\text{-}3}$	$p_{n,i\text{-}2}$	$p_{n,i\text{-}1}$	$p_{n,i}$
4	415	0.58	0.75	0.69	0.45	0.27	0.44	0.56	0.63
5	552	0.61	0.66	0.57	0.42	0.44	0.56	0.63	0.63
6	692	0.52	0.60	0.60	0.44	0.56	0.63	0.63	0.52
7	830	0.40	0.53	0.52	0.43	0.63	0.63	0.52	0.51
8	968	0.38	0.52	0.44	0.40	0.63	0.52	0.51	0.44
9	1107	0.31	0.38	0.40	0.37	0.52	0.51	0.44	0.40
10	1246	0.32	0.38	0.36	0.34	0.51	0.44	0.40	0.32
11	1383	0.30	0.32	0.32	0.31	0.44	0.40	0.32	0.34
12	1523	0.44	0.42	0.38	0.31	0.40	0.32	0.34	

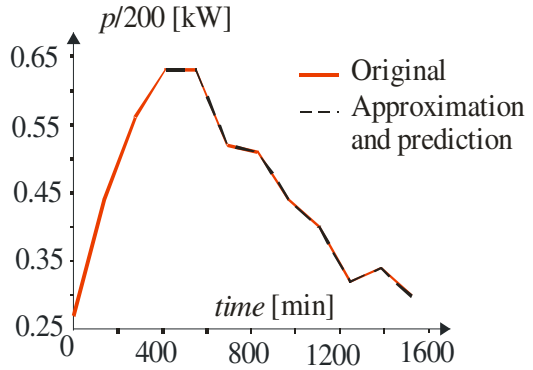

Fig. 5. The actual curve and the approximation (dashed black line) obtained by the ETCR network. The last segment of the dashed line finishes with the prediction.

that in the first row, enumerated i=4, the value $p_{n,i-3}$ is, in fact, the first value in the time series: $p_{n,1}$. The rightmost column separated by bold line is the target value for the given sample (lesson) used during training. The lowermost row, separated also by bold line, is related to the time instant where prediction should be peformed. The values given in that row will be used as excitation to the ANN obtained after training. The target value to be matched is **0.30**. One should fill the empty cell in Table II by the prediction.

By inspection of Table II despite the relatively large number of items in the table, we may conclude that the time series we are extrapolating is short in the sense that we use 11 samples in the main time frame only i.e. i=1,….,11.

After training the ETCR network with these data and, after training, exciting it as described above, the predicted value was **0.298699**. It is a miss of the target value by 0,43%. In addition, the ETCR ANN performs ideally in approximation of the load curve as can be seen from Fig. 10 where the input curve and the approximation overlap in the whole approximation interval $t \in \{0, 1383\}$. This result was obtained by an ANN with five neurons in the hidden layer as depicted in Fig. 4.

Having in mind the shape of the curve, the above prediction example may be stated as a very successful one. To check the behavior of the method on a larger set of examples we repeated the above process 11 times by moving the time window by one step to generate 11 consecutive predictions. The obtained results are presented in Fig 6. All predictions were obtained by ANNs with five neurons in the hidden layer.

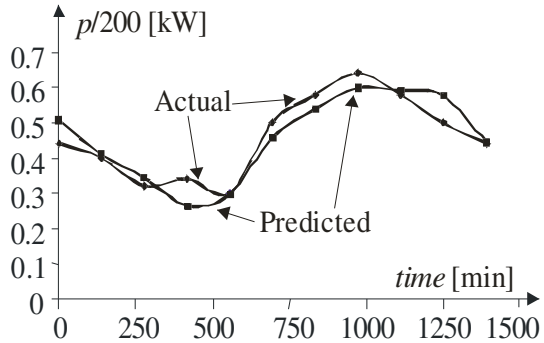

Fig. 6. Predicted and actual values (Thursday/Friday January 30/31, 2009).

As can be seen from fig. 6 not every prediction was as successful as the one related to the 07.02 hours in the morning. Nevertheless, most of the predictions are within several percent of the actual value and only two of them are significantly apart of the wanted one. The largest deviation is measured to be 14% only. One may notice from this diagram, however, that the error in prediction for a given instant does not influence the next prediction i.e. there is no accumulation of the error. The reason for that is the fact that every prediction step in our method represents a separate extrapolation task.

IV. Conclusion

The problem of short-term (hourly) forecasting of the electricity load at suburban level is considered. It is claimed first that despite "periodicity" of the phenomenon under consideration the data from previous days being from the given week or from the same day of the previous weeks are not convenient enough to be used directly. Then, architecture of ANN was proposed for the solution of the problem. Both, previous data for the given day and previous data from the same day of the previous weeks were used in the training set. The later is related to the habits of the consumers that generally influence the consumption.

Encouraging results were obtained. More detailed study will be performed in order to further improve the predictions. For example, the influence of the number of signals feed-back will be studied as well as the number of previous weeks.

It is our intention to integrate the prediction function into the remote-electricity-metering and billing system so enabling the electricity supplier to predict the load.

Finally, we want to stress the fact that we are here dealing wit extrapolation. That is to be opposed to generalization what the obvious property of the ANNs is. In our case the generalization is expressed by the excellent approximation of the input function. Namely, the ANN has the same response as is the input in between of the time interval given. That, however, is not forecasting. One should leave the input interval and predict the response value outside of the given time segment in order to achieve forecasting. That is what we do. This fact is stressed here since many of the published results are ambiguous in the sense that the term forecasting is used while interpolation is performed.

The method proposed implements ANNs that are generally widely known but creates new architecture that is fully original. It is our opinion that it may be implemented with equal success to one-step-ahead prediction of broader class of time series exhibiting inherent quasi-periodical properties.

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Computer Modeling of Three-Phase to Single-Phase Matrix Converter Using MATLAB

Georgi Kunov, Mihail Antchev, and Elissaveta Gadjeva

***Abstract*—A three-phase to single-phase matrix converter is modeled and investigated in the MATLAB environment in the present paper. Based on the state matrix vector, a mathematical analysis of the converter is performed giving the relation between the sinusoidal line voltage (current) and the output voltage (current). The results of the investigation are confirmed using computer simulation of the converter by the program product MATLAB.**

***Index Terms*—Power electronics, matrix converters, MATLAB simulation.**

I. Introduction

THE development of new methods and circuits for electrical energy conversion with improved characteristics is a basic way for increasing of the energy efficiency of power electronic converters with respect to mains network. The matrix converters realize a direct conversion of alternating current to alternating current [1, 2]. The basic principles of operation of the matrix converters are proposed by Venturini in the early 1980's [1]. Subsequently the bases were put of their investigation [2, 3]. The matrix converter theory is based on direct conversion of alternating current to alternating current. Their main application is in the three phase motor drives where the frequency of the output voltage is lower than the frequency of the mains network voltage. The matrix converters had been developed in the last years with the appearance of AC/DC converters with direct conversion of the three-phase mains network voltage in high-frequency single phase voltage [4,5,6]. The main application of the direct AC/DC matrix converters is in the power supply for the needs of the telecommunications (for example the company Rectifier Technologies). From the recent publications [7, 8], it can be concluded that the application of three-to-single phase converters is extended in the energetics and industry. This fact is a result of their main advantages: decreased gabarits, weight and price due to the lack of reactance elements (filter inductor and capacitor), a high-efficiency and high power factor.

The aim of the present paper is the investigation of the three-phase to single-phase matrix converter with a series resonant circuit load. The frequency of the single-phase output voltage is higher than the frequency of the mains network voltage. Based on the state matrix vector, a mathematical analysis of the converter is performed. The obtained equations in matrix form are solved using the program MATLAB. The results of the investigation are confirmed using computer simulation of the converter by the program SIMULINK.

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II. Principle of Operation and Mathematical Description

The equivalent circuit of the three-phase to single-phase matrix converter is presented in Fig. 1. *S*1–*S*6 are bidirectional switches, realised as shown in Fig. 1b. The converter is supplied directly by the mains network. The three-phase line input voltages are described by the vector V_{in}:

$$V_{in} = \begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} = \begin{bmatrix} V_m \sin \omega t \\ V_m \sin(\omega t - \frac{2\pi}{3}) \\ V_m \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}. \quad (1)$$

The considered matrix converter combines the functions of

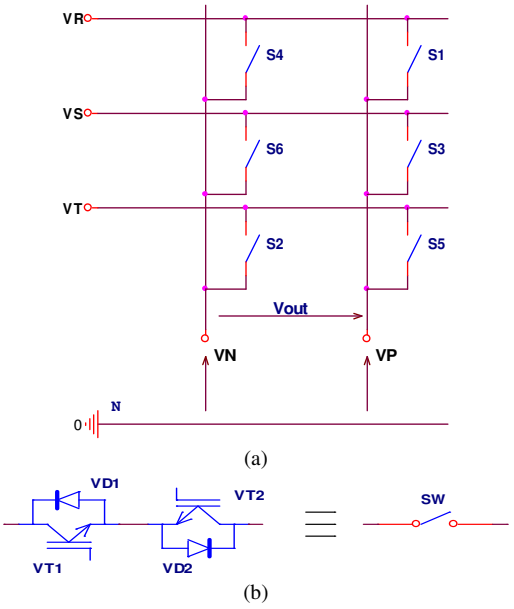

Fig. 1. Circuit for investigation: (a) equivalent circuit, (b) bidirectional power switch.

the three-phase rectifier and single-phase inverter. The possibilities for operation of the rectifier are demonstrated in Table I. For the presented six intervals one of the phases is the most positive ($V_{p\max}$) and one – the most negative ($V_{n\max}$). In the column *GP*, the working pairs of semiconductor devices are presented for the six intervals, for the case when the odd switches (*S*1, *S*3, *S*5) are diodes with common cathodes connected to *VP*, and the even switches (*S*4, *S*6, *S*2) are diodes with common anodes connected to *VN* (Fig. 1a). In this case the output voltage

$$V_{out} = V_P - V_N \tag{2}$$

is positive.

The column *GN* is related to the case of an opposite (inverse) connection of the diodes, when V_{out} becomes negative. If *S*1–*S*6 are bidirectional switches, it follows that we can change the polarity of V_{out} within each of the six intervals, commutating the switches *GN*–*GP*. It can be seen from the Table I that the work of the matrix converter within one period 360^o (2π rad) can be considered independently for each of the six intervals. It can be considered as single-phase bridge inverter for each interval [9].

The waveforms which characterise the first two intervals, are shown in Fig. 2. The origin of the coordinate system cioncides with the start of a positive halfperiod for the phase *R*.

In the interval ($\pi/6-3\pi/6$), the most positive is the phase V_R. This state is marked by the rectangle pulse *SW*1 = 1. In the same time, the most negative is the phase V_S, which is marked by *SW*6 = 1. In this interval, the equivalent circuit of the single-phase bridge inverter consists of the switches *S*1–*S*6, *S*4–*S*3. They are commutated by the opposite pulses *GP* and *GN* (Fig. 2). In the next interval ($3\pi/6-5\pi/6$) the most negative becomes the phase V_T where the ulse is *SW*2 = 1 (*SW*1 = 1). Here the equivalent circuit of the single-phase bridge inverter consists of the switches *S*1–*S*6, *S*4–*S*3. They are commutated by the opposite pulses *GP* and *GN* (Fig. 2).

TABLE I
POSSIBILITIES FOR OPERATION OF THE RECTIFIER

interval	$V_{p\max}$	$V_{n\max}$	*GP*	*GN*
π/6 – 3π/6	V_R	V_S	S1 – S6	S4 – S3
3π/6 – 5π/6		V_T	S1 – S2	S4 – S5
5π/6 – 7π/6	V_S		S3 – S2	S6 – S5
7/6 – 9π/6		V_R	S3 – S4	S6 – S1
9π/6 – 11π/6	V_T		S5 – S4	S2 – S1
11π/6 – 13π/6		V_S	S5 – S6	S3 – S3

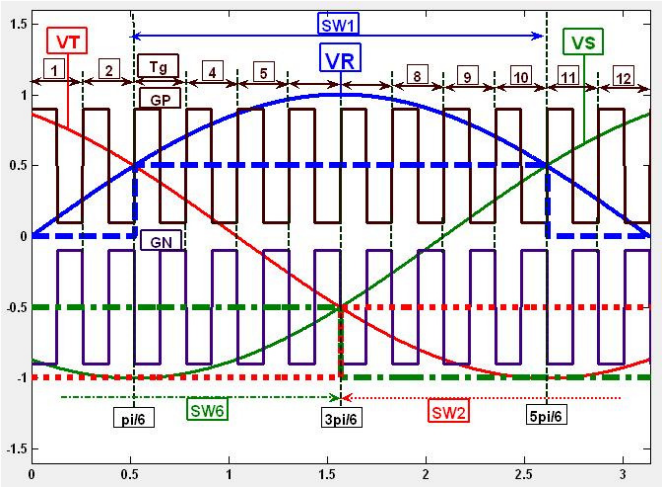

Fig. 2. Illustration of the operation in first two intervals.

All combinations of the switches *S*1–*S*6 are presented in Table I, for the six intervals corresponding to the respective equivalent circuits. The intervals in which operate the switches *S*1–*S*6 are defined by the switch pulses *SW*1–*SW*6 (Fig. 3), and their commutation – by the inverter pulses *GS*1–*GS*6.

It follows from Fig. 3 that the state of the bidirectional switches – open or closed – can be described in matrix form in the following way:

$$F_T = F_i\, F_S \tag{3}$$

or

$$\begin{bmatrix} GS1 & GS3 & GS5 \\ GS4 & GS6 & GS2 \end{bmatrix} = \begin{bmatrix} GP & GN \\ GN & GP \end{bmatrix} \cdot \begin{bmatrix} SW1 & SW3 & SW5 \\ SW4 & SW6 & SW2 \end{bmatrix}, \tag{4}$$

where F_T is the transfer function of the matrix converter, F_i is the inverter transfer function and F_S is the switching pulses transfer function.

It follows from (4) the pulses *GS*, switching *S*1–*S*6, are defined mathematically by the equations:

$$\begin{aligned} GS1 &= GP.SW1 + GN.SW4 \\ GS4 &= GN.SW1 + GPSW4 \\ GS3 &= GP.SW3 + GN.SW6 \\ GS6 &= GN.SW3 + GP.SW6 \\ GS5 &= GP.SW5 + GN.SW2 \\ GS2 &= GN.SW5 + GP.SW2. \end{aligned} \tag{5}$$

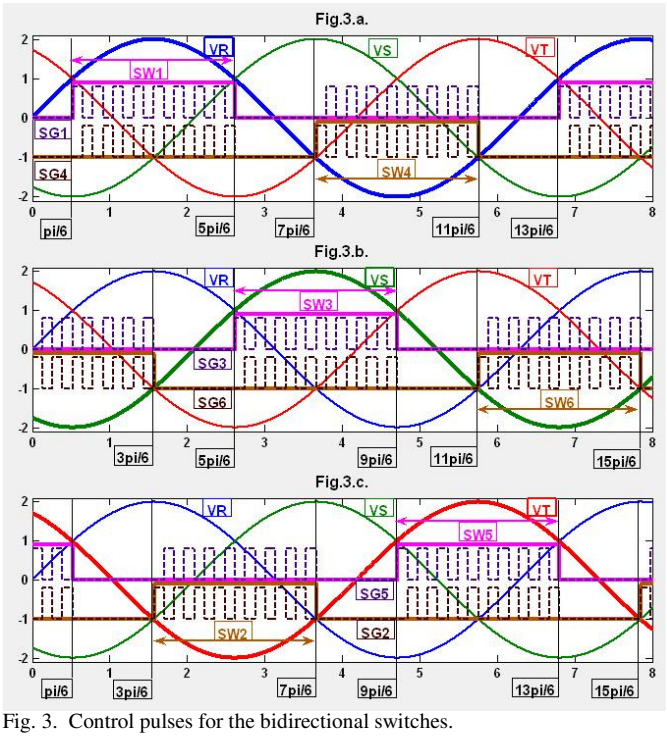

Fig. 3. Control pulses for the bidirectional switches.

The equations (5) correspond to the time intervals from Fig. 3. It is seen that

$$GS1 = \overline{GS4}$$
$$GS3 = \overline{GS6} \quad (6)$$
$$GS5 = \overline{GS2}.$$

The state of the matrix converter can be described in the following way:

$$\begin{bmatrix} V_P \\ V_N \end{bmatrix} = F_T V_{in} \quad (7)$$

or

$$V_P = VS1 + VS3 + VS5$$
$$V_N = VS4 + VS6 + VS2, \quad (8)$$

where

$$VS1 = GS1.V_R; VS3 = GS3.V_S;$$
$$VS5 = GS5.V_T; VS4 = GS4.V_R; \quad (9)$$
$$VS6 = GS6.V_S; VS2 = GS2.V_T.$$

The single-phase output voltage (2) has the form:

$$V_{out}(t) = (GS1 - GS4)\, V_R(t) + (GS3 - GS6) V_S(t) + (GS5 - GS2)\, V_T(t) \quad (10)$$

$$SW1 - SW4 = A_1.\sin(\omega_g t) + \sum_{n=3,5...}^{\infty} A_n.\sin(n\omega_g t)$$
$$SW3 - SW6 = A_1.\sin(\omega_g t - \frac{2\pi}{3}) + \sum_{n=3,5...}^{\infty} A_n.\sin(n\omega_g t - \frac{2\pi}{3}) \quad (11)$$
$$SW5 - SW2 = A_1.\sin(\omega_g t + \frac{2\pi}{3}) + \sum_{n=3,5...}^{\infty} A_n.\sin(n\omega_g t + \frac{2\pi}{3}).$$

The parameter ω_g in (11) is the commutation frequency of the bidirectional switches. The coefficient A_1 is the magnitude of the commutation function, which is assumed to be 1. The first harmonic of the Fourier expansion of A_1 is of the value $4/\pi$. The higher harmonics A_n have significantly lower magnitudes and for the purposes of the performed consideration are neglected. Replacing (11) in (10), the following dependence is obtained for $V_{out}(t)$:

$$V_{out}(t) = \frac{4}{\pi} V_m \sin\omega t.\sin\omega_g t + \frac{4}{\pi} V_m \sin(\omega t - \frac{2\pi}{3}).\sin(\omega_g t - \frac{2\pi}{3}) + \frac{4}{\pi} V_m \sin(\omega t - \frac{2\pi}{3}).\sin(\omega_g t - \frac{2\pi}{3}). \quad (12)$$

The obtained mathematical dependencies (1)-(10) are solved using the program MATLAB. The input voltage vector V_{in} is shown in Table II.

The M-files defining the inverter transfer function F_i (*GP* and *GN*) are given in Table III, where: h_p is the number of the half-periods of the vector V_{in}; n – number of commutations of the switches $S1$–$S6$ in one half-period (n=12 – Fig. 2); N – number of points (for instance 100) for one commutation period T_g.

The computational calculation step along the X axis is: $dx=pi/(n.N)$, where $0 \le x \le (h_p.pi)$. The dimension of the vector X=x[lx] in MATLAB is defined in the main program using the command line:

x = 0: dx: (hp*pi); lx = length(x);

The M-files *sw1* and *sw2* are given in Table IV. The rest elements of the switching transfer function F_S are described similarly.

The solution of equation (9) is shown in Fig. 4 and the solution of equations (8) and (2) is presented in Fig. 5.

TABLE II
M-FILES

File function *vr*	File function *vs*	File function *vt*

function y=vr(x)
lx=length(x);
y=zeros(size(x))
for i=1:lx
y(i)=sin(x(i));
end
	function y=vs(x)
	lx=length(x);
	y=zeros(size(x));
	for i=1:lx
	y(i)=sin(x(i)+
	+4*pi/3);
	end
		function y=vt(x)
		lx=length(x);
		y=zeros(size(x))
		for i=1:lx
		y(i)=sin(x(i)+
		+2*pi/3);
		end

TABLE III
M-FILES

File function *gp*	File function *gn*

function y=gp(x)
lx=length(x);
y=zeros(size(x));
i=0;
for k=1:12*4
for j=1:100
i=100*(k-1)+j;
if j<=50
y(i)=1.0;
else
y(i)=0.0;
end
end
end
	function y=gn(x)
	lx=length(x);
	y=zeros(size(x));
	i=0;
	for k=1:12*4
	for j=1:100
	i=100*(k-1)+j;
	if j<=50
	y(i)=0.0;
	else
	y(i)=1.0;
	end
	end
	end

TABLE IV
M-FILES

File function *sw1*	File function *sw2*

function y=sw1(x)
lx=length(x);
y=zeros(size(x));
for i=1:lx
if (vr(x(i))>vs(x(i)))
&(vr(x(i))>vt(x(i)))
y(i)=1.0;
else
y(i)=0.0;
end
end
	function y=sw2(x)
	lx=length(x);
	y=zeros(size(x));
	for i=1:lx
	if (vt(x(i))<vr(x(i)))
	&(vt(x(i))<vs(x(i)))
	y(i)=1.0;
	else
	y(i)=0.0;
	end
	end

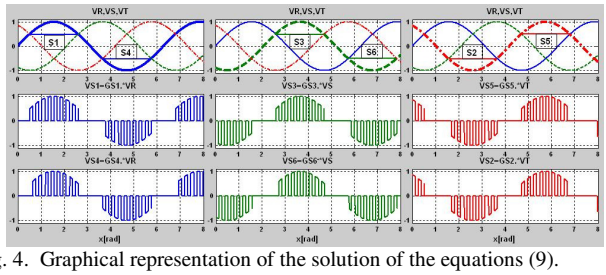

Fig. 4. Graphical representation of the solution of the equations (9).

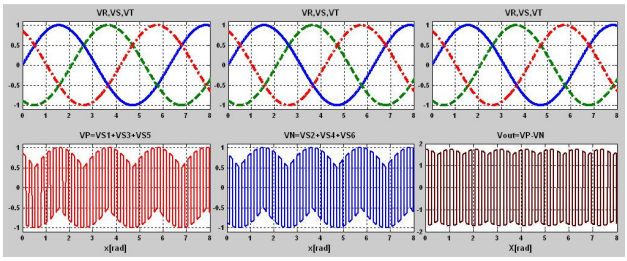

Fig. 5. Graphical representation of the solution of the equations (8) and (2).

III. SIMULINK SIMULATION

The electrical circuit for the computer simulation of the matrix converter is shown in Fig. 6. The simulation of the circuit is performed for a load series resonant circuit. The signals $SW1-SW6$, included in the switching transfer function F_S, are created in the block Subsystem1. Its electrical circuit is shown in Fig. 7.

The signals $GS1-GS6$ included in the matrix transfer function F_T are created in the block Subsystem2. Its electrical circuit is shown in Fig. 8. The functional generators Pulse Generator – *GP* and Pulse Generator – *GN* create the signals of the inverter transfer function F_i. The simulation results for the three-phase supply voltages, the output voltage and the output current of the matrix converter are shown in Fig. 9.

The sinusoidal character of the output current is represented for the so chosen *RLC* load. Fig. 9 illustrates a full confidence

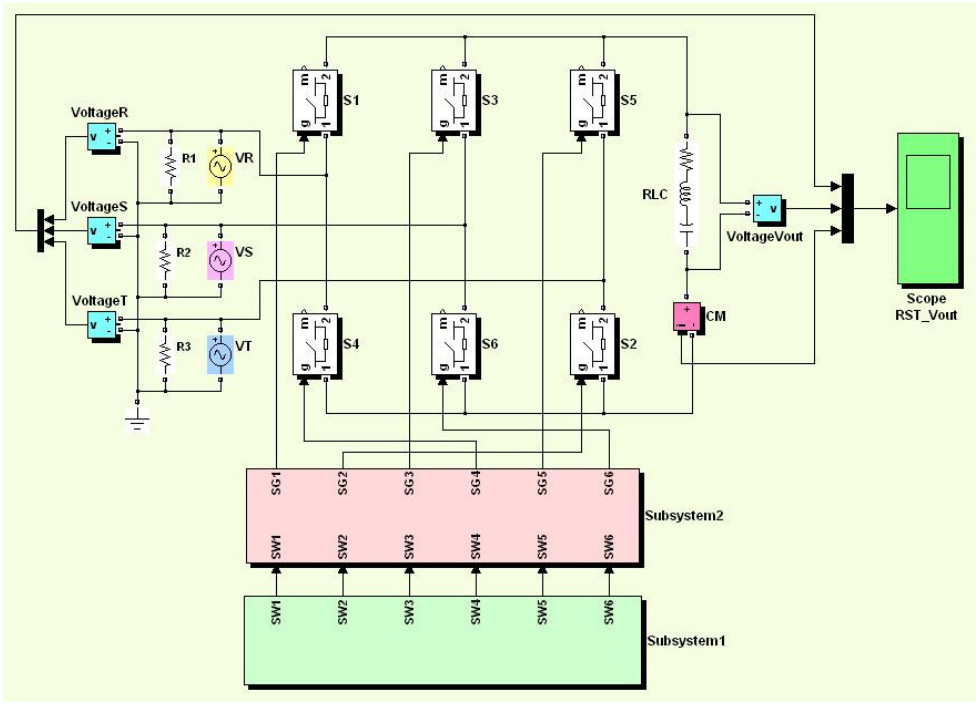

Fig. 6. Electrical circuit of the matrix converter represented in SIMULINK.

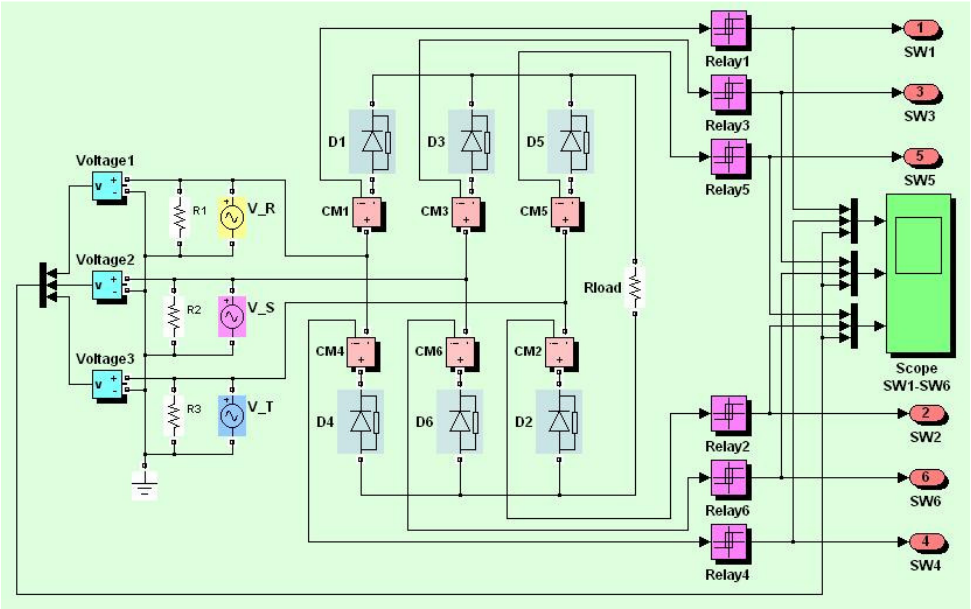

Fig. 7. Electrical circuit for creating the transfer function F_S.

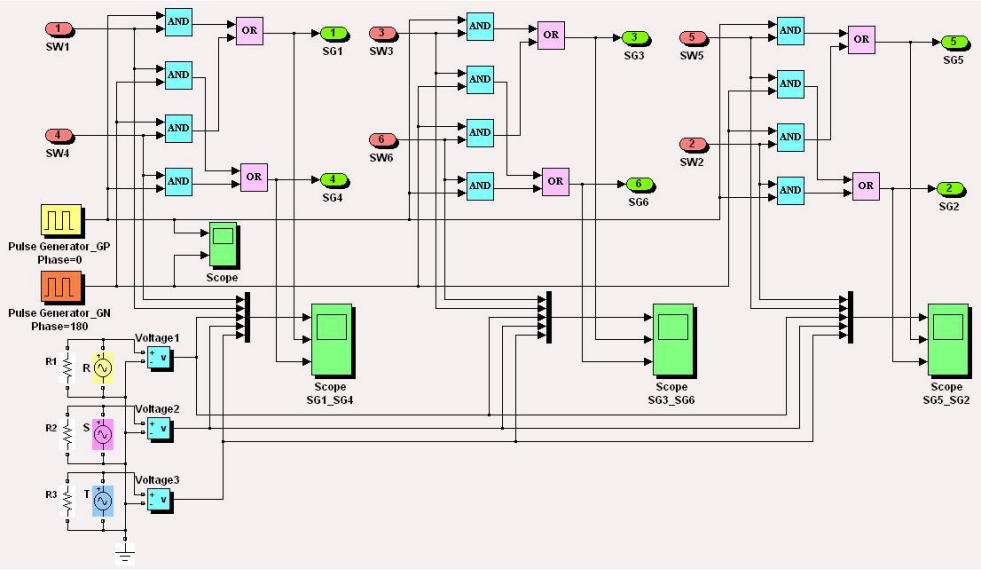

Fig. 8. Electrical circuit for creating the transfer function F_T.

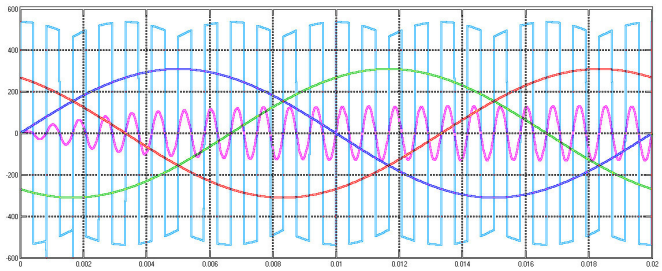

Fig. 9. Results from the computer simukation.

between the mathematical modeling using MATLAB and the SIMULINK simulation of the output voltage V_{out}.

IV. Conclusion

Mathematical dependencies have been derived, describing the operation of three-phase to single-phase matrix converter with a higher frequency. The expressions are suitable for computer simulation independently of the output load type. The simulation results using the program product MATLAB demonstrate the effective converter operation by the investigated load – series resonant circuit.

Acknowledgment

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Hierarchical Fault Diagnosis Using Sensor Data Fusion for Robotic System

Mohammad A. Nekoui, Amir R. Kashanipour, and Karim Salahshoor

***Abstract*—In this paper, we present a sensor data fusion based approach in a multi-layered, multi-agent architecture toward more reliable fault detection and isolation. This paper describes a sensor fusion approach to the detection of faults in robotic systems, based on multi-agent distributed diagnosis. Each of the agents uses an Adaptive Neuro-Fuzzy Inference System (ANFIS) and decision fusion is achieved by a Dempster-Shafer supervisor. In this work sensor level fusion used for generating residual signal more accurate and by considering uncertainties in sensors tried to compensate innate lack of model-based approach in detecting abrupt change. Based on distributing the diagnosis task by dedicating intelligent diagnosis agents for different parts of robot, decision fusion used in supervisory level to consider reliability of each agent, considering contingency faults scenario and failure symptoms. Adaptive Neuro-Fuzzy Inference System has been used as inference architecture for distributed sensor networks. Two types of ANFIS networks are used. An ANFIS based learning and adaptation is used for modeling the joints toward residual generation, while for residual evaluation another ANFIS is used. In this work online fault diagnosis based on sensor data fusion techniques for online fault diagnosis targeting robotic systems has proposed. Considering possibility of diagnosis one specific fault by more than one agent, practiced by using multiple ANFIS for different type of faults in each agent. Simulation results of controlled 3-Link Rigid Planar Manipulator controlled demonstrate capability of the proposed method toward achieving a fault tolerant controller.**

***Index Terms*—Fault diagnosis, signal processing, process control, neural networks, multi-agent system, hierarchical system, data fusion.**

I. Introduction

ROBOTIC platforms performing must be equipped with multiple and different types of sensors to accurately extract information about their surroundings toward performing their commanded operation. Using the information from the various sensors requires robust, real-time sensor fusion. When sensor error or failure occurs, multi-sensor fusion can reduce uncertainty in the information and increase its reliability [18]. Additionally, due to inherent sensor limitations and characteristic and the unknown environment it is very hard and sometimes impossible to predict a priori the failure characteristics. Therefore, there is a need to estimate online the cause of any failure and try to compensate it while the system is operating. Furthermore, many damages would happen to system because of possible obstacle which would lead to system parts like damaged actuators. This requires an algorithm that is able to diagnose the fault online toward achieving fault tolerant control over the system.

The demand for Fault Detection and Isolation (FDI) of nonlinear systems are significantly growing to improve system reliability, safety and efficiency. During last decade, FDI has increasingly used in many areas such as aerospace, chemical and mechanical systems. As robots are mostly designed to act autonomously and not directly supervised, and considering the special working environment they have been used in, attitude towards the use of autonomous fault diagnosis systems with minimum human interference magnifies the importance of these systems in robotic systems.

FDI techniques can be divided into two main Categories: techniques using either model of the system [1]–[3] or data-driven techniques [4, 5]. Using system model, where quantitative and qualitative knowledge-based models, data-based models, or combination of them are achievable, applied in more reliable manner. For data-driven approaches, only the availability of a large amount of historical process data is assumed. Different methods of extracting knowledge from historical data can lead to discriminate condition of the system healthy from faulty. There might be some overlap between the model-based and data-driven approaches; this classification is just based on whether or not the model of the process is required.

In model-based methods, generally speaking, the differences between measured and reference signals or simulated signals are computed continuously. Any non-zero differences, named residual, would declare a fault occurring. Using fuzzy logic and neural networks for fault detection and isolation has been demonstrated extensively in many theoretical and practical works.

In proposed method monitored system is modeled using Adaptive Neuro-Fuzzy Inference System (ANFIS). A hybrid method harnesses both Artificial Neural Networks (ANN) and Fuzzy Logic Systems (FLS) capabilities for modeling the nonlinear systems [6]. Due to wide range of operation domain in robotic systems (here 3-DOF manipulator) and their inherent nonlinear dynamics using hybrid approach for modeling each joint in its operational point has evaluated

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successfully. In isolation phase - determining the location of fault - by ANFIS as a classifier exact cause of fault determined. Due to burden of data in this phase, dedicating individual ANFIS to each type of faults suggested and practiced successfully.

In proposed scheme, we used distributed diagnostic agents for monitoring joints separately. Agents do not communicate by each other to decrease complexity of the overall system. Reliable decision making have achieved by availability of diagnosis of one specific fault by different agents. The overlap between duties of agents have assigned by the prior knowledge about propagation of faults in the robot. Agents have communication with supervisory system which the decision fusion takes place in it.

In many cases, different agents simply give multiple interpretations for a single event which is based on highly coupled dynamic of the system. This would bring a ambiguity and uncertainty in supervisory level for decision making. In this work each agent converts observed raw data into a preliminary declaration of fault identity. The identity declarations provided by the individual diagnosis agents are combined using decision level fusion. Many techniques for decision fusion have reported in different works such as Bayesian inference, weighted decision methods, Dempster-Shaffer Theory. In this work to handle the inherent uncertainty in fault diagnosis problems- system do not behave as it is expected and show deviation from its considered model- using Dempster-Shaffer sounds meaningful.

The proposed method is applied to fault diagnosis of a rigid 3-Link manipulator. The raw data provided form signals were measured from position and velocity sensors in each joint. Different kind of faults with variety of severity in presence of different unmeasurable disturbances simulated to evaluate the architecture. The results demonstrate the effectiveness of the method.

II. Fault Diagnosis Algorithms

In model-based diagnosis techniques, the designer uses analytical model of the plant to set up the FDI procedure. Based on relying on previous knowledge from the system or not, these methods could be categorized in two mainstreams. methods using analytical model of the process (usually known as model-based) and ones where the process model is constructed without the use of any knowledge obtained from physical laws(usually known as model-free).

In practice, owing to existence of uncertainties, it is not possible to attain an exact mathematical model of real-world processes such that it precisely mimics the system's behavior. One way to deal with the absence of a mathematical model is to build a model from input-output data. Artificial Neural Network and Fuzzy Logic/Inference systems have widely used for modeling the system behavior [7]–[10].

Basic idea behind most of these methods is using the difference between output of the healthy model and the real plant's output [11]. For detection phase, the output of the monitored system is comparing with process model, and if any magnificent change observed, occurrence of fault inferred. For isolation phase, the difference is classifying by different algorithms into corresponding classes of faults for determination the location of the fault, type of the faults and more.

Due to wide range of operational domain in robotic systems (also here in 3-DOF manipulator) and inherent nonlinear dynamics of such systems, modeling of system in its operation point to have minimum modeling error is a crucial task. Several modeling approach have suggested [12], also using multiple model in different operational point for tackling nonlinearity problem have been reported. In the most significant report [13] Local Model Networks LMNs modeling approach have suggested the division of the operating regime in parts, and then the correlation of each one with a local model approximates the plant behavior within the respective part of the operating regime. Although considering several models of the joints in the bank of models, results in a better performance, it drastically increases computational operations that are unfavorable in real-time tasks. Also, restricting the number of faults to a priory determined value does not seem reasonable. A special fault, such as variation of a parameter, can happen in a continuous domain. So it is impossible for the designer to create infinite models in the bank of models. It is a real burden to eliminate these faults using prepared models.

Implementation of these steps in this study have achieved by using ANFIS based on its modeling and identification capability. ANFIS harnesses both ANN and FLS capabilities for modeling the nonlinear systems as well as classification of data into predefined classes.

III. Adaptive Neuro-Fuzzy Inference System

There are three important characteristics of neural networks that make them suitable for modeling the behavior of the system: generalization ability, noise tolerance, and fast response once trained. Fuzzy logic also used for both fault detection via modeling and fault isolation via classification for nonlinear systems. An important advantage of fuzzy approaches is the fact that nonlinear systems can be modeled using set of linear model builds around a set of operating points.

A Fuzzy Logic System (FLS) can be introduced as a non-linear mapping from the input space to the output space. The mapping mechanism is based on the conversion of inputs from crisp numerical domain to fuzzy domain with the use of fuzzy sets and fuzzifiers, and then applying fuzzy rules and fuzzy inference engine to perform the necessary operations in the fuzzy domain. At the end, the result is converted back to the numerical domain using defuzzifiers.

Adaptive Neuro-Fuzzy networks are enhanced FLSs with learning, generalization and adaptively capabilities. In this paper, we use the Adaptive Neuro-Fuzzy Inference System

(ANFIS) structure and optimization processes because of their accuracy and our need for diagnose multiple faults.

To present the ANFIS architecture, two fuzzy if-then rule based on a first order Sugeno model are considered:

Rule 1: If (x is A_1) and (y is B_1) then ($z_1 = p_1x + q_1x + r_1$),

Rule 2: If (x is A_2) and (y is B_2) then ($z_2 = p_2x + q_2x + r_2$).

The ANFIS learning algorithm is then used to obtain these parameters. This learning algorithm is a hybrid algorithm consisting of the gradient descent and the least-squares estimate. Using this hybrid algorithm, the rule parameters are recursively updated until acceptable error is reached. In the defuzzification layer, crisp output is produced from the output of the inference layer. Maximum defuzzification and centroid defuzzification are used as defuzzifiers. Therefore, the resultant output is related to all the rules executed in the preceding layer. This is then compared with a threshold to determine whether or not a fault mode should be reported. The ANFIS used in this approach uses Gaussian functions for fuzzy sets, linear functions for the rule outputs and Sugeno's inference mechanism. The parameters of the network are the mean and standard deviation of the membership functions (antecedent parameters) and the coefficients of the output linear functions (Fig. 1).

In first stage, for modeling the system the position and velocity signals in combination with input torque and operation point of different joints of robot must fed into ANFIS to modeling the system. In the second stage to identify different abnormal cases different residuals of key variables must fed into fault isolation ANFIS. In the present work each of signals using by ANFIS for modeling recorded and used in normal operation mode. Multiple ANFIS have used for classify the residual toward diagnosing different faults. Combination of multiple ANFIS makes one diagnostic agents, applicable in different part of the system. Decomposing diagnosis task by local diagnosis agents reduce the computational burden of diagnosis system and increase the accuracy and rapidity of the system.

IV. Distributed Architecture

Recently there has been significant research activity in modeling, control and cooperation methodologies for distributed systems [8, 14]. Their applications especially in large-scale systems which have complex dynamic and spatially distributed and it is typically more convenient to decompose the system into smaller subsystems which can control locally, have been proved.

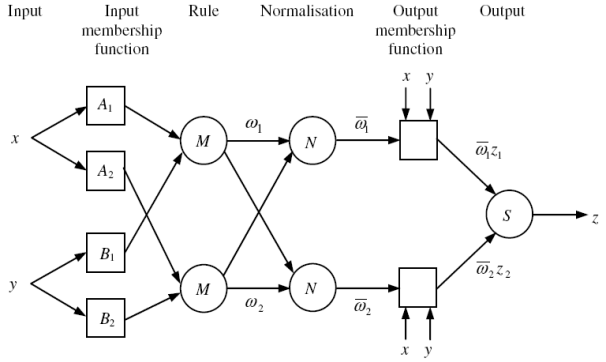

Fig. 1. ANFIS architecture to implement two rules.

In robotic systems diagnosing variety of faults based on variety of components (including mechanical, electrical, etc.) using commonly in these systems make robotic system a complex problem for fault diagnosis. Moreover the structure of robots, nonlinearity of the dynamic and wide range of task space, forces us to use hierarchical diagnosis system to reduce complexity of the problem. Using hierarchical architecture enables us to use its advantages like robustness, reliability, scalability and cooperation nature with high degree of flexibility and more demanded in this application quickness.

In this work decomposing task is done based on distribution of sensors and actuators also considering dynamics of robots. 3-DOF robotic manipulator system is partitioned into 3 areas; Note that diagnosis agents are trained to diagnosis neighbor area's faults for supporting each other in diagnosis task. Putting overlap between duty space of agents (toward diagnosing specific fault) guarantees redundancy of diagnosis and prevents ambiguity in decision making level.

V. Decision Fusion in Supervisory Level

Data fusion can be used to integrate information from a multisensor data array to validate signals and create features. At a higher level, fusion may be used to combine features in intelligent ways so as to obtain the best possible diagnostic information. In higher level, decision fusion is used to incorporate different fusion provided by different approach to use maximum knowledge. The combined result would yield an improved level of reliability about the system condition. However, one of the main concerns in any fusion technique is the probability of achieving a worse result than the best individual tool. The solution to this concern is to weigh a priori the tools according to their capability and performance. The degree of a priori knowledge is a function of the inherent understanding of the physical system and the practical experience gained from its operating history.

In the Dempster-Shafer approach, uncertainty in the conditional probability is considered. Dempster-Shaffer theory permits us to assign probability-like weights to a set of events (here faults) in a way that allows statements of uncertainty about verisimilitude of some of the cases. From the assign of weights we get two numbers; the degree to which a case is supported by the evidence (Belief), and the degree to which there is a lack of evidence to the contrary (Plausibility). These two numbers are the basis on which any belief-based decision is made.

Given many assigns of belief to the same set of events, there is a natural way of combining them to give a fused allocation of belief that deals both with uncertainty and with conflict between the original beliefs; we can then derive Belief and

Plausibility for the ensemble, and base our decision on this more acquisitive data.

We quantify the degree to which there is support contrary to the event (and by an obvious extension, a set of events) being considered. These two numbers, plausibility and belief, provide the basis for deciding that one event is more representative of the truth than another. If both values for a given event are higher than the corresponding values for all other events, then that event is the obvious candidate. In general, the event with the highest plausibility need not be the same as the event with the highest degree of belief. In this situation, a heuristic must be used that reflects the required strategy of the decision maker.

We consider three masses: the bottom-line mass m that we require, being the confidence in each sensor and agents of the power set; the measure of confidence m_s from sensors (which must be modeled); and the measure of confidence m_o from old existing evidence (which was the mass m from the previous iteration of Dempster's rule). Dempster's rule of combination then gives, for elements A;B;C of the power set:

$$m(C)=\left[\sum_{A\cap B=C} m_s(A)m_o(B)\right]\Big/\left[1-\sum_{A\cap B=\varnothing} m_s(A)m_o(B)\right] \quad (1)$$

Here in this paper we are going to investigate effect of sensor data fusion in fault diagnosis using Dempster's rule. There are six possible faults in each joint and we have two sensors in each joint. Sensor reliability was evaluated according to known characteristics, accuracy and range. We assign sensors' reliabilities according to some statistical experiments and previous knowledge on sensor characteristic in such systems which are:

In each join, reliability of position sensor is more than velocity sensor.

Reliability in the first joint elements is more than the second one and in second one is more than the third.

Dempster's rule of combination then is used to assimilate the evidence contained in the mass functions and to determine the resulting degree of certainty for detected fault modes. It can be viewed as a generalization of probability theory with special advantages in its treatment of ambiguous data and the ignorance arising from them.

VI. Simulation

A case study of 3DOF robotic manipulator is addressed for fault diagnosis purpose in this section. The studied manipulator simulated in Simulink® and controlled by an adaptive controller. A fault detection and isolation in robotic manipulator is considered. The robotic manipulator is modeled with three rigid links of length L_1, L_2 and L_3 and point masses m_1, m_2 and m_3 at the distal ends of the links. The dynamic model of a robotic manipulator is:

$$\tau = M(q)\ddot{q}+V_m(q,\dot{q})\dot{q}+G(q) \quad (2)$$

where q_1, q_2, q_3, $\dot{q}_1$, $\dot{q}_2$ and $\dot{q}_3$ are vectors of joint positions and velocities, respectively, τ_1, τ_2 and τ_3 are the input torque vector, $M(q)_{3\times3}$ is the inertia matrix, $V_m(q,\dot{q})_{3\times3}$ is a matrix containing centripetal and coriolis terms and $G(q)$ is the gravity vector. It is suggested that a Model-Reference Adaptive controller would be added to the system for controlling the manipulator. The Adaptive controller can stabilize the closed-loop system. The control law of the adaptive controller is:

$$T = K_p e + K_v \dot{e} + M_p \theta_d + M_v \dot{\theta}_d + M_\alpha \ddot{\theta}_d \quad (3)$$

where K_p, K_v, M_p, M_v and M_a are:

$$\begin{cases} K_p = \alpha\int eX_S^T + K_p(0) \\ K_v = \beta\int \dot{e}X_S^T + K_p(0) \end{cases} \quad \begin{cases} M_p = \lambda\int e\theta_d^T + M_p(0) \\ M_v = \mu\int e\dot{\theta}_d^T + M_v(0) \\ M_\alpha = \nu\int e\ddot{\theta}_d^T + M_\alpha(0) \end{cases} \quad (4)$$

and $e = X_m - X_s$ and $\dot{e} = \dot{X}_m - \dot{X}_s$.

It is shown that the closed-loop system obtained by using (3) is asymptotically stable. The stability of the closed loop system is guaranteed for any positive definite K_p and K_v, with no a priori knowledge about the system dynamics. The robotic manipulator has three input torques (τ_1, τ_2 and τ_3) and six outputs (q_1, q_2, q_3, $\dot{q}_1$, $\dot{q}_2$ and $\dot{q}_3$).

Although an adaptive controller can eliminates the faults effect after a while and take back the control of damaged or faulty (although by using wrong data acquired from faulty sensors) but diagnosing the real cause of the manipulator helps us through more reliable fault tolerant controller and maintenance purpose of manipulator.

Sensor and Actuators must accurately sense/deliver the determined value. The gains are one ($f_\alpha = 1$) while the robotic manipulator is intact. An actuator fault alarm will be set on when one of the actuators do not deliver the controller signal. Mathematically, it means that the actuator gain has become a number smaller than one.

In the proposed method, for diagnosis of the fault, no extra measurement or preprocessing is required for feature extraction. Following facts considered in the fusion process:

Position and velocity sensor faults can be approved or denied regarding velocity and sensor fault. Cross correlation between variables helps us to diagnosis sensor faults by using cluster based fusion in sensor level, here all sensor data considered in diagnosis process all Actuator fault can be detect in both position and velocity sensors in the same joint. This fact can be used for confirmation as well as combining the features existing in two recording signals.

Abnormal or large changes in the magnitude of controller signal determine an actuator fault. - If the fault represents a behavior that cannot be classified in the above categories, the fault belongs to "plant's component fault" category.

It is vital to detect all faults in minimum possible time after their occurrences. Manipulator links should track special paths. Hence, the desired position and velocity of each link, at each instance, is predetermined. For fault detection, the difference between the position sensor and velocity sensor and

model output are calculated. The desired trajectory for all links is considered to be continuous sinusoidal signal and frequency of 1/2π Hz. In simulation, some faults that occur at diverse times and result in abnormal conditions in robotic manipulator performance are considered.

The cross-dependence between the position and velocity measured signals (angle and angular velocity) is a major issue considered in dedicating duties to diagnosis agents and designing supervisory logic. If any fault occurring due to joints or manipulator both position and velocity sensors will report effects. If any damage occurs to position sensor which is directly using by controller, diagnosis agents would find out by using both position and velocity sensor.

These facts are obvious in Figs. 2 and 3 which shows the effect of actuator fault in sensor and velocity sensor of joint number 1.

Moreover, due to highly couple dynamic of the robotic manipulator, any actuator fault in any of joints would be detected in other joint sensor as shown in Fig. 4 as well as sensor faults shown in Fig. 5. These two facts play a main role through decision fusion in supervisory unit. The availability of diagnosis of fault in neighbor areas by neighbor agents needs overlapping of agent's duty. It may also seems extra computational task, but it must be noted that diagnosis of faults by neighbor agents brings the overall system extra redundancy and reliability.

Through the isolation phase, the joint position and velocities residual are utilized ANFIS inputs (the residual of the joint positions is a small range signal and must be amplified). The ANFIS outputs are trained to present integer number in output (i.e. signal 1 in the case of fault number 1) and 0 in healthy.

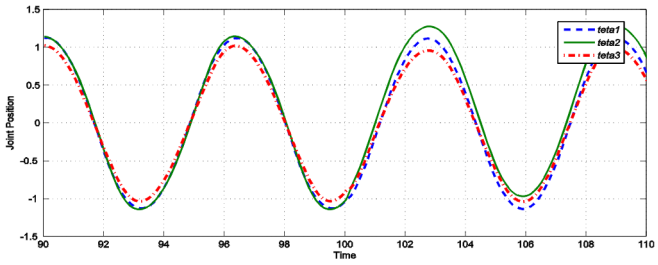

Fig. 2. Joint No. 1, actuator fault in position/angle sensor.

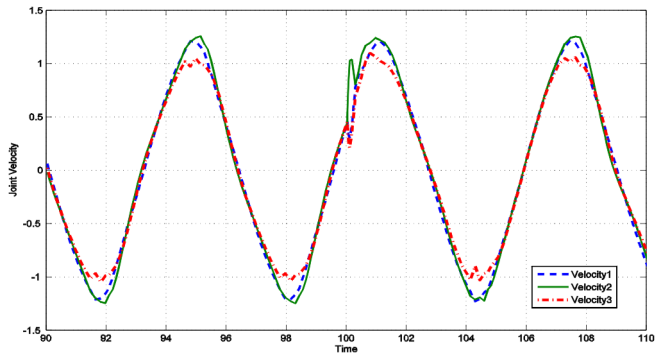

Fig. 3. Joint No.1, actuator fault in velocities sensor.

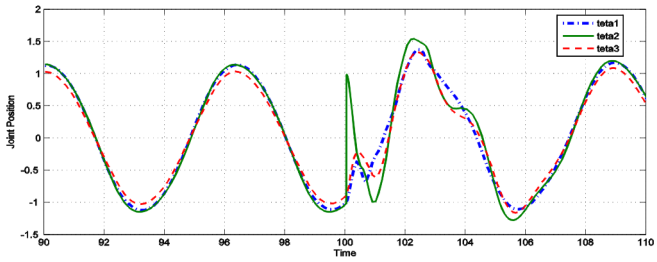

Fig. 4. Fault No. 1 in joint 2 recorded in position sensor No. 1.

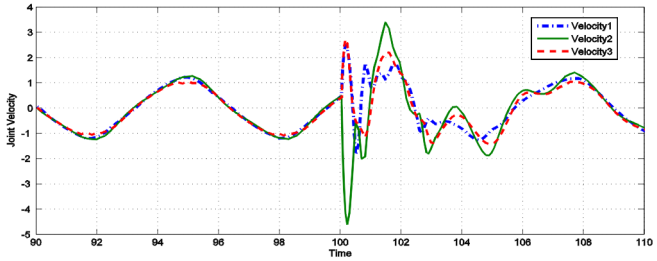

Fig. 5. Joint 2 of position sensor fault recorded in velocity sensor 1.

The fault criteria are: five consecutive signals in the ANFIS output have to be greater that 0.5 to a fault to be detected. The sensitivity of FDI system can be prejudiced adopting these criteria. However, if the sample rate is low, it does not represent a serious problem. For each fault a dedicated ANFIS classifier has been occupied to discriminate between two normal and faulty states. This strategy has been used to maximize the efficiency of diagnosing in time and computational burden aspects, according to size and nonlinearity of target dynamic. If all the faults in were put in single diagnosis unit or using just one central fault diagnosis agent ,as it is usual ,it will make the diagnosing process slower and the classification accuracy lower. Simulated faults details are given in Table I.

After training 15 different faults related to each joint Sensor reliability in Table II is evaluated according to known characteristics, accuracy and range.

Here experiment's data with the standard Dempster-Shafer

TABLE I
SIMULATED FAULTS DETAILS

Fault Type	Place of Occurrence	Observed in Sensors
Joint Lock	Actuator	Position and Velocity of Each Joint
Actuator Gain	Actuator	Position and Velocity of Each Joint
Actuator Bias	Actuator	Position and Velocity of Each Joint
Sensor Bias	Position/Velocity Sensor	Velocity/Position of Each Joint
Sensor Lost	Position/Velocity Sensor	Velocity/Position of Each Joint

TABLE II
RELIABILITY OF SENSOR BASED ON STATISTICAL STUDIES

	Fault	No. 1	No. 2	No. 3	No. 4	No. 5	No. 6
	Sensor	Reliability (percent %)					
Joint 1	Position	66	68	60	72	74	76
	Velocity	64	66	68	70	72	74
Joint 2	Position	64	66	68	70	72	74
	Velocity	62	64	66	68	70	72
Joint 3	Position	62	64	66	68	70	72
	Velocity	60	62	64	66	68	70

method results are shown in Table III. In the Table III, the reliability in each agent for different fault shown and final result for overall diagnosis system show the efficiency of proposed method.

The proposed method using separate diagnosis agent on each joint of robot, each are capable to diagnose different type of fault by using multiple ANFIS, and a supervisory unit using Dempster-Shaffer based decision fusion to localize the exact place of occurred fault by the data it receive from the diagnosis agents. This decentralization of diagnosis task helps us to diagnose and localize the fault in any demanded robot with any degree of freedom as well as mobile robots, with a rather fast and accurate efficiency. Using fusion in supervisory level help the overall system improve its efficiency in a meaningful way Simplicity and transparency in structure, high accuracy and speed, conformation with human's experience, no need for extra measurement or pre-processing are some advantages of the proposed method.

The generalization of this method relies on using distributed diagnostic agents for different parts of the system and considering relations in robotics systems in fusion process which would occur in supervisory level.

VII. CONCLUSION

This paper presented computationally simple, fast and accurate expert system for fault diagnosis of robotic systems. In this paper, a hierarchical fault diagnosis for large faults number applying to unknown nonlinear systems was investigated. Simplicity, transparency, rapidity and generalization are the dominant features of the proposed technique. Neuro-fuzzy modeling capabilities were employed to create some transparent models using fault-free input-output data. The proposed method can be extended to other applications with little modifications.

TABLE III
DECISION FUSION RESULTS IN SUPERVISION LEVEL

Fault No.	Joint 1	Joint 2	Joint 3	Diagnosis Efficiency
	Belief Value in percent			
1	97.76	97.12	96.4	99.99770%
2	98.32	97.76	97.12	99.99890%
3	98.8	98.32	97.76	99.99950%
4	99.2	98.8	98.32	99.99980%
5	99.52	99.2	98.8	100.00000%
6	99.76	99.52	99.2	100.00000%

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Optimum Torque/Current Control of Dual-PMSM Single-VSI Drive

Andrea Del Pizzo, Diego Iannuzzi, and Ivan Spina

***Abstract*—The paper deals with isotropic PM-brushless drives in configuration "single-inverter, dual-motor" operating with unbalanced load-torques. An innovative control algorithm is presented. It is suitable to minimize the resultant armature current needed to obtain an assigned resultant motor torque, whatever is the load unbalance. Simplified analytical expressions are given in order to quickly evaluate optimized reference currents with good approximation. From these reference values, a predictive feeding algorithm evaluates the reference voltage space-vector for the inverter supplying the two motors in parallel. Current and torque oscillation, torque/current ratio, dynamic response and stability are the mainly observed quantities. Effectiveness of proposed control techniques is highlighted.**

***Index Terms*—PMSM motor, dual motor, optimized control.**

I. Introduction

VECTOR and predictive control of ac drives are widely investigated and used in many application fields with reference to the classical configuration "single-inverter, single-motor". A considerable interest has been also devoted to the control of drives composed by a single inverter feeding more motors in parallel. Main targets of these drives are reduced sizes and costs with respect to the single motor drives, either in industrial or in traction applications. Some scientific papers and practical applications can be found concerning single-inverter dual-motor drives which use induction motors, either with scalar or vector control [1, 2]. In these cases, for control purposes the parallel connected motors are assumed equivalent to one single motor. The majority of the papers refer to a dynamic machine model of the combined, parallel connected, dual induction motor system [3]. In addition, these papers illustrate torque-control methods based on the previous model, which enable mean and differential torque to be controlled during transient and steady-state operations.

The above described problems are not widely dealt with in the literature in case of PM-brushless motors supplied in parallel by a single inverter, as it can occur in those traction or industrial applications where PM motors are more and more requested.

In these multi-motor drives either steady-state or transient operations could be more critical than in case of induction motors. This is due to the constancy of the rotor flux and to the absence of a rotor winding able to positively react in case of transient operations. In fact, considering two motors supplied in parallel by same frequency and voltage and with load unbalance, while in case of induction motors the rotor speeds get different values depending on the load-torque, in case of PM-brushless synchronous motors the rotor speeds are equal at steady-state, whatever is the unbalance values. As a consequence, when the load-torque of one motor suddenly varies, a risk of instability could occur if the angle between the armature voltage and e.m.f. vectors runs over $\pi/2$.

In the technical literature some authors have proposed a steady-state control of torque angle of only a motor a time, selecting that one with highest load-torque [4, 6, 7].

Other authors have suggested simple control configurations based on two main criteria: in a first case the two real motors are substituted by a single "equivalent" motor, by suitably handling measured current and speed values of each motor; in a second case the control and feeding algorithms are separately applied for the two motors and the resultant converter voltage is obtained by properly manipulating two voltage space-vectors separately evaluated. In this paper a new control technique is presented: on the basis of the measured speed and of the reference torque of both motors, the reference currents are evaluated in analytical way, imposing an optimizing condition to reduce the inverter size. A predictive feeding algorithm is used to evaluate the reference voltage space-vector for the inverter supplying the two motors in parallel.

II. Mathematical Model

We refer to two isotropic PM-brushless motors supplied in parallel by a single inverter (Fig. 1).

We assume that parameters and rated values of motors "A" and "B" are equal, but each of them can be arbitrarily charged (unbalanced loads). Assuming sinusoidal the induced e.m.f. for both motors, their mathematical models in the respective rotor reference systems (superscript *a* or *b*) are expressed by:

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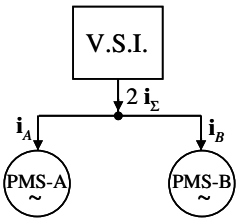

Fig. 1. Schematic representation of a single-inverter dual-motor configuration.

$$\begin{cases} \mathbf{v}_A^a = R\cdot\mathbf{i}_A^a + L_s\dfrac{d}{dt}\mathbf{i}_A^a + jp\,\omega_{r,A}L_s\mathbf{i}_A^a + jp\,\omega_{r,A}\,\Phi_{r,A} \\ T_A - T_{L,A} = J_A\dfrac{d}{dt}\omega_{r,A};\ T_A = \dfrac{3}{2}\,p\,\Phi_{r,A}\Im m\left\{\mathbf{i}_A^a\right\} \\ \omega_{r,A} = \dfrac{d}{dt}\vartheta_A \end{cases} \tag{1}$$

$$\begin{cases} \mathbf{v}_B^b = R\cdot\mathbf{i}_B^b + L_s\dfrac{d}{dt}\mathbf{i}_B^b + jp\,\omega_{r,B}L_s\mathbf{i}_B^b + jp\,\omega_{r,B}\,\Phi_{r,B} \\ T_B - T_{L,B} = J_B\dfrac{d}{dt}\omega_{r,B};\ T_B = \dfrac{3}{2}\,p\,\Phi_{r,B}\Im m\left\{\mathbf{i}_B^b\right\} \\ \omega_{r,B} = \dfrac{d}{dt}\vartheta_B \end{cases}$$

where $\mathbf{i}_A$, $\mathbf{i}_B$ are the current space-vectors of motors "A", "B", and the other symbols are explained in the list at the end of the paper. Denoting by 2ψ the angular displacement between the axes of the rotor fluxes $\mathbf{\Phi}_A$ and $\mathbf{\Phi}_B$ (Fig. 2), the equivalent *d*-axis is assumed in the mean position between $\mathbf{\Phi}_A$ and $\mathbf{\Phi}_B$, while the flux magnitude produced by permanent magnets is the same ($\Phi_{r,A} = \Phi_{r,B} = \Phi_r$), since we suppose the two motors equal.

In the new equivalent reference system (mean flux position), (1) become:

$$\begin{cases} \mathbf{v}_\Sigma = R\cdot\mathbf{i}_\Sigma + L_s\dfrac{d}{dt}\mathbf{i}_\Sigma + jp\,\omega_{r\Sigma}L_s\mathbf{i}_\Sigma + jp\,\omega_{r\Delta}L_s\mathbf{i}_\Delta + \\ \qquad + jp\,\omega_{r\Sigma}\,\Phi_r\cos\psi + p\,\omega_{r\Delta}\,\Phi_r\sin\psi \\ T_\Sigma - T_{L,\Sigma} = J\dfrac{d}{dt}\omega_{r\Sigma} \quad \text{with: } T_\Sigma = \dfrac{3}{2}\,p\,\Phi_r\left(i_{\Sigma q}\cos\psi + i_{\Delta d}\sin\psi\right) \\ \\ 0 = R\cdot\mathbf{i}_\Delta + L_s\dfrac{d}{dt}\mathbf{i}_\Delta + jp\,\omega_{r\Sigma}L_s\mathbf{i}_\Delta + jp\,\omega_{r\Delta}L_s\mathbf{i}_\Sigma + \\ \qquad + p\,\omega_{r\Sigma}\,\Phi_r\sin\psi + jp\,\omega_{r\Delta}\,\Phi_r\cos\psi \\ T_\Delta - T_{L,\Delta} = J\dfrac{d}{dt}\omega_{r\Delta} \quad \text{with: } T_\Delta = \dfrac{3}{2}\,p\,\Phi_r\left(i_{\Delta q}\cos\psi + i_{\Sigma d}\sin\psi\right) \end{cases}$$

where subscripts "Σ" and "Δ" refer respectively to "mean" and "differential" quantities, defined as (for a generic variable *G*):

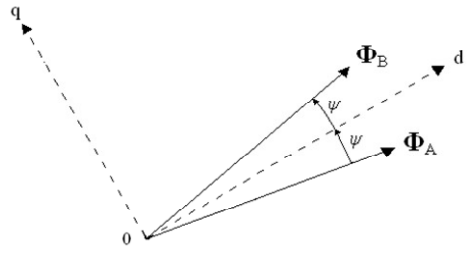

Fig. 2. Reference system.

$$G_\Sigma = \frac{G_A + G_B}{2} \quad ; \quad G_\Delta = \frac{G_A - G_B}{2}.$$

In steady-state operations, denoting by $\omega_r = \omega_{r,A} = \omega_{r,B}$ the rotor speed of both motors, the mathematical model is given by:

$$\begin{cases} \mathbf{V}_\Sigma = R\cdot\mathbf{I}_\Sigma + jp\,\omega_r L_s\mathbf{I}_\Sigma + jp\,\omega_r\,\Phi_r\cos\psi \\ 0 = R\cdot\mathbf{I}_\Delta + jp\,\omega_r L_s\mathbf{I}_\Delta + p\,\omega_r\,\Phi_r\sin\psi \\ T_\Sigma = \dfrac{3}{2}\,p\,\Phi_r\left(I_{\Sigma q}\cos\psi + I_{\Delta d}\sin\psi\right) \\ T_\Delta = \dfrac{3}{2}\,p\,\Phi_r\left(I_{\Delta q}\cos\psi + I_{\Sigma d}\sin\psi\right). \end{cases} \tag{2}$$

In a control problem, ω_r, T_Σ and T_Δ are known quantities; then, the system (2) corresponds to a set of six real equations with seven real unknown quantities ($\mathbf{V}_\Sigma, \mathbf{I}_\Sigma, \mathbf{I}_\Delta, \psi$). Due to this degree of freedom, one 'auxiliary condition' is needed in order to solve the system (2). This condition could represent the *control algorithm* for the considered dual drive.

III. Current Control Algorithm

A noticeable quantity is the torque to current ratio:

$$\rho = \frac{T_A + T_B}{\left|\mathbf{I}_A + \mathbf{I}_B\right|} = \frac{T_\Sigma}{\left|\mathbf{I}_\Sigma\right|} = \frac{T_\Sigma}{I_\Sigma}. \tag{3}$$

On the basis of (2) ρ can be expressed as:

$$\rho = \frac{A\sin\psi\cos\psi}{\sqrt{\left(B\cos\psi + C\sin\psi\cos^2\psi\right)^2 + \left(D\sin\psi + E\sin^3\psi\right)^2}}$$

$$\rightarrow \rho = \rho\left(T_A, \frac{T_B}{T_A}, \omega_r, \psi\right)$$

where:

$$A = T_\Sigma 3p\,\Phi_r Z^2; \quad B = 2T_\Delta Z^2; \qquad C = -3p^3{\omega_r}^2{\Phi_r}^2 L$$

$$D = 2T_\Sigma Z^2 \quad ; \quad E = 3p^2\omega_r{\Phi_r}^2 R; \quad Z = \sqrt{R^2 + \left(p\omega_r L\right)^2}.$$

The qualitative curve $\rho(\psi)$ is plotted in Fig. 3a for assigned values of ω_r, T_A and of load-unbalance $r=T_B/T_A$. This behavior suggests to state as control algorithm the condition:

$$\max\left\{\frac{T_\Sigma}{I_\Sigma}\right\} \quad \Rightarrow \quad \frac{\partial}{\partial\psi}\left(\frac{T_\Sigma}{I_\Sigma}\right) = \frac{\partial\rho}{\partial\psi} = 0 \tag{4}$$

which is also suitable to minimize the size of the feeding inverter.

In case of balanced shaft loads, (4) corresponds to separate maximization of both torque/current ratios $\{T_A/|\mathbf{I}_A|\}$ and $\{T_B/|\mathbf{I}_B|\}$ for the two motors.

From (2) it is easy to verify that the d-q components of the "mean" current $\mathbf{I}_\Sigma = I_{\Sigma d} + j\,I_{\Sigma q}$ are:

$$\begin{cases} I_{\Sigma d} = \dfrac{2T_\Delta}{3p\,\Phi_r}\dfrac{1}{\sin\psi} - \dfrac{\left(p\omega_r\right)^2\Phi_r L}{R^2 + \left(p\omega_r L\right)^2}\cos\psi \\ I_{\Sigma q} = \dfrac{2T_\Sigma}{3p\,\Phi_r}\dfrac{1}{\cos\psi} + \dfrac{p\omega_r\Phi_r R}{R^2 + \left(p\omega_r L\right)^2}\dfrac{\sin^2\psi}{\cos\psi}. \end{cases} \tag{5}$$

By substituting (5) in (4) we deduce that the derivative (4) becomes a transcendent function of ψ, not solvable in analytical way. However, we can demonstrate that the function $\rho = T_\Sigma / I_\Sigma$ is positive in the interval $\psi \in (0, \pi/2)$ and $\rho = 0$ either for $\psi = 0$ or $\psi = \pi/2$. Consequently, ρ has a maximum ρ_{optim} in the interval $(0, \pi/2)$ in correspondence of a ψ_{optim} value (see Fig. 3a. Diagrams b, c and d of Fig. 3 show the shifting of the point $(\psi_{optim}, \rho_{optim})$ in correspondence of different values of either $r = T_B/T_A$, or ω_r or T_A respectively.

With reference to a pair of equal motors, whose rated parameters are in Table I (see section VI), Fig. 4 show the behaviour ρ_{optim} against r (i.e. for different unbalanced conditions) in correspondence of different load torques T_A and for two different steady-state rotor speeds ω_r (continuous lines).

In correspondence of relatively low values of load unbalance, the angle ψ_{optim} is enough small to assume:

$$\sin\psi \cong \psi \quad ; \quad \cos\psi \cong 1. \tag{6}$$

Introducing this approximation, (4) becomes a 1st degree equation in ψ and a very simple analytical expression of ψ_{optim} can be found:

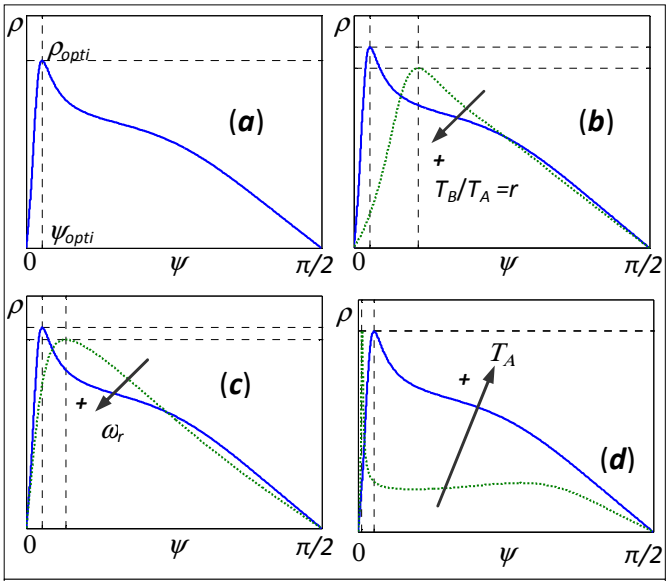

Fig. 3. Behavior of ρ as a function of ψ (a) and for different values of r, ω_r, T_A (b), (c), and (d).

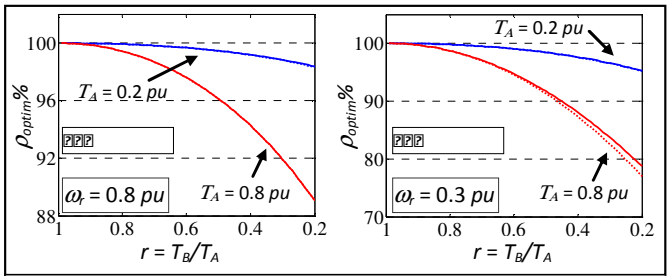

Fig. 4. Behavior of ρ_{optim} % as a function of the load-unbalance r, for two different speed values and for low and high load.

$$\psi_{optim}^{(a)} = \frac{2T_\Delta \left[R^2 + \left(p\omega_r L \right)^2 \right]}{3p^3 \omega_r^{\,2} \Phi_r^{\,2} L} \text{ ; with } T_\Delta = T_A \frac{1-r}{2} \tag{7}$$

where $\psi_{optim}^{(a)}$ is the approximated value of ψ which maximizes the $\rho = T_\Sigma / I_\Sigma$ ratio. It is independent on T_Σ and can be analytically determined. The correspondent curves of approximated ρ_{optim} are plotted against r in Fig. 4 with dotted lines. As we can see, they are generally very close to the not simplified curves and differ from them only for low values of r (≡ high load unbalance).

The validity of the approximation (6) is also confirmed by the compared behaviours of ψ_{optim} and $\psi_{optim}^{(a)}$ in Fig. 5 which refers to the same cases analysed in Fig. 4.

From Figs. 4 and 5, we also deduce that as higher load unbalance is, as lower the maximum value of ρ_{optim} and higher the shift angle ψ_{optim}.

In correspondence of the optimized condition (3), in Fig. 6 magnitude I_Σ of the mean current is drawn against unbalance r, for different speed and load conditions.

These values are compared to the approximated ones, obtained using (5)-(7), and to the ones obtained using a different control technique, named “one motor control”, better explained in section V [4]. While the differences between

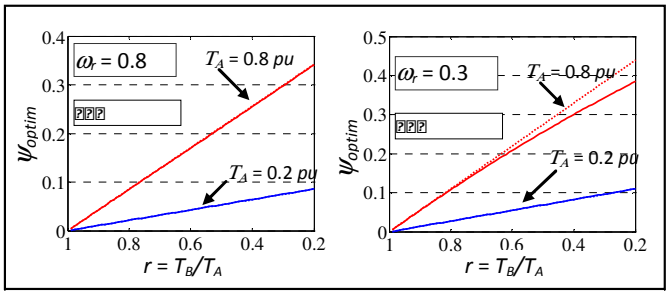

Fig. 5. Behavior of ψ_{optim} and $\psi_{optim}^{(a)}$ as a function of the load-unbalance r, for two different speed and load-torque values.

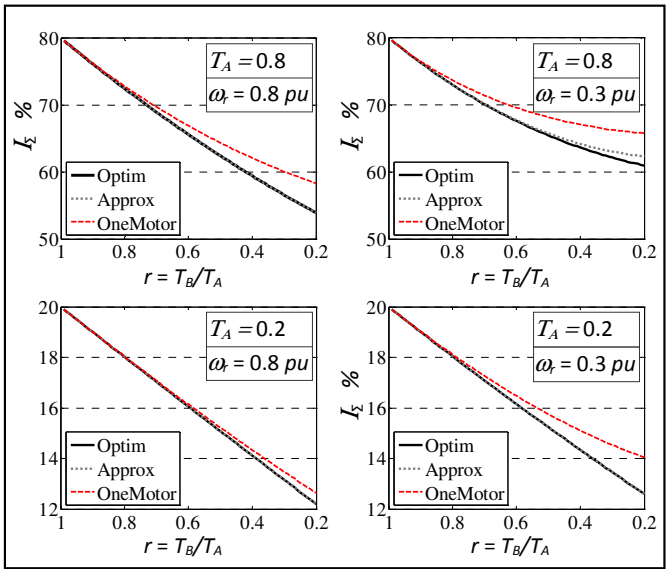

Fig. 6. Magnitude of the mean current I_Σ for different control techniques in some speed and torque operating condition.

exact and approximated I_Σ curves are very small, the current I_Σ assumes considerably higher values in the case of the "one motor control" technique, with negative consequences on the converter size.

IV. Predictive Feeding Algorithm

A predictive feeding algorithm can be useful to reduce current and torque distortion with respect to the use of hysteresis or PI current controllers [5].

We consider the discrete stator model of isotropic PM motors with all the electric quantities expressed in the mean *d,q* reference frame:

$$L_s \frac{d}{dt}\mathbf{i} + \dot{Z}_s\, \mathbf{i} = \mathbf{v}_n - \boldsymbol{\varepsilon}_n ; \quad \text{for } t \in (t_n, t_{n+1}) \tag{8}$$

where: $\dot{Z}_s = R + j\, p\, \omega_r\, L_s$; $\boldsymbol{\varepsilon}_n = j\, p\, \omega_{r,n} \Phi_r \cos\psi_n$.

In (8) $\mathbf{v}_n$ and $\mathbf{e}_n$ are evaluated at a generic sampling instant t_n. During the interval $(t_n,\ t_{n+1})$, thanks to some suitable assumptions in the model (8), we can evaluate the reference voltage $\mathbf{v}^*_{n+1} = v^*_{d,n+1} + j\, v^*_{q,n+1}$ to be applied at the instant t_{n+1}, in order to obtain – at the instant t_{n+2} – armature current $\mathbf{i}_{n+2}$ equal to the reference current at t_n (i.e, $\mathbf{i}_{n+2} = \mathbf{i}^*_n$). We have:

$$\mathbf{v}^*_{n+1} = \boldsymbol{\varepsilon}_n + \dot{Z}_s \frac{\mathbf{i}^*_{\Sigma,n} - \dot{\alpha}_t \left[\dot{\alpha}_t \left(\mathbf{i}_{\Sigma,n} - \dfrac{\mathbf{v}_n - \boldsymbol{\varepsilon}_n}{\dot{Z}_s} \right) + \dfrac{\mathbf{v}_n - \boldsymbol{\varepsilon}_n}{\dot{Z}_s} \right]}{1 - \dot{\alpha}_t} \tag{9}$$

where: $\dot{\alpha}_t = \mathrm{e}^{\frac{\dot{Z}_s}{L_s}\Delta t}$ with: $\Delta t = t_{n+1} - t_n$.

The feeding algorithm (9) needs only the knowledge of the reference current $\mathbf{i}^*_{\Sigma,n} = i^*_{\Sigma d,n} + j\, i^*_{\Sigma q,n}$ and of the motor state in t_n [i.e.: $\psi_n, i_{\Sigma d,n}, i_{\Sigma q,n}, \omega_{r,n} = (\omega_{r,A,n} + \omega_{r,B,n})/2$].

V. Control Diagram

The used speed control circuit is described in Fig. 7.

The actual speed of each motor is separately detected and compared with the imposed ω^*_r speed value. From the two reference torques T^*_A and T^*_B, the block C_1 evaluates the mean and differential reference torques T^*_Σ, T^*_Δ and, in cascade, C_2 evaluates the reference currents $i^*_{\Sigma d}, i^*_{\Sigma q}$ by means of (5) and using $\psi^{(a)}_{optim}$ calculated by block C_3 corresponding to (7). An encoder on each rotor shaft separately detects actual values of position and speed. The estimated *d,q* components $\hat{i}_{\Sigma d}$, $\hat{i}_{\Sigma q}$ of the actual mean currents are derived from measurement of the resultant inverter currents.

Reference and actual currents, together with mean actual speed $\hat{\omega}_r$, are used by the "predictive current controller" to evaluate the reference voltages v^*_d, v^*_q, which are transformed in stator coordinates *x,y* using the mean angular position $\hat{\theta} = (\theta_A + \theta_B)/2$. Comparing the proposed control technique with the ones in literature [6] we can observe that in Fig. 7 the reference currents $\hat{i}_{\Sigma d}$, $\hat{i}_{\Sigma q}$ are evaluated by imposing an optimizing analytical criterion while in [6] they are obtained simply adding the values separately obtained for the two motors. Another advantage of the proposed control is that only the feedback of the resultant stator currents is used (instead of a double current loop).

In the next section, the numerical results of the "proposed control technique" are compared to the one obtained using the simpler control diagram of Fig. 8 ("one-motor control"), as proposed in the literature [4].

VI. Numerical Analysis

A numerical analysis is carried out with reference to two three-phase PM brushless motors having equal rated values, as summarized in Table I.

The average switching frequency of the IGBT-SVM voltage source inverter is about 2 kHz. The load torque characteristic of both motors is assumed linear in function of the angular speed. Reference speed is set to $\omega^*_r = 0.8\,\omega_{r,R}$ for the case in Fig. 9.

Actual speeds, torques and currents of both motors A and B are plotted in Fig. 9, together with the mean currents $i_{\Sigma d}$, $i_{\Sigma q}$, the voltage amplitude and the shifting angle between the two rotor polar axes.

The letters inside the figure have the following meaning: A) actual speeds of both motors; B) electromagnetic and load

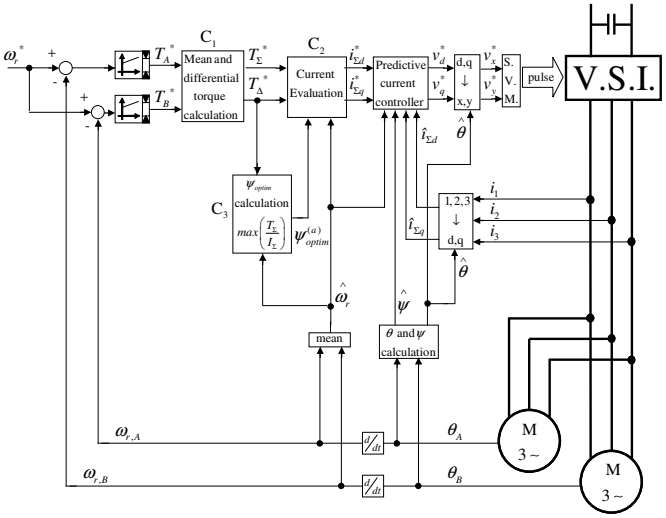

Fig. 7. Proposed control circuit.

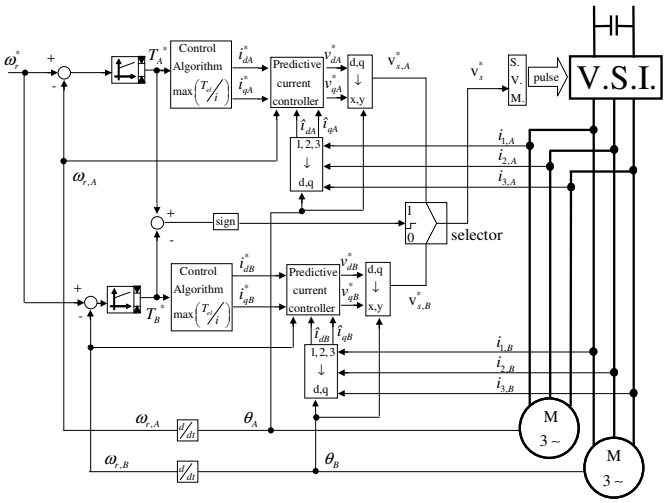

Fig. 8. One-motor control circuit.

TABLE I
MAIN DATA OF BOTH PM MOTORS

Rated power P_R	74 *kW*	Rated speed $\omega_{r,R}$	33.5 *rad s*$^{-1}$
Pole-pair p	8	Rotor inertia J_r	0.9 *kgm*^{2}
Rated voltage V_R	570 *V*	Armature inductance L	5.7 *mH*
Rated current I_R	128 *A*	Armature resistance R	0.27 Ω

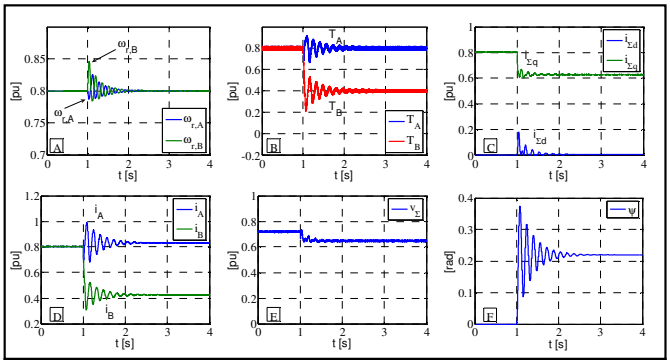

Fig. 9. Numerical results of proposed control technique for ω_r*=0.8 pu.

torque of both motors; C) *d*-axis and *q*-axis components of the mean current; D) current magnitude of both motors; E) magnitude of reference voltage space-vector; F) electrical angle ψ between the two rotor frames.

The load conditions are equal for both motors until the instant t=1 s, and correspond to load-torque values $T_{A,L}$=$T_{B,L}$=0.8 pu of the rated torque. At the instant t=1 s, a step variation from 0.8 to 0.4 pu (50%) of the load torque is introduced for motor B, in order to test the capability of the system to get a steady-state condition together with acceptable values of amplitude both of torque and current oscillations. From the diagrams we can deduce that the decrease of the load torque $T_{B,L}$ produces transient variations in all the electromechanical quantities of both motors A and B.

Referring to Fig. 9, when steady-state is reached, the speeds of the two motors assume again the initial value 0.8 $\omega_{r,R}$; the electromagnetic torques of both motors follow the respective load values; the *d*-component $i_{\Sigma d}$ of the mean current is practically equal to zero, while the *q*-component $i_{\Sigma q}$ decreases of about 25%. The angular positions of the two rotors assume different values and the shift-angle between them remains constant.

The diagrams of Fig. 10 represent the same quantities of Fig. 9, in equal operating conditions, but with reference to the control circuit of Fig. 8 ("one-motor control").

The following Figs. 11 and 12 show analogous quantities of Figs. 9 and10 with reference to low speed operating condition.

Comparing the results of Figs. 9 and 11 to the ones of Figs. 10 and 12, it is easy to deduce that the "proposed control technique" (circuit in Fig. 7) gives rise to better performance both in steady-state and dynamic operations, with respect to the "one-motor control" circuit in Fig. 8. In fact, $i_{\Sigma d}$ in Figs. 10c and 12c assumes steady-state values considerably higher than in the correspondent ones in Figs. 9c and 11c. Moreover, it is evident the greater time needed by the

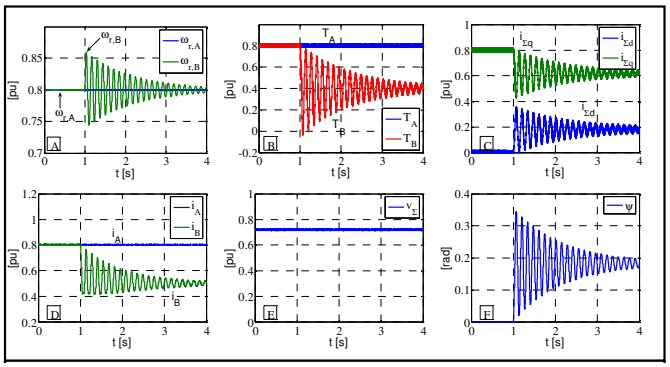

Fig. 10. Numerical results of one-motor control technique for ω_r*=0.8 pu.

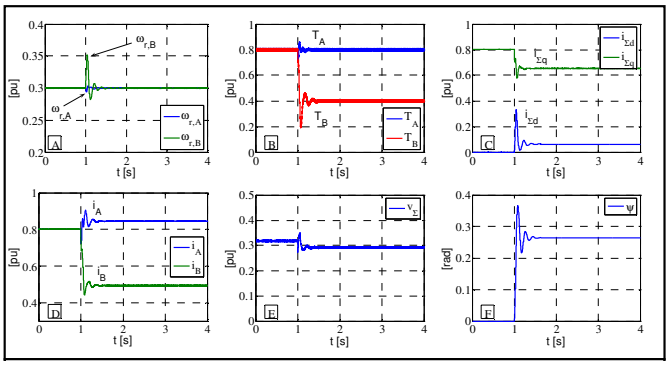

Fig. 11. Numerical results of proposed control technique for ω_r*=0.3 pu.

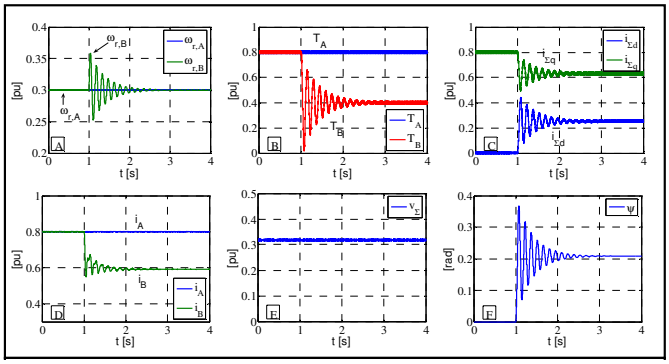

Fig. 12. Numerical results of one-motor control technique for ω_r*=0.3 pu.

"one-motor control" together with a greater magnitude of torque, speed and current oscillations.

VII. SHORT CONCLUSIVE REMARKS

With reference to a drive composed by a single inverter feeding two isotropic PM brushless motors in parallel, a new control technique is proposed in order to manage load unbalances. It is based on a control algorithm and a feeding algorithm in cascade. The feeding algorithm uses the predictive voltage evaluation already presented in [6] that is able to obtain low values of current distortion and torque pulsation. The control algorithm is based on an auxiliary condition which optimizes the set of two motors, aiming to maximize the ratio (resultant torque)/(resultant current).

The main features of the proposed control are: a reduced number of current transducers, steady-state operations with the

minimum input current for every resultant load-torque in case of load unbalance (reduction of inverter size), reduced over-shoot and acceptable dynamics in transient operations, good stability also in presence of heavy variations of the load torque on only one motor.

APPENDIX

$\mathbf{I}_A, \mathbf{I}_B$	steady-state current of motor A, B
$\mathbf{I}_\Sigma, \mathbf{I}_\Delta$	steady-state mean and differential current
L	armature inductance
p	pole-pair
R	armature phase resistance
$T_{A,L}, T_{B,L}$	load torque of motor A, B
$\theta_A ; \theta_B$	angular position of rotor A, B
Φ_r	air-gap flux of rotor magnets
ω_r	rotor angular speed
$\omega_{r,R}$	rated value of rotor angular speed
ψ_{optim}	optimized shift angle between rotor polar axes

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Power Losses in Leads and Interconnections of Coaxial Linear Transformer

Boguslaw Grzesik, Bodzek Krzysztof, and Mariusz Stepien

***Abstract*—Proposed high frequency (1 MHz) coaxial linear transformer has many advantages: high efficiency (99.26%), high coupling of windings and high power density(2.6 kW). The main drawbacks are relatively high power losses generated in interconnections and leads. The paper contains analysis of these losses that has been done with ANSYS (FEM), basing on 2D and 3D models.**

***Index Terms*—Modular, tubular, transformer, ansys, power loss, leads.**

I. Motivation and Introduction

THE needs for energy efficient transformers motivates this work, that is continuation of authors' previous work [1]. The paper describes high frequency coaxial linear transformer, cf. section 3, 4 and 9. The transformer belongs to the class of the transformers of highest efficiency. In previous work [1], authors analyzed this transformer using 2D planar FEM model in which interconnections and leads (Fig. 3) of the windings were neglected. In order to get the information about the influence of the interconnections and leads of this transformer on its characteristics and overall losses, and efficiency in it. In comparison with transformers described in [2] and [3], proposed transformer have higher coupling between primary and secondary windings and higher efficiency.

The losses in interconnections and leads of the transformer and efficiency are analyzed with FEM software and the latter are measured in the experimental transformer. Analysis was done for planar 2D, 3D and hybrid model called 2D/3D. The losses in interconnections and leads are taken from 3D model while in windings and ferrite core taken from planar 2D transformer. 2D/3D model allows one to carry on analysis of transformer of any length. It is necessary to underline that results from 2D/3D model are close with the ones obtained from 3D.

II. Assumptions

The following assumptions has been taken for the analysis.

1. Experimental transformer:
   - turn-to-turn ratio of k=3/2 (method of interconnection of elementary transformer is described in [1],
   - windings made of Cu tubes, thickness of its wall is 0.5 mm being equal three times of δ=0.167 mm (double skin penetration depth),
   - water cooling with 20 W of cooling power,
   - length of leads,
   - ferrite core outside of windings (ring: D_O=9.5 D_I=5.4, H=5 mm; Philips Ferroxcube 3F3).
   - Fotograph of the experimental transformer is in Fig. 3 (it consists of six such elementary transformers as in Fig. 1).
2. Operating frequency 1MHz (above 4 MHz the maximum efficiency of transformer decreases, because of large power losses in magnetic core).
3. Supplying from sinusoidal voltage source.
4. Analysis based on Ansys 2D and 3D models.

III. Idea of Linear Transformer

Idea of linear transformer is depicted in Fig. 1. Windings are made of copper coaxial pipes. There is an electrical insulation in between the primary and the secondary (e.g. PTFE-polytetrafluoroethylene). The transformer has one-to-one turn ratio. Cross-section of the transformer is shown in Fig. 2.

IV. Ansys Model

The ANSYS software (FEM) is used to computational analysis of power loses in the leads and interconnections.

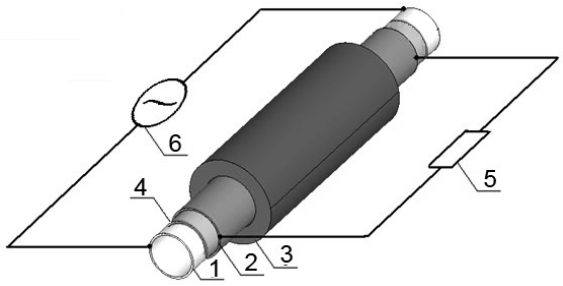

Fig. 1. Idea of linear transformer (elementary): 1-primary winding; 2-secondary winding; 3-ferrite core; 4-insulation; 5-load; 6-voltage supply.

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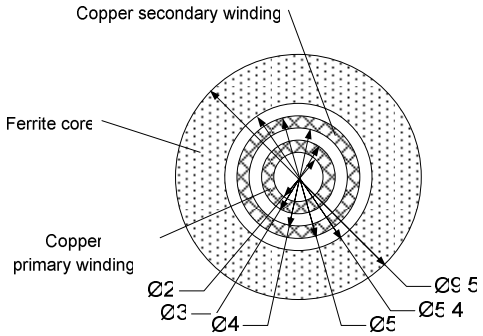

Fig. 2. Cross-section of linear transformer depicted in Fig. 1 and analyzed in this paper.

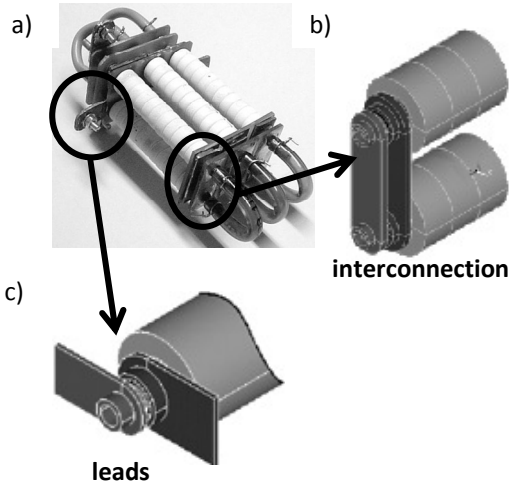

Fig. 3. (a) photograph of the experimental transformer 3:2; (b) ANSYS model of interconnection; (c) ANSYS model of leads.

A. *Planar 2D Model*

Planar 2D model was described in [1]. It was used for calculation of power losses and efficiency of the experimental transformer.

B. *3D Model*

The power losses in leads were calculated using a short (50 mm) 3D model of elementary transformer at the currents 0 to 160 A. (Fig. 4). 3D model reflects the influence of windings on current distribution in leads. The influence of the leads on power losses in windings can be neglected above 40 mm of the length of the transformers. (Fig. 6 – 3D vs. 2D/3D). Distance between ferrite core and the secondary lead is 1 mm. The same is between primary and secondary leads. The thickness of the lead is 0.5 mm. Interconnections have the same dimension.

The power losses in interconnection were calculated using 3D models (Fig. 5) that embraces 3 ferrite rings, of each elementary transformer and interconnection between primary and secondary windings of two elementary transformers.

C. *Hybrid 2D/3D Model*

The 50 mm of length of elementary transformer was introduced to limit the demand for system memory. The 3D

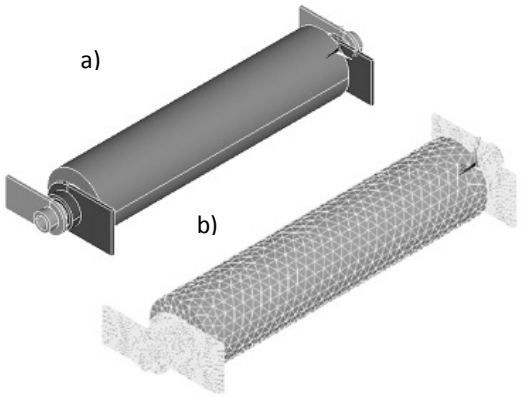

Fig. 4. (a) volumes of elementary transformer of 50 mm of length; (b) mesh volumes.

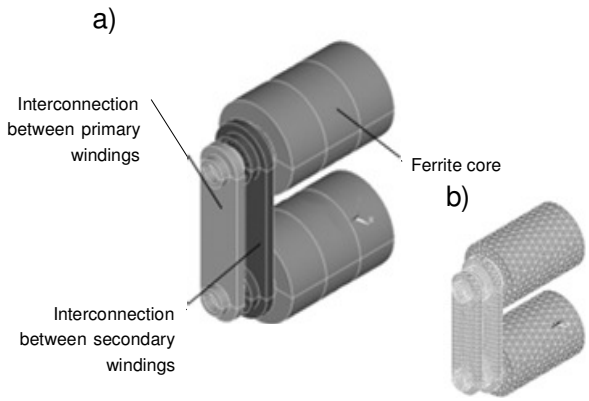

Fig. 5. Model of interconnection between two elementary transformer: (a) volumes; (b) mesh volumes.

model of elementary transformer consists of about 350 thousand elements and 60 thousand nodes. This model consumes the almost whole system memory available on 32-bit platform, and single calculation last 17 hours on a T7500 core2duo processor at 2.2 GHz. It was insufficient to calculate of power losses in interconnections and leads together with losses in windings for transformer longer than 50 mm using the 3D model. Therefore hybrid 2D/3D model was used instead of 3D one.

In the hybrid 2D/3D method the power losses in leads and interconnections were calculated using 3D models (Figs. 4 and 5). The power losses in core and windings are taken from 2D models.

The difference of power losses obtained with 2D/3D and 3D models is lower than 0.05% (Table I/4). This small difference can be observed in efficiency (Fig. 6).

V. Power Losses in Leads and Interconnections

Power losses in leads and interconnections are not exact square function of total current. It was observed making 3D calculation, and it is so because of irregular distribution of current density (Figs. 7 and 8a).

There, one can see regions with curved surfaces. For example in Figs. 7 and 8a current density is about 43 A/mm^2 while in the middle of elementary winding is only 15 A/mm^2

TABLE I
LOSSES OBTAINED WITH DIFFERENT MODELS

No	Dim.	Variant of transformer	ΔP	Why?
1	2D	Elementary 50 mm of length without leads	ΔP_1	In order to compare 2D, 3D and 2D/3D
2	3D	Elementary 50 mm of length with leads	ΔP_2	
3	2D/3D	Elementary 50 mm of length with leads	ΔP_3	ΔP_{leads} from 3D $\Delta P_{Cu} + \Delta P_{Fe}$ from 2D
4				$(\Delta P_3 - \Delta P_2)/ \Delta P2 \Rightarrow 0.05\%$
5	2D/3D	Transformer 3:2 with leads and interconnections	ΔP_4	ΔP_{leads} from 3D $\Delta P_{interconnections}$ from 3D $\Delta P_{Cu} + \Delta P_{Fe}$ from 2D (for given length)

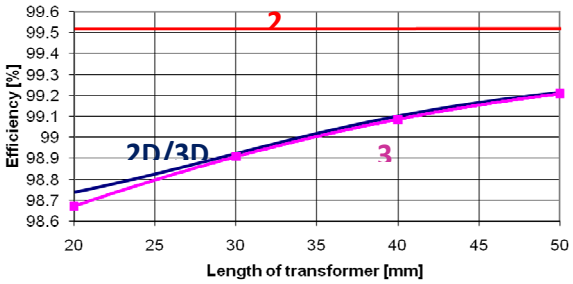

Fig. 6. Total efficiency of elementary transformer.

(Fig. 8b).

The thickness interconnection has an effect on its power losses. Because of irregularity of current density (Fig. 9). It is illustrated in Table II where power losses and maximum current density vs. thickness of interconnection at 100 kHz obtained with 3D model. The penetration depth at this frequency is 0.21 mm. Power losses in interconnection are least at thickness equal double skin penetration depth.

The power losses in leads occur due to skin effect (Fig. 10). The highest current density is observed at the edges. To have completed figures power losses in leads were calculated with 3D model. Power losses in pair of leads of primary winding is ΔP_{lp}=122 mW while in pair of leads of secondary winding is ΔP_{ls}=102 mW. That together is 4.5% of total power losses. Calculation were carry out for elementary transformer 50 mm at frequency f=100 kHz and current I_2=50 A.

TABLE II
POWER LOSSES AND MAXIMUM CURRENT DENSITY VS. THICKNESS OF INTERCONNECTION FOR 100 KHZ

Interconnection thickness D mm	Power losses ΔP mW		Maximum current density J_t A/mm	
	primary windings	secondary windings	Primary windings	secondary windings
1	127	80	43	38
0.42	125	78	44	38
0.25	200	116	116	62

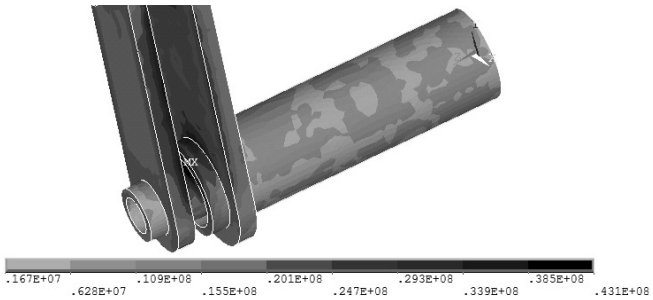

Fig. 7. Current density in interconnection.

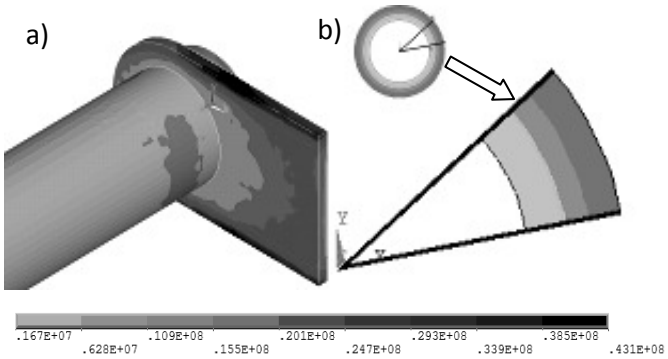

Fig. 8. (a) current density in the lead and primary winding – 3D model; (b) current density in the winding – 2D model in the middle of 50 mm elementary transformer.

VI. EFFICIENCY VS. LENGTH OF THE TRANSFORMER

Taking power losses in leads and interconnections into consideration one can determine overall efficiency of the primitive transformer (Fig. 11) as a function of the transformer length. This transformer consists of two elementary transformers. The transformer has 1:1 turn-to-turn ratio.

Efficiency vs. length (Fig. 11) of the transformer was calculated with hybrid 2D/3D model. It should be mentioned that it is maximal efficiency. That is calculated as function

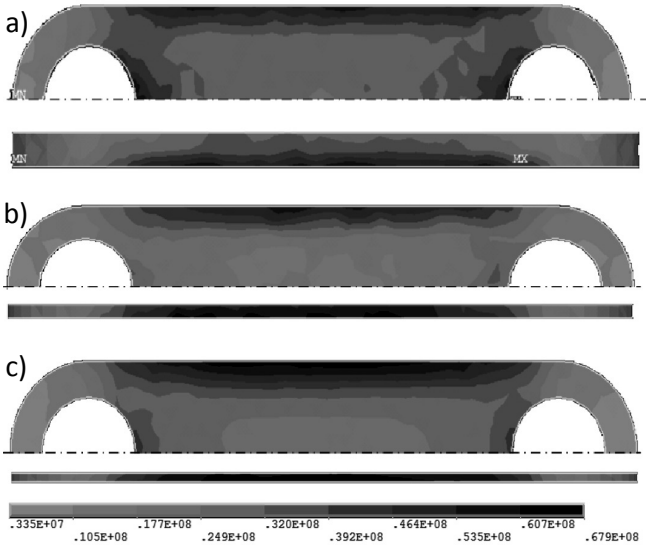

Fig. 9. Current density in interconnection in primitive transformer for thickness: (a) 1 mm; (b) 0.42 mm; (c) 0.1 mm (3D analysis).

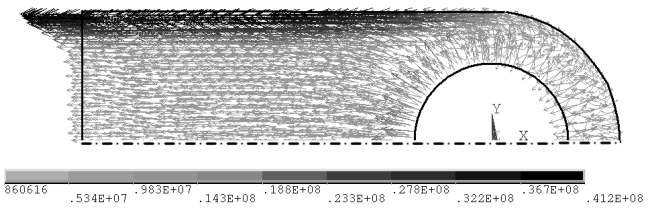

Fig. 10. Vector plot of current density in lead of primary winding of elementary transformer.

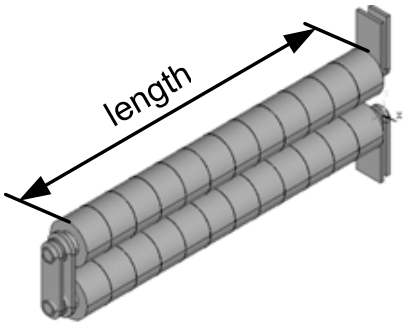

Fig. 11. Primitive transformer.

$\Delta P=f\{Z(B(U)),R,f\}$ that comes from circuit model of transformer. It could be observed that efficiency is near constant for the length higher than 300 mm.

VII. Results Comparison FEM vs. Measurements

The aim of this section is to compare efficiency of the experimental transformer (see section II and Fig. 3a) obtained from 2D, 2D/3D and experiment that is given in Fig. 14. The first step is the calculation of overall losses in leads and interconnections. Using this data the efficiency vs. output power is calculated in the second step.

The overall power losses in leads and interconnections vs. primary current of experimental transformer was calculated and depicted in Fig. 13. It has been done for experimental transformer for which losses of 4 leads and 12 interconnections were summed together.

Taking power losses in leads and interconnection into consideration one can make better model of experimental transformer. The result is depicted in Fig. 14.

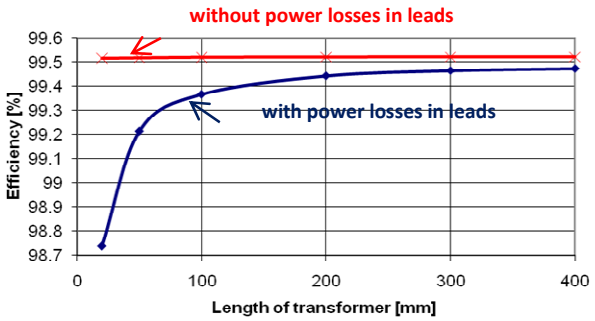

Fig. 12. Efficiency of the primitive transformer (operating at f=1 MHz and I_2~50 A).

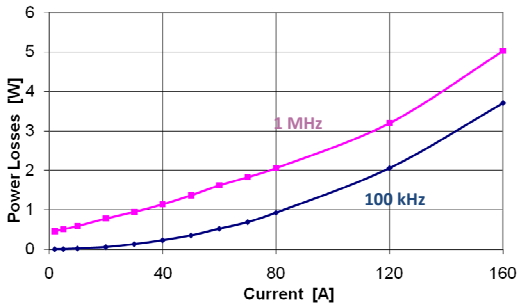

Fig. 13. Overall power losses in leads and interconnections (for input voltage of $100V_{max}$) of experimental transformer (4 leads, 12 interconnections).

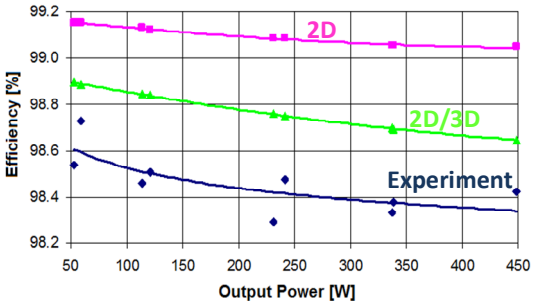

Fig. 14. Efficiency of experimental transformer.

The output power of the analyzed transformer is 2.6 kW at the efficiency ~99% at the assumption of total cooling power is 20 W.

The difference between efficiency of 2D and 2D/3D can be explained by losses in leads and interconnection. The discrepancy between efficiency of 2D/3D and experiment [1] comes from e.g. power losses in ferrite core taken for temperature that is different in comparison with temperature in experiment. The inaccuracy of calorimeter gives lower efficiency, which is the second explanation for the discrepancy.

VIII. Interconnections

Calculation of power losses in experimental transformer has to be carried out using information about arrangement of interconnections. In order to explain it the further analysis is confined to experimental transformer. The scheme of it is given in Fig. 15. Where two types of n-module is indicated, 1:2 and 1:1. The idea of n-module is given in Fig. 16, where primitive transformers are connected in series by primary windings and in parallel secondary ones.

Using primitive transformers it is possible to build transformer of near any turn-to-turn ratio [1].

It is justified to fabricated interconnection using PCB. Interconnections together with leads are depicted in Fig. 17. It is seen that 12 interconnections and 4 leads is needed for

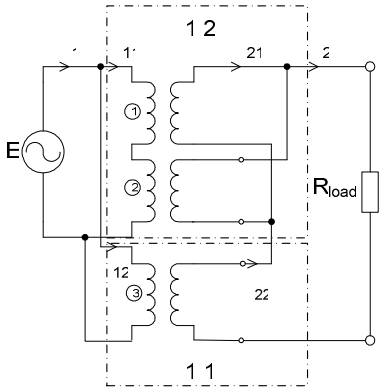

Fig. 15. Scheme of experimental transformer.

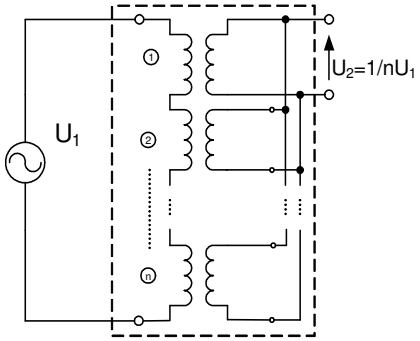

Fig. 16. n-module.

assembly elementary transformer to get complete experimental transformer.

Primary windings are connected exclusively with each other. The same is with the secondary windings. The two double-sided PCBs are needed, No 1 and No 2. The former is for primary leads. The inner side of PCBs connects secondary windings, while its external side connects primary ones.

IX. Conclusions

1. Power losses in leads and interconnections are about 5 % of total losses in linear transformer for the transformer of 50 mm of length; the higher length the higher efficiency is obtained.
2. The analysis evidenced that hybrid 2D/3D is acceptable for calculation of losses and efficiency.
3. Power losses in interconnections and leads are least at its thickness equal double skin penetration depth.
4. ANSYS software proves to be suitable tool for power electronics where energy efficient converters are needed.
5. The hybrid 2D/3D model allows having fine mesh.
6. Continuation of this work is aimed at optimization of the leads and interconnections and for technology of fabrication of the transformer.

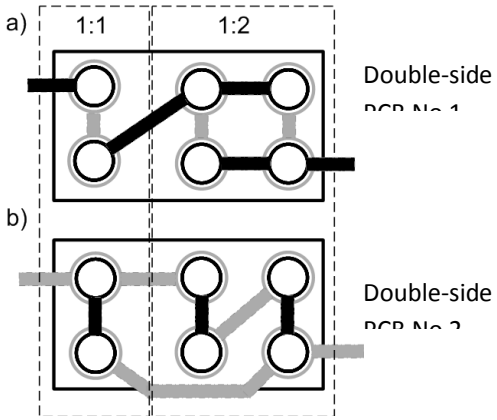

Fig. 17. Method of connection the n-modules: (a) front side; (b) back side.

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High-Performance Control of Doubly-Fed Reluctance Machines

Milutin Jovanović and Hamza Chaal

***Abstract*—The Brushless Doubly Fed Reluctance Machine (BDFRM) is a promising cost-effective alternative solution in applications with narrow speed ranges such as large wind turbines and/or pump-type drives. Apart from providing a comprehensive literature review and analysis of vector (field-oriented) control and direct torque (and flux) control (DTC) methods, the development, and results of experimental verification, of an angular velocity observer-based DTC scheme for sensorless speed operation of the BDFRM which, unlike most of the other DTC concepts, can perform well down to zero supply frequency of the inverter-fed winding, have also been presented in the paper.**

***Index Terms*—Control, brushless doubly fed reluctance machines, slip power recovery systems, wind turbines.**

I. Introduction

ALTHOUGH the inverter-fed brushless doubly fed reluctance machine (BDFRM) has not found any industrial use yet, it is an attractive low cost candidate for variable speed applications due to the high reliability and lower harmonic injection into the mains. The economic benefits [1] come from its slip power recovery property which allows the use of a smaller inverter (relative to the machine rating), and especially if the speed range required is limited (e.g. in large wind turbines or pumps [2, 3]). The BDFRM has two standard, sinusoidally distributed stator windings of different applied frequencies and pole numbers - the primary (or power) winding is with direct on-line supply and the secondary (or control) winding is also grid-connected but through a bi-directional (back-to-back) converter. In order to provide rotor position dependent magnetic coupling between the windings and torque production from the machine [4, 5], the reluctance rotor must have half the total number of stator poles. Such an unusual operating principle [6] implies the modest torque per volume of the BDFRM compared to an equivalent synchronous reluctance or induction machine [7]. The BDFRM shares all the advantages of doubly-fed machines over singly excited cousins – the operational mode flexibility, the greater control freedom, and the wider speed ranges i.e. the possibility of subsynchronous and super-synchronous operation in both motoring and generating regimes [7]. It can work as a conventional induction machine (which is an important "fail-safe" measure in case of the inverter failure) or as a fixed/adjustable speed synchronous turbo-machine [8]. One important BDFRM merit is that one can not only control torque, but also the power factor [3, 9–11], efficiency [2] or any other performance parameter of interest in an inherently decoupled fashion [12].

The absence of brush gear brings a clear advantage to the BDFRM over a conventional doubly-excited wound rotor induction machine (DEWRIM) in applications where increased reliability and lower maintenance are crucial factors (for example, off-shore wind generators). Furthermore, the BDFRM is more efficient [13] and easier to control than the closely related, brushless doubly-fed induction machine (BDFIM) having the same stator as the BDFRM but with a special cage rotor [14–17]. Recent FEA studies have shown that with higher rotor saliency-ratios, the BDFRM overall performance can be improved [7] to a level competitive with the induction machine [18]. The primary intention of this paper is to review control methodologies reported in the BDFRM literature. By integrating the existing knowledge, this survey may serve as a useful up-to-date reference for future research on this machine. Algorithms for scalar control, direct torque (and flux) control (DTC) and field-oriented control have already been proposed and evaluated by simulations [2, 19] and experimentally [12, 20]. However, these approaches all rely on using an encoder for rotor position and/or speed detection. Eliminating a shaft position sensor would not only reduce the system cost but, more importantly, would further enhance its reliability. The theoretical considerations in [21] and [22] have concerned with sensorless vector control and DTC, respectively. The simulation studies carried out in [11, 22] have been practically validated in [3, 10, 11]. This paper will reproduce the major outcomes of this experimental work.

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II. Dynamic Modeling

The space-vector equations for the BDFRM in a stationary reference frame using standard notation and motoring convention are [4, 6, 23]:

$$\underline{u}_{p_s} = R_p \underline{i}_{p_s} + \frac{d\underline{\lambda}_{p_s}}{dt} = R_p \underline{i}_{p_s} + \left.\frac{d\underline{\lambda}_{p_s}}{dt}\right|_{\theta_p \text{const}} + j\omega_s \underline{\lambda}_{p_s} \quad (1)$$

$$\underline{u}_{s_s} = R_s \underline{i}_{s_s} + \frac{d\underline{\lambda}_{s_s}}{dt} = R_s \underline{i}_{s_s} + \left.\frac{d\underline{\lambda}_{s_s}}{dt}\right|_{\theta_s \text{const}} + j\omega_s \underline{\lambda}_{s_s} \quad (2)$$

$$\underline{\lambda}_{p_s} = L_p \underline{i}_{p_s} + L_{ps} \underline{i}^*_{s_s} e^{j\theta_r} \quad (3)$$

$$\underline{\lambda}_{s_s} = L_s \underline{i}_{s_s} + L_{ps} \underline{i}^*_{p_s} e^{j\theta_r} . \quad (4)$$

The subscripts 'p' and 's' denote the primary and secondary winding quantities respectively, and '*' represents the complex conjugate. By omitting the exponential terms in (3)-(4), one obtains the rotating frame equivalents of (1)-(4) in a primary flux oriented form (λ_{pq}= 0):

$$\underline{u}_p = R_p \underline{i}_p + \frac{d\lambda_p}{dt} + j\omega_p \lambda_p \quad (5)$$

$$\underline{u}_s = R_s \underline{i}_s + \frac{d\underline{\lambda}_s}{dt} + j\omega_s \underline{\lambda}_s \quad (6)$$

$$\lambda_p = L_p \underline{i}_p + L_{ps} \underline{i}^*_s \quad (7)$$

$$\underline{\lambda}_s = L_s \underline{i}_s + L_{ps} \underline{i}^*_p = \sigma L_s \underline{i}_s + \underbrace{\frac{L_{ps}}{L_p}\lambda_p}_{\lambda_{ps}} \quad (8)$$

where $\sigma = 1 - L_{ps}^2/(L_pL_s) = 1 - k_{ps}^2$ is the leakage factor (defined as with the induction machine), $k_{ps} = L_{ps}=\sqrt{L_pL_s}$ is the coupling coefficient between the windings (as in the power transformer case), $L_{p;s;ps}$ are the respective 3-phase inductances [4, 7], and λ_{ps} is the primary flux linking the secondary winding (Fig. 1).

Applying the fundamental BDFRM theory [4, 6, 23], the following condition for the machine torque production can be established:

$$\omega_r = p_r\omega_{rm} = \omega_p + \omega_s \Leftrightarrow \theta_r = p_r\theta_{rm} = \theta_p + \theta_s \quad (9)$$

where $\omega_{rm} = d\theta_{rm}/dt$ is the rotor mechanical angular velocity (rad/s), p_r is the number of rotor poles, $\omega_{p,s} = d\theta_{p,s}/dt$ *are* the applied angular frequencies (rad/s) to the windings, and $\theta_{r,p,s}$ are the angular positions of the ro-tating reference frames as illustrated in Fig. 1 (the rotor frame is omitted for convenience). Notice that $\omega_s > 0$ for 'super-synchronous' *($\omega_{rm} > \omega_{syn}$)* and $\omega_s < 0$ for 'subsynchronous' *($\omega_{rm} < \omega_{syn}$)* machine operation where $\omega_{syn}= \omega_p/p_r$ occurs with the DC secondary winding i.e. when $\omega_s=0$. The 'negative' secondary frequency at sub-synchronous speeds simply means the opposite phase sequence of the secondary to the primary winding.

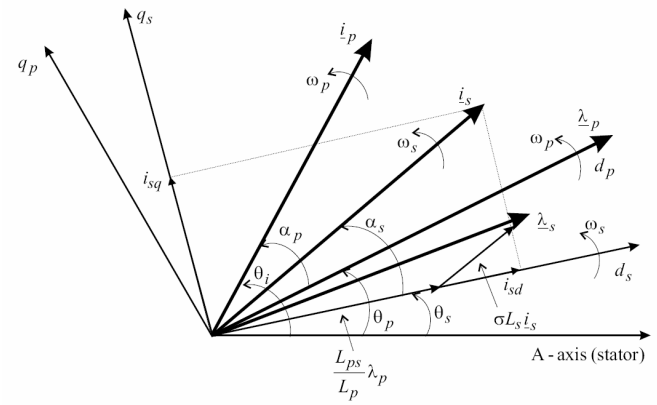

Fig. 1. Reference frames and characteristic phasors.

III. Vector Control

The secondary real power, torque and primary reactive power in a primary flux oriented form are [4]:

$$P_s = \frac{\omega_s}{\omega_p + \omega_s} P_{out} = \frac{\omega_s}{\omega_p} P_p \quad (10)$$

$$T_e = \frac{P_{out}}{\omega_{rm}} = \frac{3}{2} p_r \frac{L_{ps}}{L_p} \lambda_p i_{sq} \quad (11)$$

$$Q_p = \frac{3}{2}\frac{\omega_p \lambda_p}{L_p}(\lambda_p - L_{ps} i_{sd}) . \quad (12)$$

As can be seen from (11) and (12), Te is controlled by the secondary q-axis current, i_{sq}, and Q_p by the secondary d-axis current, i_{sd}, and there is no coupling between the two expressions (since λ_p is virtually constant). Note that the machine slip power recovery property is hidden in (10). For example, if the secondary is at the line frequency (i.e. $\omega_s = \omega_p$), the inverter has to handle half the output power (plus losses). However, if $\omega_s = 0.25\omega_p$, then the secondary contribution to the machine power production is only 20%. Therefore, in applications where the BDFRM would operate in a narrow range around the synchronous speed, a partially-rated inverter could do.

The structure of a typical BDFRM drive with vector control based on (11) and (12) is shown in Fig. 2 [12]. Considering that only the secondary winding quantities are controllable, one should first identify the secondary frame position (θ_s) using (9). The rotor position, θ_{rm}, is usually detected by a shaft sensor while the primary flux angle (Fig. 1), θ_p, follows from:

$$\underline{\lambda}_{p_s} = \lambda_p e^{j\theta_p} = \int (\underline{u}_{p_s} - R_p \underline{i}_{p_s}) dt \approx \int \underline{u}_{p_s} dt \quad (13)$$

where $\underline{u}_{ps}$ and $\underline{i}_{ps}$ can be easily determined from phase measurements. Once θ_s is known one can implement current control of the secondary d_sq_s components (and thus T_e and Q_p) in a traditional manner (Fig. 2) to optimise the desired performance parameter of the machine such as [2]: (1) the maximum torque per secondary (inverter) ampere (i.e. $i_{sd} = 0$) [7, 9]; (2) the maximum primary power factor (i.e. $i_{sd} = \lambda_p/L_{ps}$ for $Q_p = 0$) [9, 12]; (3) the unity line power factor or the minimum copper losses [9]; (4) the maximum power point tracking (MPPT) of a wind turbine [2] etc.

IV. Direct Torque Control (DTC)

The traditional DTC concept, originally developed for cage induction machines [24, 25], by virtue of its versatility and fewer machine parameter dependence, has been successfully used for stator frame control of almost all brushless machines. However, until very recently, its application to doubly-fed machines (DFMs) in general has been little reported in the literature. An alternative rotor frame based DTC technique for the BDFIM required a shaft position sensor for torque control,

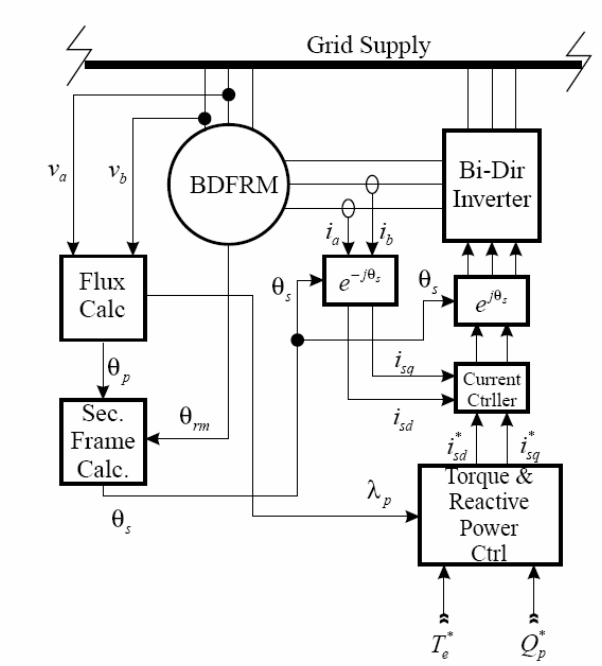

Fig. 2. A simplified block diagram of the field-oriented torque controller for the BDFRM.

and it was very complex even for DSP implementation [26]. The DTC schemes presented in [27–29] for a conventional doubly-fed induction generator (DFIG), on the other hand, have only been studied by computer simulations. In the last couple of years, predictive DTC strategies of constant switching frequency have been proposed and experimentally verified for the DEWRIM but used an encoder for control purposes [30–32]. Except for the recent practical work on the BDFRM control [10, 11], the only other test validation of sensorless DTC for DFMs has appeared in [33]. While a viable, parameter-independent algorithm for unity power factor control of the DFIG has been developed, the sustained synchronous speed operation of the machine has not been clearly demonstrated.

It is well-known that back-emf based control approaches, including DTC, have low frequency stability problems due to the flux estimation inaccuracies caused by resistance variations at lower supply voltages. It is mainly for this reason that this control method has been extremely popular for high-speed applications where the resistance effects are less pronounced. In this respect, the traditional DTC is not suitable for BDFRM applications. Fortunately, these common DTC difficulties at low secondary frequencies can be overcome in the BDFRM.

A. Main Principles

One of the key questions of the DTC of the BDFRM, as for any other machine, is how to control the secondary flux to achieve the desired torque dynamics. An answer can be found in (8) and a DTC form of (11):

$$\underline{\lambda}_s = \lambda_{sd} + j\lambda_{sq} = \sigma L_s i_{sd} + \lambda_{ps} + j\sigma L_s i_{sq} \tag{14}$$

$$T_e = \frac{3p_r}{2\sigma L_s}\left|\underline{\lambda}_{ps} \times \underline{\lambda}_s\right| = \frac{3p_r}{2\sigma L_s}\underbrace{\frac{L_{ps}}{L_p}\lambda_p}_{\lambda_{ps}}\lambda_s \sin\delta\,. \tag{15}$$

It is evident from (14) and (11) that λ_{sq} is a torque producing secondary flux component since it is directly proportional to i_{sq}. Therefore, in order to increase (decrease) instantaneous torque for a given λ_s, one needs to apply appropriate voltage vectors to the secondary winding to allow the secondary flux angle in the $d_s q_s$ frame (Fig. 1), i.e. δ in (15), to increase (decrease). This effectively means that the respective stationary frame angle, $\delta + \theta_s$, would also change accordingly as θ_s variations are negligible (and especially at low ω_s values) over a short control interval dictated by the inherently high sampling rates. There is obviously no need to know the secondary frame position, and the DTC can be implemented in a stator frame as usual for this method.

The outputs of the flux and torque comparators in the DTC algorithm (Fig. 3) can be defined as:

$$\Delta\lambda_s = \begin{cases} 1, & \lambda_s^* - \lambda_s \geq \Delta\lambda \\ 0, & \lambda_s^* - \lambda_s \leq -\Delta\lambda \end{cases} \tag{16}$$

$$\Delta T_e = \begin{cases} 1, & T_e^* - T_e \geq \Delta T \\ -1, & T_e^* - T_e \leq -\Delta T \end{cases} \tag{17}$$

where ΔT and $\Delta\lambda$ indicate a half width of the corresponding hysteresis bands. The voltage vectors generated by the inverter to achieve the desired control action for a particular sectorial location of the secondary flux vector are given in Table I. The

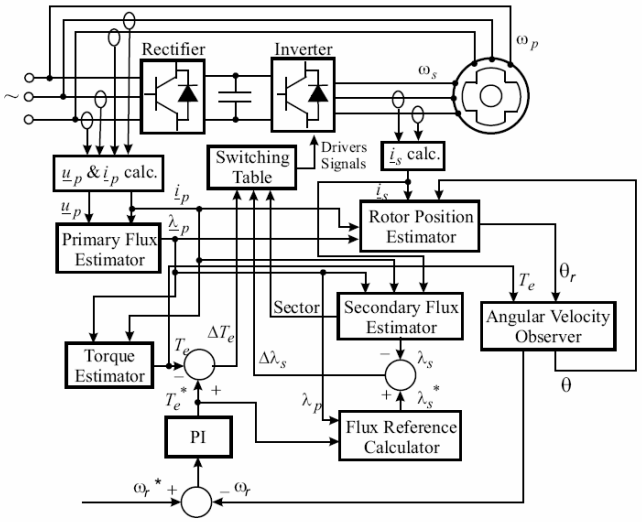

Fig. 3. Sensorless BDFRM drive with DTC.

TABLE I
INVERTER SWITCHING LOOK-UP TABLE

Comparator		Secondary Flux Sector					
$\Delta\lambda_S$	ΔT_e	1	2	3	4	5	6
1	1	U_2	U_3	U_4	U_5	U_6	U_1
1	-1	U_6	U_1	U_2	U_3	U_4	U_5
0	1	U_3	U_4	U_5	U_6	U_1	U_2
0	-1	U_5	U_6	U_1	U_2	U_3	U_4

respective magnitudes and angular positions in a stationary frame can be expressed as follows:

$$\underline{U}_k = \frac{2}{3} V_{dc} e^{j(k-1)\frac{\pi}{3}} \quad k = 1, 2, ..., 6 \tag{18}$$

where V_{dc} is the measured DC link voltage and $[(2k - 3)\pi/6; (2k-1)\pi/6]$ are the angular boundaries of the k-th sector associated with $\underline{U}_k$. The binary codes, indicating the switching status of individual inverter legs of these vectors are: $\underline{U}_1$ = 100, $\underline{U}_2$ = 110, $\underline{U}_3$ = 010, $\underline{U}_4$ = 011, $\underline{U}_5$ = 001, and $\underline{U}_6$ = 101.

The controller's main task is to ensure that the secondary flux and machine torque are kept within the userspecified hysteresis bands. In the flux case, according to (16), the λ_s values should be in the range $[\lambda_s^* - \Delta\lambda \, , \, \lambda_s^* + \Delta\lambda]$ with $\Delta\lambda_s = 1$ voltage vectors increasing, and $\Delta\lambda_s = 0$ vectors decreasing the λ_s magnitudes (Table I). Similarly in (17), $\Delta T_e = 1$ means the increase, and $\Delta T_e = -1$ the decrease of actual (not absolute) torque which is assumed positive if acting counter-clockwise as in Fig. 1. Note that the influence of zero voltage vectors ($\underline{U}_0$ = 000 and $\underline{U}_7$ = 111) on torque behavior is speed dependent (refer to [19, 22] for further details). For this reason, the switching strategy adopted is based on using the active voltage vectors only and knowledge of the machine speed for torque control is not required (Fig. 3).

B. Parameter Estimation

As discussed earlier, the use of (2) for estimating the secondary flux magnitude and stationary frame angle is not convenient in the low frequency region. However, as both the primary and secondary quantities are measurable, the following alternative expression can be derived using (1), (3) and (4):

$$\underline{\lambda}_{s_s} = L_s \underline{i}_{s_s} + \underline{i}_{p_s}^* \frac{\underline{\lambda}_{p_s} - L_p \underline{i}_{p_s}}{\underline{i}_{s_s}^*} \tag{19}$$

where λ_{ps} is given by (13). The magnitudes and angular positions of $\underline{i}_{s_s}$ and $\underline{i}_{p_s}$ can be calculated from measurements [19, 20, 22]. Applying (19) one would obviously avoid the voltage integration but at the expense of having to know the winding self inductances $L_{p;s}$.

Another significant benefit of greater control freedom, afforded by the accessibility of both BDFRM windings, is the possibility of sensorless speed control [22]. The rotor angle, θ_r, can be retrieved from (3) as follows:

$$\left.\begin{aligned} \theta_{r_1} &= \tan^{-1} \frac{\mathrm{Im}[(\underline{\lambda}_p - L_p \underline{i}_p)\underline{i}_s]}{\mathrm{Re}[(\underline{\lambda}_p - L_p \underline{i}_p)\underline{i}_s]} \\ \theta_{r_2} &= \theta_{r_1} + \pi \end{aligned}\right\} \tag{20}$$

The raw position estimates are then input to a Luenberger type PI observer to predict the rotor angular velocity $\omega_r = d\theta/dt$ for the speed control (Fig. 3).

The torque expression best suited for the BDFRM control is of the form:

$$T_e = \frac{3}{2} p_r \left| \underline{\lambda}_{p_s} \times \underline{i}_{p_s} \right| = \frac{3}{2} p_r (\lambda_{pd} i_{pq} - \lambda_{pq} i_{pd}) \tag{21}$$

where the subscripts '*pd*' and '*pq*' indicate the respective stator frame components (Fig. 1) of $\underline{\lambda}_{ps}$ and $\underline{i}_{ps}$. High estimation accuracy has been achieved in practice as (21) is nearly machine parameter independent (except for indirect R_p effects through λ_p estimates) and relies on the primary 'ripple-free' quantities of fixed line frequency.

V. Experimental Results

The sensorless control algorithm in Fig. 3 was executed in dSPACE® at 10 kHz on a small BDFRM prototype [19, 20]. The preliminary tests were conducted for the unloaded machine to assess the controller viability.

The plots in Fig. 4 represent the rotor angles (θ_r) obtained from (20), and their absolute variations from encoder measurements. A shaft position sensor was used for monitoring purposes only and is not shown in Fig. 3. The raw estimates, θ_r; are notably noisy, the error spikes being occasionally larger than 30º. Despite this, the average estimation error is reasonably low (≈ 7º).

The excellent low-pass filtering abilities of the observer are evident from Fig. 5. The average estimation error is reduced to approximately 1.5º with the maximum values being up to about 3.4º. Such accuracy improvement can be attributed to the high quality estimates being fed into the observer by the position estimator (Fig. 3). The observer last prediction, θ, has served as a reference while selecting the best raw estimate available per speed control interval i.e. the one having the least absolute deviation from θ. Therefore, the estimator block itself carries out the first filtering of noisy θ_r before inputting the best estimate to the observer for further processing. The filtered θ_r values are plotted out in Fig. 4.

Fig. 6 shows the machine response to a varying speed reference values between 950 rpm, 750 rpm and 550 rpm. The speed limits correspond to $fs \approx 13.3$ Hz in either super- or sub-synchronous mode. It can be seen that the machine can be

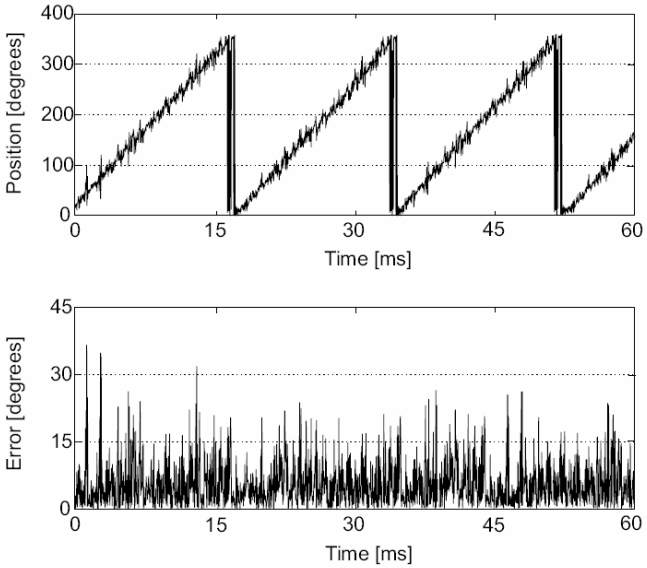

Fig. 4. Estimated position and estimator absolute errors at 850 rpm (f_S = 6.7 Hz).

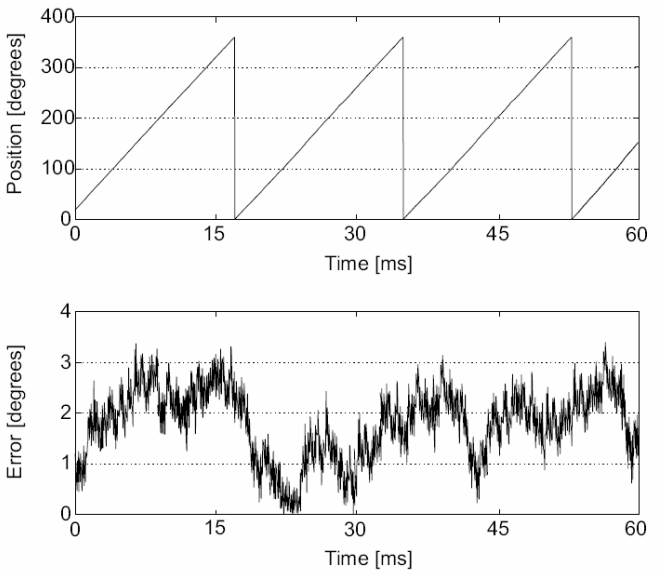

Fig. 5. Observed position and observer errors corresponding to Fig. 4.

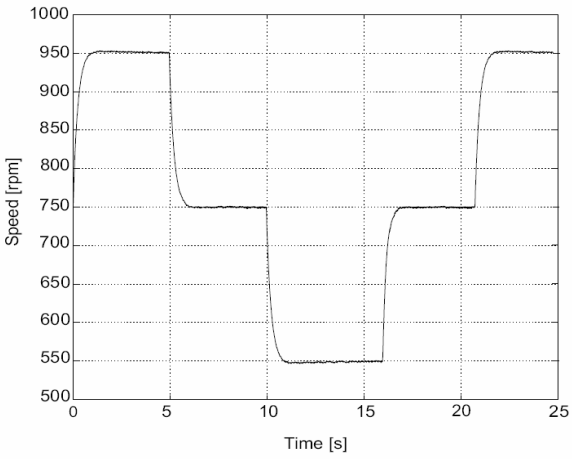

Fig. 6. Sensorless control performance down to synchronous speed.

effectively controlled over the considered speed range down to synchronous speed (750 rpm) when f_s = 0. The reliable low frequency operation of the BDFRM is an important merit of the proposed sensorless scheme, and represents a significant advantage over traditional DTC and other back-emf based control methods having difficulties (or simply not working) in this frequency region even in sensor speed mode.

VI. CONCLUSIONS

The fundamental principles and implementation aspects of different control techniques for the BDFRM have been surveyed in this paper. This kind of unified study can be extremely helpful for control development and research on this interesting and unusual slip-power recovery machine. A similar control related framework for the BDFRM or any other doubly fed machine has not been published in the refereed literature to date.

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A Modified Sensorless Control of Induction Motor Based on Reactive Power

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***Abstract*—This paper presents a modified model reference adaptive system (MRAS) speed estimator for induction motors (IM), based on the instantaneous rotor magnetizing reactive power. The proposed estimator does not use integration in the reference model and it is insensitive to the stator resistance variations. The introduced changes allow analytical tuning of the adaptation mechanism and facilitate implementation of the estimator in a digital signal processor (DSP). The robustness and accuracy of the proposed scheme were verified experimentally for a wide speed range and variable level of rotor flux.**

***Index Terms*—Induction motor drives, model reference adaptive systems, observers, control.**

I. Introduction

MRAS observers consist of a reference model, an adjustable model and an adaptation mechanism, which adapts the speed estimate based on the error between the two model outputs. The classical rotor flux-based MRAS speed estimation [1] is popular because of its simplicity. The main disadvantages of this estimator are poor low-speed operation due to the existence of pure integrators (which introduces problems of initial conditions, offset, drift and integrator saturation), and sensitivity to the variations in stator resistance. The problem of pure integration can be overcome either by replacing integrators with low-pass filters (quasi-integrators) or by using advanced integration methods. Other solutions have employed rotor back electromotive force (EMF)-based MRAS estimators [2, 3], which improve low-speed performance, but suffer from noise in the back-EMF estimate at high speeds and sensitivity to the stator resistance variations. In [4] a parallel stator resistance and rotor speed identification algorithm has been proposed. Additional answers to the problems of integration and sensitivity to the stator resistance have employed MRAS observers based on the rotor magnetizing reactive power [5, 6]. However, the majority of rotor flux, back-EMF and reactive power-based MRAS techniques suffer from inherent instability in the low-speed regenerative mode, unreliable operation at zero frequency with full-rated toque and sensitivity to the rotor time constant variations. The scheme in [7] employs rotor flux and stator current estimators with a modified slip relation and an additional stator voltage-dependent term as a remedy to low-speed instability. The usage of dot products of rotor flux and stator current [8] or rotor flux and back-EMF [9] as additional adaptation terms in the MRAS error signals and parallel stator resistance estimation has resulted in stable low-speed operation. Initially, MRAS observers had a proportional-integral (PI) regulator as the adaptation mechanism, and first tuning methods were empirical with the regulator gains constrained only by the noise in the system. The first reported analytical tuning [10] suited only certain operating modes and lacked universality. Improved MRAS dynamics and clearly defined analytical tuning of the observer, augmented with a full machine mechanical model, are given in [11] with proportional-integral-differential regulator as an adaptation mechanism. Several references combined good properties of MRAS observer for speed estimation and Luenberger observer for flux-current estimation [12, 13], or MRAS and sliding mode observers [14] that yielded improved dynamics of the estimate. Some authors propose the usage of fuzzy-logic controllers in place of the adaptation mechanism [15], or multi-layer artificial-neural-networks combined with the MRAS reference model [16], where the adaptation mechanism is inside the adjustable model. Although very complex, these solutions reported robust and accurate results. This paper contributes to the improvement of the reactive power-based MRAS speed observer, by identifying an analytical method to define parameters of the adaptation mechanism, resulting in a stable first-order system.

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II. Mathematical Model

An IM in a stationary reference frame can be modeled using complex stator and rotor voltage and flux linkage equations:

$$\begin{aligned} \underline{v}_s &= R_s \underline{i}_s + \dot{\underline{\psi}}_s \\ 0 &= R_r \underline{i}_r + \dot{\underline{\psi}}_r - j\omega_r \underline{\psi}_r \end{aligned} \tag{1}$$

$$\begin{aligned} \underline{\psi}_s &= L_s \underline{i}_s + L_m \underline{i}_r \\ \underline{\psi}_r &= L_m \underline{i}_s + L_r \underline{i}_r \end{aligned} \tag{2}$$

The voltage, current and flux space vectors from previous equations are given as

$$\underline{x} = x_\alpha + jx_\beta \ , \ x \in \{v_s, i_s, i_r, \psi_s, \psi_r\} \tag{3}$$

The IM mechanical subsystem is modeled with

$$J_m \dot{\omega}_{mr} = T_e - T_l - B\omega_{mr} \tag{4}$$

where ω_{mr} is the rotor mechanical angular frequency.

The rotor magnetizing back-EMF $\underline{e}_m$ and current $\underline{i}_m$ vectors are defined as:

$$\underline{e}_m = L_m \underline{\dot{\psi}}_r / L_r \tag{5}$$

$$\underline{i}_m = \underline{\psi}_r / L_m \tag{6}$$

The rotor back-EMF for the reference model is derived from (1), (2) and (5) as

$$\underline{e}_m^v = \underline{v}_s - R_s \underline{i}_s - \sigma L_s \underline{\dot{i}}_s \tag{7}$$

Similarly, the back-EMF for the adjustable model is obtained from (1), (2) and (6) as

$$\underline{e}_m^i = L_m' \underline{\dot{i}}_m = L_m' \left[\frac{1}{\tau_r} \underline{i}_s - \left(\frac{1}{\tau_r} - j\hat{\omega}_r \right) \underline{i}_m \right] \tag{8}$$

where $L_m' = L_m^2 / L_r$ is the equivalent magnetizing inductance and $\tau_r = L_r / R_r$. In the reference and adjustable models, the outputs are rotor magnetizing reactive powers (q_m^v, q_m^i) defined in (9) as the cross product of rotor back-EMF and stator current vector, which removes the integration and dependence on the stator resistance.

$$q_m^k = \vec{i}_s \otimes \vec{e}_m^k = \mathrm{Im}\left\{ \underline{i}_s^* \cdot \underline{e}_m^k \right\}, \quad k = v, i \tag{9}$$

The error $\varepsilon = q_m^v - q_m^i$ between the two models becomes the input to the adaptation mechanism, which gives the estimated $\hat{\omega}_r$ at its output. Fig. 1a depicts the structure of the proposed MRAS speed observer. The reference model output is averaged using a finite impulse response filter (FIR) which suppresses noise from the differentiation of stator currents in (7) and filters out the higher harmonic content. The adjustable model is divided into two sub-models that are described in the further text.

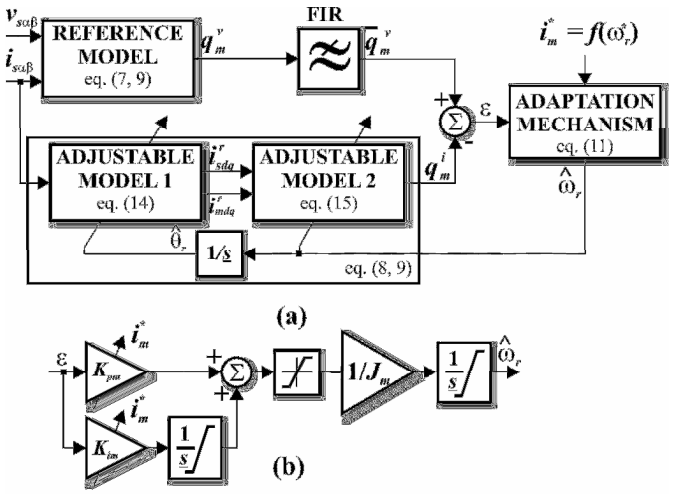

Fig. 1. (a) MRAS speed observer, (b) adaptation mechanism.

III. Adaptation Mechanism

In order to select an appropriate adaptation mechanism, a small-signal model of the MRAS observer has to be devised. Small-signal dynamics of the observer can be modeled by transforming (7)-(9) into a synchronous (d-q) reference frame and by linearizing them around the chosen steady-state point. The general assumptions are that: the synchronous angular frequency ω_e is constant, hence stationary angular slip frequencies are equal ($\omega_{sl0} = \hat{\omega}_{sl0}$); the rotor time constant τ_r is known exactly; the MRAS speed feedback results in equality of steady-state rotor magnetizing currents and zero q-axis component of rotor flux. In addition, all second-order small signals can be neglected. Following these assumptions, the transfer function of the open-loop MRAS observer describes dependence between the small-signal error and rotor speed error (I_{sq0} is a steady-state value of i_{sq}):

$$H_m(\underline{s}) = \frac{\Delta\varepsilon}{\Delta\omega_r - \Delta\hat{\omega}_r} = L_m' I_{mn}^2 \frac{\underline{s}^2 + \left(\frac{1}{\tau_r} + \tau_r \omega_{r0} \omega_{sl0} \right) \underline{s} + 2\omega_e \omega_{sl0}}{\underline{s}^2 + \frac{2}{\tau_r} \underline{s} + \frac{1}{\tau_r^2} + \omega_{sl0}^2} \tag{10}$$

Fig. 1b shows the proposed adaptation mechanism, which comprises a PI regulator (with proportional K_{pm} and integral K_{im} gains) and a simplified mechanical model with motor inertia J_m derived from (4) assuming that the friction and the load torque are neglected ($B \approx 0$, $T_l \approx 0$). The output of the PI regulator is considered proportional to T_e, thus the transfer function of the adaptation system is

$$H_a(\underline{s}) = \frac{K_{pm} \underline{s} + K_{im}}{J_m \underline{s}} \frac{p}{J_m \underline{s}} \tag{11}$$

Assuming $\omega_{sl0} = 0$, one can select parameters of the regulator by using (12), and applying cancellation of the dominant pole in the open-loop transfer function (10). Unlike solutions with PI regulators only, a mechanical model with J_m enables cancellation of a single zero in the open-loop transfer function that may exacerbate the noise at high frequencies and render the system unstable. The resulting transfer function of closed-loop speed observer (13) gives a stable system in the form of a first-order low-pass filter with a cut-off frequency $\omega_c = 2\pi f_c$.

$$K_{pm} = \frac{\omega_c J_m}{p L_m' I_{mn}^2} \approx \frac{\omega_c J_m}{p L_m' i_m^{*2}}, \quad K_{im} = K_{pm} / \tau_r \tag{12}$$

$$H(\underline{s}) = \frac{\Delta\hat{\omega}_r}{\Delta\omega_r} = \frac{H_m(\underline{s}) H_a(\underline{s})}{1 + H_m(\underline{s}) H_a(\underline{s})} = \frac{\omega_c}{\underline{s} + \omega_c} \tag{13}$$

The frequency f_c is selected to be 2–10 Hz. In order to generalize the regulator gains K_{pm} and K_{im} over a wide speed range and to maintain the desired bandwidth, the regulator employs gain scheduling such that I_{mn} in (12) is replaced with the reference magnetizing current as a function of the

reference rotor speed, i.e. $i_m^* = f(\omega_r^*)$. The τ_r in (12) is set to its rated value τ_{rn}.

IV. Experimental Results

The proposed speed-observer was verified by using an experimental setup consisting of 2 kW DC machine (posing as an active load), IM and 1.2 kW inverter, which are controlled using an indirect field oriented control topology, as shown in Fig. 2. The IM parameters were – rated power P_n = 750 W, rated voltage V_n = 195 V_{rms}, rated frequency f_n = 70 Hz, star connected stator, p = 1, R_s = 3.03 Ω, R_r = 1.89 Ω, L_s = L_r = 184 mH, L_m = 172 mH, σL_s = 21.91 mH, and $J_m = 3.53\times10^{-4}$ kgm^2.

The IM was driven by a 3-phase current-controlled voltage source inverter, which operated at 10 kHz switching frequency (the frequency was randomized ± 10% around this value) and used space vector pulse-width modulation (SVPWM) with a rated DC link voltage of 340 V. All control and estimation algorithms were implemented in a Texas Instrument DSP TMS320F2810 operating at 125 MHz. The current regulators were implemented in a synchronous reference frame and updated at the PWM rate. The bandwidth of the current loop was set to 250 Hz and incorporated decoupling terms updated at 1 kHz. The motor voltages were estimated using the DC link voltage samples and the PWM duty cycles with dead-time and IGBT voltage drops compensation. The flux and slip frequency estimators along with the flux regulator were running at 1 kHz, with the flux loop bandwidth set to 90 Hz. The speed loop was running at a 1ms sample rate with the bandwidth of 10 Hz. The IM speed was monitored via an incremental encoder. The reference model of the MRAS observer was updated at the PWM rate. The adjustable model 1 was running at the PWM rate and estimated the rotor magnetizing current in a rotor reference frame according to (14), which made the model independent of $\hat{\omega}_r$ and provided the additional filtering through integration.

$$\underline{i}_m^r = \frac{1}{\hat{\tau}_r}(\underline{i}_s^r - \underline{i}_m^r) \tag{14}$$

The rotor magnetizing $\underline{i}_m^r$ and stator currents vectors $\underline{i}_s^r$ were obtained from $\underline{i}_m$ and $\underline{i}_s$ in a stationary reference frame, through rotational transformations using $\hat{\theta}_r$. The adjustable model 2, was running at a 1ms rate and gave the rotor reactive power as

$$q_m^i = L_m'\left[\hat{\omega}_r\left(i_{md}^r i_{sd}^r + i_{mq}^r i_{sq}^r\right) + \frac{1}{\tau_r}\left(i_{md}^r i_{sq}^r - i_{mq}^r i_{sd}^r\right)\right] \tag{15}$$

The adaptation mechanism was running every 1ms with its output integrated every PWM interval in order to obtain the estimated rotor position $\hat{\theta}_r$. Since the MRAS estimator behaved as a low-pass filter, it was necessary to compensate for the introduced phase lag. If the slip frequency is neglected, the estimated rotor position is

$$\hat{\theta}_r = \int \hat{\omega}_r dt + \tan^{-1}(\hat{\omega}_r / \omega_c) \tag{16}$$

The IM magnetizing curve was experimentally determined and feed-forward compensation of saturation effects [17] was applied. The transient stator inductance σL_s is considered constant and any error in this value may become dominant at high frequencies. The proposed speed observer was tested for the entire speed region. Fig. 3 illustrates the waveforms of the rotor reactive powers, d and q-axis stator currents; measured and estimated rotor speeds with the IM running in the base speed region, for a reference speed of 540 rpm at the rated load of 1 Nm. The power q_m^v has a significant amount of high-frequency noise that originates from the differentiation of stator currents. The stator d-axis current i_{sd} is kept at the rated value, which corresponds to the rated i_m current, whilst $\hat{\omega}_r$ tracks the actual rotor speed with minimal latency and zero steady-state error. Fig. 4 depicts the waveforms of reactive powers, i_{sd} and i_{sq} currents and rotor speeds for the IM operating in the field-weakening region, once it reached the reference speed of 6300 rpm at 0.5 Nm load torque. The reference reactive power drops faster than the i_{sd} current and the harmonic content in the reactive power estimates becomes significantly higher. The estimate $\hat{\omega}_r$ accurately matches the real speed, with a marginal steady-state error. Fig. 5 shows the relevant waveforms for low-speed operation at 60 rpm and 1 Nm load. The average $\hat{\omega}_r$ matches the actual speed after 400 ms, with a significant ripple in the instantaneous value. The minimal achieved rotor frequency using the proposed estimator is 0.25 Hz at rated load, whilst the maximum speed is 210 Hz.

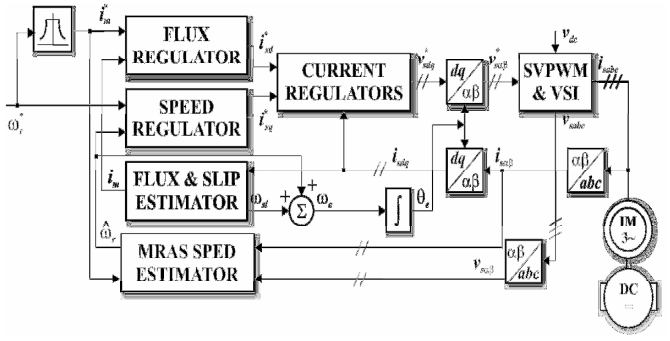

Fig. 2. Experimental setup.

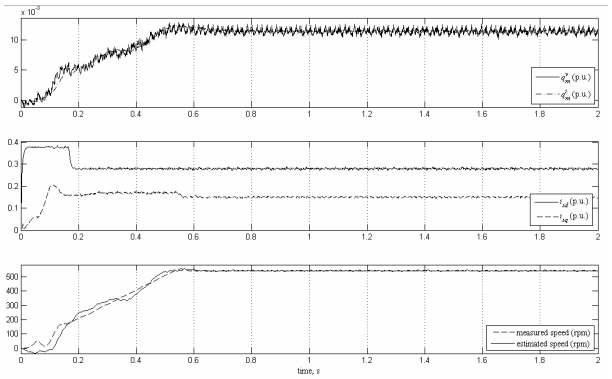

Fig. 3. Waveforms for the base speed region.

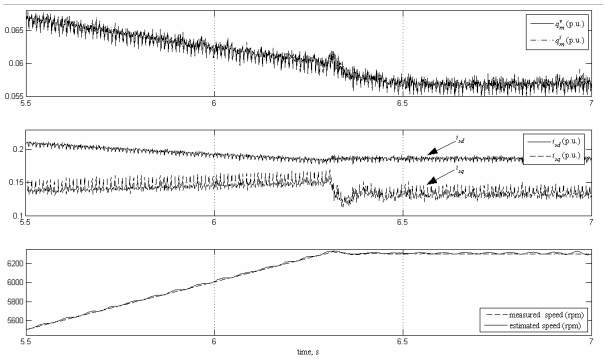

Fig. 4. Waveforms for the field-weakening region.

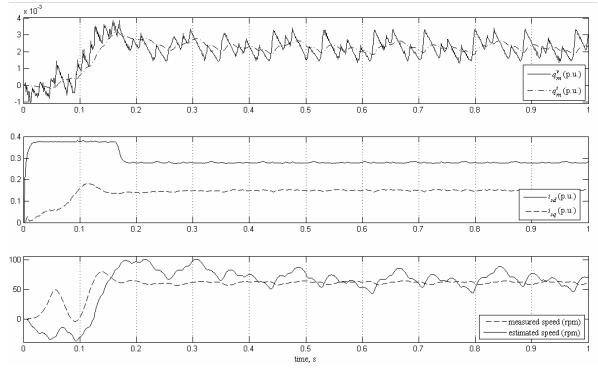

Fig. 5. Waveforms for 1 Hz reference frequency.

V. Conclusion

This paper describes a modified speed-sensorless control of an IM based on rotor reactive power. The proposed technique does not require integrators in the reference model; it is robust to the stator resistance variations, and operates reliably over a wide speed range. The observer is augmented with a simple mechanical model of the IM that helps to construct a more effective speed adaptation mechanism and enables its analytical tuning. The proposed scheme was verified experimentally and the overall system exhibited robustness and satisfactory accuracy over a wide speed range.

Appendix

v_s, e_m – stator voltage and rotor back-EMF
i_s, i_r, i_m – stator, rotor and rotor magnetizing current
ψ_s, ψ_r – stator and rotor flux
R_s, R_r – stator and rotor resistance
L_s, L_r, L_m – stator, rotor and magnetizing inductance
τ_r – rotor time constant
σ – total leakage coefficient, $\sigma = 1 - L_m^2/(L_s L_r)$
ω_r, $\hat{\omega}_r$ – actual and estimated rotor electrical angular frequency
ω_{sl}, $\hat{\omega}_{sl}$ – actual and estimated slip angular frequency
$\hat{\theta}_r$ – estimated rotor electrical position
T_e, T_l – electromagnetic and load torque
J_m, B – motor inertia and friction coefficient
p – number of pole pairs
v, i – reference and adjustable model values (super script)
0 – stationary values (subscript)
Δ – small-signal variations
α, β – stationary reference frame (subscript)
d, q – synchronous reference frame (subscript)
r – rotor reference frame (superscript)
$\dot{x}$ – first derivative (dx/dt)
$\underline{s}$ – complex angular frequency ($j\omega$)

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A Test Procedure for Determining Models of LV Equipment

Vladimir Ćuk, Joseph F. G. Cobben, Wil L. Kling, Roelof B. Timens, and Frank B. J. Leferink

***Abstract*—An automated test technique for determining parameters of low voltage equipment is presented in the paper. The aim of this research is to obtain simple models of household, office and industrial equipment which could be used to predict power quality problems during the design of low voltage installations and networks. For that purpose, several types of equipment were tested in the PQ laboratory and in this phase of the research, the emphasis is on inrush currents and interaction between voltage and currents during voltage changes (magnitude and harmonic content changes).**

***Index Terms*—Power quality, modeling, measurement, harmonics, inrush current.**

I. Introduction

LIMITATIONS for the supply voltage concerning power quality phenomena are described in the standard EN 50160 and national grid codes. These standards are applicable for normal operating conditions. On the other hand, the IEC 61000 series of standards give some guidance for determining immunity requirements for devices and large installations, but not in all situations because of some simplifying assumptions, such as idealized test conditions.

Abnormal network situations can be modeled and simulated with high accuracy in software such as Matlab, Digisilent Power Factory, Alternative Transients Program and other packages. These programs require a lot of experience and details about the models, which sometimes makes them inconvenient to use during the design of the installation.

This was the reason to start working on a tool which could give assistance for installation/network design, and prevent most of the possible power quality problems. To keep the tool user friendly, the tool should not need too many details about all of the future components.

This is one of the tasks of the recently started IOP project: Power Quality and EMC which involves Eindhoven University of Technology and University of Twente. One of the starting points of this project is model development. Models should be physically based as much as possible, but some of the model parameters should be avoided in order to achieve greater simplicity during the installation design.

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Model simplifications can be obtained through experiments, as described in the following sections, and statistical analysis of the results. This cannot be achieved for all types of equipment, but it still offers a convenient way of modeling a large number of equipment. For example, different types of office equipment, which can come in a large number, it is unnecessary to model all equipment with too much detail. The models could also include some widespread immunity limits, and therefore pinpoint some of the possible problematic locations in the installation.

II. Experimental Setup

The experimental setup for this automated procedure is schematically shown in Fig. 1.

The voltage source used in these experiments is the California Instruments MX 45, a 3 phase source with maximal apparent power of 45 kVA, maximal voltage of 300 V (phase to ground), and programmable up to the 50th harmonic. It is programmed from the PC (in Matlab) via RS232 connection, as suggested by [1] and [2].

Loads are connected to the voltage source by compliance impedances suggested by the IEC725 standard which is equal to (0.40+j·0.25) Ω for phase and neutral in total. Loads can be connected separately or in parallel, in one or three phases.

Signals are measured with a Tiepie Engineering HS3 oscilloscope, with 2 channels and resolution of 16 bits. At the moment, this is enough for one phase connection, but it can be expanded for three phase measurement in the future. The

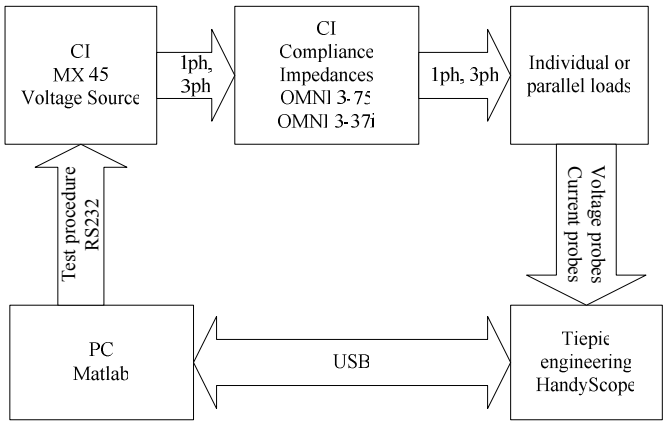

Fig. 1. Schematic diagram of the laboratory setup.

oscilloscope is connected to the PC by a USB connection, and is also controlled from Matlab.

III. Software and Experiments

The software is completely developed in Matlab, Release 2008b. It is capable to produce input voltage waveforms and record voltage and current signals at the load connection. The structure of software execution is briefly described in Fig. 2.

Multiple tests can be created by this way, and the laboratory setup can complete them autonomously and store all of the results on the PC for post processing.

First of the tests conducted is the inrush current test. It is described in the next section. Also, interaction of voltages and currents during the presence of harmonic disturbances was measured and analyzed, as an expansion of the harmonic fingerprints, described in [3] and [4].

IV. The Inrush Current Test

Inrush currents of devices can cause several power quality problems. Fast voltage variations are caused by inrushes, and their impact sometimes has to be limited [5]. This is especially the case if the installation is powered by an uninterruptible power supply. In that case, equipment selection is influenced by inrush conditions even more [6].

If the equipment is working in a regime which requires constant turning on and off, inrush currents can cause flickering effect in the nearby lighting.

In some cases, inrush currents can cause unwanted tripping (unwanted protection reactions) [7]. For this reason it is important to know the inrush characteristic before protection is selected and set.

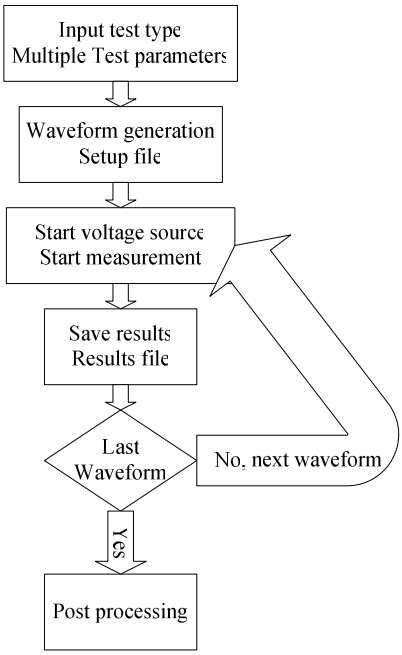

Fig. 2. Simplified execution diagram of the software.

The inrush current test consists of a series of equipment starts at different voltage phase angles, and measurements of voltage and current. For every voltage phase angle a number of repetitions can be set, in order to check the validity of results by comparing them with other results for the same starting phase.

The phase range of 360° can be divided in any number of intervals. In the results presented here, the range was divided in 24 intervals, giving a phase step of 15°. For every phase angle 3 repetitions were chosen, and deviations from the average value were calculated for all characteristics.

The test was conducted on an air inductor of 50 mH with active resistance of 3.2 Ω, and on a vacuum cleaner with electronic speed control. The speed reference of the vacuum cleaner was set to roughly one half of the maximal speed.

One measured sample of the starting voltage waveform is given in Fig. 3, with the starting phase set to 90°.

A sample of the measured inrush current waveform for the 50 mH inductor is given in Fig. 4. The starting voltage phase was set to 90°.

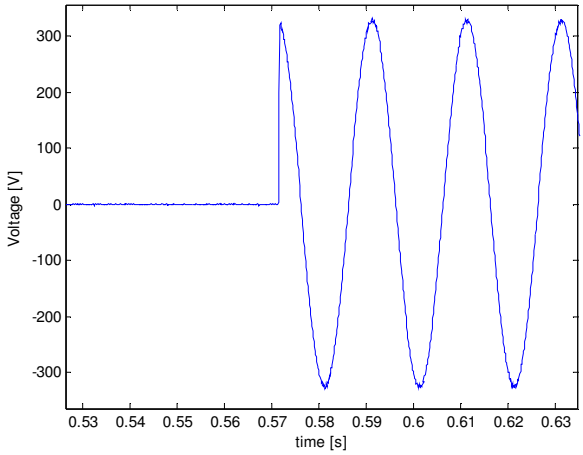

Fig. 3. Sample of the measured starting voltage.

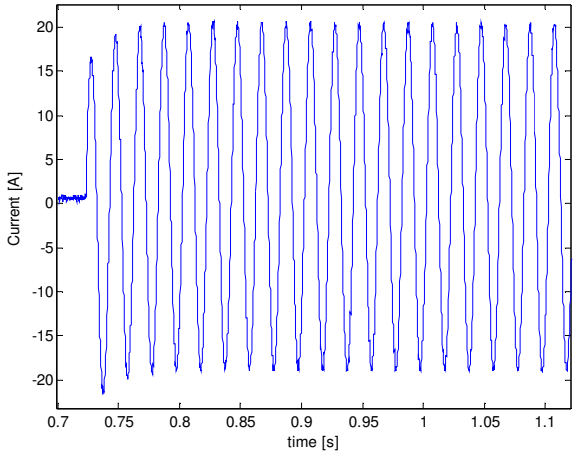

Fig. 4. Inrush current sample – 50 mH inductor.

A sample of the measured inrush current waveform for the vacuum cleaner is given in Fig. 5. The starting voltage phase was set to 90°.

The dependence of the inductors maximal inrush current (peak of the waveform) from the starting voltage phase is presented in Fig. 6. Maximal current values from Fig. 6 are average values from repetitions of that phase angle. Maximal deviations of repetitions from those average values are given in Fig. 7. It can be seen on Fig. 7 that these deviations are relatively small, as a consequence of accurate source phase triggering.

The dependence of the maximal value of the inductors DC current component from the starting voltage phase is given in Fig. 8. By comparing Fig. 6 and Fig. 8 it can be seen that the maximum of the inrush current depends mostly on its DC component, which in turn is largely dependent on voltage starting phase as an initial condition (as it was expected for an inductor).

In the case of the vacuum cleaner with electronic speed control, these dependencies cannot be explained as easy as for the inductor. The reason for that is unknown topology of the converter used.

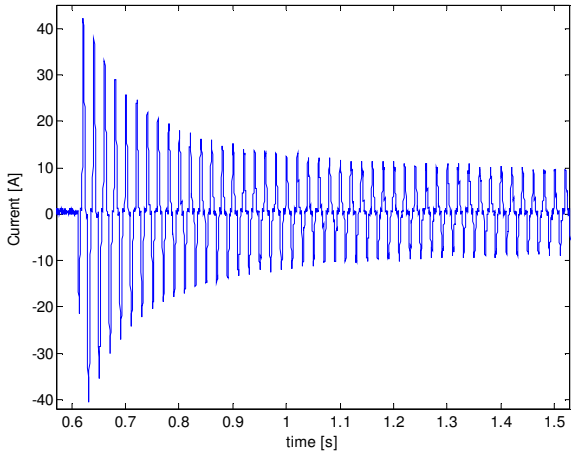

Fig. 5. Inrush current sample – vacuum cleaner.

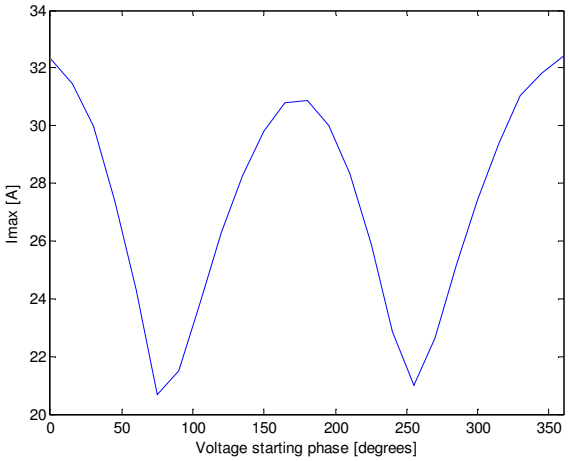

Fig. 6. Dependence of inductors maximal peak inrush current value from the voltage starting phase.

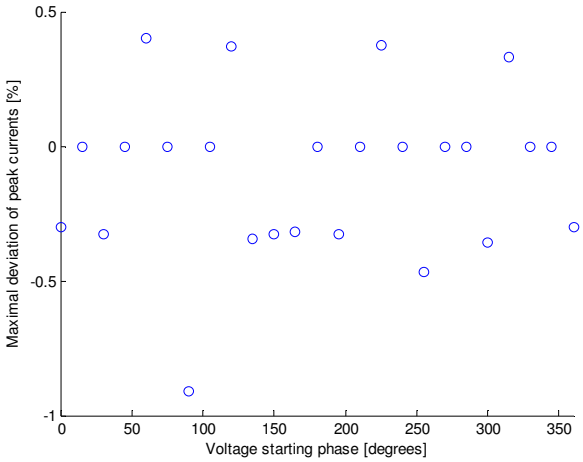

Fig. 7. Maximal deviations of inductors peak currents among repetitions.

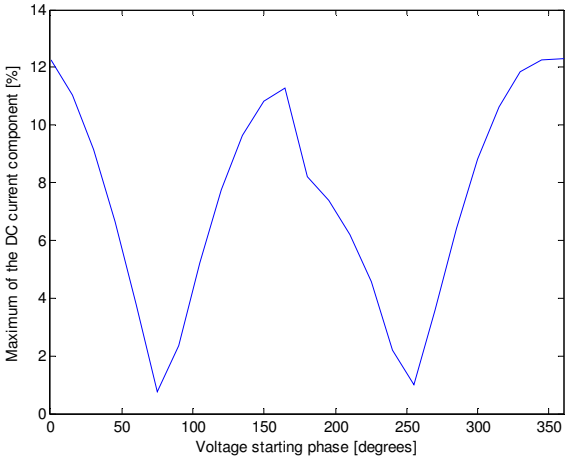

Fig. 8. Dependence of inductors maximal DC current component from the voltage starting phase.

The dependence of the vacuum cleaners maximal starting current from the starting voltage phase is given in Fig. 9. Maximal deviations of repetitions from the average values in Fig. 9 are presented in Fig. 10. It can be seen that the deviations are approximately two times bigger than in the case of the inductor. That can be explained by a higher sensitivity of the inrush current to voltage phase changes.

Random switching of devices gives an even value of probability for any voltage starting phase angle. By exploring the angle distribution of inrush characteristics it is possible to predict the inrush properties with a certain level of probability. Doing so, smaller rated values of other installation components (for example fuses) can be selected in some cases. This can be used to avoid extreme values which could be highly unlikely to appear, as suggested in [8] for a ferroresonant regulated rectifier.

From the inrush currents measured, some characteristic values were calculated as presented in Table I.

In Table I, following abbreviations are used: I_{max} is the

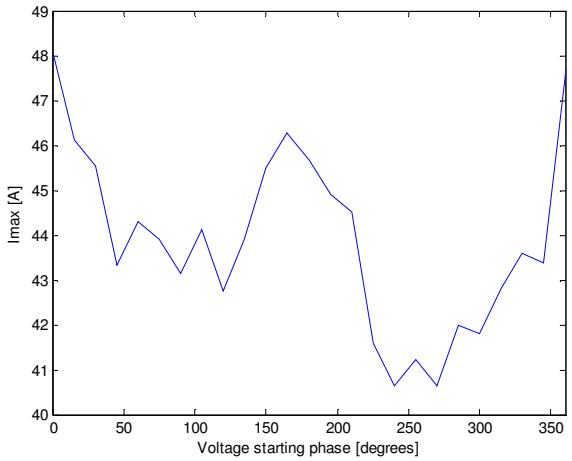

Fig. 9. Dependence of vacuum cleaners maximal inrush current from the voltage starting phase.

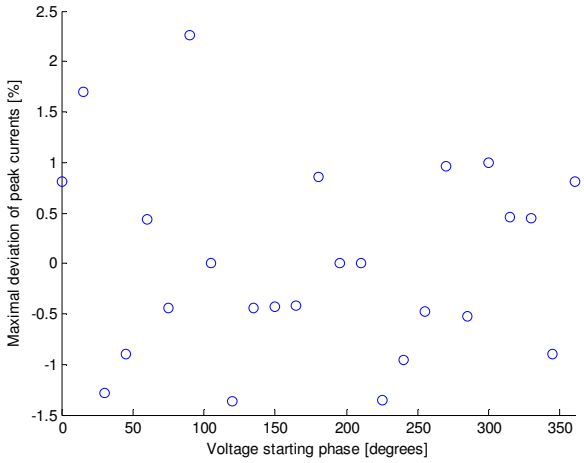

Fig. 10. Maximal deviations of vacuum cleaners peak currents among repetitions.

absolute maximal value of current for all measurements, $I_{max90\%}$ is the maximal value of current for 90% of the measurements, I_{DCmax} is the absolute maximal value of the DC current component, $I_{DCmax90\%}$ is the maximal DC current component value for 90% of the measurements, t_{inmax} is the maximal inrush duration for all measurements, and $t_{inmax90\%}$ is the maximal inrush duration for 90% of the measurements.

From Table I it can be seen that for these two devices 90% probability values are very close to absolute maximal values.

V. The Harmonic Fingerprint Test with Multiple Harmonics

Harmonic fingerprinting is a method which describes the interaction between the distorted supply voltage and the harmonic current of a device or a whole installation. The whole procedure and test results for several types of equipment are described in details in [3] and [4]. One application of this test procedure – tracing the levels of grid and installation impact on the overall current distortion is described in [9].

TABLE I
Characteristics Inrush Current Values

	50 mH Inductor	*Vacuum cleaner*
I_{max} *[A]*	*32.4*	*48.5*
$I_{max90\%}$ *[A]*	*31.8*	*46.3*
I_{DCmax} *[A]*	*12.3*	*5.59*
$I_{DCmax90\%}$ *[A]*	*12.2*	*4.31*
t_{inmax} *[s]*	*0.24*	*1.37*
$t_{inmax90\%}$ *[s]*	*0.22*	*1.20*

In short, the test procedure is done as follows. At first, the load tested is connected to an undistorted voltage. At that time, the loads current spectrum without background harmonic voltage is recorded. After that, harmonic voltages are added to the supply voltage with equidistant magnitude and phase steps, and voltages, currents, and their spectra's are recorded. With all of the measurements done, it is possible to make a load model for every harmonic frequency. Harmonic models consists of a harmonic current source (harmonic currents recorded with undistorted source voltage) in parallel with a harmonic impedance (calculated from the harmonic voltage and harmonic currents measured with and without voltage distortion).

For an approximately linear load, each harmonic impedance can have a single complex value. For loads with strong nonlinear behavior, impedances can be used as look up tables, with different impedance values for different harmonic voltage magnitudes and phase stands.

If a harmonic fingerprint is made for a single load, the results can be used to calculate harmonic currents of several parallel loads with one harmonic voltage applied. The currents calculated will match well with values measured for parallel loads, as reported in [3] and [4].

For the test presented here, model parameters were calculated for the 5th and 11th harmonic, and impedances were saved as look up tables. Voltage amplitude step was 2% of the nominal voltage, in the range from 2 to 10%. Voltage phase step used was 60°. The test was done on two devices, one with a liner behavior – a 25 W fan, and one with an extremely nonlinear behavior – an energy saving lamp.

Harmonic voltages applied for the calculation of the 5th harmonic impedances are presented in the complex plain in Fig. 11. Measured 5th harmonic currents for the fan and energy saving lamp used in complex plain are given in Fig. 12 and Fig. 13, respectively.

From Fig. 13 it can be seen that for the energy saving lamp there is a strong connection between the harmonic voltage phase and the resulting harmonic current, which justifies the usage of an impedance look up table instead of a linearized value. For the fan a single impedance value could be used, but for the sake of comparison again a look up table was used.

After the model calculation, a test was done with the 5th and the 11th harmonic voltage applied at the same time. The level of 11th harmonic was kept constant with a magnitude of 3% and phase stand of 120°, and the 5th harmonic was changed from 2 to 5% with magnitude steps of 1% and phase steps of 60°.

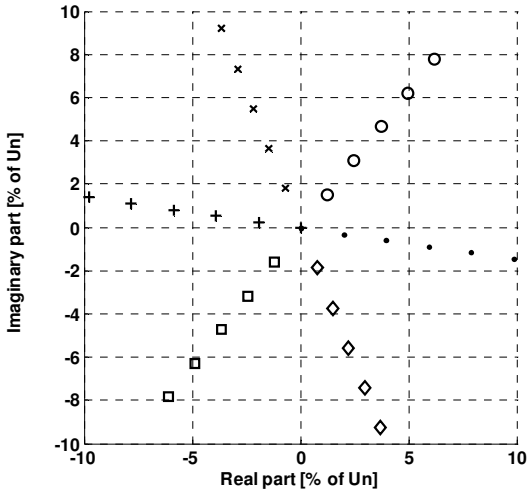

Fig. 11. Voltage values used in the test – 5th harmonic.

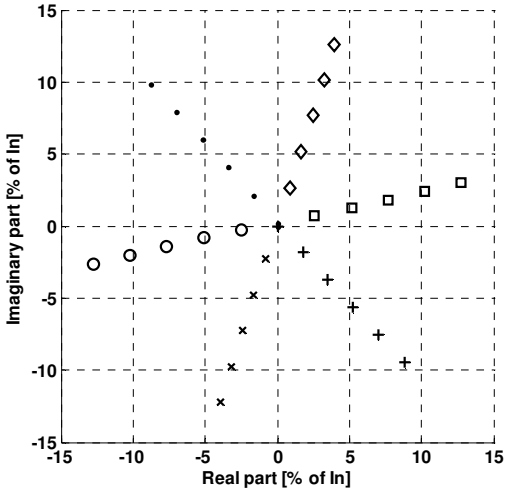

Fig. 12. Measured 5th harmonic current – fan.

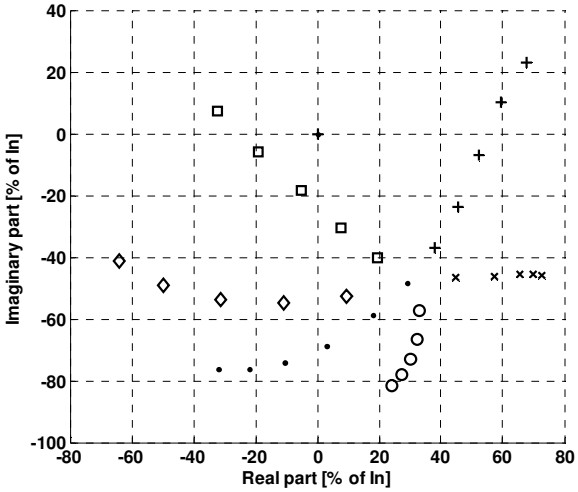

Fig. 13. Measured 5th harmonic current – ES lamp.

After the measurement, values of 5th and 11th harmonic currents were compared to the values calculated from the model obtained with single harmonic measurements. Relative calculation errors for the fan are given in Fig. 14, and for the energy saving lamp in Fig. 15.

From Fig. 14 and Fig. 15 it is obvious that the calculation is much more accurate for a mostly linear device. Also, it is noticeable that the accuracy of the calculation for the energy saving lamp is improving as the magnitude of the harmonic voltage increases (voltage magnitude is increasing with the number of measurement). One partial reason for that is the measurement accuracy for small values. Another, more important reason, is the effect of the constant harmonic in the background. For a nonlinear device, the existence of the 11th harmonic can cause a significant amount of the 5th harmonic by itself. In case of the fan, cross talk ratio for 11th harmonic (the ratio of the 11th current harmonic and the second biggest harmonic caused when only the 11th voltage harmonic is applied) is 50. In the case of the energy saving lamp, this ratio is only 1.1.

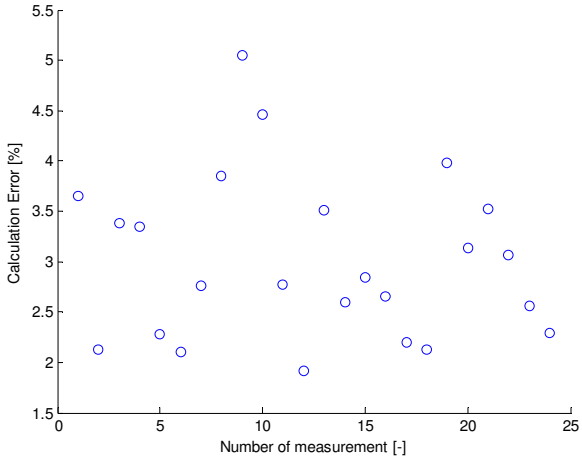

Fig. 14. Relative calculation error – fan, 5th harmonic.

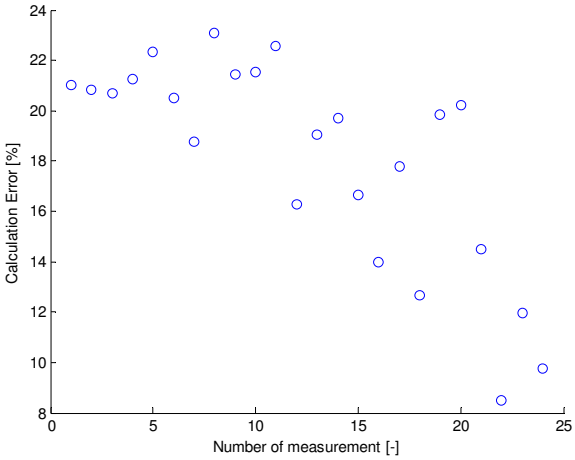

Fig. 15. Relative calculation error – ES lamp, 5th harmonic.

VI. CONCLUSIONS

Inrush characteristics of devices can be treated statistically to find the most probable values. However, in cases like the two analyzed, they can be very close to the maximal values possible.

Complete frequency decoupling in harmonic modeling gives good results when the elements are mostly linear or when the voltage distortion is mostly composed of one harmonic. With total nonlinearity and complex voltage distortions some level of frequency coupling is needed, and will be explored further.

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Attenuation of Nanocrystalline and Ferrite Common Mode Chokes for EMI Filters

Szymon Pasko, Boguslaw Grzesik, and Fabian Beck

***Abstract*—The attenuation of common mode chokes based on nanocrystalline VITROPERM 500F and Mn-Zn ferrite materials are analysed. It has been proved that the nanocrystaline choke gives much higher attenuation than ferrite one.**

***Index Terms*—EMI filter, common mode chocke.**

I. Introduction

NOWADAYS, electromagnetic compatibility is increasing-ly important issue. Most of electrical devices generate electromagnetic emissions that have negative influence on environment. Moreover, the most products to be sold have to comply with EMC directive [1], [2]. Electromagnetic interfere-ences are divided into radiated and conducted ones [3].

Two types of conducted interference can be distinguished. The first is termed as common mode (CM) interferences while the second one as differential mode (DM) interferences. The former are propagated in both phases having the same directions and coming back through ground.

The differential mode (DM) interferences are propagated in one phase in one direction and coming back via the second phase in opposite direction, the same like supplying current [3], [4].

Suppression of conducted interferences needs application of EMI filters. A one-stage structure of EMI filter is given in Fig. 1.

The CM interferences are suppressed by coupled coils L_0, and the capacitor C_{Y1}, C_{Y2}. The impedance of coupled coil is higher than impedance of capacitors C_{Y1}, C_{Y2} that's why the CM interferences flow by capacitor C_{Y1}, C_{Y2} and PE conductor (Fig. 2). The DM interferences flow by capacitor C_{X1} and C_{X2}, because the impedance of AC supply is higher than C_{X2} for high frequencies (it results from mismatch impedance conditions) [3].

The efficiency of EMI filter suppression is determined by its attenuation A_{dB} .

$$A_{dB} = 20\log\left(\frac{V_1}{V_2}\right) \tag{1}$$

where, V_1 is the voltage between terminal L, N without EMI filter, while V_2 is the voltage at the same terminal L, N with EMI filter (Fig. 2). It is given in dB [3].

The measurement method of attenuation characteristic of

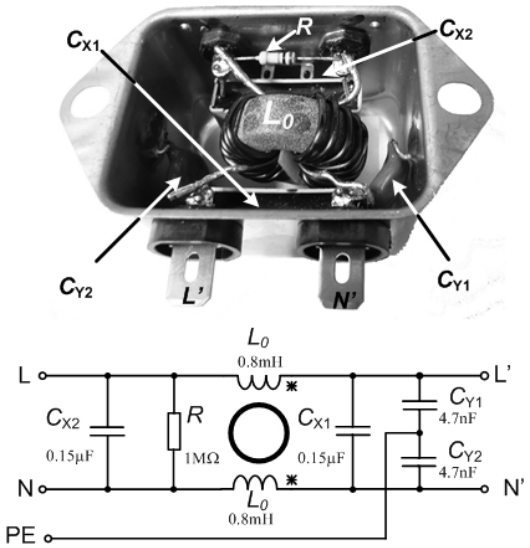

Fig. 1. The structure of one phase EMI filter.

EMI filter is described in standard [4]. According which the attenuation is measured in 50 Ω system, but it does not reflect real conditions with supply and load.

The common mode choke L_0 plays the main role in EMI filter attenuation although capacitors C_x, C_Y have decisive influence on the attenuation. That's why authors analyze only attenuation of common mode choke. What means that the analysis concerns only the attenuation of common mode interferences.

Although the analysis is based on the example chokes the results allows for generalization. Three example chokes are analyzed. Two have near the same dimensions where one is made of Mn-Zn ferrite while the second of nanocrystalline [5]. The third also made of nanocrystalline of higher permeability having smaller dimensions [5].

The attenuation of the choke is the function of the following parameters: i) value of inductance L_0 (permeability of ferromagnetic core) and its dependency on temperature, ii) geometry of the magnetic core and windings, iii) value of parasitic capacitances and iv) saturation of the magnetic flux density.

II. Examples of the Common Mode Chocke

The first choke is wound on toroidal ferrite core Mn-Zn (Fig. 3a). It has the following dimensions: outer diameter

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F. Beck is with Schaffner EMV AG, Luterbach, Switzerland (e-mail: Fabian.beck@schaffner.com).

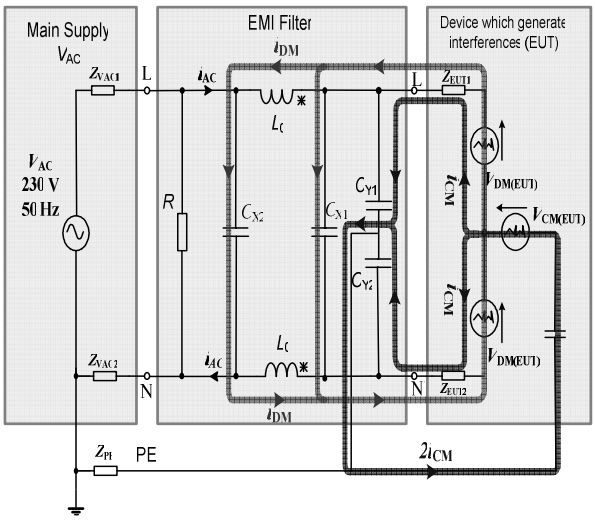

Fig. 2. Propagation of CM, DM interference in EMI filter.

D_o=20.35 mm, inner diameter D_{in}=8.85 mm, height h=7.5 mm. The initial permeability is 4 300 (Fig. 6). This choke will be called Mn-Zn in sequel.

The second choke based on nanocrystalline VITROPERM 500F core and is depicted in Fig. 3b. The dimensions of this core are: D_o=21.98 mm, D_{in}=11.67 mm, h=11.1 mm. The initial permeability is 15 000 (Fig. 6). This choke will be called VF15 in sequel.

The third choke is also based on nanocrystalline VITROPERM 500F (Fig. 3c). The dimensions of this core are: D_o=15.95 mm, D_{in}=11.93 mm, h=6.95 mm. The initial permeability is 45 000 (Fig.6). This choke will be called VF45 in sequel.

The windings are made of 1.13 mm in diameter Cu wire. The chokes Mn-Zn and VF15 have the similar geometry and the same number of turns – 13. The inductances, at 10 kHz, of the chokes are as follows: L_0=0.85 mH for Mn-Zn and L_0=4.14 mH for VF15. The choke VF45 has 10 turns and it inductance is L_0=2.3 mH.

The chokes are for nominal current of 10 A RMS.

III. Parameters Influence on Attenuation Properties

The properties of attenuation of the EMI filter depend on:

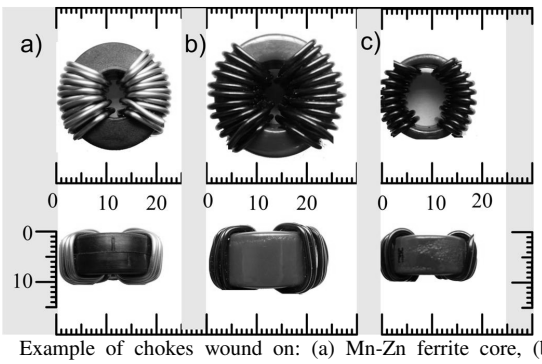

Fig. 3. Example of chokes wound on: (a) Mn-Zn ferrite core, (b) and (c) VITROPERM 500F cores.

inductance L_0, parasitic parameters of the choke and parasitic parameters of C_x, C_Y capacitors.

The inductance L_0 changes within the frequency. The higher inductance L_0 yields higher attenuation. The inductance, for given material, changes not only with frequency and permeability that in analyzed case also is frequency dependent. The inductance is described as:

$$L_0(f) = \frac{\mu_s' \mu_0 S N^2}{l_{avg}} \tag{2}$$

where,

μ'_s – real part of permeability,

μ_0 – magnetic constant $4\pi 10^{-7}$ H/m,

N – number of turns,

S – cross section of the torodial core,

l_{avg} – average length of core.

The core made by Mn-Zn is commonly used in EMI filters. The initial permeability of Mn-Zn core is small in comparison with initial permeability of nanocrystaline cores but exhibiting constant value for relatively broad range of frequency (Fig. 6). Although nanocrystaline materials offer higher initial permeability it changes significantly with frequency that is observed for VF45 (Fig. 6). The high permeability, of VF15, permits to achieve, for 10 kHz, the inductance 5 times higher than for Mn-Zn remembering that the geometry and number of turns are similar (Fig. 4).

The VF15 choke exhibits higher attenuation in the frequency range up to 10 MHz, that is suitable for attenuation of noise, generated by switching power supplies operating at e.g., 100 kHz.

Moreover, because of high permeability of VF15 the volume and weight of core, and number of turns is reduced. This reduction results in reduction of inductance L_0 and reduction of stray capacitances (Table I). The reduced stray capacitance of the winding yields to higher attenuation.

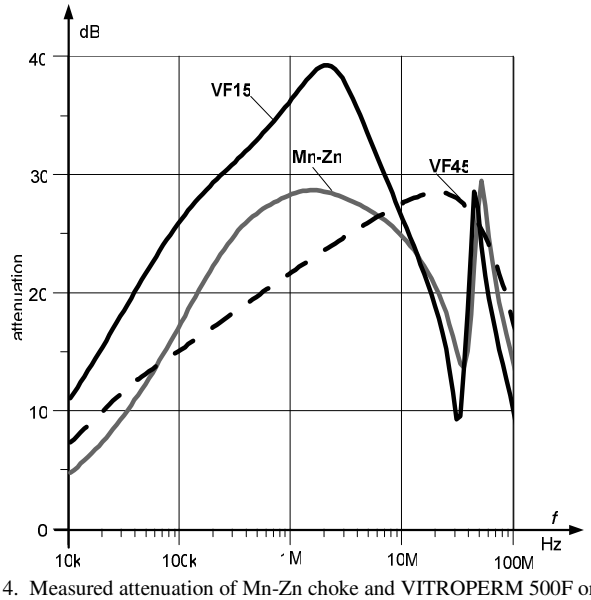

Fig. 4. Measured attenuation of Mn-Zn choke and VITROPERM 500F ones.

The value of stray capacitances depends on manner of winding of chokes and number of turns.

The stray capacitances C_1, C_2 of Mn-Zn and VF15 are similar, because the chokes have the same number of turns and similar geometry. The stray capacitances of VF45 are less due to smaller dimension and number of turns (cf. chapter 2).

The stray capacitances and other parasitic parameters of common mode choke are calculated basing on its equivalent circuit – Fig. 5.

The methods of calculation of parameters of common mode choke are based on open-circuit and short-circuit measurement of modulus of impedance [5]. The impedance is measured between terminals ab for cd are opened or shorted.

The stray capacitances are calculated using resonance frequency and the value of L_0 due to (2) for this frequency. It should be underline that this method takes into account the permeability. It is very important because it changes with frequency (Fig. 6).

The permeability has to be taken into account during the designing of common chokes. When magnetic material is taken into consideration the one with possible constant permeability within broad range of frequency is the best choice. For analyzed cores Mn-Zn core is the best one as it exhibits constant permeability within the broadest range of frequency (up to 200 kHz) – Fig. 6. The worst material is VF45 for which constant permeability is up to 10 kHz. The variation of permeability influence the attenuation properties, cf. Fig. 4.

IV. Temperature Influence of Attenuation Properties

Temperature also influence attenuation properties of common mode choke.

The permeability of magnetic material is dependent on the temperature. The inductance of common choke and relevant attenuation are proportional to permeability. The attenuation of VF15 common mode choke is much stable attenuation against temperature change compared with that of Mn-Zn common mode choke. It is observed in Fig. 7. For frequency of 10 kHz this variations is reflected in inductance L_0 which is depicted in Fig. 8. The inductances are referred to the inductance at 22°C, for Mn – Zn, $L_0|_{22C}$=0.85 mH and to inductance of $L_0|_{22C}$=4.14 mH, for VF15. The inductance is measured by LCR meter at 10 kHz.

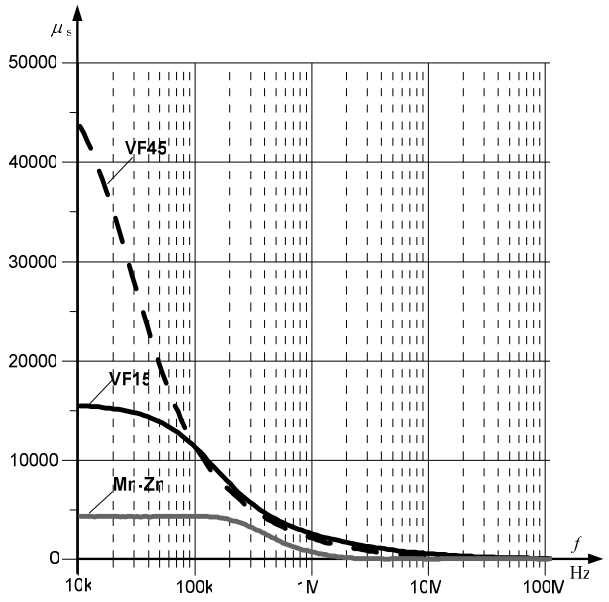

Fig. 6. Measured permeability of Mn-Zn common mode choke and VITROPERM 500F one (Agilent 4294A) [6].

Moreover the VITROPERM 500F cores have higher Curie temperature than Mn-Zn cores. The Curie temperature for VITROPERM 500F is equal 600°C while for ferrite core is equal 120°C [7].

When the Curie temperature exceeds the inductance L_0 will be steeply decreased, example is given in Fig. 8 for Mn-Zn.

The temperature has also influence of saturation currents. Along with increasing temperature the saturation flux density is decreasing. The B-H characteristics of Mn-Zn common mode choke for core for 25°C and 100°C, as an example is presented in Fig. 9.

Another advantage of VITROPERM 500F core is high saturation magnetic flux density. It can be seen in Fig. 10 where B-H characteristics are given.

The value of saturation magnetic flux density is very important for attenuation properties. If the saturation in the core occurs the inductance of the common mode choke extremely decreases. Thus the EMI filter loses its saturation properties.

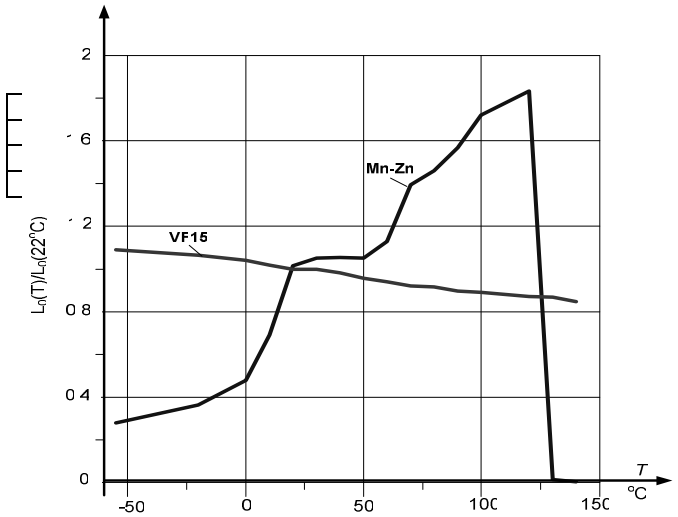

Fig. 8. Change of inductance L0 of VF15 choke and ferrite Mn-Zn one, as a function of temperature, for 10 kHz.

– represents the resistance of the wire R_W<<R, C_1, C_2 – capacitance of primary and secondary winding, C_3 – capacitance between primary and secondary).

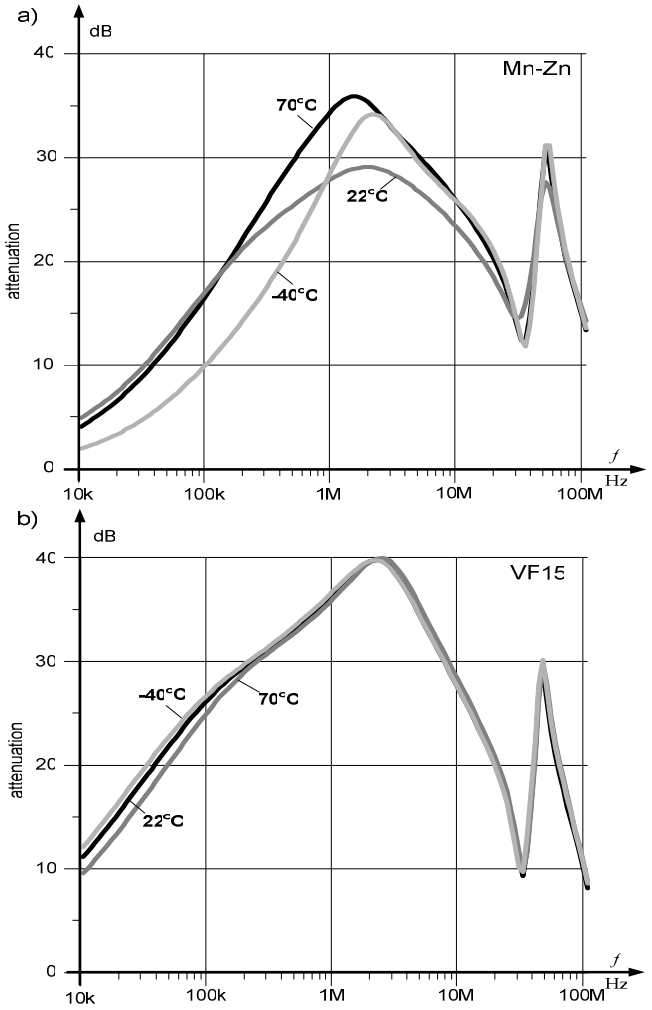

Fig. 7. Measured attenuation characteristic for three selected temperatures for: (a) Mn-Zn and (b) VF15.

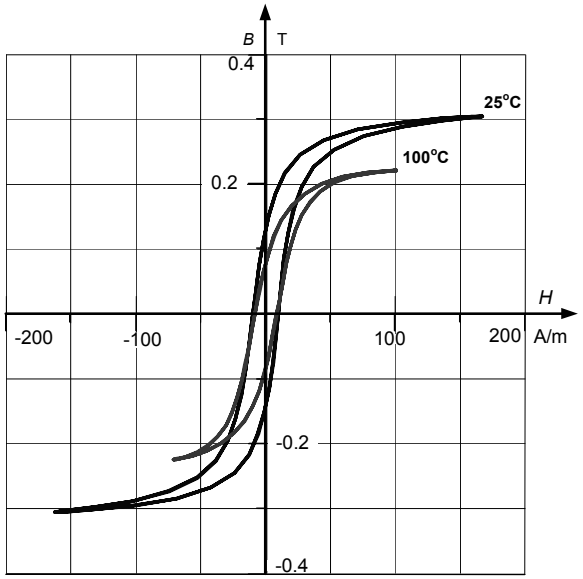

Fig. 9. Measured B-H characteristic of Mn-Zn ferrite core for 25° C and 100° C, for 10 kHz.

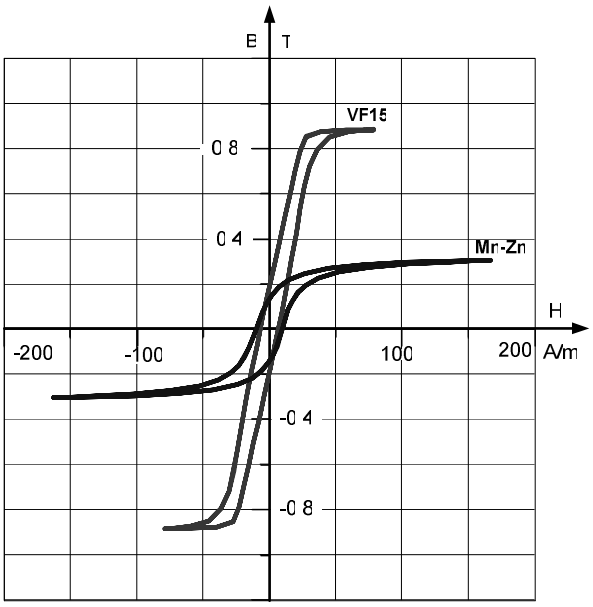

Fig. 10. Measured B-H characteristics of the VF15 core and ferrite Mn-Zn core, for 10 kHz, 22° C.

V. Conclusion

The nanocrystaline common mode chokes VF15 offer significant advantage in attenuation performance. The high permeability permits to achieve the higher inductance than for Mn-Zn common mode choke in case when the geometry and number of turns are similar (Fig. 4).

The VF15 common mode choke exhibits higher attenuation in the frequency range up to 10 MHz. Therefore the nanocrystaline core is suitable for attenuation of noise, generated by switching power supplies.

The high permeability of nanaocrystaline material permits to reduce the geometry and number of turns.

The number of turns has influence of stray parasitic parameters. The value of parasitic parameters reduces the attenuation properties of common mode choke. The stray capacitances of VF15 are less in comparison with Mn-Zn even though the bigger dimensions, because the distance between windings is higher for VF15.

The high saturation of magnetic flux density, high stable in the range of temperature of nanocrystaline material is desirable in EMI filter.

However it should be noted that the change of permeability in the range of frequency has to be taking into account. The high initial permeability not yields the high attenuation in the all necessary range of frequency. (cf. VF45 attenuation characteristic in Fig. 4).

The price of common choke has the same priority as the technical solution for manufacturer and customers.

The nanaocrystaline common mode chokes are much more expensive than Mn-Zn one and overall cost of EMI filter is higher. Therefore to find cost optimized solution, ferrite Mn-Zn with initial permeability around 7000 are still leading compared to EMI filters with nanocrystaline core material.

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Active Power Filter with Soft Switching

Petr Šimonik

***Abstract*—The paper describes used techniques, operation characteristics and develops information of the unconventional soft switched active power filter. The power part is based on progressive IGBT's and high speed voltage and current sensors. The APF is connected in parallel to the AC input of the system, and corrects all loads directly from the AC main. Control unit is based on use of digital signal processor. Used conception brings the savings of electrical energy and better EMC properties in comparison with common kinds of APF. The active power filter can be used for suppression of line current harmonics at AC main.**

***Index Terms*—Active filter, harmonics, harmonic distortion, resonant converter, resonant DC link, soft switching, ZVS converter.**

I. Introduction

THE usage of power electronics (switch mode power supplies, adjustable speed drives, and so on) and also the usage of modern and new-fashioned electronic devices has been increasing rapidly on the all world. Modern and new-fashioned devices impose nonlinear loads to the AC main that draw reactive and harmonics current in addition to active current. The reactive and harmonics current lead to low power factor, low efficiency, harmful electromagnetic interference to neighborhood appliance.

As an alternative parallel harmonics correction technique can be use parallel active power filter with resonant DC-link that will be describe in this paper. This parallel active power filter is a device that is connected in parallel to compensated devices and cancels the reactive and harmonics currents from a group of these nonlinear loads so that the resulting total current drawn from the AC main is sinusoidal. The validity of the design methodology is confirmed by use of PSpice computer simulation and by real site testing on the practical realized model of parallel active power filter with soft switching.

Power quality problems are common in most commercial, industrial and utility networks. Resulting problems from current harmonics can by varied, but typically relate to performance, safety and overheating. Power supply system polluted by current harmonics can lead to – over-voltage/current in the power supply system, over-heating in distribution system due to skin effect, iron losses in transformers, malfunction of automatic control system, damages to capacitor due to resonance, interference in telecommunication systems, voltage distortion and lagging in power factor, and others. However, a flexible and versatile solution to power quality problems is offered by active power filters.

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II. Filter Descriptions, Power Parts

This work describes an implementation of parallel active power filter (PAPF) aimed at correcting current harmonics at power supply system. PAPF compensates current harmonics

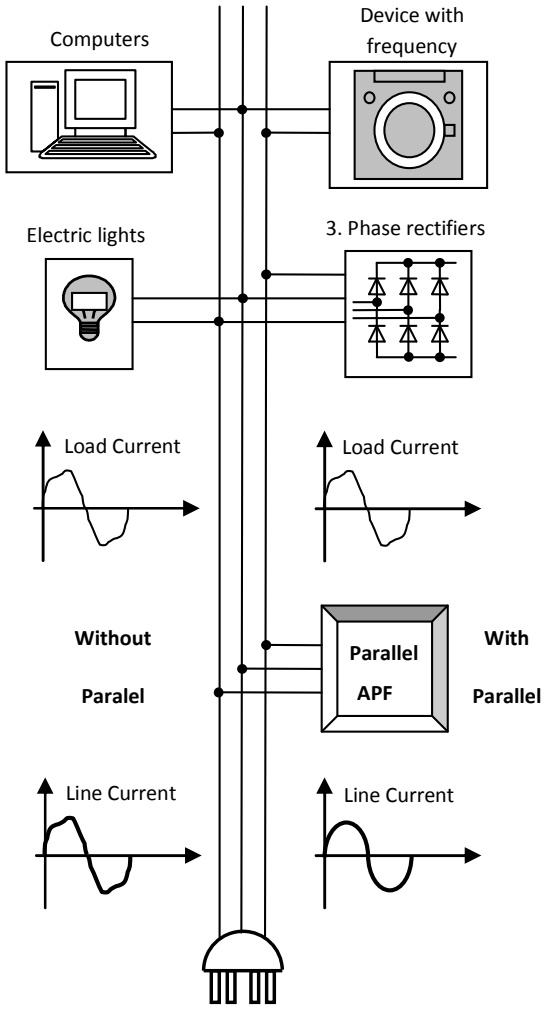

Fig. 1. Block diagram of devices connection.

by injecting equal, but opposite harmonic compensating current. This principle is applicable to any type of load considered a harmonics source.

PAPF is normally implemented with PWM voltage source inverters. In this case the PAPF using converter with resonant DC-link operates as a voltage pulse source, so current is enforced by resonant voltage pulses. Typical controls of PAPF are linear current control, digital deadbeat control, and hysteresis control. However, most methods for obtain right control require high-speed digital signal processor system with fast A/D. In this type of applications is used the special hysteresis control because the converter has resonant DC-link. Resonant circuit is connected between the DC energy store and the power switches of converter's bridge (as shown in Fig. 2).

The disadvantages of classical hard switched converter (for example the switches are subjected to a high-voltage stress, and the switching power losses of a converter increases linearly with the switching frequency) are eliminated or minimized, because the power switches are turned "on" and "off" when the voltage become zero. The current sensors (Lem sensor, shown in Fig. 2) of PAPF monitor the line current in real time and process the measured harmonics as digital signals for control system with DSP.

The output of the power switches (IGBTs) through line reactors (L_f, shown in Fig. 2) inject harmonic currents with an exactly opposite phase to those that are to be filtered. The net effect is an elimination of the harmonics and a clean sine wave as seen by the feeding transformer.

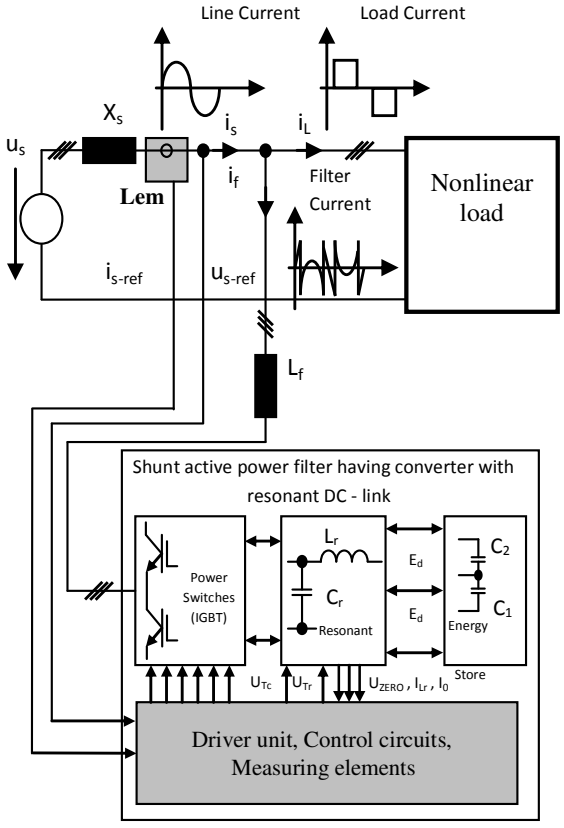

Fig. 2. Block diagram of the power structure and connection with AC main.

III. Resonant DC-Link and DSP Control Unit

The resonant DC-link has implemented a limit voltage circuit, so called the active clamp circuit. An active clamp circuits as shown in Fig. 3 can limit the link voltage which is shown in Fig. 5 (waveforms of resonant DC-link).

Voltage waveform of resonant DC-link on the Fig. 5 is divided by 10 for better visualization. Without an active clamp circuit are peaks of voltage resonant pulse slightly greater than twice the DC input voltage.

The clamp factor k is related to the tank period T_k and resonant frequency $\varpi_0 = \sqrt{LC}$ by

$$\frac{f_0}{f_k} = T_k \varpi_0 = 2\left[\cos^{-1}(1-k) + \frac{\sqrt{k(2-k)}}{k-1}\right]. \quad (1)$$

That is for fixed value of k, T_k can be determined for a given resonant circuit of the filter's converter. For the value $k = 1.5$ is $T_k = 7.65\sqrt{LC}$.

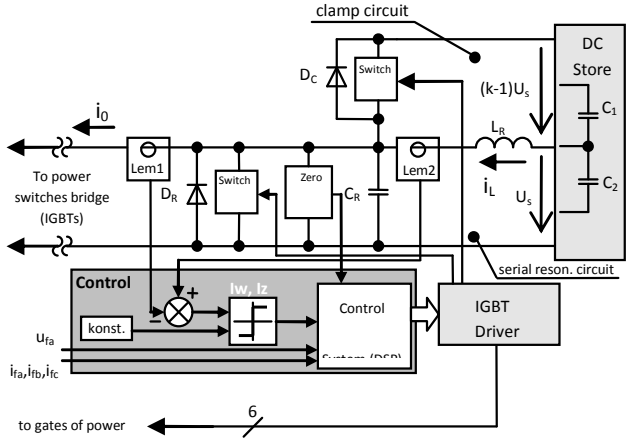

Fig. 3. Used circuit connections of resonant DC link inside the active filter converter structure.

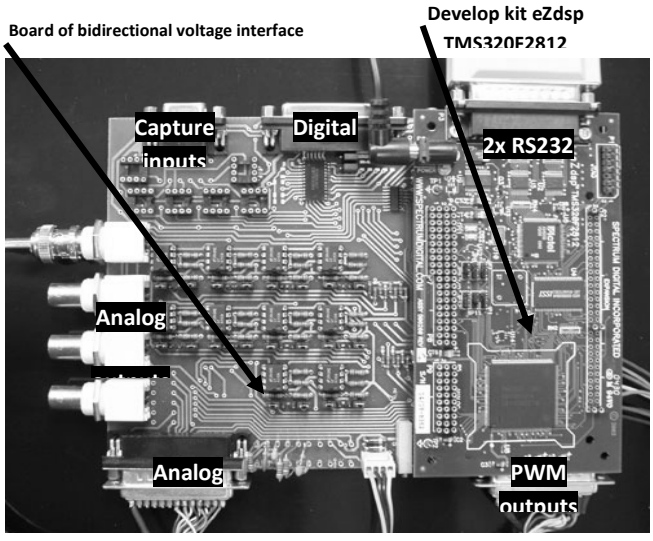

Fig. 4. Control unit based on DSP TMS320F2812.

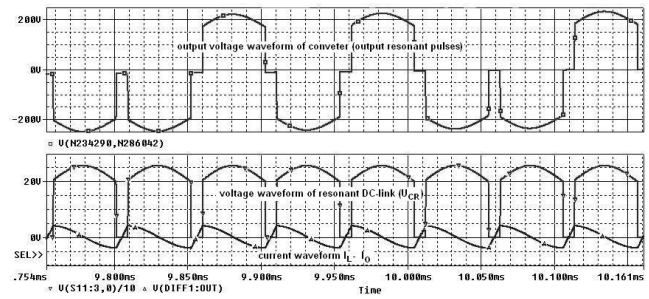

Fig. 5. Voltage and current waveforms of resonant DC-link, output voltage of the converter.

The control unit (which can be seen in the Fig. 4) was designed and executed for the use of powerful microprocessor system based on the Texas Instruments Digital Signal Processor TMS320F2812. Generation of TMS320C28x™ digital signal controllers are the industry's first 32-bit DSP-based controllers with on-board Flash memory and performance up to 150 MIPS. Developed control unit was design as universal control unit and can be used also for other types of converters (in the lab was implemented and tested with Three Level Inverter, Pulse Rectifier and so on). However primary meaning of use should be for soft switched converter which requires high-efficiency control system.

System action is divided to both fast algorithm for control of resonant oscillation in resonant DC-link (as waveforms as is shown at the bottom of Fig. 5) and compensating algorithm of own power active filter and own utility routines.

IV. Computer Simulation Results

The following experimental results were acquired by PSpice simulation model.

Fig. 6 shows the simulation waveforms of PAPF with soft switched converter (having resonant DC-link). The upper trace is current draw of the proposed PAPF (current is injected to the power supply line by the filter). The second trace is line current compensated by proposed PAPF. The third trace is the input current of device with non-linear load (harmonics: I_1= 1 A; I_3= 0,2 A; I_9= 0,2 A).

Other simulation waveforms of PAPF having soft switched converter shows Fig. 7. The upper trace is the required value

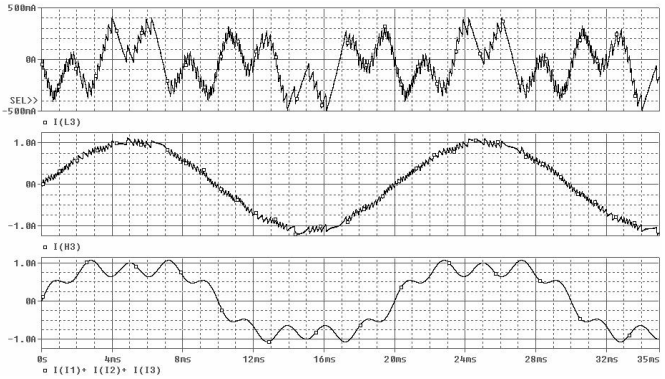

Fig. 6. Current waveforms of simulated PAPF.

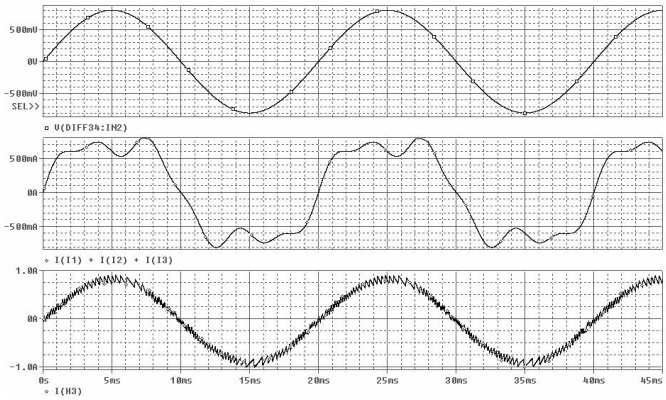

Fig. 7. Current waveforms of simulated PAPF.

of line current. The second trace is the input current of device with non-linear load (harmonics: I_1 = 1 A; I_3 = 0,2 A; I_6 = 0,1 A). The third trace is line current compensated by proposed PAPF.

Next simulation waveforms of PAPF show Fig. 8. There are three phase waveforms. The upper traces show an input current of device with non-linear load and a line current (the sinusoidal one) compensated by proposed PAPF in the phase "U". The second traces show an input current of device with non-linear load and a line current (the sinusoidal one) compensated by proposed PAPF in the phase "V". The third traces show an input current of device with non-linear load and a line current in the phase "W".

V. Measuring Results, Real Sample

Following pictures show practical realization results. In the lab was designed and realized laboratory model of parallel active power filter having resonant converter which shows Fig. 9.

The testing was separated into 3 stages. In 1st stage was tested the control unit (Fig. 4) and FFT (Fast Fourier

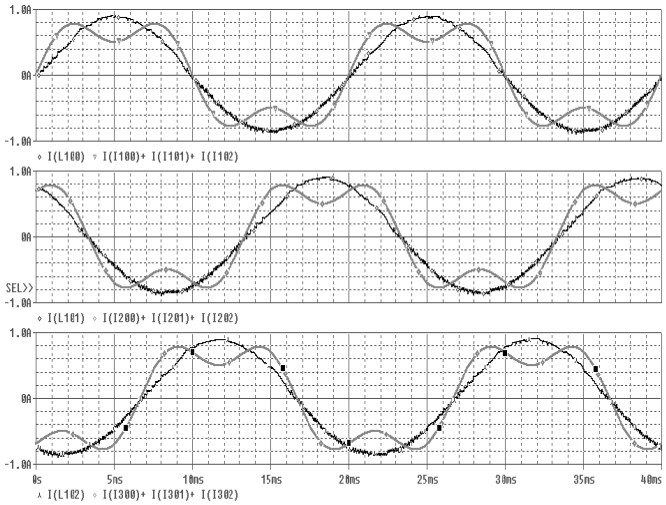

Fig. 8. Three phase simulation waveforms (phase "U", phase "V", phase "W") of PAPF with soft switched converter.

Transformation) computing algorithms. In 2nd stage was tested just resonant converter that was later implanted in PAPF structure and in last stage was tested final behavior of completed PAPF. On Fig. 9 you could see the measuring stand with new laboratory sample of PAPF.

Fig. 10 shows 1st stage testing results. All waveforms are inside signals of the control unit. The upper trace is input current draw i_{La} of device with non-linear load (load consist of resistor R = 20 Ω and inductor L = 60 mH). The second trace is the computed 1st (fundamental) harmonic (required value) of line current. The third trace is computed line angle φ_1. The waveforms are right computing results of FFT block (Fast Fourier Transformation).

Fig. 11 and Fig. 12 shows 2nd stage testing results. All waveforms are signals measured in the structure of applied soft switched converter (new type of converter with resonant DC-link as shows Fig. 3).

The upper trace of oscilloscope screen from Fig. 11 is output current draw of converter with resonant DC-link which was working as alone device (load consist of resistor R = 10 Ω and inductor L = 100 mH). The second trace is output voltage waveform of the converter and the third trace is detail (ZOOM) of out voltage.

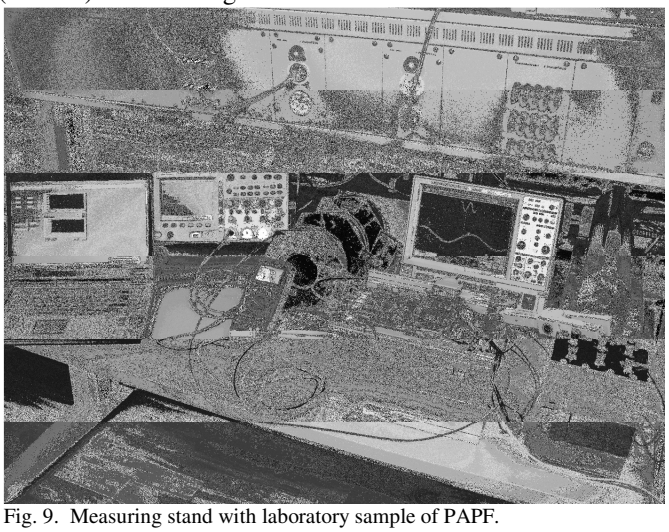

Fig. 9. Measuring stand with laboratory sample of PAPF.

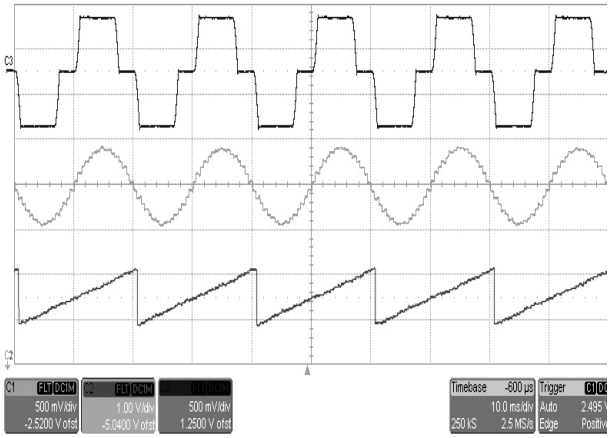

Fig. 10. Calculated data – control signals of practical realized control unit.

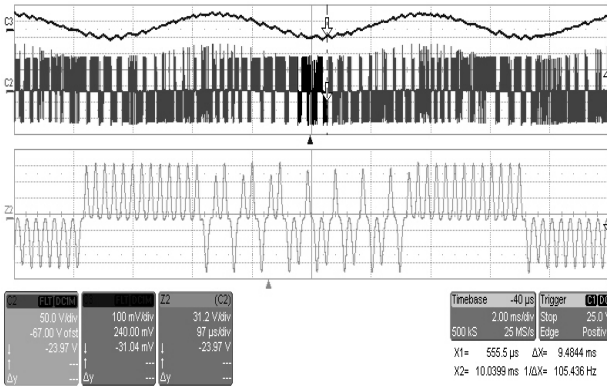

Fig. 11. Output waveforms of applied converter with resonant DC-link.

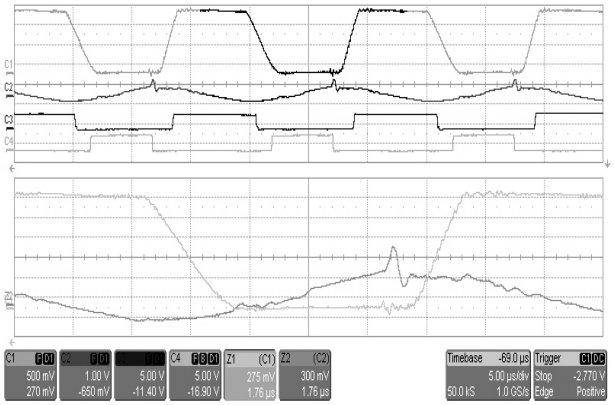

Fig. 12. Resonant DC-link waveforms, main part of practical realized soft switched converter.

Fig. 12 shows the waveforms confirming the right behavior of practical realized resonant DC-link in case of activated clamp circuit. The upper trace shows DC-link voltage waveforms where we can see right behavior of clamp circuit. Other trace shows waveform of DC-link differential current $I_L - I_0$. Next two trace shows switching of "resonant" transistor T_R and clamp transistor T_C. Below is mentioned detail (ZOOM) of DC-link voltage and DC-link differential current $I_L - I_0$.

In our case (appliance of soft switched converter) was necessary to evaluate performances of a new hysteresis current control strategy for autonomous three phase parallel active filter in harmonic currents elimination. Hysteresis control strategy is based on currents errors and their derivatives calculation each time the zero voltage vector is set at the AC side of the inverter of the active filter.

Fig. 13 and Fig. 14 show last stage testing results. The first trace in Fig. 13 is the input current of device with non-linear load (non-linear load: 3. phase non-controlled rectifier loaded by resistor R = 20 Ω and inductor L = 60 mH). The second trace is output current draw of the proposed PAPF (current is injected to the power supply line by PAPF). The second trace is line current compensated by proposed PAPF.

Fig. 14 shows current waveforms in case of load change (from 0% to 100%). There you can see the right and quick adaptation. The first draw in this figure is the input current of device with non-linear load (non-linear load: 3. phase non-

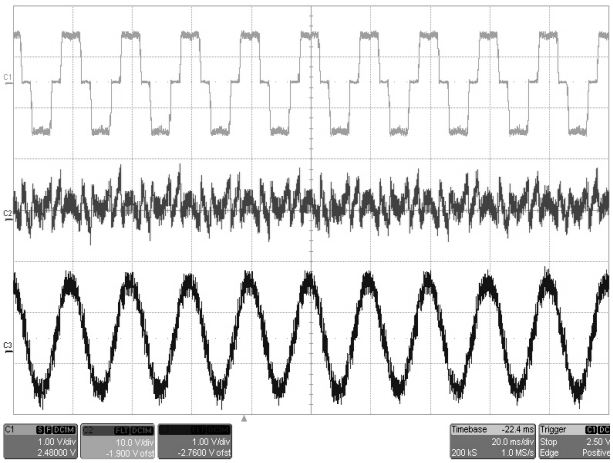

Fig. 13. Measured waveforms show right behavior of realized PAPF with soft switched converter.

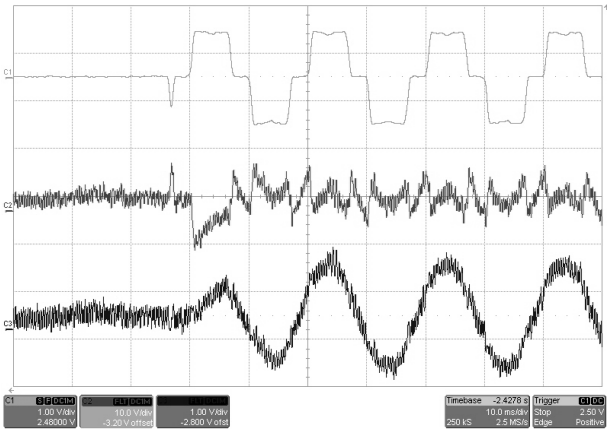

Fig. 14. Measured waveforms show right behavior of realized PAPF with soft switched converter.

controlled rectifier loaded by resistor R = 20 Ω and inductor L = 60 mH).

The second trace is output current draw of the proposed PAPF (current is injected to the power supply line by PAPF) and last trace is line current compensated by proposed PAPF.

VI. Conclusion

Active filters have wide application for controlling harmonic currents from nonlinear loads. The device and techniques described in the paper show the possible way to correct current harmonics at power supply system by the new type of parallel active power filter. The operation principles of parallel active power filter with resonant converter have been presented and analyzed in this paper.

The simulation results proved the viability of using resonant circuits (resonant DC-link) for implementation into the structure of parallel active power filters. The simulation circuits were designed as a simplified model. However, for calculation of simulative diagram is needed high – powered computer.

Practical realization was based on simulation results, which are presented in this paper. Presented results confirm right behavior of developed PAPF working as soft switching device (in mode of Zero Voltage Switching). This conception brings the advantages of resonant converters. Such as savings of electrical energy (power switches are turned-on and turned-off when the voltage becomes zero) and much better electromagnetic interference properties.

Acknowledgment

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Power Quality Measurement in a Modern Hotel Complex

Velimir Strugar and Vladimir Katić

***Abstract*—The paper presents the analysis of power quality characteristics at the 10 kV grids supplying a modern hotel complex in Montenegrin Adriatic coast. The consumer is characterized with different type of loads, of which some are with highly nonlinear characteristic. For example, smart rooms, lift drives, modern equipment for hotel kitchen, public electric lighting, audio, video and TV devices, etc. Such loads in the hotel complex may be source of negative effects regarding power quality at MV public distribution network (10 kV and 35 kV). In the first part of the paper, results of harmonic measurement at a 35/10 kV substation are presented. The measurements lasted one week in real operating conditions (in accordance with EN 50160). The results were the basis for developing a simulation model. The measurement results were analyzed and compared with simulation ones. Application of harmonic filter is simulated. Filter effects on harmonic level is calculated and discussed using simulation results.**

***Index Terms*—Modern hotel complex, harmonics, THDU, THDI, computer simulation.**

I. Introduction

TODAY, power quality problems are on the top of interests of contemporary scientific and expert authorities, dealing with electrical engineering, especially electrical power transmission and distribution networks. One of the most common problems is the appearance of harmonic voltages and currents, which are consequence of different operating regimes of connected nonlinear consumers [1]. The impact of individual consumers has been more or less determined and is known in principle. However, the effects of a large number of the similar or different consumers connected on the same PCC (Point of Common Coupling) in the distribution network (low or medium voltage), with their very different operating characteristics and very stochastic moment of access to the network, is always complicate to determine and often represent a unique case. Long term monitoring and measurements are applied for harmonic or other power quality parameters analysis, together with specialized simulation software.

In this paper, power quality analysis of a modern hotel complex on the Montenegrin Adriatic coast is presented. Objectives of measurement are determined by the fact that in modern hotels a huge of number of nonlinear loads are applied (large number of audio and video devices, public lighting and elevators, kitchen facility, air conditioning and other non-linear loads). Main objective of measurement is recording of current and voltage waveforms and performing their harmonic analysis. These results are very important for estimation of daily diagram of current variation due to operation of such load, especially in step of planning the connection of these objects, as well as prediction of possible irregular situation in distribution network, which may arise due to poor power quality during their operation.

The paper presents the results of harmonic measurements for the hotel complex during one week in full season. To enable analysis of various situations and loads operating condition, which may occur in actual operation, but not during the measurements, a simulation model of the hotel network is developed. Application of harmonic filters to decrease level of harmonic "pollution" is discussed using simulation results.

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II. Objective Measurement

Measurements were performed in the period from the 6th up to the 15th July 2009 using modern power quality monitoring equipment and fully in accordance with EU standard EN 50160. The hotel is supplied from 35 kV line over two substations 35/10 kV, which acts as electricity source for hotel complex. Part of available capacity of power transformers in substation 35/10 kV is used by the distribution operator for other consumers connected to 10kV voltage. Fig. 1 presents single-pole schema of distribution network showing connection of the hotel complex.

The connection from 10 kV busbar in substation 35/10 kV to feeder in hotel substation 10/0.4 kV is realized with 10 kV cable. This substation has four transformer units of 1 MVA rated power (TR1, TR2, TR3, TR4). Usually, they are connected in pairs – TR1, TR3 and TR2, TR4, so measurements were performed simultaneously at 10 kV PCC, with two quality analyzers Fluke 434. These devices record all relevant parameters, using of values of secondary current and voltage of current and voltage measuring transformers. Due to paper space constraints, results of measurements on the first pair TR1, TR3 will be presented, only.

Beside considered hotel complex, 10 kV feeder of TS 35/10 kV substation supply a number of other distribution customers

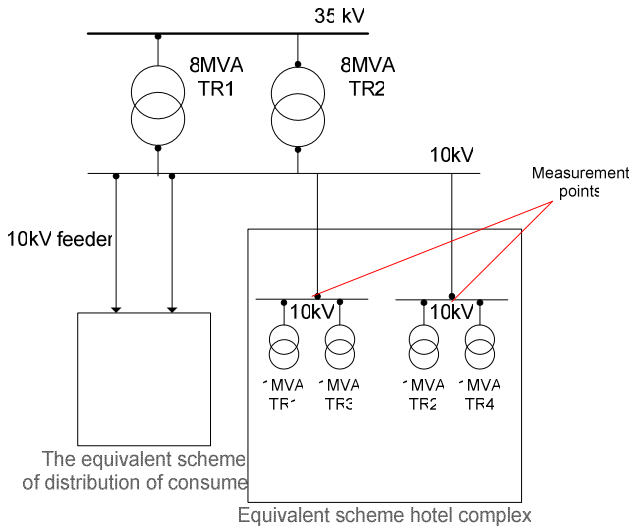

Fig. 1. Single pole schema of the hotel complex connection.

(Fig. 1) with individually less power (houses, residential buildings, as well as several markets and other retail outlets). There is high probability that possible low power quality parameters, during some operating modes of the hotel complex, will have negative effects on these customers, also. Therefore, measurements results have much wider significance.

III. Results of Measurements

R.m.s. values of current and voltage variation of in all three phases during the measurement period are recorded. Also, variations of active and reactive power were monitored. For recorded values of voltage and current, harmonic analysis is performed calculating individual harmonics (HDUn, HDIn), as well as total harmonic distortion (THDU, THDI). Figs. 2 and 3 show spectrum of voltage and current harmonics in the measurement period, respectively, while Figs. 4 and 5 show time variation of THD and some individual harmonic values.

Results show that in general case, the hotel activity does not have permanent negative effects on the network and cannot cause harmonic disturbances in higher level than that stipulated in EN 50160. Such conclusion is result of harmonics and THD values shown on Figs. 2 and 3. All harmonics values and total harmonic distortion of voltage and current are within limits stipulated in standards.

However, the default state of change short-circuit current on 10 kV grid in substation in the hotel complex, it may further affect the variance of parameters. It was also apparent relation between the changes in measuring period of the 5th harmonic voltage and current THD, and voltage and current (Fig. 4). It is obvious that dominant effect on THDU has the 5th harmonic. This is the recognizable characteristics of the distribution system.

Although the value THDU is in accordance with the limits defined in the standards [1], and not surpassed 5%, the THDI in some phases is greater than limits. Namely, for 10 kV grid

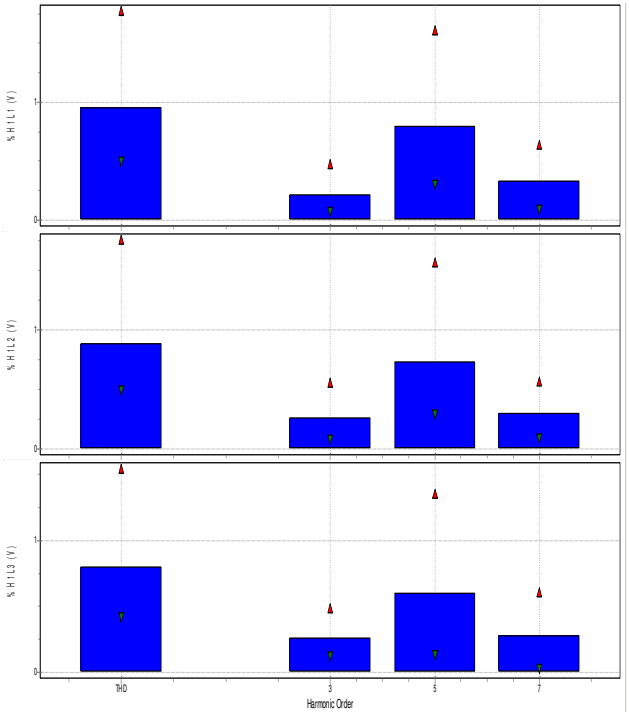

Fig. 2. THDU and voltage harmonics – HDU_3, HDU_5, HDU_7 (Line 1 – top, Line 2 – middle, Line 3 – bottom).

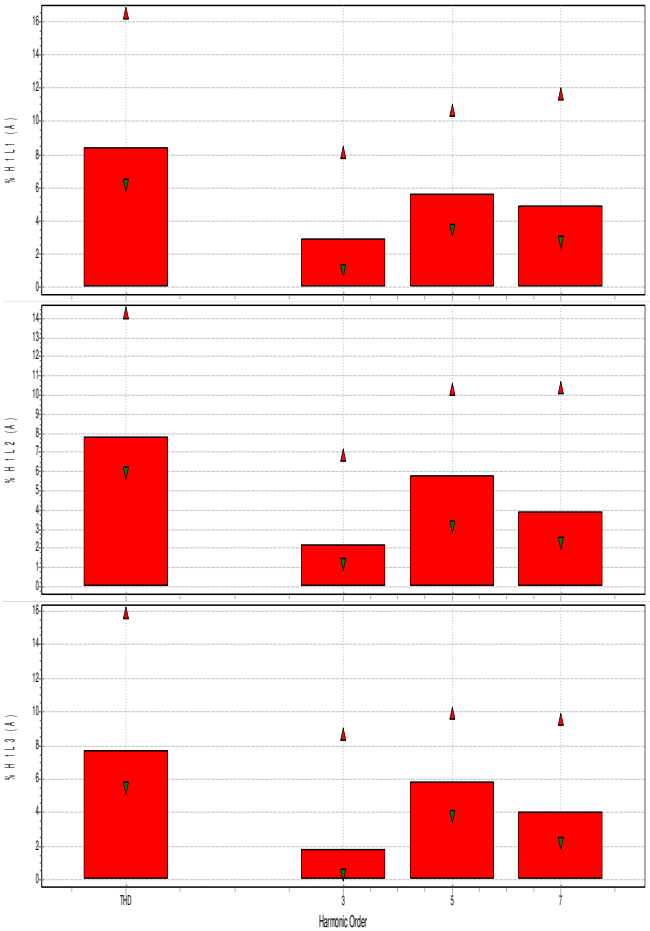

Fig. 3. THDI and current harmonics – HDI_3, HDI_5, HDI_7 (Line 1 – top, Line 2 – middle, Line 3 – bottom).

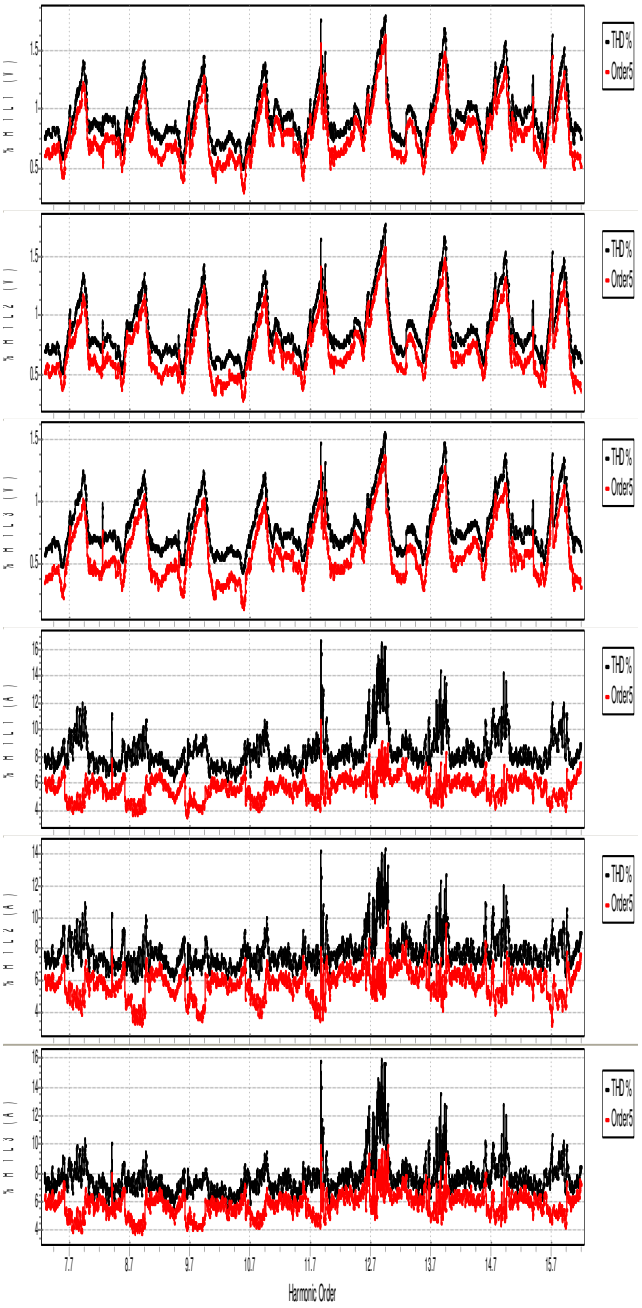

Fig. 4. Top 3 graphics: THDU (black line) and HDU_5 (red line) for three phases (L1, L2, L3); Bottom 3 graphics: THDI (black line) and HDI_5 (red line) for three phases (L1, L2, L3).

in consideration, the relationship between maximum current (load) and maximum short-circuit current on the buses [9] is

$$20 < I_{sc} / I_L < 50 . \quad (1)$$

According (1) and [9] is obviously that all values THDI greater than 8% are problem. This is especially visible in Fig. 5, for all days from the July 11, 2009 up to the end of measurement, and especially for July 12, 2009 after midnight, when the values reached level beyond 16%. It is obvious that simultaneous activity of many nonlinear consumers in these hours (air conditioning, audio video equipment, a multitude of electronic devices for entertainment, etc.) contribute to this effect.

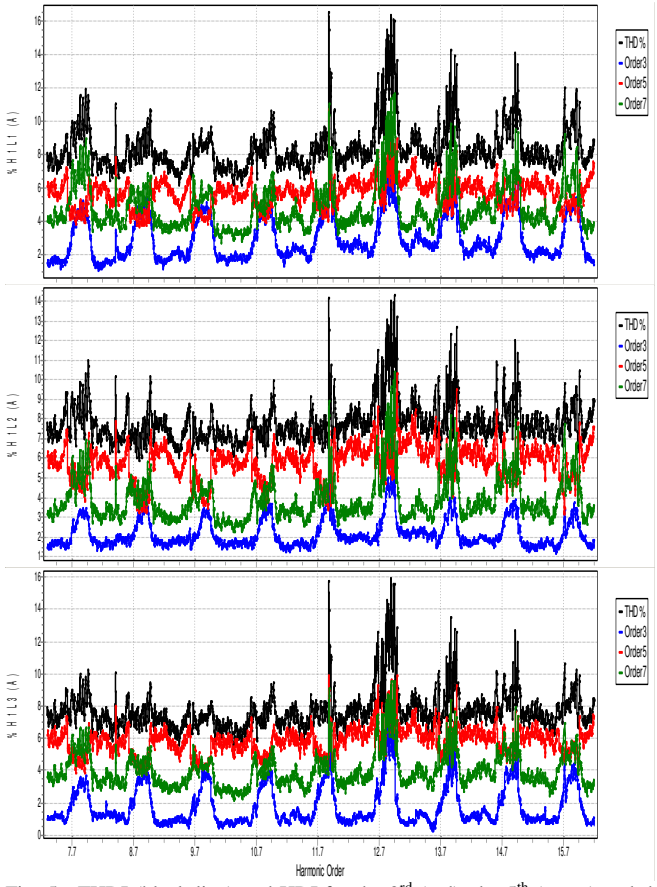

Fig. 5. THDI (black line) and HDI for the 3rd (red), the 5th (green) and the 7th (blue) harmonics in three phases (L1, L2, L3) for the entire interval measurements.

IV. Computer Simulation Model

The computer model is based on actual network and power quality parameters, which are known as result of previous measurement [2-9].

Simulation mode of part of the real distribution system, there is specialized application software PSS/VIPER (Power System Simulator/Visual Power Engineering). PSS/VIPER can model any balanced three-phase AC power system for marine, industrial, and small utility-distribution systems.

At the beginning, a simplified model of the system is arranged, with the inclusion of equivalent elements in order to obtain similar situation as in real system. Then, the varying parameters (harmonic filters and sources) required actions noted in the introduction to the system in the state of the greatest degree of stability.

Figs. 6 and 7 give an overview of the single-pole scheme of electrical network, which supplies the hotel complex. The 35 kV line supplies the 35 kV feeder at the substation 35/10 kV. The model for 35 kV source is synchronous generator. Furthermore, 10 kV busbar, as stated earlier, supplies part of the power distribution network. This part of network is presented in simultaneous model as load, similar to the 0.4 kV buses, where the hotel complex presented with

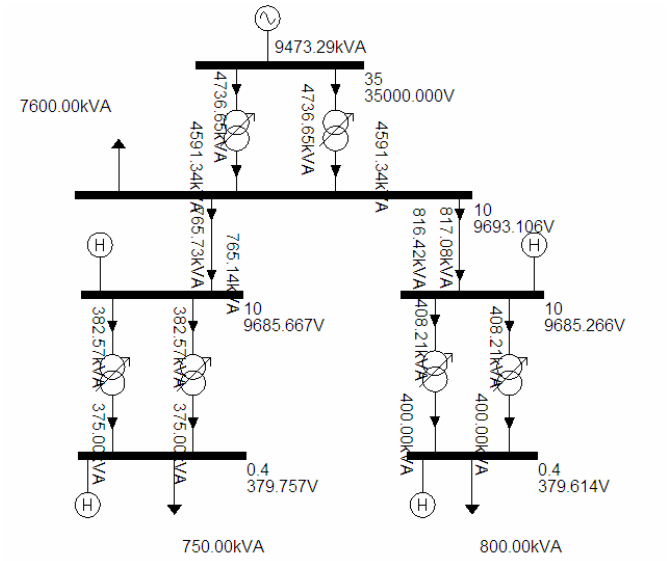

Fig. 6. Single-pole scheme model observed distribution system before the installation of filters.

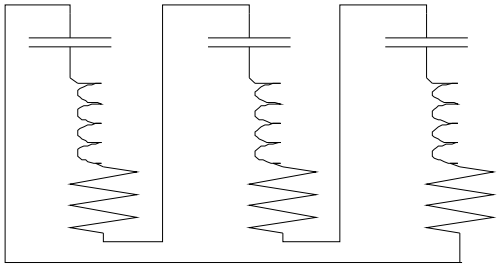

Fig. 7. Three-pole tuned filter.

characteristic load (Fig. 1). Parameterization of model elements or a standard (for the synchronous generator and transformer), are varied in accordance with the measurements (for 10 kV lines and 0.4 kV and the load, as well as harmonic sources).

Table I gives the numerical value obtained for the third, the fifth and the seventh harmonic voltage and THDU. Due to consistency, 100 (per unit) must multiply all values in the table. The effect of the filter installation is obvious comparing the data from the table below.

To improve the power quality regarding harmonic levels, a harmonic filter is considered. It is a single tuned filter as on Fig. 7. In the computer simulation, installation of harmonic filters at 0.4 kV busbar was performed with identical setting for both transformers. Filters locations are shown on Fig. 8.

TABLE I
VALUE OF HARMONIC VOLTAGE LEVELS AND THDU AFTER THE INSTALLATION OF FILTERS

	Busbar	H3 (p.u.)	H5 (p.u.)	H7 (p.u.)	THDU (p.u.)
1	35	0.000	0.000	0.000	0.000
2	10	0.000	0.002	0.002	0.003
3	10	0.000	0.002	0.002	0.003
4	0.4	0.004	0.011	0.008	0.015
5	10	0.000	0.002	0.002	0.003
6	0.4	0.004	0.010	0.012	0.016

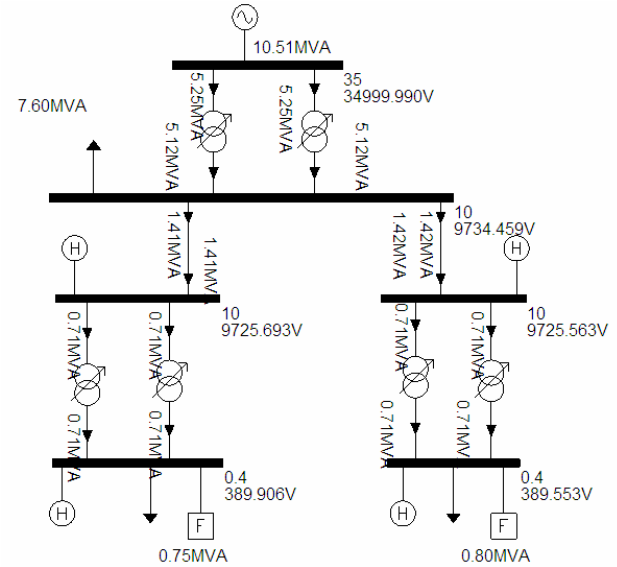

Fig. 8. Single-pole scheme model observed distribution system after the installation of filters.

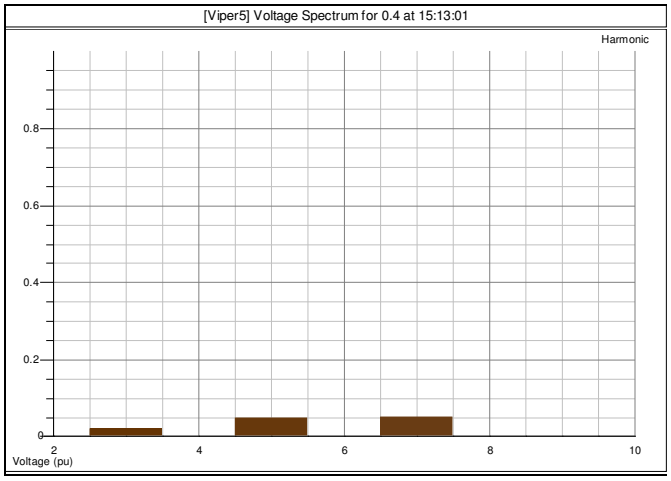

Fig. 9. Harmonic voltage spectrum of models before the installation of filters.

Settings of a filter connected in Δ are given in per unit using the following base values of the filter: $\boldsymbol{R = 0.2}$, $\boldsymbol{X_c = 2.604}$, $\boldsymbol{X_l = 0.10416}$.

Filter was chosen for the expected size of 1000 kVA.

Results of filter application are presented in Table II and on Figs. 9 and 10. It can be seen that harmonics are significantly mitigated, i.e. that negative effects of non-linear loads in the hotel complex can be lowered by installing of the described harmonic filters at 0.4 kV buses.

V. CONCLUSION

In countries with an attractive environment and incomplete developed distribution network, the challenges of modern construction can sometimes be problematic. This is particularly case in building modern hotel complex, smart buildings, modern shopping malls and entertainment centers, especially when it comes to connection of such facilities to the electric power distribution network, as they are, in principal,

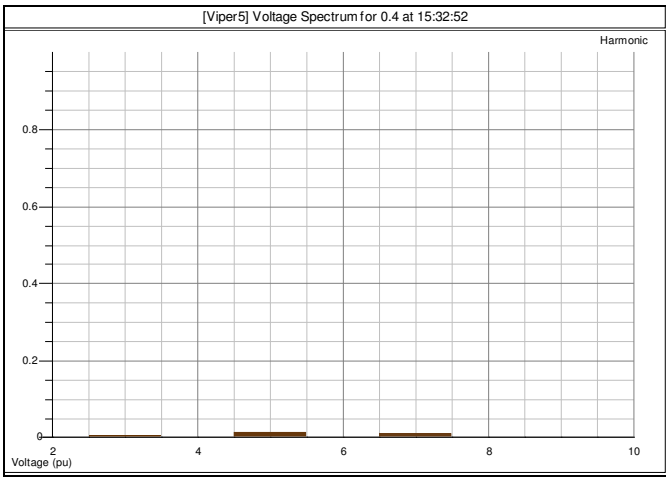

Fig. 10. Harmonic voltage spectrum of models after the installation of filters.

designed for the standard levels of nonlinearity, described by cosφ and its common values.

Today, the simultaneous operation of many nonlinear devices in modern facilities in consideration, imposes the necessity of new ways of planning of distribution networks, primarily it means the standard model of consumer connection procedure. By using standardized equivalent scheme for typical consumers (hotels, restaurants, shopping center, apartment), it is easy to come to the equivalent scheme of the part of distribution system, and then, and his planning is not particularly difficult.

In the process of issuing of conditions, that the investor has to fulfill to the end of construction to obtain approval for connection to distribution network, it is necessary to be well-acquainted modes of future consumers.

Therefore, especially importance is the modeling, especially large consumers modeling. Consequences of poor planning when it comes to the quality of delivered electricity and consumers may feel that causes disruption, but also the surrounding consumers who connected on the same point of common access. Who will pay the consequences, and final, must be the focus of attention operator distribution.

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Design of a PEM Fuel Cell Simulator Based on DC-DC Buck Converter

Georgi Georgievski and Goce L. Arsov

***Abstract*—Modeling of fuel cells is getting more and more important as power fuel cell stacks being available and have to be integrated into real power systems. This paper presents a novel circuit simulator for a PEM fuel cell that can be used to design fuel cell based systems. The simulator is consisted of a DC-DC buck converter driven by PIC 16F877 microcontroller. The proposed circuit can be used in design and analysis of fuel cell power systems.**

***Index Terms*—PEM fuel cell, modeling, design, simulation, pulse width modulation (PWM).**

I. Introduction

FUEL cells as energy source have been present since 1839. They were discovered and developed by the English physicist William Grove. But, since then, for more over one century they were not more than a laboratory curiosity [1]. After the period of 120 years since the fuel cells emerged, NASA demonstrated some of their potential applications in the space flights exploration. Consequently, the industry has started recognizing the commercial aspects of the fuel cells, which, due to the technological barriers and their high production costs, were not economically profitable at that stage of technology [2]. Today, fuel cells of various types have emerged as promising alternative sources of "clean energy" for applications ranging from automotive industry to residential and commercial installations. This has created a need for a class of specialized power converters geared to interface between the fuel cell device and the end–user appliance, often as a battery charger. Specifications for power conversion equipment depend on the fuel cell's physical properties and manufacturing economics. The cells' output voltage is dependent on the load. So, there is a need to model the fuel cell for optimizing its performance and also for developing fuel cell power converters for various applications.

The proton exchange membrane fuel cell (PEMFC) has been considered as a promising kind of fuel cell during the last 20 years because of its low working temperature, compactness, and easy and safe operational modes. The proton exchange membrane (PEM) fuel cell is very simple and uses a polymer (membrane) as the solid electrolyte and a platinum catalyst.

It is possible, during the design process, to avoid use of very expensive fuel cells by using electric circuit which would be able to simulate the characteristics of a real fuel cell. Such simulator circuit can simulate characteristics of different fuel cells only by changing the parameters which control the operation of the circuit.

Up to now different type of models of PEM fuel cell were proposed [4]–[12]. Unfortunately, most of the proposed models cannot be used for practical realization of a fuel cell simulator.

In this paper the design of PEM Fuel Cell simulator based on DC-DC buck converter [3] digitally controlled by PIC 16F877 microcontroller is presented. Such fuel cell simulator can be used in preliminary design of fuel cell based systems.

II. Fuel Cell Characteristics

The fuel cell directly converts chemical energy into electrical energy. The chemical energy released from the fuel cell can be calculated from the change in Gibbs free energy (Δ_{gf}) which is the difference between the Gibbs free energy of the product and the Gibbs free energy of the reactants [14]. The Gibbs free energy is used to represent the available energy to do external work. For the hydrogen/oxygen fuel cell, the overall chemical reaction can be expressed as:

$$H_2 + \frac{1}{2} O_2 \rightarrow H_2O \tag{1}$$

and the change in the Gibbs free energy as:

$$\Delta g_f = (g_f)_{H_2O} - (g_f)_{H_2} - (g_f)_{O_2} . \tag{2}$$

The change in Gibbs free energy varies with both temperature and pressure:

$$\Delta g_f = \Delta g_f^0 - RT_{fc} \ln \left[\frac{p_{H_2} p_{O_2}}{p_{H_2O}} \right] \tag{3}$$

where Δg_f^0 is the change in Gibbs free energy in standard pressure (1 bar) which varies with temperature T_{fc} in Kelvin. The partial pressures p_{H2}, p_{O2} and p_{H2O} of the hydrogen, oxygen and vapor are expressed in *bar*. R is the universal gas constant, 8.31454 J/(kg·K). The value of Δg_f is negative, which means that the energy is released from the reaction.

For each mole of hydrogen, two moles of electrons pass

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around the external circuit and the electrical work done (charge × voltage) is:

$$W = -2FE \quad \text{(J)} \tag{4}$$

where F is the Faraday constant (96485 C) which represents the electric charge of one mole of electrons and E is the voltage of the fuel cell. The electrical work done would be equal to the change in Gibbs free energy if the system were considered reversible:

$$\Delta g_f = -2FE\,. \tag{5}$$

The reversible open circuit voltage of the fuel cell or "Nernst" voltage of hydrogen fuel cell is:

$$E = -\frac{\Delta g_f}{2F} = \frac{\Delta g_f^0}{2F} + \frac{RT_{fc}}{2F}\ln\left[\frac{p_{H_2}\,p_{O_2}}{p_{H_2O}}\right] \tag{6}$$

$$E = 1.229 - 0.85\times10^{-3}(T_{fc} - 298.15) + 4.3085\times10^{-3}T_{fc}\left[\ln(p_{H_2}) + \frac{1}{2}\ln(p_{O_2})\right]. \tag{7}$$

T_{fc} is expressed in Kelvin, and p_{H2} and p_{O2} in atm.

The actual voltage of the fuel cell is less than the value calculated by equation (7). Typical PEM fuel cell performance plot is given in Fig. 1. The differences are result of losses or irreversibilities.

The current density, cell current per cell active area A_{fc}(cm^2), is:

$$i = \frac{I_{st}}{A_{fc}}\,. \tag{8}$$

The fuel cell losses are attributed to three categories: the *activation* loss, the *ohmic* loss and the *concentration* losses.

The voltage drop due to activation loss is dominated by the cathode reaction conditions. The relation between the activation overvoltage v_{act} and the current density is described by the Tafel equation:

$$v_{act} = a\ln\left(\frac{i}{i_0}\right) \tag{9}$$

where, a is a constant and i_0, the exchange current density, is also a constant. Both constants can be determined empirically. For low temperature PEM fuel cell, the typical value of i_0 is about 0.1 mA/cm^2.

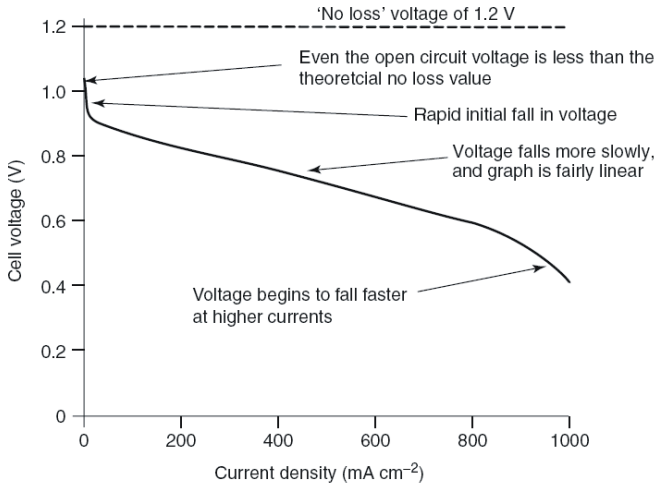


Fig. 1. Graph showing the voltage-current dependence of a typical PEM fuel cell.

The ohmic loss arises from the resistance of the polymer membrane to the transfer of protons and the resistance of the electrode and the collector plate to the transfer of electrons. The voltage drop that corresponds to the ohmic loss is proportional to the current density:

$$v_{ohm} = i \cdot R_{ohm} \tag{10}$$

R_{ohm} ($\Omega\cdot$cm^2) is the internal electrical resistance. The resistance depends strongly on the membrane humidity and the cell temperature.

The concentration loss or concentration overvoltage results from the drop in concentration of the reactants as they are consumed in the reaction. These losses are the reason for rapid voltage drop at high current densities. The voltage drop due to concentration losses is given by:

$$v_{conc} = i\left(c_2\frac{i}{i_{\max}}\right)^{c_3} \tag{11}$$

where c_2, c_3 and i_{max} are constants that depend on the temperature and the reactant partial pressure and can be determined empirically. The parameter i_{max} is the current density that causes precipitation voltage drops.

By combining all voltage drops associated with all the losses, the single fuel cell operating voltage can be expressed as:

$$v_{fc} = E - a\cdot\ln\left(\frac{i}{i_0}\right) - [i\cdot R_{ohm}] - \left[i\cdot\left(c_2\frac{i}{i_{\max}}\right)^{c_3}\right] \tag{12}$$

where, the open circuit voltage E is given by (7).

The fuel cell stack comprises multiple fuel cells (n) connected in series. The stack voltage can be calculated as:

$$v_{st} = nv_{fc}\,. \tag{13}$$

III. PEM Fuel Cell Simulator Design

The proposed PEM fuel cell simulator is composed of two parts: the power circuit and the control circuit. To achieve appropriate power supplied to the load the digitally controlled DC-DC buck converter [17] is proposed as a main power circuit. The control is performed by the microcontroller PIC 16F877 [18]. The microcontroller is connected in the feedback loop of the main power stage. This way, the output voltage is automatically changed in response to any change in the output current in accordance to the *V-I* polarization characteristics of any PEM fuel cells.

The complete circuit diagram realized with simulation program PROTEUS PROFESSIONAL is shown in Fig. 2.

A. Design of the Power Part – DC-DC Buck Converter

DC-DC buck converter is realized with MOS-transistor switch (SW), diode (D) and *LC* filter (inductance L and capacitance C) that are selected in the following manner (Fig. 3.).

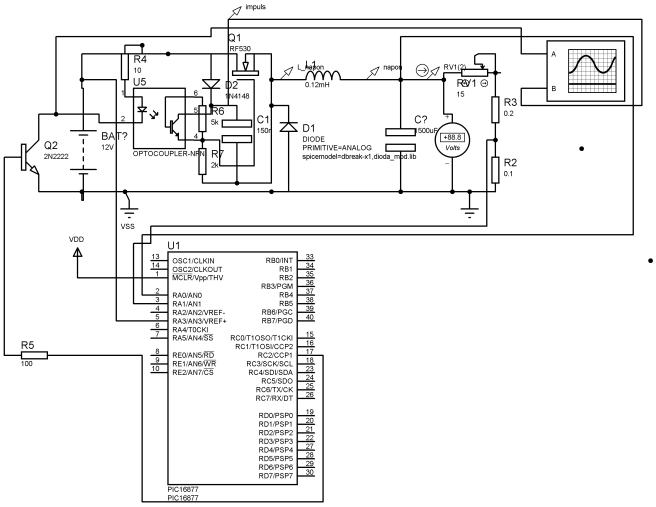


Fig. 2. Circuit diagram of the realized DC-DC buck converter.

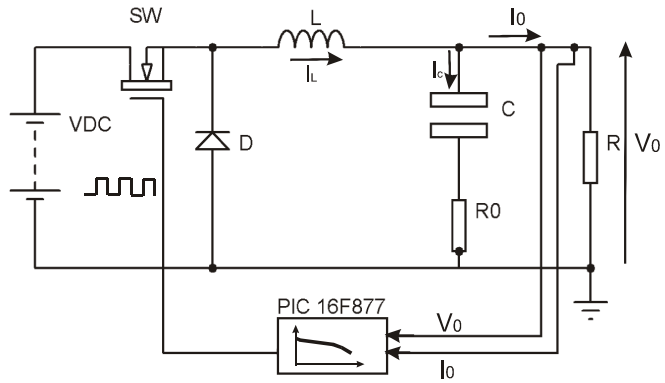


Fig. 3. The basic circuit of the DC-DC buck converter controlled by microcontroller.

As a main switch the MOSFET IRF 530 has been chosen. Its main characteristics are: fast switching characteristics and low on-resistance.

As a diode MUR 860 with low forward voltage drop and ultra fast reverse recovery time (t_{rr}<60 ns) has been selected.

In general the output voltage of the DC-DC buck converter is independent of the switching frequency [17]. Because the *AC* losses in the DC-DC buck converter are inversely proportional to the switching period *T*, decreasing the period *T* results in decreased size of the filter elements (*L* and *C*), but increased losses in the switching transistor and, possibly, necessity to use larger heat sink to keep the switching transistor temperature within desired limits. The optimal switching frequency for this type of circuits may vary in the range of 20–50 kHz, in order to minimize the switching losses in the MOSFET. For this project it is set to 40 kHz.

The inductance *L* is chosen in the manner that it is current does not become discontinuous before the DC output current falls to its specified minimum value, which, in most cases, is one tenth the nominal value. The inductor must be designed so that it does not saturate at DC current of $1.1I_{on}$. So we have:

$$L = \frac{(V_{dc} - V_0)T_{on}}{0.2I_0} = \frac{(12-6)\cdot 25\cdot 10^{-6}}{0.2\cdot 5} = 150\,\mu\text{H}. \quad (14)$$

The capacitance, *C*, determines the output voltage ripple. Because the capacitor is not an ideal one, it has parasitic inductance (L_0) and resistance (R_0) in series with its capacitance. They are characterized as equivalent series resistance (ESR) and equivalent series inductance (ESL). The influence of the series inductance can be neglected for switching frequency below 300 kHz [17]. There are two ripple components in the output voltage, one due to R_0 and second due to *C*. The ripple component due to *ESR* is proportional to the peak to peak inductor ramp current (I_2-I_1), and the ripple component due to *C* is proportional to average current value. For a capacitor selection, it is necessary to know the value of R_0 which is given by capacitor manufacturers. Over a large range of voltage ratings and capacitors values, for aluminum electrolytic capacitors, the product $R_0 \cdot C$ tends to be constant. It ranges from $(50–80)\cdot 10^{-6}$ usually. Let us assume that the resistive ripple component is V_{rr}=0.05 V peak-to-peak. Then we may write: $0.05=(I_2–I_1)\cdot R_0=1\cdot R_0$ and R_0=0.05Ω. For $R_0 \cdot C = 50\text{x}10^{-6}$:

$$C = 50\cdot 10^{-6} / 0.05 = 1000\,\mu\text{F}. \quad (15)$$

The capacitive ripple voltage V_{cr} is:

$$V_{cr} = \frac{I\cdot t}{C} = \frac{0.25\cdot 25\cdot 10^{-6}}{1000\cdot 10^{-6}} = 0.00625\text{ V} \quad (16)$$

where, the average value of current is $(I_2$-$I_1)/4$=0.25 A. Usually the capacitive ripple voltage may be neglected, because it is much smaller compared to the ripple voltage due to the resistance R_0.

B. Design of the Control Part of the DC-DC Buck Converter with Microcontroller PIC 16F877

The microcontroller PIC 16F877 is used to control the proper work of the DC-DC buck converter. PIC 16F877 contains two 10-bit A/D convertors by which the measured analog output current and voltage values are converted to digital for further processing. The PWM module generates the driving pulses for the switching transistor in the power stage. The PEM fuel cell polarization *V-I* characteristic can be either calculated using the relations (5)-(13), obtained by using some of the referred simulation models, or measured using a real fuel cell. For simplicity, here, the measured curve of a single fuel cell, at specified conditions, is implemented in the PIC memory. The values should be modified according to the stack current and voltage capabilities and the working temperature for any particular case. In this case the basic curve is modified for simulating the 12V/5A PEM fuel cell stack.

In accordance to the PEMFC *V-I* polarization characteristic the microcontroller controls the output voltage in the relation to the output current. The control algorithm is shown in Fig. 4. The microcontroller PIC 16F877 uses a set of 35 instructions by which the control process is defined. The control program was developed using the simulation program PROTEUS PROFESSIONAL [3].

Since control circuit is almost always referenced to ground, it is necessary to have a gate drive circuit that allows the MOSFET to be isolated from the ground. This can be realized

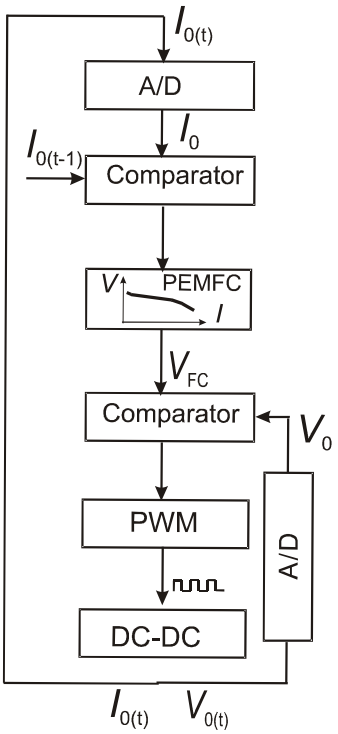


Fig. 4. Block diagram of the control algorithm.

using either optical isolation circuits or pulse transformers. In this project the optical isolation (optocoupler 4N25) is used (Fig. 5).

When the current flows through the photo-diode the photo-transistor is turned on. Consequently, the gate to source voltage rises above the threshold value and the MOSFET is turning on.

The current is measured through the voltage drop across the 0.1 Ω resistor (R_0). The voltage divider may be used to adjust the output *V-I* characteristics of the DC-DC buck converter (Fig. 6). This way, by this simulator circuit, different *V-I* characteristics may be realized in order to satisfy PEM fuel cell *V-I* characteristics for different working temperatures or pressures.

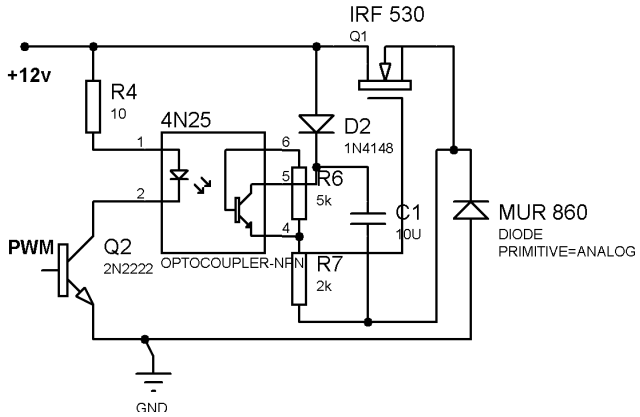


Fig. 5. Part of driving gate circuit realized with optocoupler 4N25.

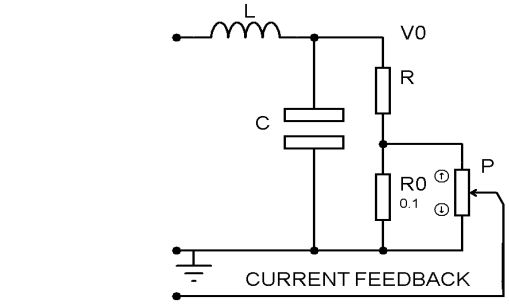


Fig. 6. Current feedback with voltage divider.

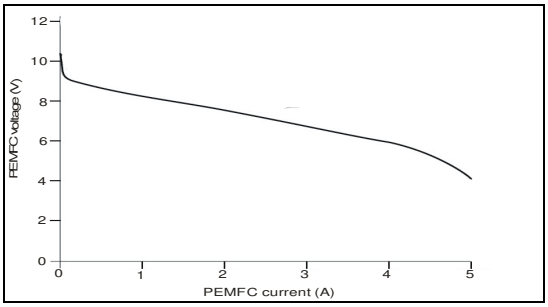
IV. Results and Discussions

The extensive experimental investigation of the proposed simulator has been performed. Here, some experimental results for simulation of a 12V/5A PEM fuel cell are presented.

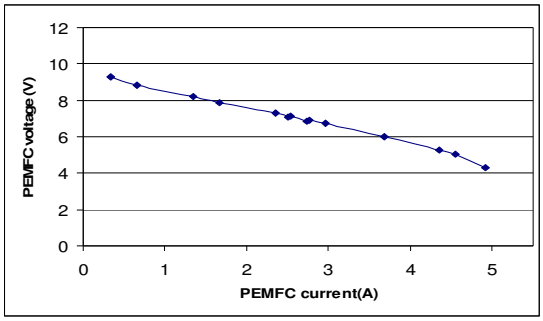
The *V-I* polarization characteristics implemented in the PIC memory was obtained by increasing the ideal stack voltage to 12 V, and the active cell area by 5 (to support the current of 5 A). These values are multiples of the initial polarization characteristics implemented in the PIC memory. This characteristic is shown in Fig. 7a).

The microcontroller PIC 16F877 is programmed according to the block diagram given in Fig. 4.

The microcontroller PIC 16F877 measures current I_0 and voltage V_0 and with the software, implemented in its memory, creates PWM pulses for driving the buck converter. The period of the PWM pulses is constant and was chosen to be 25 μs. The pulse width is controlled by the implemented polarization curve and measured values of the output current, I_0, and voltage, V_0. The output voltage varies from 12 V, at



(a)



(b)

Fig. 7. Polarization V-I curves of a 12V/5A PEMFC: (a) theoretical PEMFC curve, (b) experimental results for the realized PEMFC simulator.

system idle, to about 5 V, at rated current of 5 A. The experimentally attained *V-I* characteristics, using the proposed simulator, are shown in Fig. 7 b). It can be seen that the curves presented in Figs. 7a and 7b match very well.

Using the voltage divider in the current feedback, it is possible to obtain very quickly the *V-I* polarization characteristics for other working temperatures or pressures. An example is shown in Fig. 8.

In comparison with the real PEM fuel cell dynamic characteristics, the realized simulator has very quick transient response. By suitable programming of the microcontroller PIC 16F877 it is possible to obtain similar transient response which will correspond to that of a real PEM fuel cell.

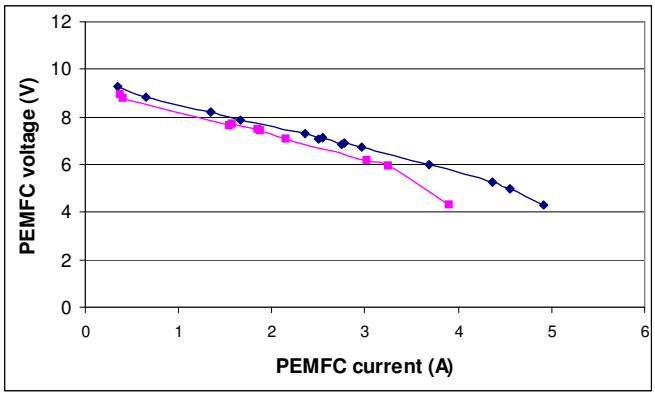


Fig. 8. Obtained V-I characteristics from the realized PEMFC simulator with the voltage divider.

V. Conclusion

The design of a PEM fuel cell simulator based on digitally controlled DC-DC buck converter is presented. The proposed simulator can be easily used in design, analyses and realization of fuel cell power systems. Due to the digital nature of the control system, it is possible to make quick changes to the mathematical model, thus avoiding as much as possible changes in the system hardware.

The hardware changes may affect only the power stage, especially when larger stuck current and/or voltage have to be obtained. The temperature and pressure characteristics can be easily implemented in the proposed simulator, either by implementing them in the control algorithm or by changing the current feedback signal using voltage divider as shown in Fig. 6.

The proposed simulator can also be used to test power systems designed to interact with PEM fuel cells, in order to prevent stack degradation caused by the electric behavior of the system. The foreseen benefits of the proposed simulator are also, the ability to work without reagents in a non-specialized environment, in a reproducible way and with faster start-up/turn-off operation.

The experimental investigations performed on the 12V/5A PEM fuel cell simulator have shown very good behavior of the proposed system and good match of the simulator output characteristics with the real PEM fuel cell polarization curve.

Acknowledgment

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Dual-Array Based MPPT for Grid-Connected Photovoltaic Systems

Darko Ostojić, Gabriele Grandi, and Darko Marčetić

***Abstract*—A novel maximum power point tracking (MPPT) algorithm for three-phase grid-connected photovoltaic (PV) generation systems is presented in this paper. Reference is made to a conversion scheme consisting in two balanced arrays of PV modules, each one feeding a standard 2-level three-phase voltage source inverter (VSI). The dc-link voltages of each VSI are regulated according with the requirement of the proposed MPPT algorithm, based on the comparison of the operating points of the two PV arrays. Inverters are connected to grid by a three-phase transformer with open-end windings configuration on inverters side. The resulting conversion structure performs as a power active filter, doubling the power capability of a single VSI, with the additional benefit of multilevel voltage waveforms. The proposed MPPT algorithm has been successfully verified by experimental tests.**

***Index Terms*—Photovoltaic power systems, multilevel inverters, maximum power point trackers.**

I. Introduction

PHOTOVOLTAIC (PV) energy sources have been initially developed for small-power and portable applications. However over the last two decades there was strong trend towards high-power plants with peak power reached 60 MW [1]]. This new field demands specific topologies and power electronic converters research, together with new control methods. Multilevel converters already applied for high-power drives are finding their way in this PV application, bringing benefits such are lower *dv/dt* and reduced harmonic distortion of the output voltage.

Another indispensable issue for PV plants is provision of maximum output power. Due to strong nonlinear characteristic of PV cell, a maximum power point tracking (MPPT) control algorithm is utilized to maximize conversion of available solar energy. A considerable number of techniques have been developed with a particular expansion in the last decade and the interest of the research community remains strong [2]. Still, different MPPT techniques suit different applications depending also on the topology and the rated power. In this paper, the dual VSI topology [3] is considered, and a novel MPPT algorithm has been applied to maximize power injection into the grid, according to the block diagram of Fig. 1. The two standard two-level VSI are connected to open-end primary windings of a standard three-phase transformer. The whole PV field is shared into two equal arrays, with each inverter directly wired with one of the PV arrays. The secondary windings are connected to the grid with a traditional star (or delta) configuration. Note that the transformer contributes with its leakage inductance to the ac-link inductance which is always necessary for the grid coupling of a VSI. Furthermore, the presence of a low-frequency transformer enable the direct connection of high power generation systems to either medium- or high-voltage grids (10 kV or more). The resulting three-phase converter is able to operate as a voltage multilevel inverter, equivalent to a three-level inverter, with corresponding multilevel benefits.

Strictly speaking, only permanent sweeping of the V-I characteristic can determine exact position of the MPP in every instant for all the circumstances (different irradiance, shading and temperature). However, this mode of constant perturbation is unacceptable for application, leading to development of many "approximate" methods today commonly accepted under name MPPT. It can be noted that "sweep" can represent the appropriate method in some cases (e.g. for low-power applications if performed in regular and not so often intervals) [3]. Generally, methods can be divided in two classes, based on type of the applied loop.

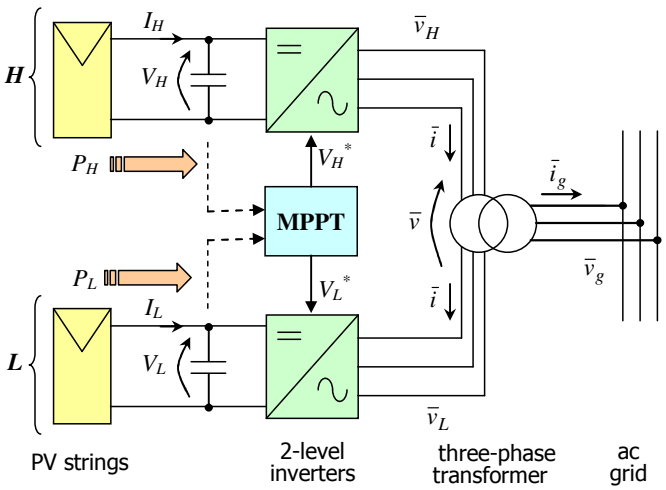

Fig. 1. Block diagram of the dual VSI topology including an open-winding three-phase transformer.

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1) Open loop control, using *a priori* model of the panel behavior (usually eventually updated). Basic representatives are
   - application of pilot cells [2],
   - open-circuit voltage/short-circuit current based methods [4],
   - model (parameter) based methods [5], particularly "one cycle control" [6].
2) Closed loop control, since they compare the current state with previous in order to determine position of the MPP. Basic representatives are
   - perturb and observe (P&O, sometimes called "hill climbing") [7],
   - incremental conductance (INC) [8],
   - fuzzy logic and Neural network [9], [10],
   - ripple correlation control (RCC) [11],
   - load current/voltage maximization [12],
   - sliding mode control [13].

Among all the methods most of the focus has been on P&O and INC method. They practically established themselves as almost standard methods due to their simplicity and ease of application. Other methods such are fuzzy logic and neural networks are more complex to implement and require field-specific tuning. P&O usually uses PV power, but it has been shown that output electric parameters of the converter can be used as well [12]. The MPPT algorithm proposed in this paper is based on a forced small displacement in the working points of two identical PV arrays, allowing sharing of data between them on the basis of instantaneous currents measurement. Similar MPPT schemes have been recently presented in [14] and [15], but with reference to different PV conversion structures.

II. Converter and Control System

In the present case of PV applications, the proper inverter dc voltage range can be obtained by adjusting the number of series-connected modules for each PV array (string), avoiding the use of intermediate dc/dc choppers. In this case, inverters regulate dc-bus voltages according to the MPPT requirements, as explained in the following. With reference to the scheme of Fig. 1, using space vector representation, the output voltage vector of the multi-level converter is given by the contribution of the voltage vectors and , generated by inverter H and L respectively,

$$\overline{v} = \overline{v}_H + \overline{v}_L \tag{1}$$

$$\overline{v}_H = (2/3)V_H(S_{1H} + S_{2H}e^{j2\pi/3} + S_{3H}e^{j\pi 4/3}) \tag{2}$$

$$\overline{v}_L = -(2/3)V_L(S_{1L} + S_{2L}e^{j2\pi/3} + S_{3L}e^{j4\pi/3}) \tag{3}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverter legs [16]. Fig. 2 shows the corresponding voltage space vectors.

The conversion system is symmetric, having both inverters with equal ratings and two equal groups (arrays) of PV modules supplying them. The dc bus voltage references

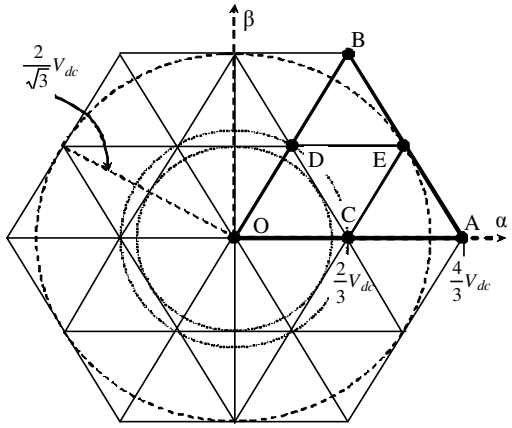


Fig. 2. Dual inverter voltage vector plot in case $V_H = V_L = V_{dc}$.

generated by the MPPT controller, V_H* and V_L*, are very close one to the other, as discussed in the next section. Two distinct voltage controllers have been implemented, according with the block diagram shown in Fig. 3. In particular, the two dc voltages (V_H, V_L) are regulated by two controllers, here called "sigma" (Σ) and "delta" (Δ). The voltage controller Σ acts in order to regulate the average value of dc bus voltages, V_{dc} (i.e., their sum), whereas the voltage controller Δ acts in order to set the difference between the dc bus voltages (ΔV). The input signals of both voltage controllers, V_Σ and V_Δ, can be built by adding and subtracting one from the other the individual dc voltage errors ΔV_H and ΔV_L, as follows

$$V_\Sigma = \Delta V_H + \Delta V_L = (V_H + V_L) - (V_H^* + V_L^*) \tag{4}$$

$$V_\Delta = \Delta V_H - \Delta V_L = (V_H - V_L) - (V_H^* - V_L^*) \tag{5}$$

being:

$$\begin{cases} \Delta V_L = V_L - V_L^* \\ \Delta V_H = V_H - V_H^*. \end{cases} \tag{6}$$

The voltage controller Σ directly generates the current reference for the dual inverter, I^*, corresponding to the active power injected into the grid, regardless to the power sharing between the two inverters "H" and "L", as shown in Fig. 3. If the ac current is in phase with the grid voltage, the resulting current space vector reference is

$$\overline{i}^* = I^* \hat{v}_g \tag{7}$$

being $\hat{v}_g$ the unity space vector of the grid voltage. It can be noted that reactive and/or harmonic compensation current references can be included in (7) if active power filter operation is required.

To solve the problem of current control in grid-connected application a simple proportional controller with a feed-forward action (grid voltage) has been adopted, due to its simplicity, good dynamic response and immunity to harmonic disturbance. In particular, the reference voltage is calculated as

$$\overline{v}^* = K_c(\overline{i}^* - \overline{i}) + \overline{v}_g' \tag{8}$$

being $\overline{v}_g'$ the space vector of the grid voltage at the inverter side.

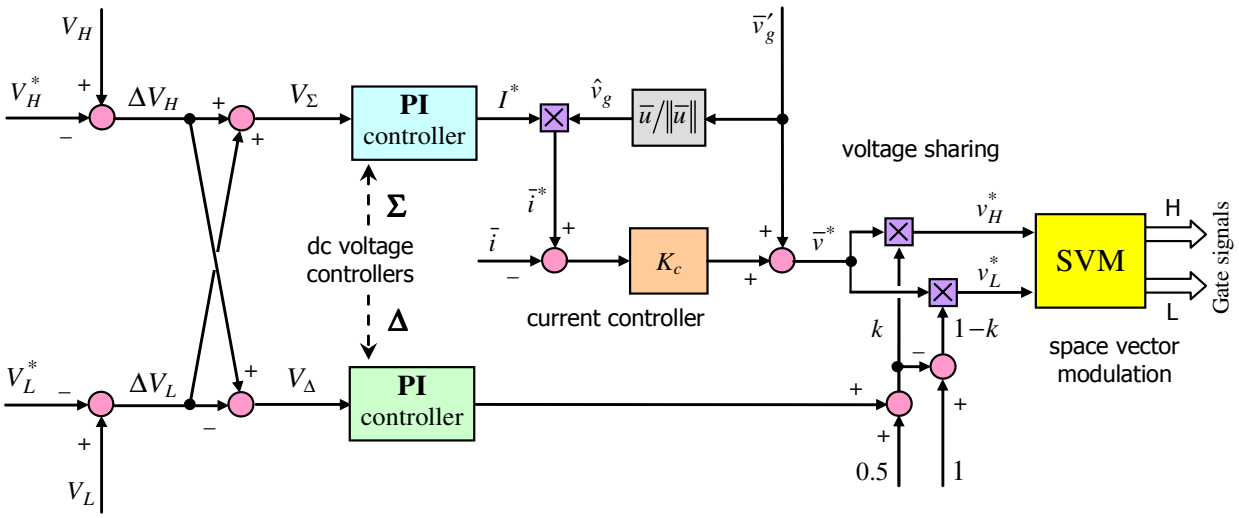


Fig. 3. Schematic diagram of proposed control system.

Being the converter supplied by two distinct PV arrays, it is necessary to regulate the power flow from the two sources. A possible approach to achieve the power sharing control is to define the decomposition of the total reference into two collinear vectors [3]:

$$\begin{cases} \bar{v}_H^* = k\,\bar{v}^* \\ \bar{v}_L^* = (1-k)\,\bar{v}^*. \end{cases} \tag{9}$$

The condition (9) allows maximum dc voltage utilization. Being the output ac current of the two inverters the same, the coefficient k also defines the power sharing between the two inverters. In terms of averaged values within the switching period, the output power can be expressed as

$$p = \frac{3}{2}\bar{v}^*\bar{i} = p_H + p_L \tag{10}$$

where p_H and p_L are the individual powers from the two inverters. By combining (9) with (10) leads to

$$\begin{cases} p_H = \frac{3}{2}\bar{v}_H^* \cdot \bar{i} = k\,p \\ p_L = \frac{3}{2}\bar{v}_L^* \cdot \bar{i} = (1-k)\,p. \end{cases} \tag{11}$$

Once the inverter reference voltages $\bar{v}_H^*$ and $\bar{v}_L^*$ are determined by (9), they must be synthesized by the dual two-level inverter and applied to the open-end windings of the transformer. A SVM providing proper voltage multilevel waveforms and avoiding double simultaneous commutations have been presented in [16]. This method leads to switching sequences that can be implemented in the sole PWM generation unit of an industrial DSP which usually provides a unique carrier for all three phases. It has been achieved by introducing asymmetrical PWM pattern to avoid different carriers. This new algorithm has been adopted here.

III. Proposed MPPT Algorithm

The well-known problem of the maximum power point tracking consists in finding the MPP voltage, V_{MPP} (or the MPP current, I_{MPP}), at which the PV field provides the maximum output power, P_{MPP}. MPP continuously moves, according to variations in environmental conditions (i.e. solar irradiation and cell temperature). Among the numerous known solutions [2], [4]–[15], the one proposed in [14], [15] is particularly suitable for the dual inverter configuration, due to the presence of two identical groups of PV modules. The algorithm is based on deliberate introduction of a small difference ΔV^* (in the order of %) between reference voltages of the two PV fields V_H^* and V_L^*, as follows

$$V_L^* = K_v\,V_H^* \tag{12}$$

$$\Delta V^* = V_H^* - V_L^* = (1-K_v)\,V_H^* \tag{13}$$

where the coefficient K_v slightly differs from 1 ($K_v \cong 0.95$-0.98). Due to the particular shape of power vs. voltage characteristic (P-V curve), the powers generated by the two PV fields, P_L and P_H, practically coincide if the operating points are on the "flat" in neighborhood of MPP, according to Fig. 4a. Conversely, on "sloped" parts of the P-V curve, one of the powers is higher than the other, or vice-versa, depending on the position of the operating points with respect to the MPP. In particular, the following three possibilities occur:

$$\begin{cases} P_L < P_H \;\Rightarrow\; V < V_{MPP} \\ P_L = P_H \;\Rightarrow\; V \cong V_{MPP} \\ P_L > P_H \;\Rightarrow\; V > V_{MPP}. \end{cases} \tag{14}$$

In effect, the difference between P_H and P_L gives an estimation of the slope of the P-V characteristic:

$$\frac{dP}{dV} \cong \frac{P_H - P_L}{(1-K_v)V_H} \cong K_p\left(P_H - P_L\right). \tag{15}$$

Hence, reference dc voltages V_H^* and V_L^* can be found as the output of a simple PI-controller acting on the error between the two powers, as represented in Fig. 4b.

The choice of a proper value for K_v is a tradeoff between efficiency, which is higher as K_v approaches 1, and immunity to both noise and PV modules asymmetry, which increase as

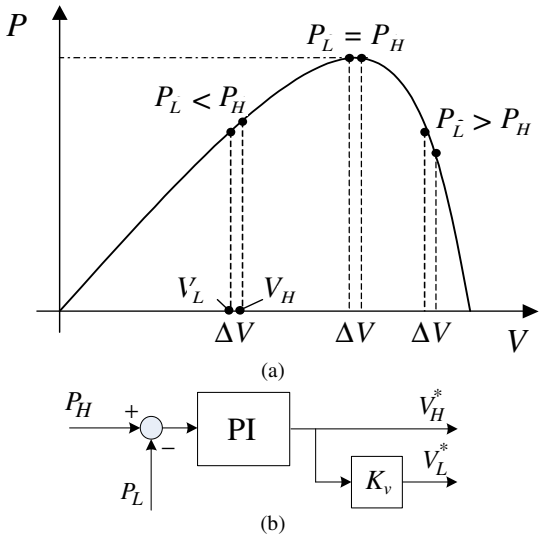


Fig. 4. Principle of MPPT algorithm: (a) P-V diagram, (b) control scheme.

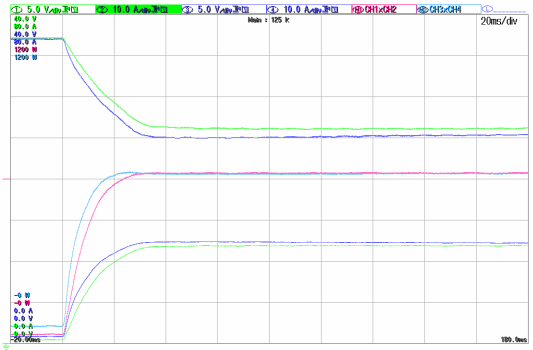
K_v diverge from 1. Obviously, the proposed algorithm is based on the assumption that the two PV arrays have the same P-V (or I-V) characteristic. For this reason, the PV arrays should consist of equal number and same type of PV modules. In spite of P-V characteristics of two identical PV modules slightly differ one from the other (the dispersion is in the order of few %), when many PV modules are arranged in two big arrays, their global P-V characteristics are averaged and practically coincides. On the basis of (2) and (3), the effects of PI regulators Σ and Δ lead to the following steady-state conditions

$$V_\Sigma = 0 \;\Rightarrow\; V_H + V_L = V_H^* + V_L^* \tag{16}$$

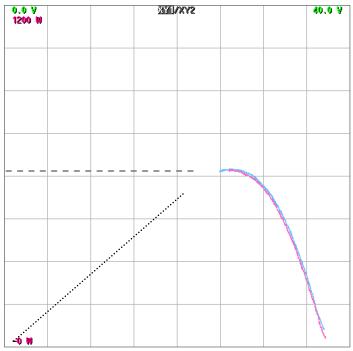
$$V_\Delta = 0 \;\Rightarrow\; V_H - V_L = \Delta V^* . \tag{17}$$

IV. Experimental Results

To ensure the safety, the system has been implemented by using only parallel connections of PV modules, since the presence of a grid-transformer with the proper turn ratio



(a) V_H, V_L (5 V/div, top), P_L, P_H (150 W/div, middle), I_L, I_H (10 A/div, bottom)



(b) P_L vs. V_L and P_H vs. V_H (5 V/div, 150 W/div)

Fig. 6. Experimental results: transient from no-load to MPP with Kv =0.98.

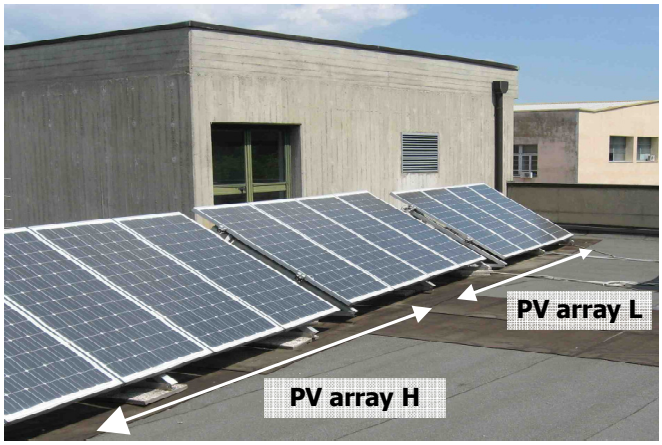
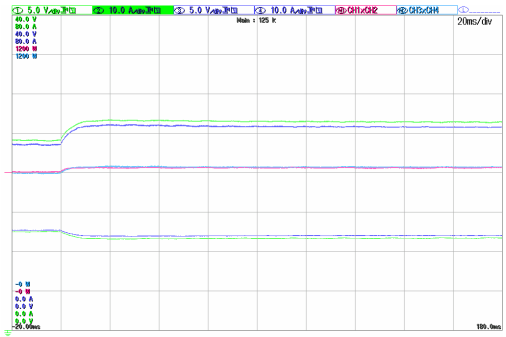


Fig. 5. Arrangement of 6+6 PV modules on the roof.

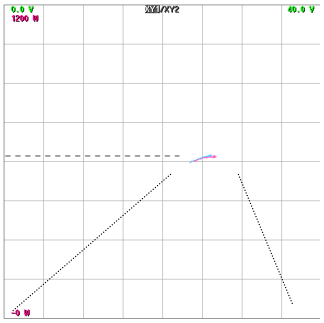
enables voltage adaptation. The resulting PV array voltage range is the same of a single PV module, in the range 20–40 V, allowing use of low-voltage MOSFETs. These types of switches are cheap, being widely used in automotive applications, and they feature good efficiency, since its on-state resistance is a strong decreasing function of the blocking voltage rating. The main characteristics of the whole PV generation system prototype are summarized in Table I, and some pictures of the experimental set-up are given in Fig. 5. Reference is made to the scheme presented in Fig. 1, with the two PV arrays consisting each in six PV modules in parallel, directly connected to the inverters. The experimental results show the action of the MPPT controller with reference to opposite voltage starting conditions with respect to the MPP voltage (V_{MPP}). In all experiments a coefficient K_v = 0.98 has been selected, leading to a small difference between V_H and V_L, about 0.5 V.

Fig. 6 shows the transient to the MPP starting from the open-circuit voltage (Fig. 6a in time domain, Fig. 6b in I-V diagram).

Fig. 7 shows the transient to the MPP starting from the minimum dc voltage. Steady states and settling times are proving that also with a very small voltage displacement a



(a) V_H, V_L (5 V/div, top), P_L, P_H (150 W/div, middle), I_L, I_H (10 A/div, bottom)



(b) P_L vs. V_L and P_H vs. V_H (5 V/div, 150 W/div)

Fig. 7. Experimental results: transient from minimum dc voltage to MPP with Kv =0.98.

satisfactory behavior of the MPPT algorithm can be obtained, reached without oscillations in about 40 ms. In all the examined cases, both the steady-state powers PH and PL practically coincide with the MPP, proving the effectiveness of the proposed MPPT algorithm.

TABLE I
MAIN PARAMETERS OF THE CONVERTER

INVERTERS	
configuration (H and L)	two-level VSI
MOSFETs (6 in parallel per switch)	IRF2807
MOSFETs ratings	V_{DSS}=75[V]; R_{DS}=13[mΩ]
dc-bus capacitance	23 [mF]
switching frequency	20 [kHz]
TRANSFORMER and GRID	
turn ratio	230/24 [V/V]
converter/grid-side winding connection	open ends/star
rated power	1500 [VA]
short circuit voltage	6.9 [%]
ac link inductance (converter side)	0.4 [mH]
grid voltage (line-to-line), frequency	250 [V], 50 [Hz]

V. CONCLUSION

The MPPT algorithm proposed in this paper is based on the comparison of the operating points of two PV arrays, each one directly connected to a standard 2-level three-phase inverter. This method shows good results applying considerably low difference between the two PV array voltages. The coefficient K_v represents a degree of freedom that can be tuned depending on different conditions or demanded dynamic response. It is suitable for application for high-power applications where V-I characteristics of two groups are expected to be quite similar by the law of large numbers. The measuring system might require initial tuning (calibration). The case of different characteristics due to partial shadowing is not of importance for high-power application since the installation is projected to avoid such a problem.

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Analytical Modeling of Quantum Mechanical Tunneling in Germanium Nano-MOSFETs

Amit Chaudhry and Jatinder N. Roy

***Abstract*—In this paper, a simple analytical model has been developed to study gate oxide tunneling in a germanium substrate MOSFET including the inversion layer quantization effects in the substrate. The model has been developed using the WKB approach. Explicit continuous surface potential model has been used to increase the accuracy of the developed tunneling model. High-k dielectrics HfAlO, GeON and HfO2 to reduce the gate oxide tunneling have also been studied. The results have also been compared with the numerically reported results. The results compare well with the existing reported work.**

***Index Terms*—WKB, energy quantization, dielectric, tunneling, EOT.**

I. Introduction

As Complementary Metal Oxide Semiconductor (CMOS) technology scales down aggressively, it approaches a point, where classical physics is not sufficient to explain the behavior of a MOSFET. Due to extremely thin oxide and high doping concentration very high electrical fields at the oxide/substrate interface occur. This results in the charge carriers occupying quantized two-dimensional sub-bands which behave differently from the classical three dimensional case. Simple analytical models of the MOSFETs including quantum mechanical effects (QME) are needed for computer-aided design of digital and analog integrated circuits at nanometer scale containing thousands to millions transistors on a silicon chip. To model a MOSFET in the presence of QME, the quantization of energy levels in the direction perpendicular to the oxide/silicon substrate interface, the quantum mechanical charge carrier density directly tunneling from in the gate oxide need to be properly understood and studied.

The paper is organized as follows: The paper starts with an overview of the compact MOSFET models. Secondly, study and modeling of energy quantization effect has been done for germanium substrates and its impact has been studied on inversion charge density of the nanoscale MOSFET . Thirdly, a quantum mechanical direct tunneling due to the scaling down of the oxide thickness to angstrom levels has been studied. The possible solution to the tunneling gate currents is the use of high dielectric constant materials. Some alternate dielectrics have also been studied.

II. MOSFET Models

The charge based models include the basic SPICE (Simulation Program with Integrated Circuit Emphasis) Level 1, Level 2, Level 3, BSIM (Berkeley Short Channel Insulated gate Field effect transistor model) models, and the other advanced models such as BSIM 4 and 5 [1]–[5]. Secondly, the potential based models include the SP (Surface Potential) model, MOS Model 11, HiSIM (Hiroshima Starc Insulated gate Field effect transistor model) model etc. [6]–[9] and thirdly, the conductance based models like the EKV(Enz, Krummenacher, Wittoz) model [10]. In the modeling research area, attempts are being made to include the QME in these standard models also. The other models which include the energy quantization effects though empirical in nature are hanoch model [11], van Dort model [11], inversion charge model [12] etc. In all these above models silicon substrate MOSFETs may have been discussed but quantum mechanical effects in germanium MOSFETs have not been studied.

III. Inversion Layer Quantization in Germanium Substrate

The research in the area of Energy Quantization started in the early 1950s. The research [13]–[17] mainly focused on only calculating the inversion charge density in the presence of energy quantization effects using variation approach in the MOSFET. The use of such techniques required the calculation of surface potentials at the interface of silicon and its oxide. The lack of availability or slow development of surface potential models six decades ago, never allowed the growth of research in the area of modeling QME in MOSFETs. But as the MOSFETs are being scaled down to the nm scale, the need of research has risen, to analytically model the QME in MOSFETs. Various models have been developed already to study silicon substrates at the nanometer scale but very less research has taken place in Ge substrates at the nanometer scale. Whatever models developed so far for Ge are either numerical or are empirical [18].

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The germanium MOSFET electrostatics is evaluated using the variation approach to find the shift in the energy bandgap of the Ge-MOSFET.

Solving the Poisson equation in the inverted channel, we get the total charge density Q_s.

$$Q_s = -\left(2qN_a\varepsilon_{Si}\varepsilon_0\right)^{1/2}\left[\varphi_s + V_t e^{-\frac{2\varphi_f}{V_t}}\left(e^{\frac{\varphi_s}{V_t}} - 1\right)\right]^{1/2}. \quad (1)$$

Similarly, the depletion charge Q_b is approximated as

$$Q_b = -\left(2\varepsilon_{Si}\varepsilon_0 qN_a\varphi_s\right)^{1/2}. \quad (2)$$

Therefore, the inversion charge density Q_{inv} is given by (1)-(2):

$$Q_{inv} = -\gamma C_{ox}\left[\left\{\varphi_s + \frac{kT}{q}e^{\frac{q(\varphi_s - 2\varphi_f)}{kT}}\right\}^{1/2} - \left(\varphi_s\right)^{1/2}\right] \quad (3)$$

where γ – body effect parameter, C_{ox} – oxide capacitance, φ_s – surface potential, φ_f – Fermi potential, N_a – substrate concentration, $V_t = kT/q$ – thermal voltage.

The main problem with (3) is that the surface potential has to be evaluated explicitly in all the regions of inversion and then only, the (3) can be solved. An explicit solution has been evaluated in the [19]. The widening of the energy bandgap is analytically modeled as for both silicon and germanium substrates.

The wave function solution of the Schrödinger's equation is given using variation approach is [13]

$$\Psi(x) = \frac{b^{3/2}x}{\sqrt{2}}\exp\left(-\frac{bx}{2}\right) \quad (4)$$

where b is a constant given by

$$b = \left[\frac{48\pi^2 m^* q^2}{\varepsilon_{Ge}\varepsilon_0 h^2}\left(0.33Q_{inv} + Q_{dep}\right)\right]^{1/3} \quad (4a)$$

where;

m^* – effective Quantization mass

ε_{Ge} – relative permitivity of Germanium.

The corresponding shift in the energy [13] is given by

$$E_0 = \frac{3h^2b^2}{8m^*}. \quad (5)$$

The shift in the surface potential is equal

$$E_0 / q. \quad (6)$$

The effective quantization masses in the longitudinal direction for the Si and Ge substrates, is shown in Table I. The Ge electron effective quantization mass is smaller in L valley (The ground state of the quantized energy level in Ge) than the silicon electron quantization effective mass in Δ_2 valley (the least energy state in the silicon).

TABLE I
VARIOUS PARAMETERS IN SILICON AND GERMANIUM FOR ELECTRONS [18]

Material	Quantization Mass	E_g(eV)	Relative permitivity ε_r	Intrinsic carrier concent. /m^3
Si <100>	$0.98m_o$ at the lowest state: Δ_2 valley	1.12	11.2	$1.3\text{x}10^{16}$
Ge <100>	$0.12m_o$ at the lowest state: L valley	0.67	16	$2.5\text{x}10^{19}$

A. Surface Potential in the Substrate Channel

The potential-based models are more physics-based, and are therefore, more accurate. However, a major disadvantage of the potential based models is that potential is related to the MOSFET terminal voltages such as gate voltage or drain voltage by an implicit relation that needs to be solved iteratively, incurring expensive computation time. By solving the Poisson's equation in the substrate, the surface potential is obtained as:

$$\varphi_s = \left(2qN_b/\varepsilon_0\varepsilon_{Si}\right)^{1/2}\left[\varphi_s + V_t e^{-2\varphi f/V_t}\left(e^{\varphi_s/V_t} - 1\right)\right]^{1/2} \quad (7)$$

The analytical explicit surface potential model in the absence of drain and body bias has been reported in [19].

$$\varphi_s = f + a \quad (8)$$

where

$$f = \varphi_f + 0.5\varphi_{swi} - 0.5\left[\left\{\left(\varphi_{swi} - 2\varphi_f\right)^2 + 0.0016\right\}^{1/2}\right] \quad (9)$$

$$a = 0.025\ln\left[\left\{x - y\left(1 + 100y^2\right)^{-1/2}\right\}^2\left(0.16\gamma\right)^{-2} - 40f + 1\right] \quad (10)$$

and

$$\varphi_{swi} = \left\{\left(V_{gs} - V_{fb} + 0.25\gamma^2\right)^{1/2} - 0.5\gamma\right\}^2 \quad (11)$$

is the weak inversion surface potential, where $x = V_{gs} - V_{fb} - f$ and $y = \varphi_{swi} - f$.

Using the surface potential model (8) in (1) and (2) , we can calculate explicitly depletion charge density and inversion charge density, and then using (1) and (2) in (6), the shift in the surface potential due to energy quantization effect can be evaluated.

Equation (6) obtained from (4a) is then included in the explicit surface potential expression given by [19] and total surface potential in the presence of QME and hence the quantum inversion density is obtained after one iteration.

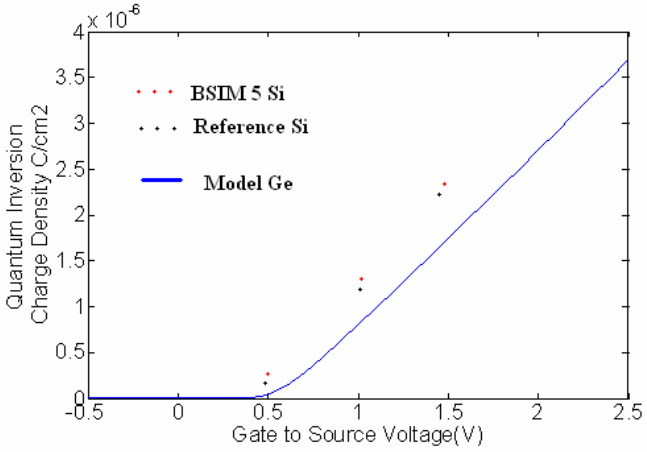

Fig. 1. Simulated results of quantum mechanical inversion charge density using variation approach for Ge-MOSFET.

The results in Fig. 1 show a reduced inversion charge density in Ge as compared to Si. The reduced electron mass in germanium has resulted in reduced inversion charge densities in the channel showing that the energy quantization is more severe in germanium than in silicon. The corresponding results of silicon reference [20] and the BSIM 5 are also reported for comparison [21]. It is also observed that at higher gate voltages, the inversion charge density in germanium reduces further predicting more severe energy quantization at higher gate voltages due to more pronounced energy bandgap widening.

IV. Gate Oxide Tunneling

In extremely scaled oxides, the charge carriers in the inverted channel directly tunnel into the gate oxide. A model has been developed which describes the gate oxide tunneling using the WKB (Wentzel-Krammers-Brillouin) approach [22, 23] including energy quantization effect. The direct tunneling current is calculated using the tunneling parameters listed in Table II. Calculated electron tunneling current in both Si and Ge NMOS with HfO_2 gate dielectric is shown in Fig. 2.

To avoid tunneling in the gate oxide, instead of using GEON, high-k (dielectric constant) gate insulators such as HfO_2 (Hafnium oxide) and HfAlO (Hafnium aluminum oxide) have been used and the leakage currents in these dielectrics have also been modeled using the parameters in Table II as shown in Figs. 2 and 3.

The main issue in the current density calculation is transmission probability *T(E)*. The general expression for the transmission probability is given by [22]:

$$T(E) = \exp\left[-2\int_{x_1}^{x_2} |k(x)|\,dx\right] \tag{12}$$

where *k(x)*, wave factor, is given by $\left[2m_{ox}\frac{V(x)-E}{\hbar^2}\right]^{1/2}$,

where m_{ox} $=0.5m_o$ is the effective electron mass in the oxide [18] and $0.32m_o$ in silicon oxide [24]. $\hbar$ – effective Planck's constant.

The direct tunneling current density in the gate oxide is given as [23]

TABLE II
Various Parameters to be Considered to Model High Dielectric Constant MOSFET Tunneling Phenomenon [18]

Material Parameters	HfAlO	GeON	HfO_2	SiO_2
Barrier Height (V) eV (χ)	2.0	1.5	1.9	3.1
Effective Mass of electrons in the dielectric, m_o=electron free mass	$0.21m_o$	$0.5m_o$	$0.18m_o$	$0.32m_o$
Relative permittivity	18.4	4.8	22	3.9

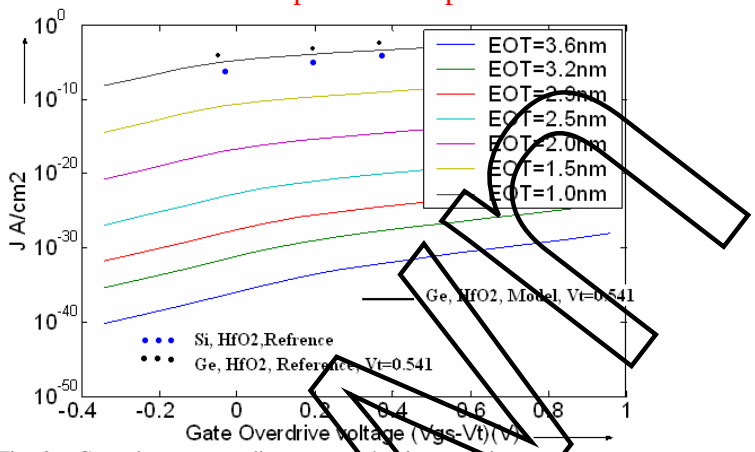

Fig. 2. Gate electron tunneling current density at various gate to source voltages (V_{gs}=0.2–1.5 V) in case of HfO_2 as an insulator at N_b=1x10^{18} /cm^3 when EOT is varying from 3.6, 3.2, 2.9, 2.5, 2.0, 1.5, and 1.0 nm (V_t is threshold voltage calculated for Ge in the presence of energy quantization) [18].

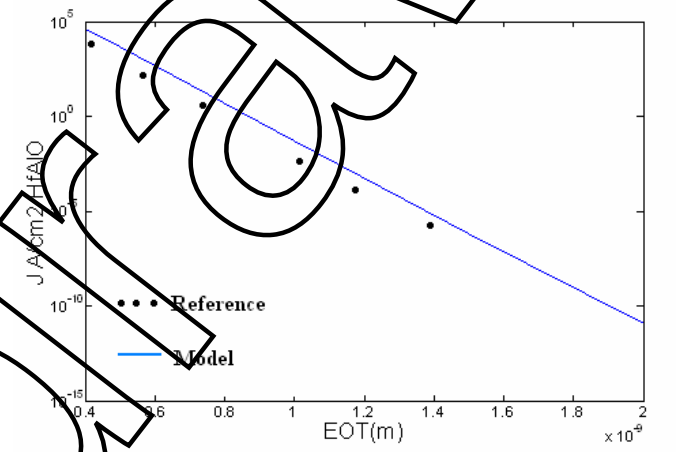

Fig. 3. Gate electron tunneling current density at various gate to source voltages (V_{gs}=1.5 V) in case of HfAlO dielectric as an insulator at N_b=1x10^{18} /cm^3 [18].

$$J_T = \frac{4\pi m_t q}{h^3}\int_0^V \left\{\int_0^\infty [f_S(E) - f_G(E)]\,dE_t\right\} T(E_S)\,dE_x \tag{13}$$

where:

$f_S(E)$ – electron distribution at the Source/Substrate interface:

$$f_S(E) = \left[1 + \frac{\exp(E - E_{fS})}{kT}\right]^{-1} \tag{14}$$

$f_G(E)$ – electron distribution at the Drain/Substrate interface:

$$f_G(E) = \left[1 + \frac{\exp(E - E_{fG})}{kT}\right]^{-1} \tag{15}$$

E_{fs} – Fermi Energy at the Source

E_{fd} – Fermi Energy at the Drain

E – total energy of the electrons

E_x – energy in the direction of tunneling i.e. from source to drain

E_t – energy in the transverse direction

m_t – electron transverse mass in Ge = $0.30m_o$ [18].

Using (12) and (13), the tunneling current density can be calculated.

In Fig. 2, the Ge-MOSFET exhibits considerably higher leakage current than Si MOSFET under same conditions. This is due to the stronger energy quantization in Ge as compared to Si. This is one of the most serious obstacles in scaling the Ge-MOS devices. The results in Fig. 2, show that for gate voltage equal to 1.5 V, and the dielectric as HfAlO, the tunneling current falls as the EOT increases. All the results match quite closely with the results reported in [18].

V. Conclusion

In this paper, a model has been developed for the quantum mechanical tunneling in the nanometer scale Ge-MOSFET. High-dielectric constant materials reduce the gate tunneling currents. A stronger energy quantization is found in Ge than in Si as the lower valleys in Ge are at a higher energy than Si. Though Ge, promises a better future than Si owing to its higher carrier mobility, yet its usage as replacement to Si at nanoscale is still under question due to the above limitations which need to be properly understood and possible solutions to be found out at all levels of research in this area.

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Hardware Based Strategies Against Side-Channel-Attack Implemented in WDDL

Milena J. Stanojlović and Predrag M. Petković

***Abstract*—This contribution discusses cryptographic algorithm in hardware that protects the information leaks out of the device through so called „side channels". Attacks on crypto-processors are based on analyses of the leaked data are known as side-channel attacks (SCA). Important information, such as secret keys, can be obtained by observing the power consumption, the electromagnetic radiation, the timing information etc. There are several types of protection and some will be discussed in this paper. Special attention is paid to Wave Dynamic Differential Logic (WDDL) that was evaluated in terms of load symmetry on an example.**

***Index Terms*—Side channel attack, wave dynamic differential logic.**

I. Introduction

DATA security becomes very important issue in everyday life. Starting from credit cards, coded alarm systems to all types of cipher-protected data transfer it is necessary to hide code keys from unauthorized misuse. The first defending line is using complex multi-bit ciphers. Crushing them by simple software tools based on proper combination search become very time-consuming. Longer password and more sophisticated coding algorithms result to the bigger number of combinations and therefore the better protection. One can say that the problem of data protection could be solved just by increasing the number of combinations. However, the value of encrypted data enormously increases. This inspires potential attackers to invest more money and brainstorm in order to crack cipher. It has been shown in [1] that monitoring power helps a lot in finding cipher. Thereafter other methods emerged that make cipher cracking easier. Some of them are Simple Power Analysis (SPA), Differential Power Analysis (DPA) and Electromagnetic Analysis (EMA) [2]. Common to all these methods is analysis of information that leaks from physically implemented hardware. They can be collected only if somebody intentionally uses sophisticated probes to attack crypto-processor. Therefore they are named side channel attack. There are different attack tactics like Fault induction attack, Timing attack, Probing attack [2].

The scientific community responses with new hardware and software based countermeasures.

The aim of this paper is to enlighten some strategies in fighting against SCA. Especially authors are interested in protecting data from power-meters during automatic meter reading [3]. It is expected that new solid-state power-meter designed as ASIC in Laboratory for Electronic Design Automation at University of Niš, comprise a communication block resistible to SCA. Therefore it is desirable to fight against SCA within standard CMOS technology and preferably using standard cell library. With that aim *Wave Dynamic Differential Logic* (WDDL) [4] is in scope of our interest and it will be discussed from implementation point of view. Our goal is to determine the permitted amount of load mismatch that still guarantees resistivity to DPA attack and to observe effects of V_{DD} faults on vulnerability of WDDL.

The paper is organized as follows. The subsequent section gives a brief survey of countermeasures. The third section presents basics of WDDL. Influence of unsymmetrical load of a WDDL cell to the SCA resistivity is described on example of AND gate in the fourth section together with simulation results. The fifth section considers influence of faults made by attacker to the crypto-processor with WDDL cells.

II. Strategies against SCA

Although power analysis and EMA requires using different type of probes the source of data leakage is common in both cases. The leakage is the consequence of changes in I_{DD} during logic state transitions. Each change 0-1 requires additional charge to be passed from bias to the output capacitance. In contrary change 1-0 discharges load and no current flows from V_{DD}. The amount of the additional charge is proportional to the number of capacitors being charged. For one who has elementary knowledge of digital cell circuitry this is valuable information that helps him to get the figure about transitions inside IC. Therefore, digital signal tracking supported with monitoring I_{DD} becomes powerful tool for discovering digital circuit behavior.

All strategies in fighting against leaking data through power changes relay on hiding correlation between the logic state changes and the waveform of power. Depending on the level where performed they can be sorted as measures at

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architectural, algorithmic or gate level.

In scope of methodology they can be categorized as *randomizing*, *masking* and *blinding*.

Randomizing at algorithmic level relies on frequently change of secret key to avoid possibility of finding the correlation.

Masking techniques require additional logic operations to cover real data. It is possible to perform them on algorithmic level and on the gate level, as well. However, higher order power analyses are able to crack masking.

Blinding makes power consumption of a cell independent on data flow. Basically there are two ways to make power consumption of a cell independent on data flow:

- to keep constant power consumption all the time (by inserting analog modules but the overall consumption of power is considerably high);
- to force all digital cells to have the same power pattern for every logic change.

The second class of methods is known as Dual-rail with Precharge Logic (DPL) [5]. All signals are duplicated and have true and false representations. The cells operate in alternated pre-charge and evaluation phases to ensure exactly one switching event per cycle. Wave Dynamic Differential Logic (WDDL) [4] is good representative of DPL. It can be implemented with standard CMOS cells and therefore it is good candidate for implementation in standard ASIC technologies.

III. WAVE DYNAMIC DIFFERENTIAL LOGIC

The main purpose of a WDDL cell is to provide uncorrelated power consumption to the operated data. Therefore it should have the same number of transitions for every combination of input signals. In case of inverter it means that every change on input must have the same contribution to I_{DD}. This is possible if inverter is realized with two standard invertors (connected to the same V_{DD}) as Fig. 1a shows.

Indexes *t* and *f* denotes true and fault signals, respectively. Knowing that $\mathbf{a_f}$=NOT($\mathbf{a_t}$) it is obvious that for same load on outputs y_t and y_f, any change on $\mathbf{a}=\mathbf{a_t}$ will produce the same I_{DD}.

However, for other types of cells it is not sufficient to have duplicated hardware. Each cell should have own dual cell. This means that for every $\mathbf{y_t}=\mathbf{a_t}$ ¤ $\mathbf{b_t}$ the complement output is needed such as $\mathbf{y_f}$=NOT($\mathbf{y_t}$)=NOT($\mathbf{a_t}$) * NOT($\mathbf{b_t}$). Note that ¤ and * denote different (complementary) operators. For AND operator OR is complementary and vice versa. Fig. 2 represents symbol and circuitry of WDDL AND cell.

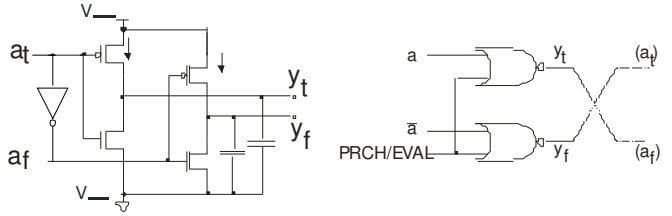
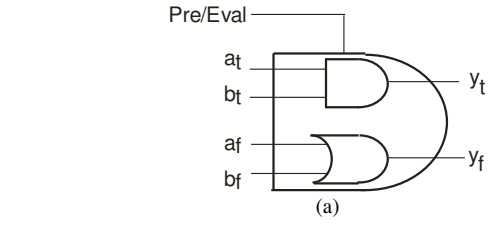


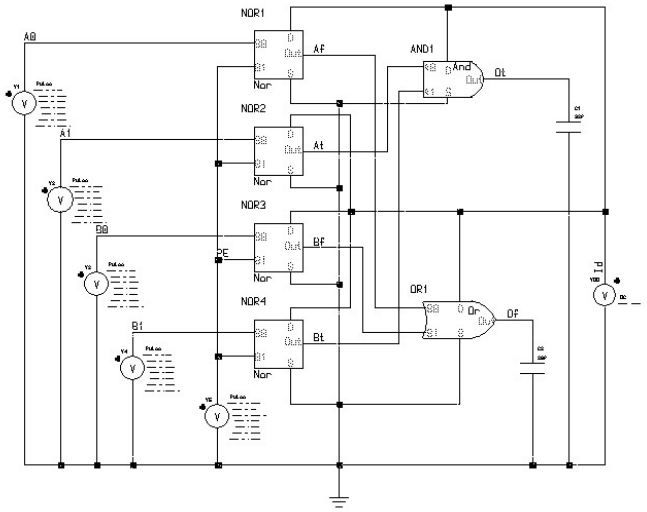
Fig. 1. WDDL inverter.

In order to provide the same I_{DD} for every input change, combinational cells should work in two phases. During *pre-charge* phase all signals are forced to the low logic level. Thereafter, in *evaluating* phase outputs establish the proper values. Hence, the inverter cell is not realized as in Fig. 2a but rather as shown in Fig. 2b. The same architecture is used to generate waveforms of true and false signals that drive WDDL operators ($\mathbf{a_t}$ and $\mathbf{a_f}$ from **a** signal and $\mathbf{b_t}$ and $\mathbf{b_f}$ from **b** signal).

Fig. 3 shows waveforms of controlling Precharge/Evaluation signal and all input and output signals for the case that corresponds to the single-rail AND cell stimulated with patterns **a**=1, **b**=0 and **a**=1, **b**=1.



(a)



(b)

Fig. 2. WDDL AND cell (a) symbol, (b) circuitry.

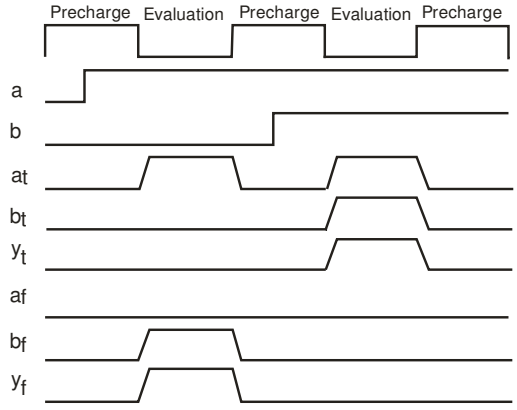


Fig. 3. Waveforms at ports of WDDL AND cell.

During pre-charge phase all signals are set to low level. During evaluating phase only exactly one of outputs goes to the high level. Therefore only one load capacitance will charge from V_{DD}.

If input signals come in slightly different moment WDDL architecture implemented for NAND cell will generate glitches observable to attacker. Simultaneously this will produce leakage and all design becomes vulnerable. This is reason why WDDL works only with "positive" gates (AND, OR) and not with negative gates (NAND, NOR). The negative gates would require forcing gates to V_{DD} instead to zero during pre-charge. There is modification of WDDL that is capable to work with negative gates named Dual Spacer Dual Rail Logics [6].

So far it is clear that good SCA protection costs duplication in hardware. Unfortunately with sequential gates the price is even higher. To retain good DPA protection it is necessary to quadruple number of flip-flops [7]. In practical realizations in FPGA it is reported that hardware overhead is over five times and that operating frequency is lower for more than twice [7].

This price is acceptable having in mind the security aspect. However, WDDL is reliable only if loads of both "true" and "false" signals are balanced. When that is not case there is leakage due timing difference [8] that jeopardizes the overall concept.

The main advantage of WDDL is that it can be implemented with standard cell libraries. Hence, it is desirable to utilize standard routing tools, as well. Unfortunately they are not optimized for symmetry and tricky part is how to obtain symmetrical wires with minor intervention in standard routing algorithms. Therefore, several algorithms were developed to provide symmetrical routing [8].

The aim of this article is to determine amount of load misbalance allowable to protect design from SCA based on power analysis. In the following section we will present the influence of mismatched load on power leakage.

IV. WDDL RESISTIVITY TO UNBALANCED LOAD

As an example AND gate implemented in WDDL (WDDL AND) will be considered. It is designed in TSMC CMOS035 technology. The I_{DD} waveform of a single-rail AND (SR AND) gate designed in the same technology will serve as a reference. Thereafter, an ideally balanced WDDL AND cell is simulated.

Figs. 4a and 4b depicts waveforms of both gates. Fig. 4a shows that I_{DD} waveform (bottom, denoted as I(V3POS)) of single raid AND gate exploits very clear difference when output (VOUT, diagram above I_{DD} in Fig. 4a changes state from 0 to 1 and from 1 to 0. Moreover, these changes are significantly higher in comparison with those that characterize neutral events. Therefore, the whole information about state at the output is visible through I_{DD}.

In contrary, supply current of WDDL AND gate have regular pattern independently on output logic states as the bottom diagram in Fig. 4b presents. This is consequence of change on "false" output (the waveform just above I_{DD} in Fig. 4b whenever "true" output (the third waveform from bottom in Fig. 4b is still. Obviously false output changes during input combination that gives neutral transitions (0-0 and 1-1) for SR AND. If the I_{DD} waveform has the same pattern for every combination of input signals there will be no leak of information about output logic state. Integral of I_{DD} is suitable to be adopted for measure of leaking the data and accordingly, for design apprising. Practically the dynamic of power change is traced as the potential attacker would do implementing Power Analysis SCA.

For the case of SR AND cell it is reasonable to compare the integral corresponding to 0-1 output transition with that obtained for change 1-0. Their discrepancy represents so called *power signature*.

For WDDL cell we compare integrals of I_{DD} during evaluation phase with each other.

As noted in the previous section WDDL will work well only if loads of true and false outputs are in balance.

It is interesting to evaluate what leakage should be expected under different amount of mismatched load.

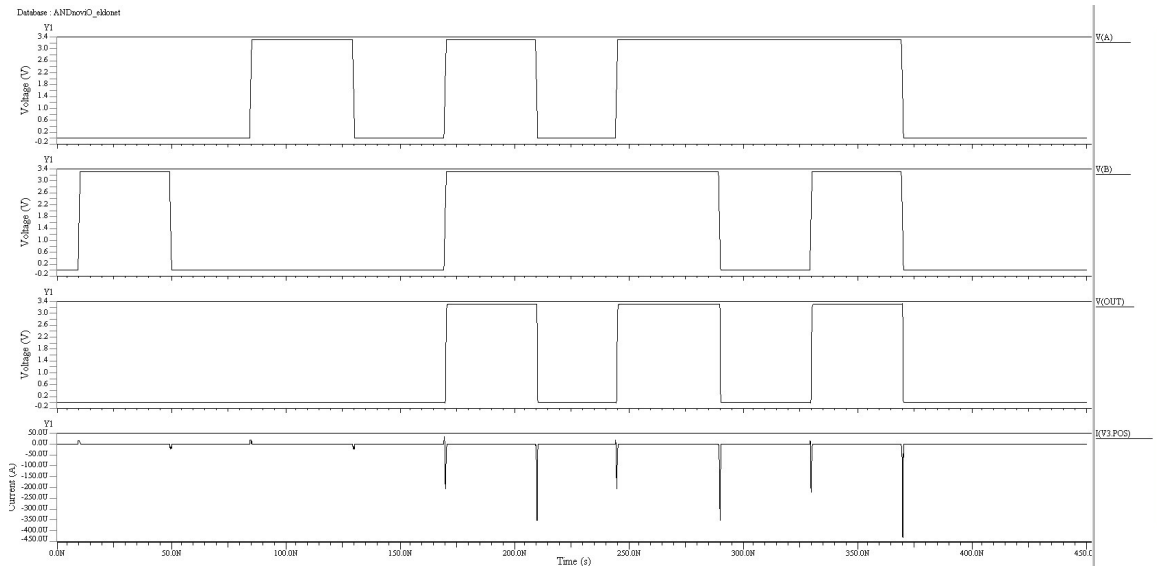
Therefore a set of several simulations were done for different rate of capacitive load mismatch. Particularly WDDL AND gate was analyzed for load capacitances unjust of up to ±15%.

Table I summarizes results for different mismatch of load values.

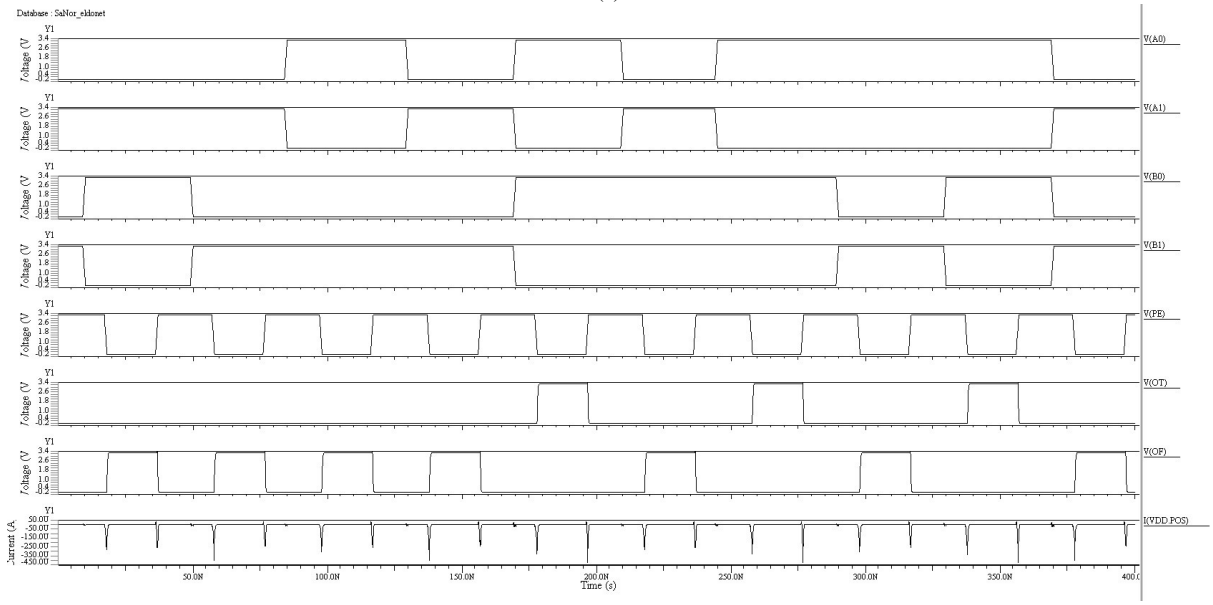
The first column shows actual input signal transitions. Second column gives energy, i.e. integral of power in time, during input signal change for SR AND cell.

TABLE I
WDDL GATE MISMATCHED

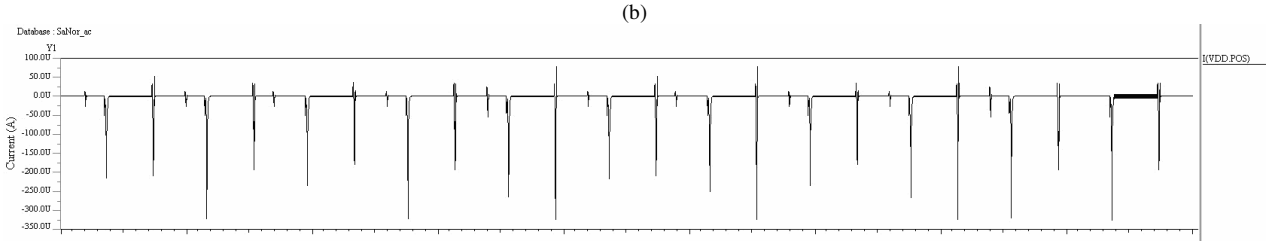
Tran A	Tran B	Single rail AND	WDDL Ct/Cf=1	WDDL ΔC=5%	WDDL ΔC=15%
0	0->1	4.60E-14	-1.0233E-12	1.81%	5.43%
0	1->0	-4.83E-14	-1.0108E-12	1.87%	5.60%
0->1	0	4.80E-14	-9.6789E-13	1.86%	5.58%
1->0	0	-5.38E-14	-1.0021E-12	1.88%	5.64%
0->1	0->1	-2.14E-13	-1.0772E-12	1.69%	4.88%
1->0	1	-4.50E-13	-1.0352E-12	1.78%	5.37%
0->1	1	-2.51E-13	-1.0613E-12	1.71%	5.07%
1	1->0	-4.94E-13	-9.7665E-13	1.85%	5.54%
1	0->1	-2.56E-13	-1.0693E-12	1.70%	4.91%
1->0	1->0	-5.16E-13	-1.0101E-12	1.83%	5.63%



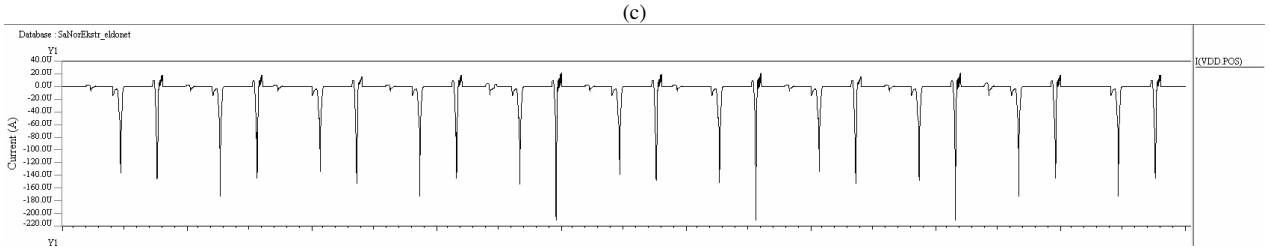
(a)



(b)



(c)



(d)

Fig. 4. Waveform of I_{DD} for (a) single-real AND gate; (b) WDDL AND gate with balanced load, (c) WDDL AND attacked with V_{DD}=2.4 V, (d) WDDL AND attacked with V_{DD}=4.2 V.

The subsequent column represents the energy used by WDDL AND cell. Obviously, the energy is increased especially (two orders of values) for combinations that produce neutral output change for simple AND cell. Even for cases when an event occur on SR AND, the WDDL AND cell needs ten times higher energy. This is an outcome of double transitions (to low-high and high-low).

Third column presents relative difference in required energy in respect to the nominal, balanced load for every input signal combination when mismatched load capacitances for 5%.

The last column shows case when imbalance was raised to 15%.

Assuming that mismatch of 10% is sufficient to explore observable leakage, one can conclude that it can be reached for load mismatch up to 20%.

V. WDDL RESISTIVITY TO V_{DD} FAULTS

As another example we consider influences of faults entered by attacker to resistivity of WDDL AND gate. Actually, observing circuit behavior under intentionally caused faults can help attackers to discover the secret code. Potential attackers are able to increase or decrease V_{DD} over/under the standard limits. Such attacks are simulated in case when V_{DD} was decreased from nominal 3.3 V to 2.4 V. Thereafter the case when V_{DD} is increased to 4.2 V is simulated, as well.

The obtained waveforms of I_{DD} are presented in Fig. 4c and Fig. 4d respectively. Although I_{DD} for balanced load could not be presented in this paper in the same scale as these two, the differences are obvious.

In addition, results are summarized in Table II.

Similarly to Table I, the first column indicates input vector signal. Results obtained for WDDL AND cell with balanced load biased for nominal V_{DD}=3.3 V are shown in the second column. Thereafter results obtained for V_{DD-}=2.4 V and V_{DD+}=4.2 V are listed respectively in columns three and four.

Last three rows present average value of energy, maximum, minimum values and relative difference between extreme values. The last parameter illustrates observability of different input sequence through I_{DD}. Larger δ corresponds to higher correlation between circuit behavior and consumed power.

One may observe that ratio of average values of energy in columns 2 and 3 E_{WDDL24}/E_{WDDL33}= 0.37, are not proportional to ratio V_{DD-}/V_{DD} = 0.72 that could be expected. Therefore it is not caused only by lower voltage bat by decrease of I_{DD} and decreased time needed to accomplish transition from low to high level and reverse.

Similarly, for case when voltage was increased to 4.2 V (V_{DD+}/V_{DD} = 1.27) the energy was increased for factor 5.42 (E_{WDDL24}/E_{WDDL33}= 5.42). This is caused by increased current but also with increased time needed to charge/discharge load and parasitic capacitances.

Although differences in energy are more than five times greater, the waveform shape hides IDD changes much better. This confirms parameter d that is more than two times smaller.

TABLE II
WDDL GATE UNDER V_{DD} ATTACKS

Tran A	Tran B	E_{WDDL}[Ws] @ V_{DD}=3.3V	E_{WDDL}[Ws] @ V_{DD}=2.4V	E_{WDDL}[Ws] @ V_{DD}=4.2V
0	0->1	-1.0233E-12	-3.94E-13	-5.52E-12
0	1->0	-1.0108E-12	-3.81E-13	-5.50E-12
0->1	0	-9.6789E-13	-3.60E-13	-5.40E-12
1->0	0	-1.0021E-12	-3.77E-13	-5.49E-12
0->1	0->1	-1.0772E-12	-3.97E-13	-5.65E-12
1->0	1	-1.0352E-12	-3.96E-13	-5.54E-12
0->1	1	-1.0613E-12	-3.94E-13	-5.62E-12
1	1->0	-9.7665E-13	-3.67E-13	-5.45E-12
1	0->1	-1.0693E-12	-3.97E-13	-5.61E-12
1->0	1->0	-1.0101E-12	-3.79E-13	-5.50E-12
average		-1.02E-12	-3.84E-13	-5.53E-12
Max		-1.08E-12	-3.97E-13	-5.65E-12
Min		-9.68E-13	-3.60E-13	-5.40E-12
δ [%]		11.29	10.28	4.63

VI. CONCLUSION

This paper presented some of countermeasures against SCA. In particular WDDL topology was examined in scope of resistivity to power analysis based SCA.

The results obtained for ideally matched outputs were compared to two mismatch levels for typical exploitation conditions. The obtained results will be analyzed in scope of technology and geometrical parameters. Actually for known tolerances of particular technology one can estimate appropriate wire width and/or metal level that should be used for the best complementary matching of power signature at false and true signals.

Capacitance and resistance of a wire depend on technological and geometrical parameters.

Therefore, for known amount of the parameter mismatch it is possible to calculate physical dimensions of wires that could keep matching within acceptable limits. Besides layout designer could decide what shape and width of wires to use. It is known that it is easier to match larger patterns. Hence, wire dimensions could be customized for better matching. Tolerances of wire capacitance and resistance depend on metal layer. It is feasible to establish some kind of design rule that

will limit wire length in respect of matching similar to the *antenna rule*.

When analyzing load mismatch it is important to be aware of different timing effects that should open up under different faulty circumstances.

In order to get good insight into WDDL vulnerability one needs to perform thorough corner analysis for lower V_{DD}, higher temperature, quicker/slower excitation. As example, results obtained for extreme V_{DD} values were reported as well. They showed that timing effects related to faster or slower capacitor charging have remarkable effect on SCA possibilities.

The obtained results will help in making decision on what type of SCA protection should be most appropriate for implementation in integrated power meter.

ACKNOWLEDGMENT

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Multi Channel ΣΔ A/D Converter for Integrated Power Meter

Dejan D. Mirković and Predrag M. Petković

***Abstract*—This paper describes three architectures for multi-channel sigma-delta ADC IC design. The proposed solution is aimed for the front-end of a three-phase integrated power meter. The pervious version of the power meter is to be redesigned by substituting six ADCs with two: one for converting currents and another for converting voltages in the three-phase power system. Therefore one pair of analog 3-to-1 multiplexers precedes ADCs. Discussion of advantages and drawbacks of the proposed solutions is illustrated by simulations using ADMS simulator that is a part of Mentor Graphics design kit.**

***Index Terms*—A/D converter, ΣΔ modulator, multiplexer, power-meter.**

I. Introduction

THE analog frontend of an integrated power meter is relatively small comparing to the digital part, especially when number of transistors is used as a measure. However, in all other aspects it represents the crucial part of the overall system on chip (SoC). The functionality of the system depends on the analog part. Moreover, even small inconsistencies in this block considerably ruin measurement characteristics of the SoC. Consequently designing of the analog part requires a lot of time, strict sticking to the design rules and a lot of designer's care and concentration.

In this paper we consider redesigning the front-end of three-phase solid-state power meter. Current version of the chip named IMPEG-2 has been designed in LEDA laboratory within Faculty of Electronic Engineering in Niš, Serbia. The new one is the third member of IMPEG solid-state power meter series. The first is IMPEG-1 dedicated for power metering in single phase power systems [1, 2, 3]. It consists of analog front-end, digital filters and DSP block as Fig. 1 presents.

The power meter is based on measurement of instantaneous values of voltage and current. They are sampled in two separated channels that consist of two SC oversampled ADCs

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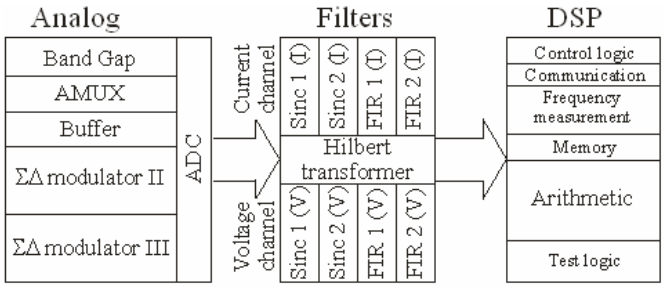

Fig. 1. Structure of IMPEG chip.

that launch digital filters and store data in corresponding registers. DSP block calculates active, reactive and apparent powers and energies. Accuracy of the calculated powers and energies mainly depends on precision of measured current and voltage.

IMPEG 1 was designed in 2003/04 and prototyped and tested in 2005.

Encouraged with the obtained results the LEDA team designed three-phase version of IMPEG in 2006/07. It differs from IMPEG-1 mainly in digital part. The analog front-end was triplicate of the analog part of the basic IMPEG version.

LEDA team is motivated to optimize area, power consumption and performances in the new variation of IMPEG. Therefore the digital part has been enriched with temperature self-calibration and low-power-driven design. The aim is to decrease area of the analog part replacing six ADCs with as few as possible. This paper analyses possible architectures for multichannel sigma delta A/D convertors.

The paper is organized as follows. The subsequent section describes architecture of IMPEG-2. The third section considers possible solutions for multiplexed AD converter and suggests type of architecture that fits the best to the specification. Thereafter, the behavior and performances of the chosen circuitry are verified in the fourth section.

II. IMPEG-2

IMPEG-2 represents three-phase version of IMPEG-1. However it is not plain triplication of the mono-phase version.

Fig. 2 represents the structure of IMPEG 2 [4]. The main differences are in digital part. Computation engine that has relayed on DSP block is accomplished with embedded MCU 8052. Besides, drivers for LCD display, real time clock, digital PLL, original acquisition block and converter for battery

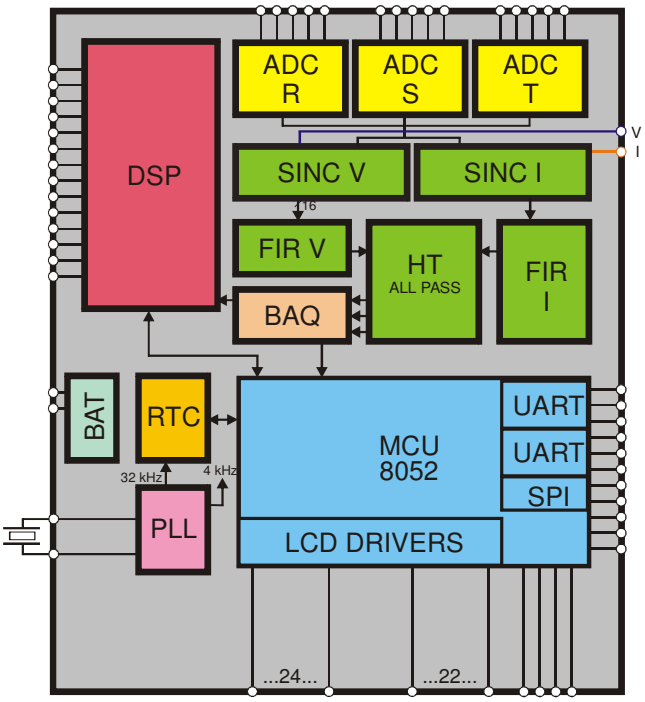

Fig. 2. Structure of IMPEG 2.

driven bias are incorporated as well. Moreover, major innovations have been made in digital filter block [5]. Namely, Sinc, FIR and Hilbert transformer filters implement compact MAC architecture and time multiplexing technique. As result the overall area for digital filters is increased only for 3% in comparison to the mono-phase realization. Practically, all three phases in voltage and current channel separately share the same hardware for digital filtering, as Fig. 3 shows.

Obviously, six sigma-delta modulators spoil the compactness of the solution. Therefore the next section considers possibilities for designing more compact solution. All of them are based on multiplexed approach.

III. MULTIPLEXED SD MODULATOR

The basic idea is to put as much channels as possible through the same ADC and avoid differences due to different offset, integral and differential nonlinearities and other ADC imperfectness. Besides, the goal is to spare chip area for as many modulators as possible without lost of functionality. Simultaneously it is desirable to retain already designed and tested full custom designed macro-cells. In the scope of analog frontend it means not to change the order of modulator and its basic blocks: integrators, opamps, band gap reference, quantizer and single-bit DAC.

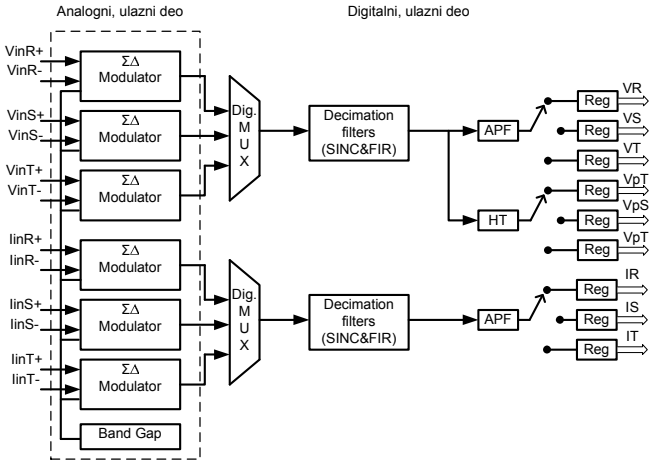

Fig. 3. ADC part of IMPEG 2.

The structure of used ΣΔ modulator is shown in Fig. 4 [3].

Integrators are realized using switch capacitor (SC) method [8]. Although differential architecture is practically used, for the sake of simplification it will be illustrated in single-ended version as Fig. 5. presents.

Observing Fig. 3 and Fig. 5 one can conclude that the most compact solution would be to replace all six modulators with one as Fig. 6 illustrates. The proposed architecture is inspired by [7, 8].

All six inputs, three for voltages of three phases denoted with VR, VS and VT and three for the corresponding currents denoted as IR, IS and IT comes to the input of multiplexer 6 to 1 (MUX6-1 in Fig. 6). However, to retain the same sampling frequency as the original circuit has (Fig. 3) and to persist in-phase sampling of all six signals, the multiplexer is driven from sample and hold circuits. All analog signals should be sampled with the same clock at frequency of 524288 Hz. The hold time should last long enough to allow conversions for all six channels. To accomplish this task one needs at least six times faster switching in modulator than the sampling frequency. Namely it requires clock of 3.14 MHz.

Digital signals are sent to the appropriate registers at the output where clock rate is returned to the sampling frequency rate of 524288 Hz. Therefore the rest of SoC will not be disturbed.

Knowing limitations of the used folded cascode operational amplifier of GBW=7.3 MHz and slew-rate of 5 V/μs [6], this means that the proposed architecture is close to the acceptable upper margins of the design.

Opposite solution is to multiplex only two channels: one for voltage and another for current within a single modulator. Three-phase power meter needs three such architectures, one for every phase. Supposing that sampling data rate remains 524288 Hz this implies that modulator has to be switched with rate of 1.05 MHz .This is below limits of implemented opamps and therefore a feasible solution. However the overall spare in area is less than 1/2 of the solution presented in Fig. 3.

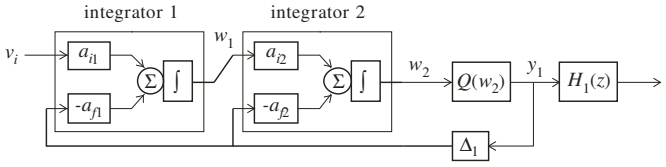

Fig. 4. Structure of second order ΣΔ modulator.

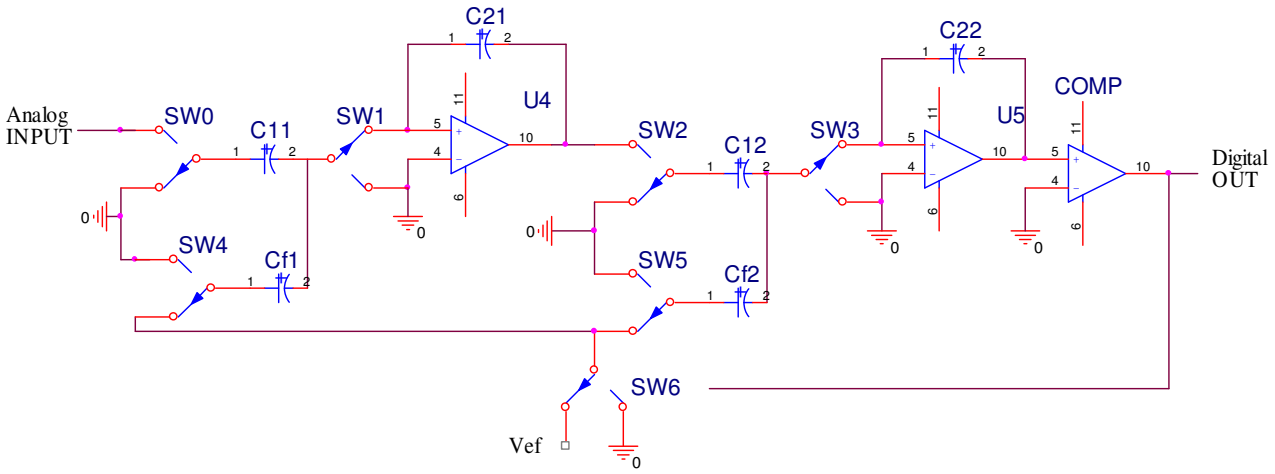

Fig. 5. Second-order ΣΔ modulator realized in SC architecture suitable for standard CMOS.

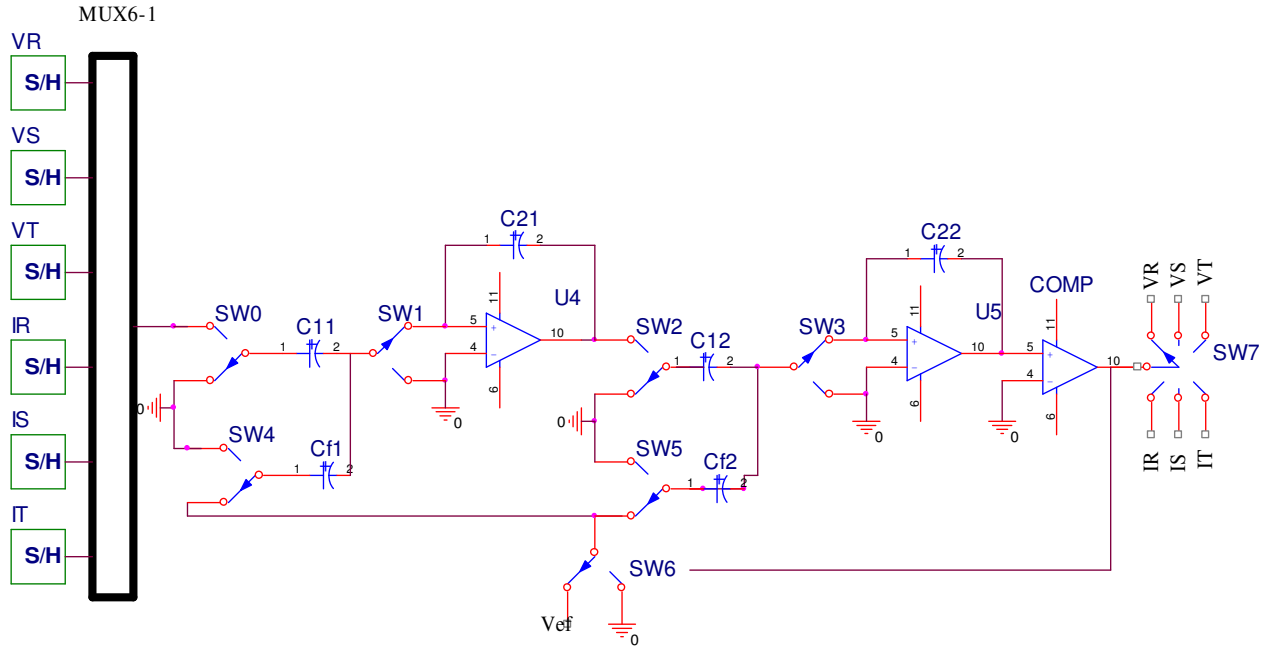

Fig. 6. Single second-order ΣΔ modulator with six multiplexed inputs/outputs.

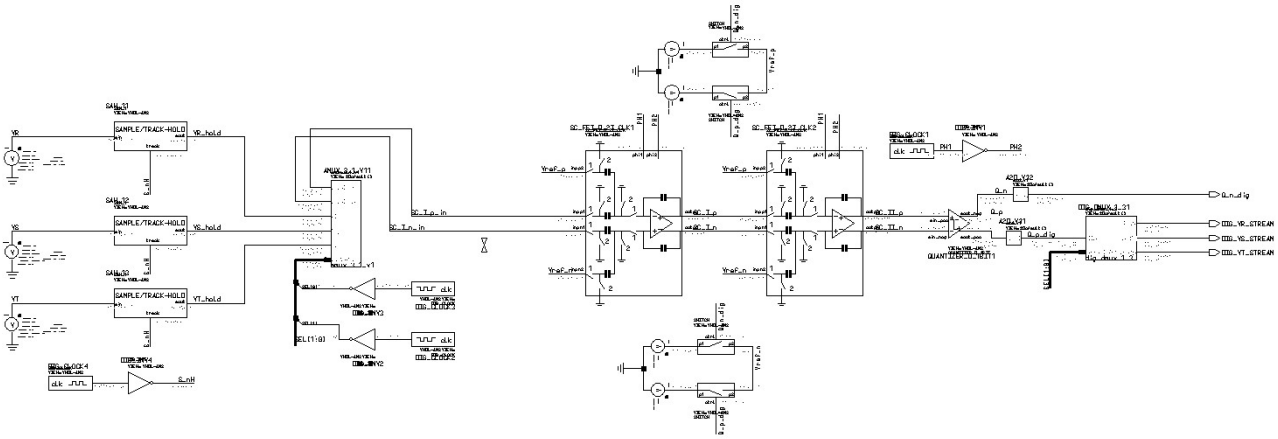

Fig. 7. Second-order differential ΣΔ modulator with three multiplexed inputs/outputs.

Although the number of ADC is decreased, the number of capacitors in C_{f1}, C_{f2}, C_{21} and C_{22} will be duplicated. However, due to the increased frequency the value of capacitances will be halved. Therefore the overall gain should be analyzed carefully. Besides, successive sampled values on SCs will differ considerably due to the different order of magnitudes and dynamic signal ranges in voltage and current channels.

The third solution for multiplexed ADC suitable for the integrated power meter consists of 3 to 1 multiplexer. The system requires two identical blocks, as Fig. 7 presents. One for three voltages (for each of three phases) whiles another being for three currents. Therefore it fits well to the general architecture presented in Fig. 3 because voltage and current channels are separated. This pursues the natural data flow to distinct digital filters and driven by different dynamic ratio in current and voltage channels. Moreover, for fixed sampling rate of 524288 Hz this requires moderately increased switching frequency of 1.57 MHz. The overall area will be shrunken less than 1/3 of the solution presented in Fig. 3. The decreased gain in area is caused by circuit complexity that is not shown in Fig. 5 to Fig. 7. Namely, although sizes of capacitors were shrunken, additional circuitry is needed to store previous sample for every channel.

IV. Simulation Results

The former architecture has been thoroughly verified by simulation.

Firstly, behavioral VHDL-AMS model has been developed and confirmed. It is used to check timing for S/H and two-phase clock signals needed to switch modulator.

Fig. 8 presents the accepted timing of clock waveforms. SH denotes switching in S/H circuits. Low logic level corresponds to the sampling phase while the high logic level defines the hold status. CLK1 and CLK2 denote controlling switching signals within modulator.

During high level of CLK1 input signal drives C11 and C12, while during CLK2 high the charge is transferred to C21 and C22.

Simulations confirmed expected functionality. Some of the representative waveforms are presented in the following figure.

Fig. 9 illustrates the obtained results for analog multiplexer. Sampled values of the corresponding input signals are presented at the output of analog multiplexer. The input of ΣΔ modulator is fed by this output.

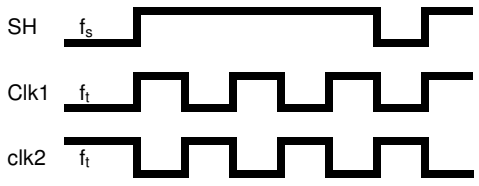

Fig. 8. Simplified timing diagram of driving signals in three input multiplexed ADC.

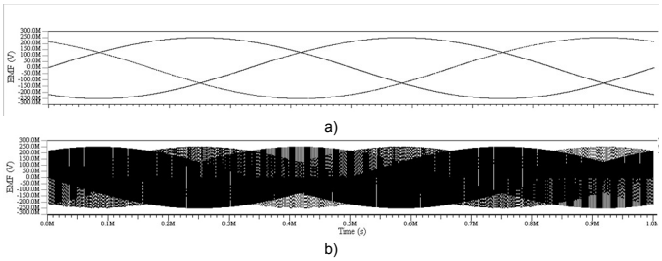

Fig. 9. Simulation results obtained for three channel architecture: input a), and output b) of analog multiplexer.

After modulation, signal is decimated using decimation filter with decimation factor of 128. Finally 19-bit word is obtained at the output of the converter. Fig. 10 represents the Fast Fourier Transformation of one of the converted outputs.

In this case effects of different kinds of noise (clock jitter, operational amplifier, KT/C) are taken into account. As result, suppression of harmonics is decreased, but still in the acceptable margins. For generating results presented in Fig 10. MATLAB is used as tool. Decimation filter and ΣΔ modulator with noise effects are modeled combining MATLAB scripting and Simulink test bench environment.

V. Conclusion

Three architectures for multiplexed ΣΔ ADC suitable for implementation within a three-phase solid-state power meter were discussed. All of them rely on using sampling-and-hold circuits at inputs to synchronize sampling of all input signals. The goal was to use as much of already designed analog and digital blocks as possible. Therefore it is necessary to sample SH circuits with the frequency of 524288 Hz and to obtain oversampled digital output with the same rate. This request can be fulfilled only if modulator switching frequency is increased as much as multiplexed signals are driven into it. This opens the issue of performances of used operational amplifiers and the issue of reliability of the overall SoC. Power

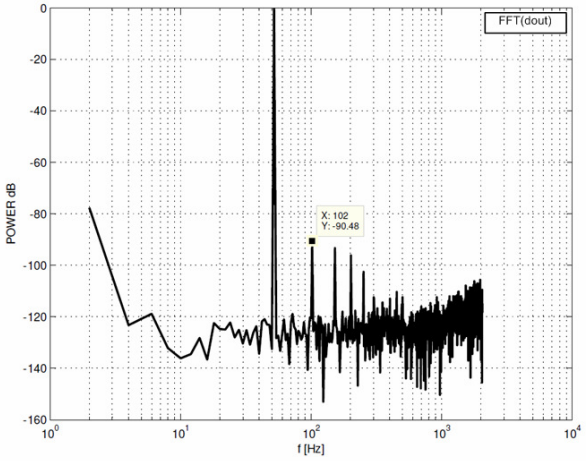

Fig. 10. FFT of one of the channels after decimation.

meter is expected to work persistently and reliably for at least ten years. Therefore it is better to design them to run in modest operation conditions. Timing properties of operational amplifier are crucial for achieving high frequency switching rate of modulator. Eventually it is better to trade small amount of chip area for more robust and reliable component.

As the modulator is realized in SC manner, the increase of switching frequency reflects to the component size. Namely resistors are realized as SC. Hence their value is defined with $T/2C$, where T is $1/f_{sw}$; f_{sw} being the switching frequency. Consequently the increase of f_{sw} requires smaller C for the same R. From other side, the bandwidth of the integrator is defined by RC product. Remaining the same RC can be achieved by decreasing C. In both cases dimensions of one of the implemented capacitors will be decreased. Moreover coefficients in Fig. 4 are defined as ratio of corresponding capacitances. Therefore if one is decreased, the other should be shrinking as well. Fortunately all this leads to the very slight modifications of layout. Namely, due to their dimensions, all capacitors are laid out as matched structures out of the modulator areas. This satisfies the basic request to reuse already designed macro cells.

However, the existing, previously tested opamp has precisely defined GBW and slew rate. This put boundary to the maximum switching rate.

Finally, the chosen solution is based on using 3 to 1 multiplexed ADCs. One is used for three voltages, another for the corresponding currents. This architecture match to the overall SoC concept that considers voltages and currents separately in order to protect sensible current channels from possible crosstalk produced in voltage channels. Moreover, this fits to the basic layout rule stressed in [9] “if it looks good, it will work”.

ACKNOWLEDGMENT

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