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Guest Editorial

FROM a historical point of view, electronics is relatively new and still rapidly growing and rapidly changing area. There is a need for electronics professionals, but they are required to constantly update and even upgrade their knowledge to remain competitive in the field. Having in mind current trends of making average career last longer, electronics majors pursuing their BS degrees at this moment are likely to retire in 50 years, or even later. There is a challenge to select a set of basic concepts the students should master in order to be capable to update their skills to follow job market requirements for such a long time in an unpredictable and rapidly changing environment. On the other hand, there is a trade-off between the fundamental knowledge and the applied skills needed to get an "out of the box" engineer, and these two directions compete for limited time available to train students. Should engineers be highly specialized, and does this reduce their ability to move around to look for more attractive employment options? Or, on the contrary, one specialization, accompanied by a solid background in fundamental knowledge, makes them confident and capable to specialize in another direction, according to the job market of the moment? Would these career opportunities be attractive enough to motivate prospective students to enroll engineering?

To make things even more complicated, the field of education is being revolutionized by massive open online courses (MOOCs), that increase rapidly in number, content, and variety of topics, characterized by highly polished software interfaces and attractive multimedia content, being taught by prominent teachers from respected institutions. How to include this technological and social achievement of undoubtedly great potential into everyday teaching practice? Furthermore, offering of free textbooks and other teaching materials on the web is in constant increase, making education more available than ever, but some students might experience a language barrier, or difficulties how to select appropriate material and how to focus and organize their time. Definitely, technology and education are interrelated, and this interaction raises questions on everyday basis. Some of the questions are technical, some psychological, some social, and professionals from different disciplines that address these questions not always speak the same language, neither perfectly understand each other.

Having all these questions in mind, being a teacher himself, and most of all not having all the answers, the Guest Editor for the Special Issue "Education in Electronics" decided to make a call for papers, to ask colleagues to share their experiences, to tell how they teach something they find important. New courses, new teaching approaches, review articles that cover educational systems or different approaches to teach specific topics were of interest. Also, papers describing new laboratory exercises were welcome. Focus of the issue was on engineering, and the methods and experiences in teaching engineering classes. The result is here. The Guest Editor hopes that the papers would inspire new ideas and new publications, and would like to thank all the authors for their effort and fine contributions. The Guest Editor would also like to thank Professor Goce Arsov for his help and interest in organizing the Special Issue.

Prof. Predrag Pejović, Ph.D.
Guest Editor

Prof. Predrag Pejović, Ph.D.
Biography

Predrag Pejović (http://tnt.etf.bg.ac.rs/~peja/) is a Professor at the University of Belgrade, Faculty of Electrical Engineering. He received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, in 1990 and 1992, respectively, and the Ph.D. degree from the University of Colorado, Boulder, in 1995. In 1995, he rejoined the University of Belgrade. His research interests are wide, ranging from analog circuit design, power electronics, three-phase high power factor rectifiers, dynamics of nonlinear systems, electronic measurements, techniques for computer-aided analysis and design of power electronic systems, up to positioning in communication systems. He authored a book "Three-Phase Diode Rectifiers with Low Harmonics - Current Injection Methods," Springer, 2007, ISBN 978-0-387-29310-3, and coauthored an open-access book chapter "Positioning in Cellular Networks," in "Cellular Networks --- Positioning, Performance Analysis, Reliability," Intech, 2011, ISBN 978-953-307-246-3. Currently, he teaches Electrical Measurements, Analog Electronics, Power Electronics, Software Tools in Electronics at the undergraduate level, as well as Power Electronics 2 (M.S. studies), and Selected Topics in Power Electronics (Ph. D. studies). He authored several lecture notes for his classes, freely available from http://tnt.etf.bg.ac.rs/~peja/. At the moment his Google Scholar profile lists 75 publications with 614 citations. Besides that, he has 64 publications in Serbian.

Professor Pejović was a Visiting Scientist at the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zürich, in two one-month terms in 2006 and 2009. In 2008, he held a seminar for graduate students at the Universitat Rovira i Virgili, Tarragona, while in 2012 he held a graduate seminar in three-phase rectifier systems at the Universidad Politécnica de Madrid, available at http://tnt.etf.bg.ac.rs/~peja/seminar.html.

Prof. Pejović served two terms as a Chairman of the Department of Electronics, Faculty of Electrical Engineering, University of Belgrade, from 2006 to 2012. He is a member of the Institute of Electrical and Electronic Engineers (IEEE), and the Free Software Foundation.

Celebrating 65th Anniversary of the Transistor

Goce L. Arsov

***Abstract*—The paper is dedicated to the 65th anniversary of the invention of the revolutionary electronic component that actually changed our way of life—the transistor. It recounts the key historical moments leading up to the invention of the first semiconductor active component in 1947. The meaning of the blend "transistor" is explained using the memorandum issued by Bell Telephone Laboratories. Certain problems appeared in the engineering phase of the transistor development and the new components obtained as a result of this research are reviewed. The impact of this invention on the development of power electronics is being emphasized. Finally, the possibility that the most important invention of the 20th century has been conceived not once but twice is discussed.**

***Index Terms*—history, semiconductor, transistor.**

Review Paper
DOI: 10.7251/ELS1317063A

I. Introduction

The invention of the transistor about 65 years ago was one of the most important discoveries of the 20th century. It has had enormous impact on our entire way of life. Officially it was invented by a group of scientists at Bell Telephone Laboratories (BTL), led by Shockley, on December 16, 1947, and it was demonstrated on Christmas Eve 1947. Yet, the announcement of this invention was delayed until June 1948.

For this invention Bardeen, Shockley and Brattain were awarded the Nobel Prize in Physics in 1956, "for their researches [sic] on semiconductors and their discovery of the transistor effect".

However, it should be mentioned that the pursuit of the solid-state amplifier has longer history than the transistor. It dates back to 1924–1925 and the work of Julius Edgar Lilienfeld [1]–[3], as well as to the work of Russell Ohl and his invention of the p-n junction, in 1940 [4], [5].

This invention also had great impact on the development of power electronics as a field born in 1901, this year celebrating its 112th anniversary.

Additionally, it may be interesting to note that 1947 was the centennial of A. G. Bell's birth, as well as the 50th anniversary of the discovery of the electron by J. J. Thomson, and of the publication of J. C. Bose's paper "On the Selective Conductivity Exibited by Certain Polarizing Substances" [6], which directly led to the invention of the first semiconductor diode detector.

Although one could say that the electronics age started with Braun's cathode ray tube (1897) and Fleming's vacuum tube rectifier (1904), the real electronics era began with Lee de Forest's triode, where, by placing a wire "grid" between the cathode and anode, he transformed Fleming's rectifier into an amplifier. With the amplification, radio communications and long-distance telephony became a reality.

Despite the fact that the triode was very successful, its long-term limitations became obvious. It was a fragile device that required a lot of power. So in the mid-1920s, J. E. Lilienfeld, occupied by radio technology, began his work on finding a solid-state replacement for the vacuum triode.

II. The Invention of the Transistor at BTL

Aware of the limitations of vacuum tubes, several groups of scientists in different parts of the world began examining the possibility of developing semiconductor devices.

In the mid-1940s a research group for investigating the aspects of possible semiconductor applications was established at BTL. The leaders of this group were W. Shockley and S. Morgan. Two key members of the group were J. Bardeen and W. H. Brattain. Other members included G. Pearson, B. Moore, and R. Gibney. The group members had already had good theoretical and practical experience with the existing semiconductor materials and devices.

At that time, all attempts to create the semiconductor amplifying device were based on the field-effect principles described by Lilienfeld [1]–[3].

Before and after World War II, Shockley, aware of these principles, studied and analyzed different field-effect structures. He concluded that this effect should produce amplification in feasible structures (Fig. 1).

In January 1946, the group adopted two very important decisions.

The first was to focus the group's attention only on crystals of silicon and germanium and to ignore other, more complex, materials that were frequently considered in previous investigations. At that time it was already assumed that, for most applications, silicon should be a better transistor material than germanium. This is mainly because of the higher energy gap of silicon—1.1 eV compared to 0.67 eV for germanium.

The second decision was to pursue the field-effect principle as the most promising for leading to realization of a useful device.

Manuscript received 26 November 2013. Received in revised 24 December 2013. Accepted for publication 25 December 2013.

This paper was prepared as a special contribution to celebrating the 40th anniversary of the International Symposium on Power Electronics. Its original version was presented at the 17th International Symposium on Power Electronics - Ee 2013 as an invited paper.

G. Arsov is with the SS Cyril and Methodius University, Faculty of Electrical Engineering and IT, Karpos II b.b., Skopje, Macedonia, (e-mail: g.arsov@ieee.org).

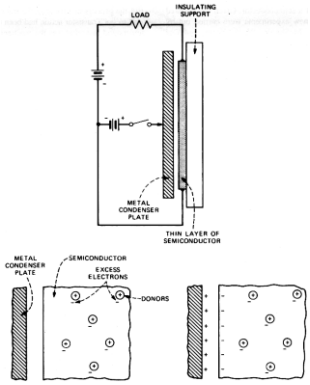


Fig. 1. Schematic of Shockley's field-effect idea [7].

Between the mid-1920s and the early 1950s numerous attempts to achieve the field-effect in semiconductors were made, but all failed. Bardeen and Brattain tried confirming this theory by experimenting with metal probes placed on the germanium surface. They showed that the theory was correct. So, for the first time, they came to some understanding of the reasons they had failed to observe the field-effect, but also to some knowledge of how to intervene. After several attempts Bardeen replaced the two contacts with an ingenious arrangement of two strips of gold foil separated by just a few millimeters that were pressed onto the germanium surface. In the case when one gold contact was forward-biased and the other reverse-biased, he observed power gain. That was the discovery of the transistor action [8] (Fig. 2). This happened on December 16, 1947, nearly two and a half years after the establishment of the Shockley group.

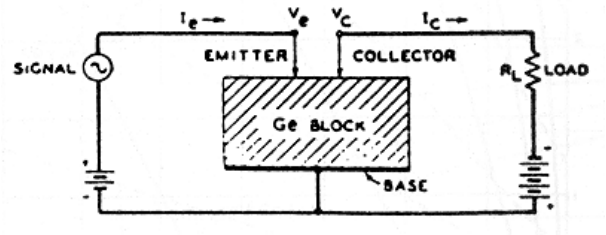
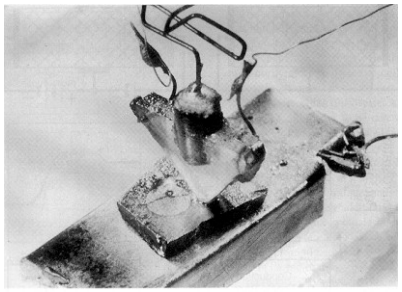


Fig. 2. Schematic of the "semiconductor triode" [8].

The transistor effect was demonstrated for the top management of Bell Labs by Brattain and Moore on Christmas Eve, 1947. (The original structure and the inventors are shown in Fig. 3.) However, the announcement of the invention was postponed until June 1948. This six-month period was used to gain better understanding of the device and its possible applications, but also to obtain adequate patent position (Fig. 4) [9].

Bardeen and Brattain directed their attention to the surface effect [10] and continued experiments on that basis. Shockley, on the other hand, recognizing the role of minority carriers, worked on formulating a p-n junction theory that would include the role played by the injection of minority carriers in the case of a forward-biased junction and their collection when it was reverse-biased [11]. This research and analysis resulted with the invention of a *junction transistor.*



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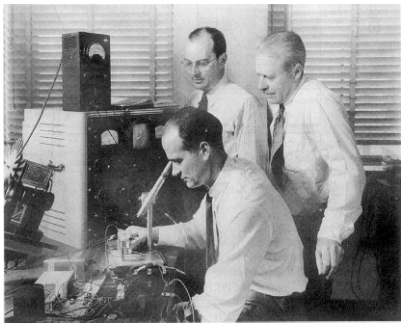


(b)

Fig. 3. (a) The original point-contact transistor structure. (b) W. Shockley (seated), J. Bardeen (left), and W. Brattain (right) photographed in 1948.

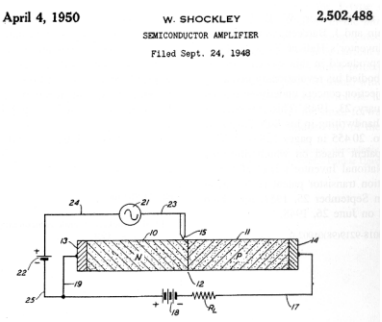
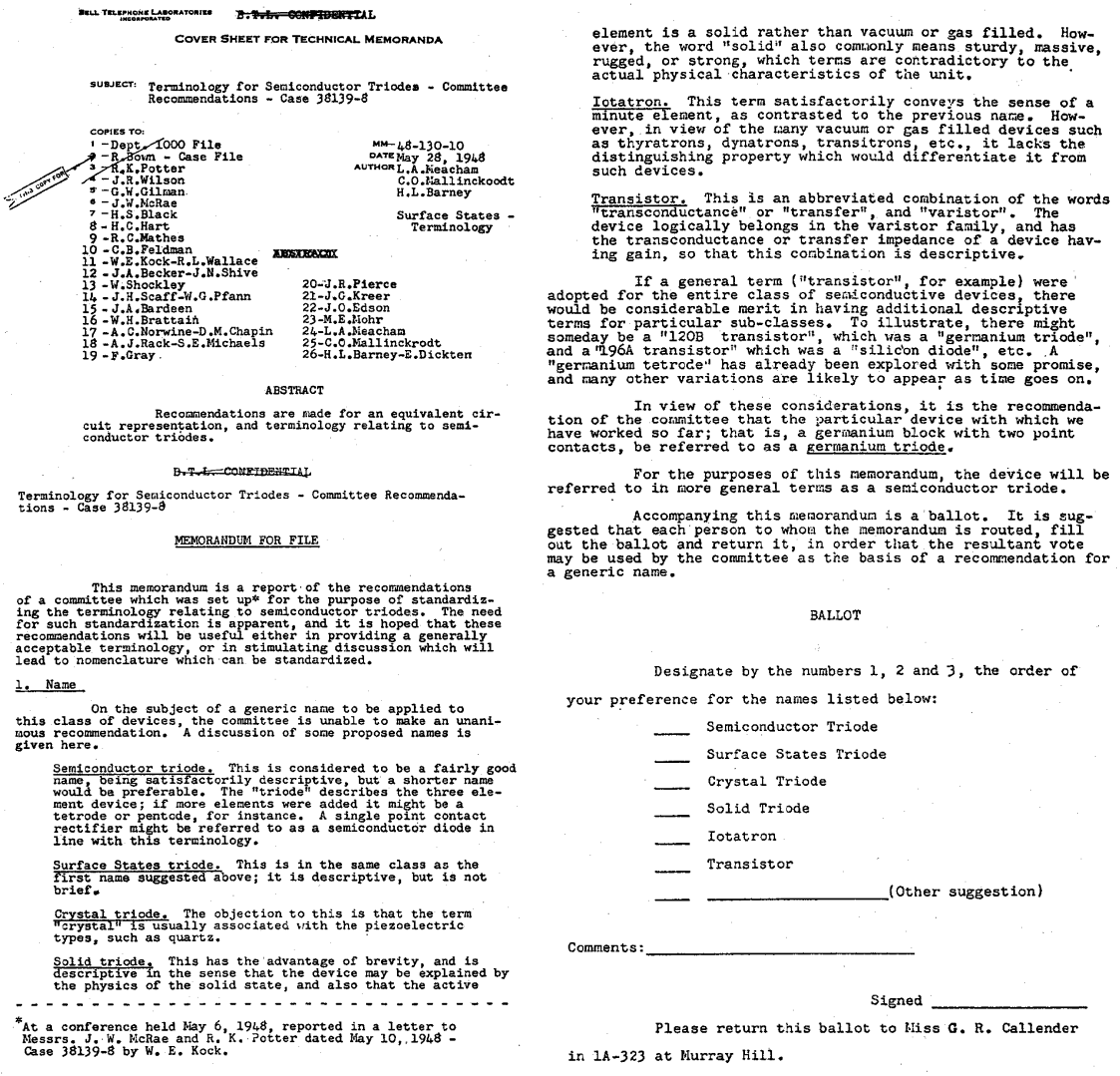

April 4, 1950 W. SHOCKLEY 2,502,488
SEMICONDUCTOR AMPLIFIER
Filed Sept. 24, 1948

Fig. 4. Extract from the patent 2502488 (W. Shockley – Semiconductor Amplifier) [9].

In an attempt to increase the gain, Shockley proposed a structure with a fourth region obtained by the addition of an extra junction at the collector. This was sometimes called a "hook collector" [12]. He noted that this would lead to a current gain which is greater than unity. It was later discovered that silicon p-n-p-n diode had a bistable characteristic, behaving like a reverse-biased junction in one state and a forward-biased junction in the second state, which led to the invention of the "thyristor" in 1957.

III. Naming the Transistor

In all dictionaries and textbooks, the word transistor is explained as a blended form of the words "transfer" and "resistor". But, the internal "Memorandum for File" of Bell Telephone Laboratories concerning the name of the newly-invented device, "semiconductor triode", issued on 28 May 1948 [13], [14], clearly shows that the word transistor is a blended form of the words "transconductance" or "transfer" and "varistor". This memorandum, together with a ballot, was sent to 26 individuals or groups, including



BELL TELEPHONE LABORATORIES INCORPORATED ~~B.T.L.— CONFIDENTIAL~~

COVER SHEET FOR TECHNICAL MEMORANDA

SUBJECT: Terminology for Semiconductor Triodes - Committee Recommendations - Case 38139-8

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24-L.A.Meacham
25-C.C.Mallinckrodt
26-H.L.Barney-E.Dickten

MM-48-130-10
DATE May 28, 1948
AUTHOR L.A.Meacham
C.O.Mallinckoodt
H.L.Barney

Surface States - Terminology

~~ABSTRACT~~

ABSTRACT

Recommendations are made for an equivalent circuit representation, and terminology relating to semiconductor triodes.

~~B.T.L.—CONFIDENTIAL~~

Terminology for Semiconductor Triodes - Committee Recommendations - Case 38139-8

MEMORANDUM FOR FILE

This memorandum is a report of the recommendations of a committee which was set up* for the purpose of standardizing the terminology relating to semiconductor triodes. The need for such standardization is apparent, and it is hoped that these recommendations will be useful either in providing a generally acceptable terminology, or in stimulating discussion which will lead to nomenclature which can be standardized.

1. Name

On the subject of a generic name to be applied to this class of devices, the committee is unable to make an unanimous recommendation. A discussion of some proposed names is given here.

Semiconductor triode. This is considered to be a fairly good name, being satisfactorily descriptive, but a shorter name would be preferable. The "triode" describes the three element device; if more elements were added it might be a tetrode or pentode, for instance. A single point contact rectifier might be referred to as a semiconductor diode in line with this terminology.

Surface States triode. This is in the same class as the first name suggested above; it is descriptive, but is not brief.

Crystal triode. The objection to this is that the term "crystal" is usually associated with the piezoelectric types, such as quartz.

Solid triode. This has the advantage of brevity, and is descriptive in the sense that the device may be explained by the physics of the solid state, and also that the active element is a solid rather than vacuum or gas filled. However, the word "solid" also commonly means sturdy, massive, rugged, or strong, which terms are contradictory to the actual physical characteristics of the unit.

Iotatron. This term satisfactorily conveys the sense of a minute element, as contrasted to the previous name. However, in view of the many vacuum or gas filled devices such as thyratrons, dynatrons, transitrons, etc., it lacks the distinguishing property which would differentiate it from such devices.

Transistor. This is an abbreviated combination of the words "transconductance" or "transfer", and "varistor". The device logically belongs in the varistor family, and has the transconductance or transfer impedance of a device having gain, so that this combination is descriptive.

If a general term ("transistor", for example) were adopted for the entire class of semiconductive devices, there would be considerable merit in having additional descriptive terms for particular sub-classes. To illustrate, there might someday be a "120B transistor", which was a "germanium triode", and a "196A transistor" which was a "silicon diode", etc. A "germanium tetrode" has already been explored with some promise, and many other variations are likely to appear as time goes on.

In view of these considerations, it is the recommendation of the committee that the particular device with which we have worked so far; that is, a germanium block with two point contacts, be referred to as a germanium triode.

For the purposes of this memorandum, the device will be referred to in more general terms as a semiconductor triode.

Accompanying this memorandum is a ballot. It is suggested that each person to whom the memorandum is routed, fill out the ballot and return it, in order that the resultant vote may be used by the committee as the basis of a recommendation for a generic name.

BALLOT

Designate by the numbers 1, 2 and 3, the order of your preference for the names listed below:

____ Semiconductor Triode
____ Surface States Triode
____ Crystal Triode
____ Solid Triode
____ Iotatron
____ Transistor
____ _____(Other suggestion)

Comments:_____

Signed _____

Please return this ballot to Miss G. R. Callender in 1A-323 at Murray Hill.

*At a conference held May 6, 1948, reported in a letter to Messrs. J. W. McRae and R. K. Potter dated May 10, 1948 - Case 38139-8 by W. E. Kock.

Fig. 5. The copy of the “Memorandum for File” concerning the name for the transistor (“semiconductor triode”) [13].

Shockley, Brattain and Bardeen. The propositions: "Semiconductor Triode", "Solid Triode", "Surface States Triode", "Crystal Triode", "Iotatron" and “Transistor”, were all considered (Fig. 5). Although “Semiconductor triode” was recommended by the creators of this memorandum, "Transistor" was the clear winner of the internal poll. The rationale for the name was: “Transistor is an abbreviated combination of the words ‘transconductance’ or ‘transfer’, and ‘varistor’. The device logically belongs in the varistor family, and has the transconductance or transfer impedance of a device having gain, so that this combination is descriptive” [13].

IV. The Development and Production Phase

The invention of the transistor itself did not resolve the problems of its production. The challenge was to find ways to design a product that could be manufactured and that could succeed on the market. Eight additional years were needed to fulfill this engineering task.

In early 1950s there were two transistor structures that were proven to work—the point-contact transistor and the junction transistor—but neither of them was suitable for large-scale manufacturing. The former was difficult to make and its electrical characteristics were far from ideal. It was very variable, hard to control, and inherently unstable, but nevertheless it was manufactured for ten years, starting from 1951. Point-contact transistors were used in telephone oscillators, hearing aids, an automatic telephone routing device, and the first airborne digital computer (TRansistorized Airborne DIgital Computer – TRADIC).

The latter, on the other hand, had predictable and more desirable electrical characteristics. But, it was wasteful in its use of precious semiconductor material and required very special contacting techniques. Crystals were grown using a precise doping procedure to create a single thin layer of base material embedded in material of the opposite type from which the “emitter” and “collector” were made. It was possible to “grow” only one “slice” of base material in one

crystal. The process was very complex; it was conducted in special laboratories and was not convenient to automatization.

The manufacturing of the "grown" junction transistor began in 1952. It was the same year that the development of the alloy junction transistor was announced at GE by J. E. Saby [15].

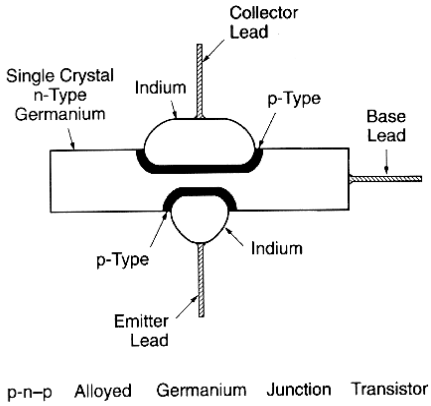


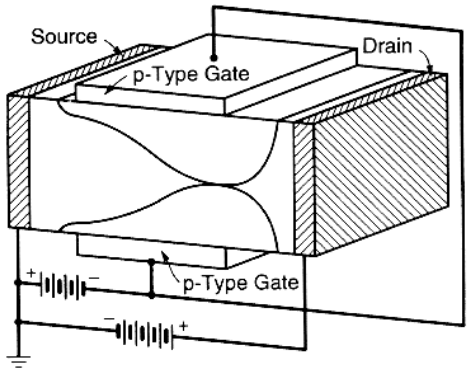
Fig. 6. Schematic of the alloy transistor.

The alloy device was the first junction transistor to be easily manufactured and it was the leading semiconductor product of the industry for a number of years (Fig. 6). On the other hand, the research on the alloy junction process had an interesting byproduct—the junction field-effect transistor (FET). In fact, in 1951 Shockley "reinvented" the field-effect transistor, but this time as a junction device. So, in 1952 he asked G. C. Dacey and I. M. Ross to try and build a unipolar field-effect transistor. The structure built (Fig. 7) conducted exactly as Shockley's theory had propounded [16]. Unfortunately, at that time they could not find any significant advantage of the new device over the bipolar transistor. Moreover, it was much more difficult to produce unipolar than bipolar transistors. So, although the field-effect theory was validated, its production was abandoned for a while.

In 1952 it was recognized that dopants could be introduced to very precise depths by diffusion from the semiconductor surface. The diffusion process could achieve precise control of surface concentration over a range of 10,000 to 1, and control of the number of atoms introduced over a range of 100,000 to 1. But, most importantly, the depths of diffused layers were easily controllable in the range from a fraction of a micrometer to 20μm [17].

Another problem to solve was the reliability of the transistor. Different methods were investigated. In an attempt to solve this problem, M. M. Atalla and D. Kahng studied the surface properties of silicon in the presence of a silicon dioxide layer. A byproduct of their investigations was the fabrication of another design of a field-effect device—the metal-oxide-semiconductor field-effect transistor (MOSFET) [18].

Since the beginning of the semiconductor era in electronics, the number of transistors in an integrated circuit has been increasing exponentially with time [19]. The bipolar technology has been largely replaced with CMOS and it has been improved many times, but above all it has been miniaturized to an inconceivable level. Also, the number of transistors produced per year has been growing incessantly [20].



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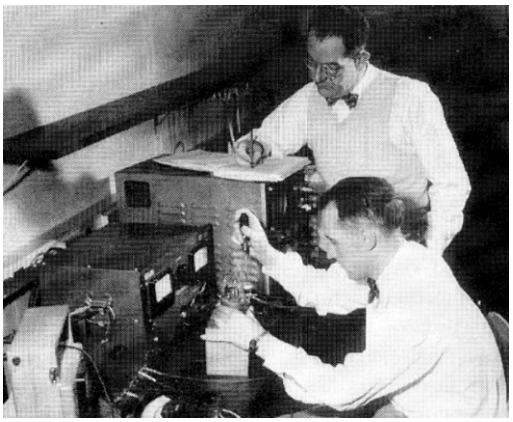

(b)

Fig. 7. (a) Schematic of the junction field-effect transistor. (b) G. C. Dacey and I. M. Ross (seated) testing a field-effect transistor.

V. The Impact on Power Electronics [21]

The invention of the transistor had a major impact on power electronics and its development.

Officially, power electronics was born in 1901 with the invention of the glass-bulb mercury-arc rectifier by Peter Cooper Hewitt of USA [22]. Then, it went through the eras of gas tube electronics in the 1930s and saturable core magnetic amplifiers in the 1940s. Hot cathode thyratron was introduced in 1926 and the ignitron rectifier in 1933. The applications of power electronics began to expand and in 1930 the New York Subway installed a grid-controlled mercury-arc rectifier (3 MW) for DC drive. Then, in 1931 the German railways introduced a mercury-arc cycloconverter for universal motor traction drive. In 1934 the thyratron cycloconverter (synchronous motor 400 hp) was installed in the Logan Power Station as a first variable frequency drive.

The present era of solid-state power electronics started with the introduction of the thyristor, or silicon controlled rectifier (SCR). Actually, the Silicon Controlled Rectifier or Thyristor was proposed by William Shockley in 1950. It was theoretically described in several papers by J.J. Ebers [23], and especially by J. L. Moll [24] and others at Bell Telephone Laboratories (BTL). In 1956 the SCR was developed by power engineers at General Electric (G.E.) led by Gordon Hall. The commercial version was developed 55 years ago, in 1958, by G.E.'s Frank W. "Bill" Gutzwiller (Fig. 8).

Fig. 8. Frank "Bill" Gutzwiller.

The idea of the p-n-p-n switch was first simulated by a circuit model, the Ebers' model [23] (Fig. 9). The principle of operation of a proposed p-n-p-n switch was that a p-n-p transistor (bottom) is driving an n-p-n (top) and, in turn, the n-p-n is driving the p-n-p. The collector of the one, either one, drives the base of the other. That produces a positive feedback that is guaranteed to yield instability. When the voltage from A to K (A+ to B-) reaches avalanche breakdown of the "n-p" diode (between R_1 and R_2 in Fig. 9) and sufficient current flows in emitter shunt resistors R_1 and R_2 to bias "on" the emitters, the sum of α_{PNP} and α_{NPN} approaches unity, and to maintain current continuity, switching to low voltage occurs. The two collectors switch from reverse to forward voltage, and to the "on" state of the A-K switch, which, of course, is still not a p-n-p-n switch in a single "slab" of Si.

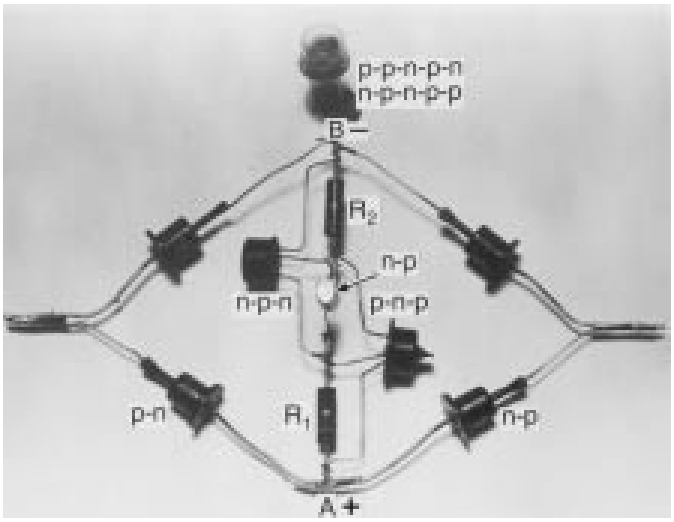

Fig. 9. Circuit model of a p-n-p-n switch [23].

The first prototype of an actual "Silicon Controlled Rectifier" (SCR) was demonstrated in 1957. The SCR became a huge success for General Electric. It was reported in the press by *Business Week* in their December 28th issue, under the headline "New Way to Change AC to DC". Commercial SCRs were on the market in early 1958 [25] and Bill Gutzwiller was responsible for their technical and promotional support.

Nowadays, the SCR family consists of: SCR – Thyristor; ASCR – Asymmetrical SCR; RCT – Reverse Conducting Thyristor; LASCR – Light Activated SCR (or LTT – Light Triggered Thyristor); DIAC & SIDAC – both forms of trigger devices; BOD – Breakover Diode or Diode Thyristor (a gateless thyristor triggered by avalanche current); TRIAC – Triode for Alternating Current (a bidirectional switching device); BRT – Base Resistance Controlled Thyristor; SITh – Static Induction Thyristor (or FCTh – Field Controlled Thyristor) containing a gate structure that can shut down anode current flow; LASS – Light Activated Semiconducting Switch; GTO – Gate Turn-Off Thyristor; MCT – MOS Controlled Thyristor (has two additional FET structures for on/off control); IGCT – Integrated Gate Commutated Thyristor; ETO – Emitter Turn-Off Thyristor. The last four are thyristors with forced turn-off capabilities.

VI. Discussion And Comments

An interesting question to be discussed is: who really invented the transistor? This question can be answered in different ways. There were many preceding discoveries (starting with the isolation of "silicium" by Jakob Berzelius in 1824) and inventions that were used in the development of the transistor by the BTL group. The work of J.C Bose [6], Pickard [26], Adams [27] etc. should be seriously considered.

The work of Russell Ohl and his discovery of the p-n junction and the photovoltaic effect about 73 years ago [4], [5] during the investigation of silicon rectifiers used in radar detectors, should also be given credit. Although accidental, the discovery of the p-n junction was one of the critical inventions for the further development of semiconductor electronics.

Another experimenter of this era who deserves far greater credit is Dr Julius Lilienfeld from Germany, who, in the early 1930s, patented the concept of a field-effect transistor (FET). He believed that applying voltage to a poorly conducting material would change its conductivity and thus amplification can be achieved. Lilienfeld is justly renowned for his work on the electrolytic capacitor, but according to his patents [1]-[3] he should also be recognized for his pioneering work on semiconductors. He created his non-tube device around 1923, with one foot in Canada and the other in the USA. The date of his Canadian patent applications was October 1925. These patents were followed by American ones, which should have been familiar to the Bell Labs patent office. Lilienfeld demonstrated his remarkable tubeless radio receiver on many occasions. He followed his 1925 (Canadian) and 1926 (American) patent applications for a "Method and Apparatus for controlling Electric Currents" with another granted in 1933. US patent 1,900,018 [2] clearly describes the field-effect transistor, constructing it using thin film deposition techniques and using dimensions that became normal when the metal-oxide FET was indeed mass-produced well over 30 years later. The patent (and subsequent ones) describes the advantages of the device over "cumbersome vacuum tubes".

The next question here is how should be evaluated the "Transistron" invented by Herbert Mataré and Heinrich Welker (Fig. 10) in early 1948, while working at

Westinghouse Subsidiary in Paris [28]. The first germanium devices with a negative Hall coefficient capable of amplification were developed in July of 1948 (Fig. 11). The diode and transistor production was based on the ceramic holder design. Manufacturing started immediately. The complete production was sold to the French telecommunications laboratories and the military.

On April 21, 1948, Mataré applied for a patent in the United States, which was granted on May 8, 1951. On August 13, 1948, Westinghouse applied for a French patent that was granted on March 26, 1952.

The more we study the history of an invention, the fewer examples we find of entirely new devices conceived and perfected by one individual in isolation.

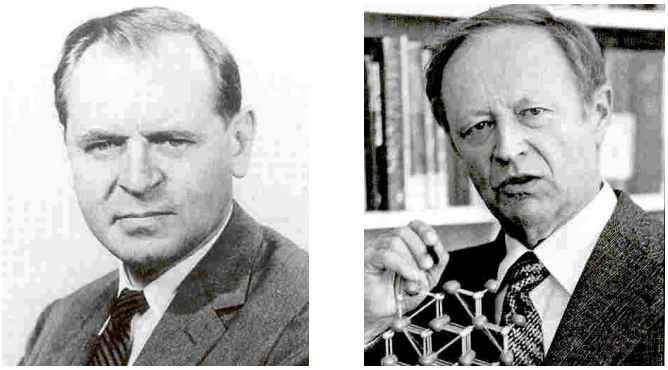

Fig. 10. Herbert Mataré (left) and Heinrich Welker (right).

Fig. 11. First European transistor constructed in June 1948 in France.

Looking at the existing documents, we might get the impression that Bell Labs did not invent the transistor, but that they re-invented it. Yet, what is more important is that they succeeded in its practical realization, although they were not the only ones to do so. The fact that they completely failed to acknowledge the pioneer work done by others could be explained in different ways. It is perfectly true that the world was not ready for the previous incarnations of the transistor, but that was no reason to deny the fact that Lilienfeld patented the original solid-state triode oscillator/amplifier well before others claimed all the credit.

Moreover, the most important "re-invention" of the 20th century remarkably occurred twice—and independently. On account of the secrecy surrounding the Bell Labs device until late June 1948, it is highly unlikely that Mataré and Welker knew anything about it before July 1948. And it seems clear from the still-sketchy historical record that they had really had a working, reliable device by that time.

This dual, nearly simultaneous breakthrough may be attributed in part to the tremendous wartime advances in purifying silicon and, in particular, germanium. In both cases, germanium played the key role, as in the immediate postwar years it could be refined much more easily and with considerably higher purity than silicon. Such high-purity semiconductor material was absolutely necessary for fabricating the first transistors. But the Bell Labs team had a clear advantage with their better physical understanding of how the electrons and holes were flowing inside germanium. This proved crucial to the following achievements. The first among them was Shockley's junction transistor, which was much easier to manufacture with much higher reliability and homogeneity.

However, regardless of who invented the transistor, the BTL group initiated the semiconductor revolution, which has completely changed our way of life. Many new semiconductor components followed the BJT: FETs, MOSFETs, thyristors and the whole family of power electronics devices, integrated circuits etc. They have enabled the design and production of many different types of electric and electronic equipment that have become indispensable in contemporary life.

VII. In Lieu of a Conclusion

Since the beginning of semiconductor electronics the number of transistors in an integrated circuit has been doubling approximately every 18 months. This exponential trend was first described by Gordon Moore [19] and has become known as Moore's Law. In Fig. 12 the number of transistors in successive Intel processors is plotted as a function of time [29].

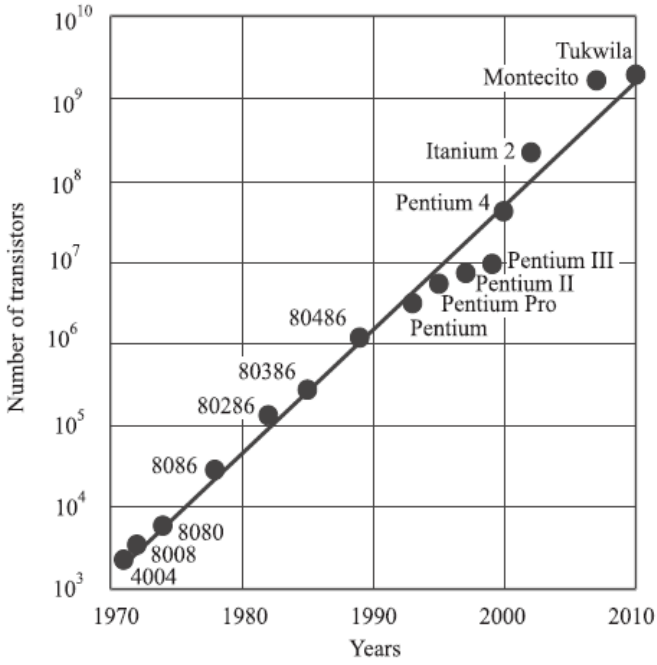

Fig. 12. Number of transistors in successive Intel processors as a function of time [29].

The capabilities of many digital electronic devices are strongly linked to Moore's Law: processing speed, memory capacity, sensors and even the number and size of pixels in digital cameras. All of these have been improving at (roughly) exponential rates as well. This exponential improvement has dramatically enhanced the impact of digital electronics on nearly every segment of the world economy.

Although nowadays over 90 percent of integrated circuits are manufactured in CMOS technology, Moore's Law is still true in many aspects of the development trends of semiconductor microelectronics (with the appropriate time constant). The MOS transistor has been improved countless times but it has also been miniaturized exceeding all expectations.

The reduction in feature size, as shown in Fig. 13, has been more or less exponential. As a matter of fact, the current technology allows solid matter to be manipulated at the molecular and atomic level. So, the production and use of nano-scaled systems has become feasible.

It should also be noted that the number of transistors produced per year and the average cost, shown as a function of time in Fig. 14, have been changing exponentially, as well. In fact, in 2010, more than a billion transistors were produced for every person living on the Earth.

But, it does not end here. Nowadays, extensive research is being carried out in different areas (materials and devices): graphene, organic electronics, quantum devices, microsystems, integration of silicon with other materials and many other issues. Thus, many improvements and new discoveries are to be expected in the very near future.

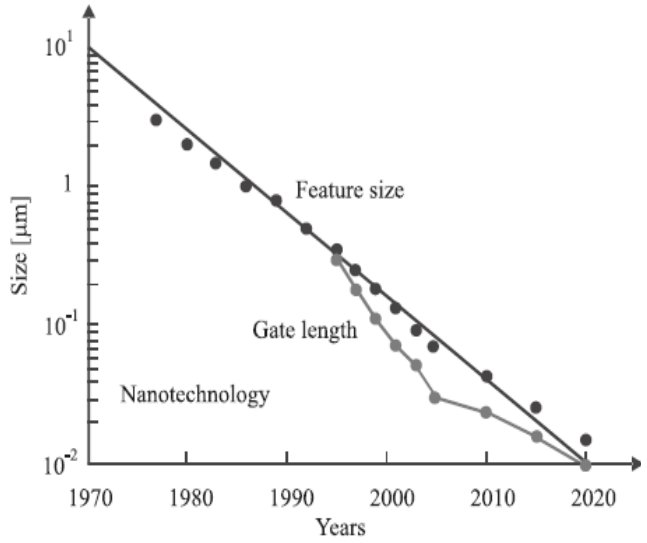

Fig. 13. *Feature size as a function of time* [30].

Therefore, there is no need to discuss the importance of the invention of the transistor for the development of electronics in the last 65 years. It is quite obvious from the fact that electronic equipment nowadays permeates all aspects of our lives.

So, in lieu of a conclusion, the words of Robert Wallace, said at a BTL meeting on the problems in emulating the vacuum tube, are given here [32]: "Gentlemen, you've got it all wrong! The advantage of the transistor is that it is inherently a small size and low power device. This means that you can pack a large number of them in a small space without excessive heat generation and achieve low propagation delays. And that's what we need for logic applications. *The significance of the transistor is not that it can replace the tube but that it can do things that the vacuum tube could never do!*"

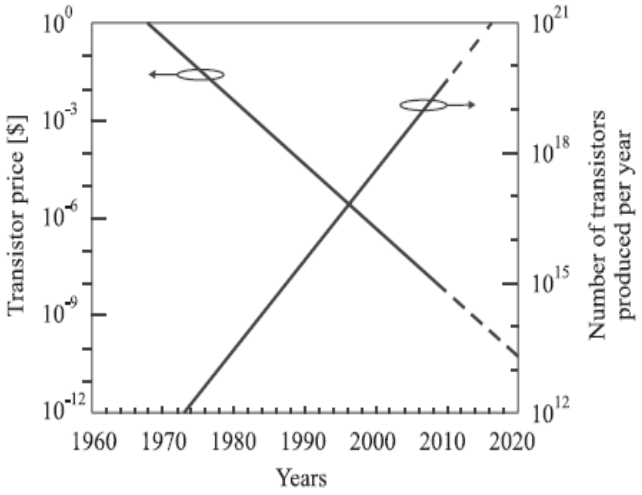

Fig. 14. Number of transistors produced per year and transistor price as a function of time [31].

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The author wishes to express his sincere gratitude to Prof. Vladimir Katić from the University of Novi Sad, Serbia, for his very helpful comments and suggestions.

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An Operational Standpoint in Electrical Engineering

Frédéric Rotella and Irène Zambettakis

***Abstract*—In electrical engineering education exists a major difficulty for first level students, namely the Laplace transform. The question is: does this ubiquitous tool is needed in an electrical engineering course? Our answer is: Obviously, not. Based on an operational standpoint the paper describes some guidelines and results for a primer on handling signals and linear systems without using the Laplace transform. The main advantage is that the operational standpoint leads to simplified proofs for well-known results.**

***Index Terms*—Transfer operator, operational calculus, Laplace transform, Carson transform, signal generator, Heaviside, Mikusiński.**

Original Research Paper
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I. Introduction

In signal processing, electrical engineering or automatic control the Laplace transform is used as an ubiquitous tool. First level courses in electrical engineering or basic textbooks on these areas contain lessons on properties and uses of Laplace transforms. For instance, in automatic control the Laplace transform approach leads to define the Laplace transform of a signal or the transfer function of a system. On the one hand it is used to get the corresponding response signal of a system with respect to a given input signal. On the other hand it is important for the analysis and design of control systems [14]. This tool appears thus as a necessary and unavoidable burden for students participating in electrical engineering courses. Nevertheless, the induced mathematical background leads to some problems for teachers from a pure educational standpoint [7], [27], [27] For instance, one of the conclusions of [27] is "*that the Laplace transform is one of the most difficult topics for learning engineering electric circuit theory.*"Roughly speaking, the difficulty arises with the connection between mathematical framework and physical world. However, this transform has some skeletons-in-the-closet [33], [40]. In this article, we discuss an alternative approach to the use of Laplace transform. This approach is based on a pure operational standpoint which has been proposed more than a century ago by Oliver Heaviside. Based on this standpoint an automatic control course has been detailed in [51], [52].

In the following, we describe guidelines for starting a course without using the Laplace transform. The presentation is based on the use of a pure operational point of view that provides an opportunity to link methods developed in electrical engineering with experiments and applications. The paper is organized as follows. In a first part we remind some well-known problems about the use of Laplace transform in operational calculus. Among engineers and mathematicians Heaviside appears, in the historical developments of operational calculus, as the focal point. His ideas on the use of the differential operator and on the definition of the transfer (*resistance*) operator are the basis of guidelines for an engineering course without the Laplace transform. A particular subsection is devoted to Oliver Heaviside. The second part deals with the transfer operator definition. Let us insist here that it must not be confused with the transfer function definition which can be related to the frequency response only. This point is detailed in the third part of the paper. The next part is devoted to some linear models analysis. For instance, we point out that poles and zeros meaning, DC gain calculus or error analysis are obvious within our approach. The final part talks about a recent application of operational calculus, namely algebraic estimation.

The essential proofs based on Laplace transform theorems can be read in standard textbooks on automatic control (*e.g.* [24], [28], [36]). Nevertheless, we will see that the operational standpoint leads to simplified proofs of well-known results.

Concerning the notation, we consider signals as elements belonging to the set C of integrable real valued functions $f = \{f(t)\}$, supposed to be m times continuously differentiable on $[0, \infty)$ except at isolated points where it is assumed that both left limit and right limit exist. As $\{f(t)\}$ denotes the signal f while $f(t)$ stands for its value at time t, we write for two signals a and b in C: for all $t \geq 0$, $a(t) = b(t)$, or $\{a(t)\} = \{b(t)\}$, or $a = b$. However, when no confusion is possible the braces or "for all $t \geq 0$" may be dropped.

II. Operational Calculus

Let us consider a signal $x(t)$ defined for a positive time t and satisfying some appropriate growth conditions. The Laplace transform of $x(t)$ is

$$X(s) = \mathcal{L}\{x(t)\} = \int_0^\infty x(t)e^{-st}\mathrm{d}t, \tag{1}$$

where s is a complex variable. This definition requires advanced mathematical machinery [40], [56] which is very demanding, and usually, beyond the skills of most undergraduate students. This generates difficulties that lead desertion of students from basic electrical engineering classes. Equation (1) assumes that all considerations, diagrams and developments are embedded in a space of transformed signals. Students ask frequently two questions in regards to the usefulness of equation (1). How can we experimentally exhibit or visualize the

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transformed signals for example by mean of an oscilloscope? Are some signals forbidden in controlled systems or linear electronics? For instance, $\exp(t^2)$ has no Laplace transform [43].

Some fundamental theorems linked to Laplace transform have also provided some misunderstandings about the actual meaning of s. For instance, consider the Laplace transform of a derivative function with the initial condition $x(0)$, namely, $\mathcal{L}\{\dot{x}(t)\} = sX(s) - x(0)$. When $x(0)$ vanishes the complex variable s is considered as a time derivative operator. However, it just stands in the space of transformed signals only. Concerning definition (1), the lower limit of integration is often replaced by 0^-, 0^+, or $-\infty$ [14], [36], [46] to overcome discontinuity problems arising in case of particular functions. An attempt to solve this question and to unify the Laplace formalisms is proposed in [38]. For the ∞ case, we are faced with the bilateral Laplace transform, which is questionable as well [40]. The purpose of this article is to show that the mathematical machinery required by the Laplace transform [57] can be avoided. Moreover, the pedagogic difficulty can be cleared in a natural way.

When the transfer function of a linear system has to be defined, Laplace transform is applicable. For a single-input single-output system the transfer function is defined as the quotient of the Laplace transform of the output $y(t)$ to the Laplace transform of the input $u(t)$ with the assumption of zero initial conditions. In other words, the transfer function is defined by

$$F(s) = \frac{\mathcal{L}\{y(t)\}}{\mathcal{L}\{u(t)\}} = \frac{Y(s)}{U(s)}.$$

Although the name *transfer function* as a mathematical tool is adequate for $s = j\omega$, where $j^2 = -1$ and ω is the frequency [3], [29], this *ad-hoc* definition generates some interesting questions. The Laplace transform of signals cannot be obtained in practice, and sometimes we wonder how to determine the transfer function of a system? For instance this question is avoided in identification procedures [37] which use ARMAX models involving recurrence relationships instead of transfer functions. In several high quality textbooks on discrete-time systems (*e.g.* [2]), the complex variable z of the Z-transform [32] and the shift-forward operator q are both used. However, the choice between z and q is not always argued. So this subtle differences, which is mysterious for students, is not really useful. According to our personal experience in teaching automatic control, it is very important to be able to give an experimental meaning of the transfer of a system, irrespective of previous formal definitions. In practice students often forget to relate the transfer to the differential operation induced by the system. Indeed, the use of Laplace transforms leads to the diagram depicted in Figure 1 which describes the relationship between the Laplace transforms of input and output signals and the transfer function $F(s)$ of the system. But this formalism hides the time variable and, there is no different notations between signals and systems. So, the essential meaning is lost. The reader can already notice that with the forthcoming developments we will not use anymore the term *transfer function* but just *transfer* for the transfer model of a system.

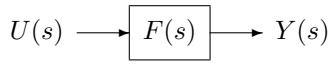

Fig. 1. Basic block diagram.

III. Historical Standpoint

As a matter of fact, the use of Laplace transforms is one method among many others [35], [39] to justify the Heaviside operational calculus (Figure 2). Note that the operational calculus is used to solve differential equations (in most cases linear) rather than automatic control problems. The history of the Laplace transform has been studied extensively by Deakin [9], [10]. It has been first introduced in the form (1) by Bateman in 1910 to solve the differential equation $\dot{x}(t) = -\lambda x(t)$ where λ is a nonzero real number.

Nevertheless and independently, Oliver Heaviside (1850-1925), electrical engineer at the Great Northern Telegraph Company, has introduced a pure operational calculus. His seminal works have been collected in two books :

- *Electrical Papers*, 1873→1891;
- *Electromagnetic Theory*, 3 volumes, 1891→1893 (*ET1*), 1894→1898 (*ET2*), 1900→1912.

During his life he brought great breakthroughs on different electrical or electromagnetic topics such as :

- Maxwell's field equations. He reworded them in terms of electric and magnetic forces and energy flux. The use of vector analysis to write them as a fourth-order system is due to Heaviside. Consequently, the well-known Maxwell equations should be known as the Maxwell-Heaviside equations;
- atmospheric layers. He predicted the existence of ionized layers by which radio signals are transmitted around the Earth's curvature. The existence of the ionosphere was confirmed in 1923 only. These layers are bearing the name KennellyHeaviside;
- transmission lines. He developed and patented (1880) the coaxial cable;
- fractional derivatives. He introduced a 1/2-order derivative operator to modelize a diffusive process;
- operational calculus. The major part of its ideas about operational calculus are gathered together in *ET2*. The writing is oriented for practice :
  - "*Of course, I do not write for rigourists but for a wider circle of readers who have fewer prejudices,*"(*ET2*);
  - "*There is, however, practicality in theory as well in practice.*"(*ET1*)

  while the proposed developments lead him to name his method "*my operational method*".

The interested reader about life and works of Oliver Heaviside can see the following biographies : G. Lee, *Oliver Heaviside*, 1947; H.J. Josephs, *Oliver Heaviside ; a biography*, 1963; G.F.C. Searle, *Oliver Heaviside, the man*, 1987; P.J. Nahin, *Oliver Heaviside : sage in solitude*, 1988; I. Yavetz, *From obscurity to enigma : the work of Oliver Heaviside*, 1995. Let us briefly, describe the Heaviside operational method.

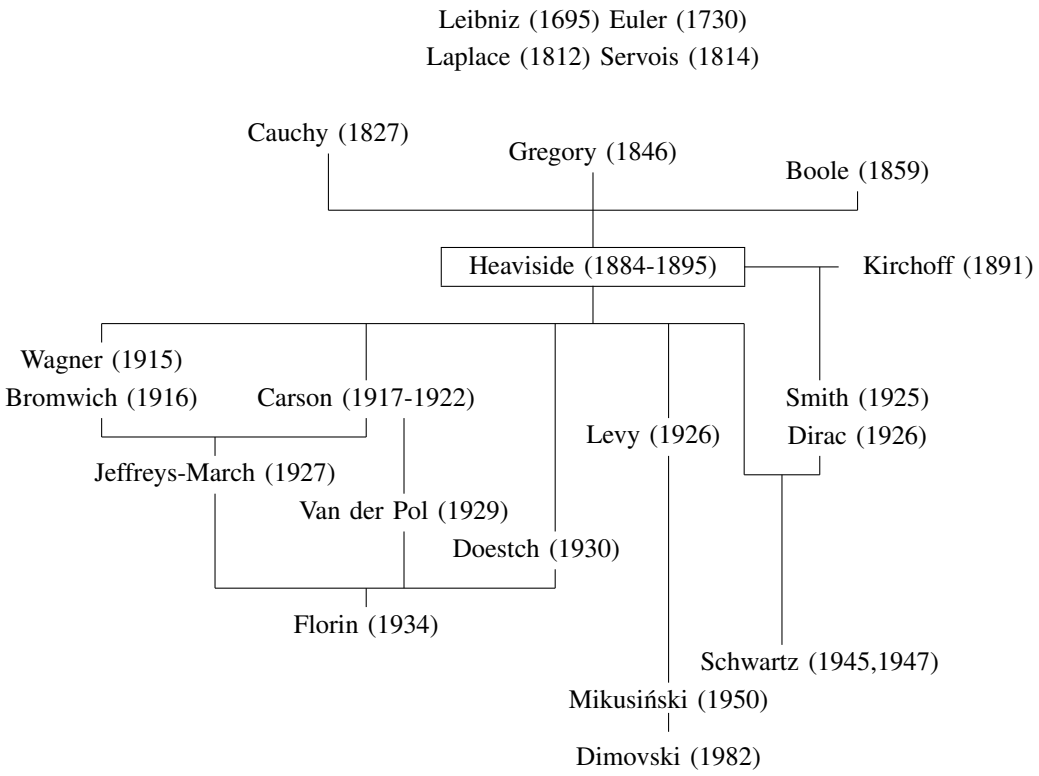

Fig. 2. Genealogy of operational calculus. This diagram is detailed in (Rotella, Zambettakis, 2006). Date indicates publication year of a major contribution in operational calculus.

1) *Coding*. Introducing the derivative operator

$$\frac{\mathrm{d}}{\mathrm{d}t} \triangleq D \text{ (before 1886)} \triangleq p \text{ (after 1886)},$$

he codes a linear differential equation (1884) for an electrical circuit or every system that can be, by analogy, reduced to an electrical circuit. In this framework, he points out the *resistance operator*, namely the transfer operator, $Z(p)$ to defines the *operational solution* $C = \dfrac{E}{Z(p)}$ where C et E are the output and input voltage respectively.

2) *Algebrization*. When E is fixed at the outset he proposes different methods to get the solution of the differential equation. For example, let E be the Heaviside function or step signal $H(t)$ defined by $H(t) = 1$ for $t \geq 0$ and 0 elsewhere. Using the *expansion theorem* (1886) he gets

$$C = \frac{E}{Z(0)} + E \sum_k \frac{e^{\lambda_k t}}{\lambda_k Z'(\lambda_k)},$$

where $Z(\lambda_k) = 0$. Later on, using the series expansions with respect to p (1888)

$$C = \sum_{n \geq 0} \alpha_n p^n H(t),$$

and supposing $p^n H(t) = 0$ he gets $C = \alpha_0$. Then, using the series expansions with respect to p^{-1} (1892)

$$C = \sum_{n \geq 0} a_n p^{-n} H(t),$$

and because $p^{-n} H(t) = \dfrac{t^n}{n!}$ he gets

$$C = \sum_{n \geq 0} a_n \frac{t^n}{n!};$$

In 1895, he deals with the sinusoidal input $E = \sin(nt) = \Im(\exp(nt))$. Using of the Euler shifting theorem

$$\varphi(p) e^{at} f(t) = e^{at} \varphi(p + a) f(t),$$

he proposes to solve the differential equation by successively replacing p with ni and, then i with $\dfrac{\mathrm{d}}{\mathrm{d}(nt)}$.

Let us consider for example The RL circuit with $Z(p) = R + Lp$. For the input $E = H(t)$, the expansion theorem yields

$$Z(0) = R,\ k = 1,\ \lambda_k = -\frac{R}{L},\ Z'(\lambda_k) = L,$$

thus

$$C = \frac{E}{R}\left(1 - e^{-\frac{Rt}{L}}\right).$$

The series expansion with respect to p^{-1} leads to

$$\begin{aligned} C &= \frac{E}{Lp} \frac{1}{1 + \frac{R}{Lp}}, \\ &= \frac{E}{Lp}\left(1 - \frac{R}{Lp} + \frac{R^2}{L^2 p^2} - \cdots\right), \\ &= \frac{E}{R}\left(1 - e^{-\frac{Rt}{L}}\right). \end{aligned}$$

For the input $E = \sin(nt)$, the successive replacements method induces

$$\begin{aligned} C &= \frac{1}{R+Lp}\sin(nt) = \frac{R-Lni}{R^2+n^2L^2}\sin(nt), \\ &= \frac{R}{R^2+n^2L^2}\sin(nt) - \frac{Ln}{R^2+n^2L^2}\frac{\mathrm{d}}{\mathrm{d}(nt)}\sin(nt). \end{aligned}$$

Despite the fact that Oliver Heaviside was disapproved by mathematicians, at the begining of the twentieth century the operational calculus became a high challenge. For instance, in 1928 E.T. Whittaker quotes

"*We should now place the operational calculus with Poincaré's discovery of automorphic functions and Ricci's discovery of the tensor calculus as the three most important mathematical advances of the last quarter of the nineteenth century. Applications, extensions and justifications of it constitute a considerable part of the mathematical activity of today.*"

Justifications of the operational calculus (see [39], [47] and references therein) can be gathered together in two different kinds of methods : on the one hand the integral transforms such as the Laplace transform and, on the other hand the algebraic methods based on the Paul Lévy standpoint linked to the integral operator. These last ones, which to our point of view are the only ones to preserve the practical meaning have lead to the Mikusiński operational calculus. In the sequel we carry on with the way paved by Heaviside approach, keeping in mind that the mathematical background must not cover up the practical meaning.

IV. Transfer Operator

We begin by considering a linearized system around an equilibrium point. We suppose this system can be described by the linear differential equation

$$\begin{aligned} &y^{(n)}(t) + a_{n-1}y^{(n-1)}(t) + a_{n-2}y^{(n-2)}(t) + \cdots \\ &+a_1y^{(1)}(t) + a_0y(t) = \\ &b_mu^{(m)}(t) + b_{m-1}u^{(m-1)}(t) + \cdots \\ &+b_1u^{(1)}(t) + b_0u(t), \end{aligned} \tag{2}$$

where $y(t)$ and $u(t)$ stand for the differences of output and input signals with their setpoint values respectively and n and m are two integers. In (2) the coefficients a_i and b_j are constant parameters.

A. Coding

The aim is to provide a tool making easy the manipulation of linear time-invariant differential equations and, which allows to separate input and output variables from the system. Following Heaviside [30], [47] or Carson [5], we introduce the *derivative operator*

$$p \triangleq \frac{\mathrm{d}}{\mathrm{d}t},$$

which applied on $x(t)$ in C gives the codings

$$\dot{x}(t) = px(t),\ \ddot{x}(t) = p^2x(t), \ldots,\ x^{(n)}(t) = p^nx(t), \ldots \tag{3}$$

In view of these codings and using the distributivity property we get, for every real numbers α and β,

$$[\alpha p^n + \beta p^m]x(t) = \alpha x^{(n)}(t) + \beta x^{(m)}(t).$$

So, equation (2) becomes

$$\begin{aligned} &\left[p^n + a_{n-1}p^{n-1} + a_{n-2}p^{n-2} + \cdots + a_1p + a_0\right] y(t) = \\ &\left[b_mp^m + b_{m-1}p^{m-1} + \cdots + b_1p + b_0\right] u(t). \end{aligned} \tag{4}$$

To separate input and output signals from the system we divide equation (4) by the polynomial factor $p^n + a_{n-1}p^{n-1} + \cdots + a_0$, which yields to code the input-output relationship as $y(t) = F(p)u(t)$ with

$$F(p) = \frac{b_mp^m + b_{m-1}p^{m-1} + \cdots + b_1p + b_0}{p^n + a_{n-1}p^{n-1} + a_{n-2}p^{n-2} + \cdots + a_1p + a_0}. \tag{5}$$

We must insist here that $y(t) = F(p)u(t)$ cannot be considered as the solution of the differential equation (2). Indeed, the initial conditions are not known. $y(t)$ is determined with this writing as with the writing (2). In equation (5), $F(p)$ stands for the transfer operator. In essence, it is the transfer, which represents the operation induced by the system to transform the input signal into the output signal. The operational approach provides an opportunity to relate the transfer operator (5) to the differential equation (2). The diagram, depicted in figure 3, corresponds to an experimental situation. Notice that, in this figure, t denotes the time variable and p the derivative operator. The difference between signals and system is due to the use of these notations. The action performed by a system on an input signal is retained. The essential meaning of the transfer $F(p)$ is the linear differential equation that links the output signal to the input signal.

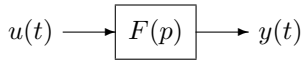

Fig. 3. Operational block diagram. The output signal $y(t)$ is obtained by $F(p)u(t)$ where $u(t)$ is the input signal.

B. Operational Calculus As Polynomial Calculus

Operational calculus is understood as algebraic methods for solving differential or recurrence equations, specifically in a linear time-invariant framework. In our point of view solving a differential equation for a given input is a mathematical exercise only [40]. In electrical engineering or, more generally, in automatic control operational calculus means rules for transfer connections or decompositions through polynomial calculus. Thus the coding (4) is useless when we are not allowed to associate transfer operators. From the operational standpoint the connection rules can be demonstrated through the following steps. The transfers of the connected system provide differential equations. The connections and the elimination of intermediate signals lead to a differential equation between the output and input signals. The encoding of this differential equation with p ensures the results. Although we can use this procedure in every case, it is sufficient to exemplify it with respect to series or parallel connections for two first-order systems.

Let us consider such two linear systems described by $y_1(t) = F_1(p)u_1(t)$ and $y_2(t) = F_2(p)u_2(t)$ where $u_1(t)$ and

$u_2(t)$ are the input signals, $F_1(p)$ and $F_2(p)$ the transfers of the systems, and $y_1(t)$ and $y_2(t)$ the corresponding output signals. In this regard, we have

$$F_1(p) = \frac{b_1 p + b_0}{a_1 p + a_0} \text{ and } F_2(p) = \frac{\beta_1 p + \beta_0}{\alpha_1 p + \alpha_0},$$

where a_0, a_1, b_0, b_1, α_0, α_1, β_0, and β_1 are constant parameters. The series connection is defined by $u_2(t) = y_1(t)$, $u(t) = u_1(t)$, and $y(t) = y_2(t)$. The application of the procedure yields

$$y(t) = \frac{\beta_1 b_1 p^2 + (\beta_0 b_1 + \beta_1 b_0)p + \beta_0 b_0}{\alpha_1 a_1 p^2 + (\alpha_0 a_1 + \alpha_1 a_0)p + \alpha_0 a_0} u(t),$$

where we recognize the product $F_1(p)F_2(p)$. The parallel connection is defined by $u_2(t) = u_1(t) = u(t)$ and $y(t) = y_1(t) + y_2(t)$, which yields

$$y(t) = \frac{\begin{array}{r}((a_1\beta_1 + \alpha_1 b_1)p^2 + (a_1\beta_0 + b_1\alpha_0 + a_0\beta_1 \\ + b_0\alpha_1)p + (a_0\beta_0 + b_0\alpha_0))\end{array}}{\alpha_1 a_1 p^2 + (\alpha_0 a_1 + \alpha_1 a_0)p + \alpha_0 a_0} u(t),$$

where we recognize the sum $F_1(p) + F_2(p)$. These results can be extended to any order by induction, thus the transfer of the series connection of two systems is the product of their transfer and the transfer of the parallel connection of two systems is their sum.

Parallel and series rules give a meaning to the decompositions and the handling of transfer operators with polynomial calculus. These operations on transfer operators are the basis of operational calculus in automatic control. We can apply usual techniques as Mason's rule associated to the signal-flow graphs [41]. This operational calculus can be applied also for multiple-input multiple-output systems with the difference that commutativity does not occur anymore. Let us note that the polynomial formalism is used in several textbooks on multivariable systems [33], [34] with no need of the Laplace transform.

C. The Delay Operator

A pure time delay of T between input and output signals induces $y(t) = u(t - T)$. This particular linear system cannot be associated to a differential equation as (2). A special treatment must be used for delay equations. Following an idea of Euler [15], the Taylor expansion of $u(t - T)$ yields

$$u(t-T) = u(t) - \dot{u}(t)T + \ddot{u}(t)\frac{T^2}{2} - \cdots + u^{(n)}(t)\frac{(-T)^n}{n!} + \cdots,$$

which is encoded to give

$$\begin{aligned} y(t) &= u(t) - pTu(t) + p^2\frac{T^2}{2}u(t) - \cdots + p^n\frac{(-T)^n}{n!}u(t) + \cdots, \\ &= \left(\sum_{n\geq 0}\frac{(-pT)^n}{n!}\right)u(t) = (\exp(-pT))\,u(t). \end{aligned}$$

We obtained the transfer operator for the time delay T as $F(p) = e^{-pT}$.

V. System Responses

System analysis is often the study of some particular responses of the system and, specially, the step and frequency responses.

A. Step Response

The step response of a system is the solution of the differential equation of the system to a step input signal with zero initial conditions. With operational calculus, we can expand transfer operator as a linear combination of simple transfers

$$\frac{a^n}{(p+a)^n} \text{ or } \frac{1}{p^n},$$

where a stands for a nonzero complex number and n for an integer. The step response of a multiple integrator with the transfer $\frac{1}{p^n}$ is $\frac{t^n}{n!}$. Let us consider the step response $s_n(t)$ of the Strejć system [48] with the transfer $\frac{a^n}{(p+a)^n}$. For $n = 1$ the associated differential equation to the transfer $\frac{a}{p+a}$ is $ay(t) + \dot{y}(t) = au(t)$ and we obtain by usual methods [61] the corresponding response to a given input $u(t)$ with the initial condition $y(0)$

$$y(t) = e^{-at}\left(y(0) + a\int_0^t e^{a\nu}u(\nu)\mathrm{d}\nu\right).$$

For $u(t) = 1$ and zero initial conditions the step response becomes

$$s_1(t) = 1 - e^{-at}.$$

For $n = 2$ we have $s_2(t) = \frac{a}{p+a}s_1(t)$ from which it follows

$$s_2(t) = ae^{-at}\int_0^t (e^{a\nu} - 1)\,\mathrm{d}\nu = 1 - e^{-at}(1 + at). \quad (6)$$

For the general case $n \geq 1$, let us suppose

$$s_n(t) = 1 - e^{-at}\left(\sum_{i=0}^{n-1} c_{i,n}t^i\right),$$

and

$$s_{n+1}(t) = 1 - e^{-at}\left(\sum_{i=0}^{n} c_{i,n+1}t^i\right),$$

where the coefficients $c_{i,n}$ and $c_{i,n+1}$ are constant parameters. These signals are linked by the differential equation

$$\dot{s}_{n+1}(t) + as_{n+1}(t) = as_n(t),$$

which leads to the the relationships $c_{0,n+1} = 1$ and, for $i = 1$ to n,

$$c_{i,n+1} = \frac{a}{i}c_{i-1,n} = \frac{a^i}{i!}.$$

We deduce the well known result that, for the Strejć model, $\frac{a^n}{(p+a)^n}$, the step response is

$$s_n(t) = 1 - e^{-at}\left(\sum_{i=0}^{n-1}\frac{a^i t^i}{i!}\right).$$

So, the step response of a given system defined by a transfer operator can be calculated using polynomial calculus.

Stability analysis does not use the Laplace transform. However, we may insist again on the link between the transfer operator, the differential equation and the transient behavior. Let us consider the transfer operator $\frac{a^n}{(p+a)^n}$ where a and n have the same meaning as before. From the previous paragraph we can see that the step response is composed of a constant term and a time-dependent term. The first term is the forced response and the second term is the transient behavior. The transient behavior tends asymptotically to zero if and only if the real part of a is strictly negative. More generally, consider the n-th order transfer

$$F(p) = \frac{b_m p^m + \cdots + b_1 p + b_0}{(p-p_1)^{\rho_1}(p-p_2)^{\rho_2}\cdots(p-p_r)^{\rho_r}},$$

where $p_1, p_2, \ldots, p_r$ are the r complex poles of $F(p)$ and ρ_i are the respective multiplicities with $n = \sum_{i=1}^{r} \rho_i$. The poles generate terms associated with the signals $e^{p_1 t}, e^{p_2 t}, \ldots, e^{p_r t}$ weighted by time polynomials of order $\rho_i - 1$ respectively. So, when all the poles have strictly negative real part, the transient behavior tends asymptotically to zero. Namely, the system is asymptotically stable.

B. Frequency Response

For asymptotically stable systems the frequency response is deduced from the steady-state output response to a given sinusoidal input signal $u(t) = e^{j\omega t}$ where ω is the frequency and $j^2 = -1$. Consider a system defined by the transfer operator $F(p) = \frac{B(p)}{A(p)}$ where $A(p)$ and $B(p)$ are two polynomials. The operational approach leads to the encoded input-output differential equation as $A(p)y(t) = B(p)u(t)$. For the sinusoidal input $u(t) = e^{j\omega t}$, we obtain

$$B(p)u(t) = |B(j\omega)|\, e^{j(\omega t + \arg(B(j\omega)))},$$

where $|B(j\omega)|$ and $\arg(B(j\omega))$ denote the module and the argument of the complex number $B(j\omega)$ respectively. The output $y(t)$ is the sum of a particular solution of the differential equation and the general solution of the differential equation without second member. The general solution characterizes the transient response that vanishes in case of asymptotically stable systems. For a particular solution, we look for the steady-state behavior as the form $y(t) = Ye^{j(\omega t+\varphi)}$ where Y and φ are constant parameters. Replacing this expression for $y(t)$ in the differential equation yields

$$Y = \frac{|B(j\omega)|}{|A(j\omega)|} = |F(j\omega)|\,,$$
$$\varphi = \arg(B(j\omega)) - \arg(A(j\omega)) = \arg(F(j\omega)).$$

The frequency response is defined by the evolution of $(|F(j\omega)|\,, \arg(F(j\omega)))$ as the frequency ω varies from 0 to $+\infty$. We can notice that $F(j\omega)$ is the transfer function of the system such as Harris defined it [29]. In our standpoint, this transfer function must not be confused with the transfer operator $F(p)$. Nevertheless, $F(j\omega)$ such as a function of the frequency is the only actual transfer function. Graphic representations such as Bode, Black-Nichols, or Nyquist loci may be used to analyze the frequency response [36]. For unstable systems the loci are valid as calculated representations only. While for stable systems experiments can allow to get the frequency response as well.

VI. Analysis

A. Poles and Zeros

The names of poles and zeros come from the interpretation of a transfer operator $F(p)$ as a function of a complex variable p. This interpretation is a consequence of the formulation of Laplace transform and it misunderstands the physical meaning of these notions. The consideration of a transfer operator as a coding of a differential equation provides an immediate physical interpretation. Namely, let us consider the transfer operator

$$F(p) = \frac{p+a}{p+b}, \tag{7}$$

where a and b are constant parameters. In the operational standpoint the transfer (7) corresponds to the input-output differential equation $\dot{y}(t)+by(t) = \dot{u}(t)+au(t)$ where $y(t)$ and $u(t)$ are the output and input signals. First, consider $u(t) = 0$ for $t > 0$ and a nonzero initial condition $y(0)$ we then get $y(t) = y(0)e^{-bt}$ for $t > 0$. Second, consider a zero initial condition for the output and the input signal $u(t) = e^{-at}$ for $t > 0$ we obtain $\dot{u}(t) + au(t) = 0$ so $y(t) = 0$ for $t > 0$.

More generally, poles correspond to signals generated by the system with zero input. Zeros correspond to signals absorbed or blocked by the system. Let us write the transfer operator (5) as

$$F(p) = k\frac{(p-z_1)^{\nu_1}(p-z_2)^{\nu_2}\cdots(p-z_d)^{\nu_d}}{(p-p_1)^{\rho_1}(p-p_2)^{\rho_2}\cdots(p-p_r)^{\rho_r}},$$

where $k = b_m$, z_i, $i = 1, \ldots, d$ and p_i, $i = 1, \ldots, r$ are complex numbers, and ν_i, $i = 1, \ldots, d$ and ρ_i, $i = 1, \ldots, r$ are integers. For $i = 1, \ldots, r$, $e^{p_i t}$ is solution of the coded differential equation

$$(p-p_1)^{\rho_1}(p-p_2)^{\rho_2}\cdots(p-p_r)^{\rho_r} y(t) = 0,$$

and for $i = 1, \ldots, d$, $e^{z_i t}$ is solution of the coded differential equation

$$(p-z_1)^{\nu_1}(p-z_2)^{\nu_2}\cdots(p-z_d)^{\nu_d} u(t) = 0.$$

On the one hand we can use the correspondence between $e^{p_i t}$ and the transfer denominator roots p_i that characterizes the transient rate in the linear constant parameter framework only. The same remark can be said about the correspondence between $e^{z_i t}$ and the transfer numerator roots z_i. On the other hand this signal approach for the pole and zeros meaning can be extended to time-varying or nonlinear multivariable systems with an algebraic standpoint [16], [17].

In order to underline and to exemplify the important problem of pole/zero cancellation let us consider the series

connection with the systems :

$$y(t) = \frac{1}{p-1}u(t),$$
$$z(t) = \frac{p-1}{p+1}y(t).$$

The pole 1 induces, in the transient behavior or in the initial conditions effect for the first system, an e^t signal. This signal is blocked by the second system, which has 1 as zero. As $\lim_{t\to\infty} e^t = \infty$, this fact forbids such a connection. Indeed, while the input and output signals are zero, there exists in the system a non observed and non controlled unbounded signal. The conclusion is different if we consider the series connection with the systems :

$$y(t) = \frac{1}{p+1}u(t),$$
$$z(t) = \frac{p+1}{p-1}y(t).$$

Due to the pole/zero cancellation at -1, $y(t)$ has an e^{-t} component that vanishes at ∞. Except during the transient behavior, the pole/zero cancellation is acceptable for asymptotically stable canceled zeros.

B. DC Gain

Let us keep in mind that the transfer operator $F(p)$ in equation (5) is just a coding of the differential equation (2). In the case of an asymptotically stable system, with a constant value U as input, the step response analysis indicates that the output tends, as t goes to $+\infty$, to a constant value Y given by the relationship $a_0Y = b_0U$. The ratio $\frac{Y}{U}$ defines the DC gain of the system G_{DC} . The stability condition implies $a_0 \neq 0$, and from (5) we obtain $G_{DC} = F(0)$.

C. Steady-State Error Analysis

In all this section systems are supposed to be asymptotically stable, namely the transient behavior vanishes and only the permanent behavior remains. For the reference inputs $r_i(t)$ defined by, for $t > 0$, $r_i(t) = \frac{t^i}{i!}$, and for $t < 0$, $r_i(t) = 0$, the corresponding outputs are $y_i(t) = F(p)r_i(t)$. The input-output error $\varepsilon_i(t) = r_i(t) - y_i(t)$ is called the system error of order i. Two notions can be pointed out here. First a norm of the instantaneous system error $\varepsilon_i(t)$ characterizes the system performance. Secondly, the value $\varepsilon_i(\infty) = \lim_{t\to\infty} \varepsilon_i(t)$ during the permanent behavior characterizes the steady-state error. In a basic lecture of automatic control this last notion is usually considered. We detail it according to our formulation, namely without the use of the final value theorem.

A steady-state error of order N is ensured if $\varepsilon_i(\infty) = 0$, for $i = 0$ to N, and $\varepsilon_{N+1}(\infty) \neq 0$. Consider the transfer operator $F(p)$ of an asymptotically stable system defined in (5). The corresponding permanent step response value is given by the DC gain $\frac{b_0}{a_0}$, so $\varepsilon_0(\infty) = 0$ if and only if $b_0 = a_0$. Thus we conclude that a steady-state error of zero order is fulfilled whether the DC gain is equal to 1. In other words since the input-error transfer is $1 - F(p)$, we obtain a steady-state error of zero order when the input-error DC gain is zero. This is a fundamental remark for the following.

Let us notice that $r_1(t)$ is the integral of $r_0(t)$. Namely, $r_1(t) = \frac{1}{p}r_0(t)$, thus we have

$$\begin{aligned}\varepsilon_1(t) &= r_1(t) - y_1(t),\\ &= \frac{1}{p}r_0(t) - F(p)\frac{1}{p}r_0(t),\\ &= \frac{1-F(p)}{p}r_0(t).\end{aligned}$$

Clearly, from the previous result for $\varepsilon_0(\infty)$, $\varepsilon_1(\infty)$ vanishes if and only if the DC gain of the transfer operator $\frac{1-F(p)}{p}$ is equal to zero. Since

$$\frac{1-F(p)}{p} = \frac{(a_0-b_0)+(a_1-b_1)p+(a_2-b_2)p^2+\cdots}{p(a_0+a_1p+a_2p^2+\cdots+a_np^n)}$$

we obtain $\varepsilon_1(\infty) = 0$ if and only if $a_0 = b_0$ and $a_1 = b_1$. It can be seen that :

- when $a_0 \neq b_0$, we have $\varepsilon_0(\infty) \neq 0$ and $\varepsilon_1(\infty) = \lim_{p\to 0} \frac{a_0-b_0}{pa_0} = \pm\infty$;
- when $a_0 = b_0$, we obtain $\varepsilon_0(\infty) = 0$ and $\varepsilon_1(\infty) = \frac{a_1-b_1}{a_0}$. Moreover, $\varepsilon_1(\infty) = 0$ when $a_1 = b_1$.

In the same way we can show by induction that the system has a steady-state error of order N if and only if its transfer $F(p)$ in equation (5) is such that, for $i = 0$ to N, $a_i = b_i$. The steady-state error of order $N+1$ is then

$$\varepsilon_{N+1}(\infty) = \frac{a_{N+1}-b_{N+1}}{a_0},$$

and the next ones have an infinite module. Thus, the degree of the steady-state error can be obtained just by a visual inspection of the transfer operator of the system.

VII. Algebraic Estimation

Recently, M. Fliess and his co-workers [21], [22], [42] have proposed new methods to estimate the parameters of a system or the first derivatives of a measured signal. For instance, the last point is implemented in a model-free control of a system [19], [20]. These methods are based on operational calculus. According to the presented operational framework of our paper, let us describe the used skills for the particular case of derivative estimation.

Firstly, the signal $s(t)$ is approximated on a short-time window $[-T, 0]$ with the polynomial :

$$s(t) = s_0 + s_1t + s_2t^2, \tag{8}$$

where s_1 stands for the estimation of the first derivative, $s_1 = \widehat{\dot{s}(0)}$.

Secondly, the time functions 1, t and t^2 are associated to operational forms, namely, their signal generators.

A. Signal Generators

The main reason of using the Laplace transform is the tables we have at our disposal. Firstly, they contain information to determine the response of a system with respect to a given input signal. Secondly, they allow to get the discrete transfer operator of a computer controlled system with a formula given in [52]. Although transforms are not used in our presentation, we show that these tables can be used without any change. To do that, let us introduce the notion of generator of a continuous signal, which consists in writing the time expression of this signal by means of the operator p.

The previous parts show that the transfer operator allows to link input $u(t)$ and output $y(t)$ signals of a linear system by a differential equation coded as $y(t) = F(p)u(t)$. Until now, we get the step response by solving this differential equation when initial conditions are all zero. In case of no input and non zero initial conditions, such a transfer operator produces an output signal solution of the associated homogeneous differential equation. The coding of this differential equation with the p operator defines then the generator of this signal. Two ways can be considered to take into account initial conditions in this coding. Namely, on the one hand the Mikusiński operational calculus and on the other hand the integral form of a differential equation.

Indeed, all the previous developments can be rigorously proved by means of operational calculus of Mikusiński [44], which is based on convolution algebra of operators. Let us briefly describe this operational calculus whereas keeping in mind that the considerations below are not needed in a first level course. Convolution product is a fundamental tool in dynamic systems field [54], [55], specifically in case of linear systems [11], [25]. This tool is defined by

$$(f, g) \mapsto gf = \int_0^t f(\tau)g(t-\tau)d\tau,$$

while the Heaviside function $H = \{1\}$ is of great importance due to the fact that we have for every f in the set of integrable function C

$$Hf = \left\{ \int_0^t f(x)\mathrm{d}x \right\}.$$

Consequently, H appears as the integration operator. The successive powers of H with respect to the convolution product are, for all n in $\mathbb{N}$, $n \geq 1$,

$$H^n = \left\{ \frac{t^{n-1}}{(n-1)!} \right\}.$$

To distinguish a constant signal $\{\alpha\}$ with the operator defined by the constant gain α we denote it $[\alpha]$. For all f in C

$$\{\alpha\} f = \left\{ \alpha \int_0^t f(\tau)d\tau \right\} \text{ and } [\alpha] f = \{\alpha f(t)\}.$$

The unit element for the convolution is $[1]$ and we can give a meaning to H^0 as $H^0 = [1]$. We define then the derivative operator as the solution of the convolution equation $pH = [1]$, and we write $p = H^{-1}$. With the understanding $p^0 = H^{-0} = [1]$, we have $p^n = H^{-n}$ for n in $\mathbb{N}$.

Mikusiński [44] has proved the two results below, which are essential to our purpose.

Theorem 1 *For every continuous function f in C, $\left\{f^{(1)}(t)\right\} = pf - [f(0)]$. More generally, for every integer k*

$$\left\{f^{(k)}(t)\right\} = p^k f - \sum_{i=0}^{k-1} \left[f^{(i)}(0)\right] p^{k-i-1}. \tag{9}$$

Theorem 2 *For every f in C such that $\int_0^\infty e^{-tp} f(t)dt$ exists*

$$f = \int_0^\infty e^{-tp} f(t)dt.$$

Theorem 1 allows to write the generator of a signal $\{f(t)\}$ when the differential equation whose this signal is solution is known. Indeed, let us suppose that this differential equation is

$$\sum_{i=0}^{n} \alpha_i f^{(i)}(t) = 0, \tag{10}$$

with initial conditions $f(0) = f_0, \dot{f}(0) = f_1, \ldots, f^{(n-1)}(0) = f_{n-1}$, where n is an integer and the α_i are real numbers. With (9) the coding of (10) leads to

$$\left[\sum_{i=0}^{n} \alpha_i p^i\right] f(t) - P_{\text{IC}}(p, f_0, \ldots, f_{n-1}) = 0,$$

where $P_{\text{IC}}(p, f_0, \ldots, f_{n-1})$ is a polynomial in p that depends on the initial conditions and the coefficients α_i. We obtain then the generator of $\{f(t)\}$

$$\{f(t)\} = \frac{P_{\text{IC}}(p, f_0, \ldots, f_{n-1})}{[\sum_{i=0}^{n} \alpha_i p^i]}. \tag{11}$$

Theorem 2 indicates that when the one-sided Laplace transform of a signal exists, its expression is identical to the generator of the signal, the complex variable s of Laplace transform being changed into the derivative operator p (to avoid any confusion). A major consequence is that the tables [13], [58], can be used. Since $H = p^{-1}$ we remark that the generator can be written indifferently with the operators H or p.

For example, when we look for the generator of $\sin(\omega t)$, we have just to observe that $\sin(\omega t)$ is the solution of the differential equation

$$\ddot{x}(t) + \omega^2 x(t) = 0,\ x(0) = 0,\ \dot{x}(0) = 1. \tag{12}$$

Using (9) the coded form is then

$$p^2 x(t) - 1 + \omega^2 x(t) = 0,$$

which leads to the generator of $\sin(\omega t)$

$$\{\sin(\omega t)\} \underset{\text{M}}{=} \frac{1}{p^2 + \omega^2},$$

where the symbol "M" denotes "in the Mikusiński sense".

Indeed, this definition for the generator of a signal is not unique because it depends on the used integral transformation. For instance, the reader can find in [52] another way to handle

a differential equation which leads to the signal generator of $f(t)$ in the Carson sense. It is based on the result below [53]

$$\{\dot{x}(t) = f(t),\ x(0) = x_0\} \text{ if and only if } x(t) = x_0 + \int_0^t f(\tau)\mathrm{d}\tau, \tag{13}$$

but for shortness sake we don't develop this point here. The Carson transform was introduced in 1926 [6] and it differs from the Laplace transform by a factor p. The Carson tables can be used in this framework as well.

Let us mention that the Mikusiński operational calculus has been extended recently by the convolutional calculus [12].

For a system defined by the transfer operator $F(p)$ we can calculate the response $y(t)$ to an input $u(t)$ by using Carson or Laplace transform tables. Indeed when $U(p)$ is a generator of $u(t)$ the generator of the output $y(t)$ is $F(p)E(p)$. We must remark here that the generators can be obtained in any sense as defined (Mikusiński or Carson). However, we must keep the consistency in using tables. For example, following the Heaviside series expansion, when we want to know the beginning of the response we can write the power series with respect to p^{-1} of the generator of $y(t)$. However, different functions may be associated to p^{-k} according to the adopted generator sense.

Moreover, in order to see the importance of the generator for operational calculus, let us consider the following example where two signals y_1 and y_2 are defined by the differential equations

$$(p-1)y_1(t) = u(t), \tag{14}$$

$$(p-1)y_2(t) = u(t), \tag{15}$$

and the initial conditions y_1^0 and y_2^0 respectively. Let us consider the parallel connection $y(t) = y_1(t) - y_2(t)$. It yields

$$y(t) = \frac{1}{p-1}u(t) - \frac{1}{p-1}u(t) = 0.$$

This conclusion is obviously wrong. Indeed, our setting indicates that we consider formal differential equations, namely, without initial conditions. When we write

$$y(t) = \frac{1}{p-1}u(t),$$

it is just a coding of differential equations (14) and (15). The initial conditions can be taken into account by means of the generator notion. We can write (14) and (15) as, respectively,

$$y_1(t) \underset{M}{=} \frac{1}{p-1}u(t) + \frac{y_1^0}{p-1},$$

$$y_2(t) \underset{M}{=} \frac{1}{p-1}u(t) + \frac{y_2^0}{p-1},$$

in the Mikusiński's generator sense. It yields for $y(t) = y_1(t) - y_2(t)$ the generator

$$y(t) \underset{M}{=} \frac{y_1^0 - y_2^0}{p-1}.$$

This result indicates that $y(t)$ is solution of the differential equation

$$(p-1)y(t) = 0,\ y(0) = y_1^0 - y_2^0,$$

or, equivalently, $y(t) = (y_1^0 - y_2^0)e^t$.

This standpoint can also be explained in a more algebraic framework as the Fliess'module-theoretic approach [18]. Nevertheless, let us quote a sentence of a recent paper [22] where this point of view is used for the design of an algebraic identification procedure : "*Let us add we tried to write the examples in such a way that they might be grasped without the necessity of reading the sections on the algebraic background. Our standpoint on parametric identification should therefore be accessible to most engineers.*"

B. Derivative Estimation

Let us associate to the signal $\frac{t^n}{n!}$, $n \geq 0$, its signal generator in the Mikusiński sense $\frac{1}{p^{=}n+1}$. The polynomial approximation (8) of a signal $s(t)$ can then be written

$$s(t) = s_0\frac{1}{p} + s_1\frac{1}{p^2} + s_2\frac{1}{p^3}.$$

To obtain s_1 let us follow the steps :

1) Multiply with p^3

$$p^3 s(t) = p^2 s_0 + p s_1 + s_2.$$

2) Derivate with respect to p

$$3p^2 s(t) + p^3 s'(t) = 2p s_0 + s_1,$$

where $s'(t)$ stands for $\frac{\mathrm{d}s(t)}{\mathrm{d}p}$.

3) Divide with p

$$3p s(t) + p^2 s'(t) = 2s_0 + \frac{s_1}{p}.$$

4) Derivate with respect to p

$$3s(t) + 5p s'(t) + p^2 s''(t) = -\frac{s_1}{p^2}.$$

As p^2 stands for a double time-derivative it cannot be implemented. Thus, the following step consists in a division with p^3. So, we obtain the operational estimation

$$3p^{-3}s(t) + 5p^{-1}s'(t) + p^{-1}s''(t) = -p^{-5}s_1.$$

Notice that the use of a sufficient number of time-integrals induces noise filtering.

In order to implement the derivative estimator we have then to come back in the time domain. There is no difficulty to translate the time-integrals on $[-T, 0]$

$$-p^{-5}s_1 = -\frac{T^4}{24}s_1,$$

$$\frac{1}{p^3}s(t) = \int\int\int s(\tau)\mathrm{d}\tau = \int \frac{(t-\tau)^2}{2}s(\tau)\mathrm{d}\tau.$$

For the other terms we must prove in a operational way the following well known result

$$\frac{\mathrm{d}^k}{\mathrm{d}p^k}s(t) = (-1)^k t^k s(t). \tag{16}$$

For simplicity sake, let us consider the signal

$$x(t) = \sum_{\nu=0}^{\infty} x^{\nu}(0)\frac{t^{\nu}}{\nu!}.$$

With the signal generators $\dfrac{t^{\nu}}{\nu!} = \dfrac{1}{p^{\nu+1}}$, we get

$$x(t) = \sum_{\nu=0}^{\infty} x^{\nu}(0)\frac{1}{p^{\nu+1}},$$

which leads to

$$\begin{aligned}
\frac{\mathrm{d}}{\mathrm{d}p}x(t) &= -\sum_{\nu=0}^{\infty}(\nu+1)x^{\nu}(0)\frac{1}{p^{\nu+2}},\\
&= -\sum_{\nu=0}^{\infty}(\nu+1)x^{\nu}(0)\frac{t^{\nu+1}}{(\nu+1)!},\\
&= -\sum_{\nu=0}^{\infty}x^{\nu}(0)\frac{t^{\nu+1}}{\nu!},\\
&= -t\sum_{\nu=0}^{\infty}x^{\nu}(0)\frac{t^{\nu}}{\nu!}.
\end{aligned}$$

Thus $\dfrac{\mathrm{d}}{\mathrm{d}p}x(t) = -tx(t)$. It is easy to state the announced result (16) by induction.

We can then state the final form of the derivative estimation as

$$\widehat{s^{(1)}(0)} = -\frac{24}{T^4}\int_{-T}^{0}\left[\frac{3}{4}T^2 - \frac{13}{2}Tt + \frac{27}{4}t^2\right]s(t)\mathrm{d}t.$$

An example of a real-time application is given in figure 4 where we show the signal corrupted with noise and the real-time estimation of its derivative.

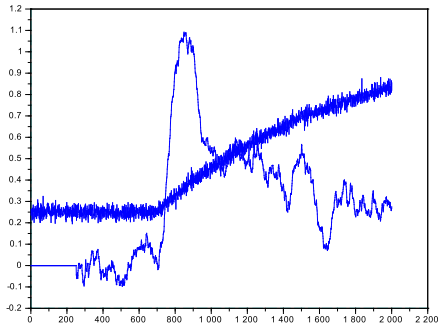

Fig. 4. Algebraic derivative estimation.

VIII. Conclusion

We show in this short survey that from the use of the differential operator we obtain all the usual results derived by means of the Laplace formulations. The teaching of a basic lecture in electrical engineering and in automatic control using the operational method offers some advantages. The integral or derivative operators allow to link every notion to its physical meaning. We keep in mind that a transfer operator is always related to a differential equation. Mathematical background is minimized, however, when a rigorous justification is needed the Mikusiński operational calculus may be used. This operational calculus is based on the convolution operator, which is a natural tool for linear equations.

Moreover, we meet here, through a pedagogical step, the operational standpoints adopted directly in some advanced textbooks to modelize the input-output relationship induced by a linear system. For instance, the discrete-time autoregressive moving-average model $A(q^{-1})y_k = B(q^{-1})u_k + C(q^{-1})\epsilon_k$ where $A(q^{-1})$, $B(q^{-1})$, and $C(q^{-1})$ are polynomials in the delay operator, $\{\epsilon_k\}$ a noise signal, is used in [1], [8] for identification purposes to describe the difference equation between the sampled input u_k and the sampled output signals y_k of a given system. For multivariable continuous-time linear systems the following model is introduced in [49], [59], [60]

$$\begin{aligned}
P(p)\xi(t) &= Q(p)u(t),\\
y(t) &= R(p)\xi(t) + W(p)u(t),
\end{aligned}$$

where $P(p)$, $Q(p)$, $R(p)$, and $W(p)$ are matrix polynomials in the differential operator and $\xi(t)$ is a vector-valued function of time named the partial state. More recently, the generator of a multivariable system is defined in [4] as the polynomial matrix $M(p)$ in the derivative operator, which allows to write the relationship between input and output signals as $M(p)\begin{bmatrix} y(t) \\ u(t) \end{bmatrix} = 0$. The generator in the sense defined in [4] must not be confused with signal generators. The interested reader can see the quoted literature.

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Project-Based Learning and Agile Methodologies in Electronic Courses: Effect of Student Population and Open Issues

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***Abstract*—Project-Based Learning (PBL) and Agile methodologies have proven to be very interesting instructional strategies in Electronics and Engineering education, because they provide practical learning skills that help students understand the basis of electronics. In this paper we analyze two courses, one belonging to a Master in Electronic Engineering and one to a Bachelor in Telecommunication Engineering that apply Agile-PBL methodologies, and compare the results obtained in both courses with a traditional laboratory course. Our results support previous work stating that Agile-PBL methodologies increase student satisfaction. However, we also highlight some open issues that negatively affect the implementation of these methodologies, such as planning overhead or accidental complexity. Moreover, we show how differences in the student population, mostly related to the time spent on-campus, their commitment to the course or part-time dedication, have an impact on the benefits of Agile-PBL methods. In these cases, Agile-PBL methodologies by themselves are not enough and need to be combined with other techniques to increase student motivation.**

***Index Terms*—Project-based learning, agile methodologies, scrum, engineering education, electronics.**

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I. Introduction

ENGINEERING education is one of the most modern sciences, specially when compared to physics, mathematics or medicine. However, the teaching methods have been historically dominated by the "chalk talk", emphasizing the teaching of the mathematical and physical background. However, according to a report by the Career Space Consortium [1], industry demands today's engineers to apply their knowledge in real-life situations. Moreover, personal and business skills, including team work skills, are considered to be an important part of the curriculum. Thus, university education needs to provide students with hands-on experiences and practical learning skills, that enable them to become competitive graduate students.

This need becomes particularly important in telecommunication and electronic engineering studies, because of the mixture of computer science, signal processing and communications courses. Hands-on experiences and practical scenarios help students understand the basis of electronics, as well as the design and integration phases of a product, and need to be a key part in the engineering education program.

Because of the particular needs of engineering education in general and electronics in particular, Project Based Learning (PBL) and Agile methodologies become very interesting instructional strategies. When adopting PBL in the classroom, the benefits sought are: the usage of a student-centric approach that allows the development of interdisciplinary skills (i.e. planning, team work or the learning of tools such as version control systems) and its beneficial impact on student motivation.

Agile methodologies, such as Scrum [2], outline methods for flexible and adaptable software development. Even though these methods come from the business pressure on software development companies, they have moved into the academic world quite fast, mainly because of their beneficial results on student learning and motivation. However, because they are initially thought to be applied to the industry world, the principles of the Agile Manifesto [3] need to be mapped into pedagogical principles [4].

In this paper we analyze and evaluate the results of applying Scrum and PBL in two electronic engineering courses of the Electronic Engineering Department at Universidad Politécnica de Madrid. The main teaching goals pursued when introducing these methodologies in the classroom are the following:

- Engaging students in real-world tasks, with realistic constraints in economic cost and development effort, that enable them to handle complex systems. From the electronic perspective, a whole team working on the design and implementation of a solution provides more work power than individuals. Students need to learn how to tackle cost and time design constraints, by negotiating the scope of a project with customers without a penalty in the quality of the solution.
- Cooperation and team work in a self-regulated environment. Students should be able to organize themselves, dividing the work in a way that enables them all to learn, and then integrate work together to deliver a solution. For an effective team work, they need to understand the benefits of good planning and the usage of development tools, e.g. software version control tools.
- A better understanding and learning of electronic design,

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that delivers high-quality solutions to a problem. Students are faced to a problem that needs to be solved. They have to learn new techniques in the areas involved in the design and implementation of their solution. To match the customer requirements, they have to take decisions during the design process, coping with incompleteness and imprecise information.

- Leveraging creativity and pro-activeness: students are encouraged to find their own solutions to a problem, either by becoming proficient in certain areas, or by seeking the advice of experts (i.e. instructors).

The Electronic Engineering Department where this courses are taught, has a comprehensive background on PBL strategies and many years of experience in several courses of the electronics area [5]. More recently, the Scrum Agile development framework started to be used as teaching methodology in one undergrad PBL course. Until 2011, all PBL courses were part of the electronics curriculum of undergrad students. However, a couple of years ago, an Scrum PBL course also started to be taught in the master of science on electronic engineering. The contents of both courses, the undergrad and the master course are similar in terms of the contents taught: both focus on embedded systems design, covering from the system architecture and interface design to the programming of microcontrollers and drivers, and sensor conditioning.

In this work we evaluate Scrum-based Agile-PBL methodologies in two different courses, one undergraduate and one master course, with similar teaching goals from the electronic curricula perspective, but in which the students' profiles are very different, specially in terms of their dedication and engagement to the course. We analyze the influence of some population factors such as student motivation, group cohesion and part-time study in the results of Agile approaches in engineering courses. We show the impact of accidental complexity in our methodology, i.e. problems due to inefficient team works, planning, tool complexity, or any other impediment that diverts the attention from the electronics learning process. We analyze how this complexity affects the instructors and reduces the amount of time spent in really useful electronics-related problem solving, and propose contention methods to minimize the impact of accidental complexity.

We discuss solutions to the above mentioned problems and propose a Project-and-Problem Based Learning (P^2BL) that is being applied to former students this semester. The technique consists on generating real-life problems that affect the usual PBL work flow and put students face to face to common situations in a real-world scenario that they would not encounter in a typical classroom PBL project.

The remainder of this paper is organized as follows. Section II details the related work on the topic. Section III describes the methodology followed in the two courses, whereas Section IV shows the results and discussion. Finally, the most important conclusions are drawn in Section V.

II. Related work

For years, researchers from all areas, but especially from the pedagogy and psychology fields have claimed that from a constructivist perspective, humans are active learners that construct knowledge based on their effort and experience. Vigotsky [6], one of the better-known researchers in social constructivism, highlights the importance of the social context and the interaction with others in the process of thinking that leads to learning. From his perspective, students cannot be passive subjects that absorb knowledge from an instructor. Research in the area of engineering education also supports this claim and shows that learning and retention are more likely [7] when students are actively engaged in the learning experience. These works support that student-centric approaches, including PBL learning or Agile methodologies, which involve the student in the learning process, are likely to increase student motivation. In general, the feedback provided by students is very positive and the impact on learning is large [8]. Applying Agile methodologies to engineering courses implies the mapping of principles from the Agile Manifesto to the classroom. Previous work by Stewart et.al. [4] shows how this mapping can be done, and the considerations needed to be taken into account in the teaching scenario.

Most of the experiences in PBL applied to engineering education have focused on computer science courses for software development [9], [10]. Fewer approaches tackle the implementation of PBL and Agile methodologies in electronic design, hardware or hardware-software integration [11]. In order to design and implement complex systems, the project is developed by a group of students, between 7 and 14. However, complex systems and more manpower means more complexity in the project management. Because of the nature of the problems encountered by electrical and electronic engineers in the real world, applying PBL and Agile methodologies to electronics is particularly beneficial. On the one hand, it enables students to manage more complexity and face design decision problems with constrained costs and effort. On the other hand, professors have daily feedback checking the methodology reports and the group is focused on the achievement of the sprint goal.

The most common metric to evaluate the beneficial impact of PBL and Agile methodologies in education is student satisfaction, quantified by means of questionnaires filled in by students [12]–[14]. Moreover, research by Layman et.al. tries to correlate the appeal of Agile techniques with the personality types and learning styles of students [15]. Even though several works only provide the metric of student perception, others complement the data with course marks obtained by students [16], or even by monitoring the student activity (e.g. via version control tools) to identify metrics that would allow instructors to act proactively and identify patterns of low engagement and inefficient team work [17]. We propose the usage of both metrics, i.e. student satisfaction and students marks, in a quantitative way to measure the benefits of Agile methodologies in two different courses, and compare results to those obtained in traditional courses.

Several works highlight in a qualitative way the most common issues found, such as the quality of the results being dependant on certain people, or the difficulties encountered to evaluate the time spent by students to learn and complete assignments [14]. Research by Kagan. et al. [18] highlights the

importance of the teacher in the management of issues and considers him the customer that, within the scope of Agile methodologies, is part of the project team and establishes and negotiates the system requirements. Our work leverages this concept by analyzing the impressions of students and instructors, comparing the results obtained in the two PBL courses with traditional courses to understand the different problems that students encounter and how they can be solved. Moreover, we evaluate the impact on team work of part-time students enrolled in PBL courses.

III. Method

In this section we present the method followed in the two Agile-PBL courses under study, providing information on the structure of the study and the teaching goals, the project to be undertaken and the assessment.

A. Scope of the study and teaching objectives

The two Agile-PBL courses under study are respectively LSEL ("Laboratory of Electronic Systems") undergraduate course and LSE ("Laboratory of Embedded Systems") Master course. LSEL belongs to the Bachelor of Telecommunication Engineering, whereas LSE belongs to the Master of Electronic Engineering. Both courses are elective, take place during the winter semester, and the average number of students enrolled in each course is 10. In this paper we analyze the results corresponding to the last two academic years: 2011 and 2012.

The program of both courses is similar and covers the following topics:

- Electronic system architecture design, including the integration of various systems, and the design of their interfaces
- Design and implementation of sensors and actuators
- Microcontroller programming and communication protocols
- Linux device drivers programming
- Development of automatic benchmarks to test and debug the system

Moreover, because students work in groups to pursue certain goals, they are also required to:

- Learn to use software version control tools to share code with their team mates
- Analyze and measure the amount of time spent in tasks
- Division of complex tasks in simpler ones
- Tasks planning and effort estimation in terms of manpower
- Development of communication skills to interact with their team mates in an effective way.

From a pedagogical perspective, the particular goals that the professors of these courses pursued when implementing the methodology were the following:

- To propose the students a real-life project, similar to one they could face in industry, with more ambitious goals and a broader scope than other projects proposed in traditional pair-programming laboratories.
- To teach students a collection of new techniques regarding planning, code sharing, collaboration, team work and management.
- Motivate students towards electronics, leveraging proactiveness and creativity, letting them take their own design decisions according to the different abilities of the team.
- Understanding and learning the basics of electronic design and programming by devoting time to think and interact with the team members, producing high-quality solutions to problems.

B. Project undertaken and methodology

All the students in the course have to carry out together a complex project. The projects undertaken vary depending on the course and the academic year, but have the same methodology and planning, and the tasks they have to perform are similar. For the purpose of clarification, we briefly describe the projects developed by students in the courses and years under study: i) an automated model train that travels at variable speed depending on the traffic signaling in the railway and stops in each station, respecting barriers, ii) the electronic control of a car, including a motherboard that controls sensors (temperature, rain, doors opened) and actuators (lights, automatic cleaners, airbag, ABS, etc.) via a CAN bus; and iii) an intelligent house with automatic lights, flooding sensors, fire and security alarms that alert the owners via e-mail or SMS.

At the beginning of the course, the objectives of the project as well as the teaching goals are presented to students. There is just one team in the course, composed of all the students enrolled. The teacher plays the role of a customer, and discusses with the team the scope of the project. Once students and instructor agree on the requirements of the product, they generate a product backlog and students organize themselves, naming a team leader, and distributing themselves to different tasks.

Following the Scrum methodology, the project is divided into 5 sprints, each one with a duration of 2 weeks. In each sprint, tasks are prioritized according to the customers' needs and students estimate the effort needed to complete each task. The time per week devoted by students to the project is fixed below a maximum by the teacher, so the scope is flexible and can be modified by negotiating with the instructor. Depending on the effort estimation, students are committed to develop a certain number of tasks for that sprint. Tasks are further divided into sub-tasks and assigned to specific students or groups.

Students are required to hold weekly team meetings that allow them to be aware of the evolution of the overall project. Because the course officially consists on three hours of laboratory per week, these hours are used to hold the weekly meetings and discuss with the instructors. Students are also asked to track the time they devote to each sub-task in the sprint, so that in every meeting impediments and bottlenecks can be easily spotted. They also need to fill-in the sprint burndown chart every day, that indicates the total remaining team task hours within one sprint.

In the present method, the teacher plays multiple roles: customer, advisor and expert in the field. Scrum methodology includes two special roles, that are performed by two students: the Product Owner and the Scrum Master. The Scrum Master is responsible for the correct implementation of the methodology by the team, the preparation of the Scrum tool, checking that it is being used properly, and the fostering of the team interaction. The Product owner is responsible for the communication with the client in order to solve impediments that might appear. The course does not have a fixed amount of theory classes, but students are advised to request teachers a theory lesson when they need more background on a certain topic. These lessons are requested at any time by the Product Owner, who negotiates the topic with the professor.

At the end of each sprint, the students present the results obtained (i.e. tasks performed) in that sprint. Students must always deliver, at least, one complete functional task per sprint. They comment the impediments and difficulties encountered and negotiate with the instructor the next tasks to be performed, the priorities and, again, estimate the effort.

At the end of the semester, the students have to make an oral presentation to the customer and the open public, presenting the work developed and the goals achieved. They also have to handle high-quality technical documentation on the solution.

C. Assessment

The assessment of the courses is divided into three different aspects. Some aspects have an impact on the final mark of the course, whereas others are just gathered for the purpose of qualitative and quantitative analysis of the PBL courses. The goal is to be able to assess the proficiency of students in the following areas:

- Delivering a product that meets the requirements of the customer.
- Learning the basic electronic concepts of the course, completing tasks with the highest possible quality given the time constraints.
- Facing the challenges proactively, proposing alternatives that lead to a solution.
- Using the planning and software version control tools provided by the instructors.

1) Teachers: Teachers evaluate the students in two different ways: i) grading the overall team and ii) grading students individually.

In each sprint, teachers evaluate the team work, in terms of the number of tasks accomplished and delivered to the customer, grading them from 0 to 10. Only functional tasks are evaluated, and marks are given depending on the degree of accomplishment of the requirements and the quality of the work. Non-functional tasks count as not delivered and are not evaluated at all.

At the end of the semester, the grades obtained by the team in each sprint are averaged. Team work evaluation mark has a weight of 40% on the overall course grade. As can be seen, final assessment is highly dependent on team work evaluation. This way, students always give more importance to task delivery and team work than to individual aspects and competitiveness within the team members.

Teachers also provide an individual grade at the end of the semester to each student. This mark has a weight of 40% on the overall course grade. It is based on the individual degree of proficiency students showed on the tasks that were assigned to them during the course, as well as on the management and team work skills exhibited.

2) Team mates: In each sprint, all the students provide an overall assessment of their team mates in terms of their ability to accomplish the assigned tasks, their team work skills, and their contribution to the project.

At the end of the semester the grades obtained by a student in each sprint are averaged. The assessment of team mates has a weight of 20% on the overall course grade.

3) Individual assessment: For teachers to gain a deeper knowledge on the learning process of students and to obtain their opinion on how profitable the course was, students have to fill-in some self-assessment questionnaires, which do not have an impact in the final mark of the course.

At the beginning of the course the students are asked to evaluate their skills in a broad range of topics, grading themselves from 0 to 10 in the following aspects: i) management skills, ii) electronic systems design, iii) electronic programming, iv) team work experience and iv) use of English

At the end of the course, they fill-in again the same questionnaire, so that teachers can analyze how much the students have learned during the course, and gain a general impression on the benefits.

IV. Results and discussion

In this section we evaluate the advantages and drawbacks of the Agile-PBL experiences when compared to other traditional laboratory courses by means of analyzing student satisfaction. We also provide a qualitative analysis of the most common issues perceived by the teachers when applying these methodologies. Furthermore, we analyze in a quantitative and qualitative way the differences between the experience in the LSE Master course and the LSEL undergraduate course, in terms of students' marks and teacher's perception.

A. Agile-PBL courses vs pair-programming laboratories

1) Quantitative analysis: At the end of the semester, all students from all courses are asked to fill-in a questionnaire to gather their opinion on metrics related to their satisfaction on the courses they have taken. The questions are the same for all courses, and students need to grade them from "0: disagree" to "5: completely agree". Here we summarize the questions that reveal to be most important to our study:

- Q1 : The workload of the course is in accordance with the amount of credits
- Q2 : The dedication needed to pass this course is in accordance with the program
- Q3 : The assessment is in accordance to the assignments
- Q4 : I've increased my knowledge in the skills described in the course program

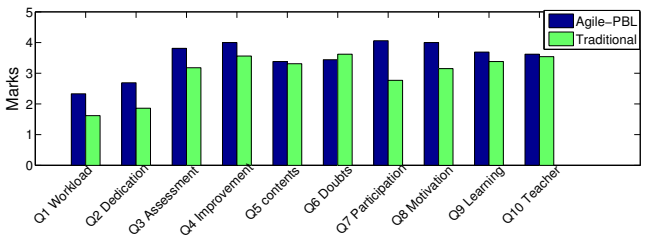

Fig. 1. Average marks in the questionnaire for the Agile-PBL undergraduate course vs an undergraduate traditional laboratory

- Q5 : The course contents are clearly explained and important topics are highlighted
- Q6 : The assistance of the professor during office hours to solve my questions has been very helpful.
- Q7 : The teacher promotes student participation and proactiveness
- Q8 : The course has motivated me
- Q9 : The professor has helped me to learn and I've increased my skills
- Q10 : The professor has fulfilled my teaching expectations

To assess student general satisfaction towards the Agile-PBL courses in a quantitative way, we compare the results obtained in this questionnaire in the LSEL Undergraduate course, with the results obtained for a traditional pair-programming electronics laboratory course of the Bachelor of Telecommunication Engineering. This traditional course is taught by the same professors than LSEL, the average number of students per course is also 10, and the contents cover similar but more basic aspects of electronic design and microcontroller programming.

Figure 1 shows the average marks obtained in the questionnaire for the students in the LSEL course when compared to the traditional course. So that the two populations are equivalent, we show the comparison only between undergraduate students (from LSEL and the traditional course), without including the Master students.

As can be seen, students belonging to the Agile-PBL undergraduate course (LSEL) give higher marks in almost all metrics, including the ones related to motivation, learning and participation. The lack of theory classes does not have an impact on the perception of students about the important topics of the course. However, the students consider that in a traditional course, their doubts are better solved during office hours.

We see that Agile-PBL methodologies outperform the metrics of student satisfaction in almost all areas. However, even though students are satisfied with the methodology, we next highlight some drawbacks spotted by the teachers.

2) Qualitative analysis: To qualitatively analyze the drawbacks of the Agile-PBL methodologies, we interview the teachers of both the Master and the Undergraduate course to know their perception. Instructors from the two courses agree on the following issues that arise when implementing agile methodologies in the classroom:

- Planning and team work organization represent an overhead to the work developed by students. For some groups it is easier to meet outside the laboratory to coordinate their tasks. For other groups, specially for Master courses, students have difficulties coordinating their work. They lose many time in planning and their organization is sometimes inefficient.
- The usage of code-sharing tools is, in general, not efficient. Students have trouble learning how to use software version control tools, do not understand the benefits and often abandon its usage.
- Accidental complexity is large and complicated to manage by instructors. By accidental complexity we understand all those impediments that are not directly correlated with the tasks assigned to students, i.e. team work issues or students not managing properly coding tools (i.e. cross-compilers, IDEs, etc.).
- Only the team leader has an overall vision of the problem, whereas the other team mates are only experts in their task. This works properly in the real-world environment, however, in the classroom, all students should learn at least the minimum important concepts of each task and understand and participate in the high-level design.

B. Master vs Undergraduate courses

The profile of students attending the master and undergraduate courses is significantly different, and this has an impact on the results of the PBL experience.

On the one hand, undergraduate students are full-time students that in most cases share classroom with their team mates in several other courses. They spend more time together in class, at the library or doing their assignments together, and thus consider themselves a group. This improves team communication and allows them to keep track on the project. They are more motivated towards innovative techniques and face Agile-PBL methodologies as a challenge.

On the other hand, Master students are generally part-time students. They spent most of their time off-campus and only meet their team mates during the laboratory sessions of other courses, or sometimes just during the weekly meetings. Communication between these teams is less fluid, and planning is worse. By investigating the time spent by the Master course teams filling-in the backlog and the burnout charts, we can observe that they tend to do these tasks in the last minute, just before the meeting. They also exhibit less proactivity and tend to demand less theory classes. The usage of software version control tools is also lower than in the Undergraduate course. Even though Master students should be more motivated towards these methodologies, because they expect to apply for a job in a very short time (some of them already work part-time), they seem less committed than the Undergraduate students. However, it is important to note that they are not less efficient than Undergraduates in completing the assigned tasks, even though their solutions have poorer quality. Regarding the individual marks assigned by teachers, the average for Undergraduate students is 8.6 on 10, whereas for Master students it decreases to 7.4 on 10.

These facts can also be observed by analyzing the marks that the students give to their mates in sprints of the Master

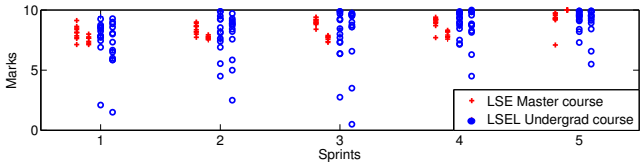

Fig. 2. Marks given by students to their team mates for each sprint, split between Master and Undergraduate courses

and Undergraduate courses (see Figure 2). The average of the marks for each sprint is similar, however, there is much more variance in the marks given by undergraduate students. As can be seen, Master students tend to always give the same mark to all students, whereas Undergraduate students are more strict and assess their fellow students with higher or lower marks depending on their commitment or the degree of task accomplishment.

C. Discussion

Generally speaking, Agile-PBL methodologies increase student satisfaction when comparing them to a traditional approach. However, instructors highlight several important issues that have to be tackled to improve the efficiency of these methodologies. Perhaps the most critical one is managing accidental complexity. To this end, we propose the development of tutorials and examples that lead the students when they learn the usage of new tools. We also believe that developing semi-automated tools to review the code written by students could help spot the main bottlenecks in the development flow and, thus, indicate instructors where to center the focus of their explanations. By reducing the accidental complexity of these methodologies, instructors will be able to focus on the real problem solving of the electronic design, thus making the learning process more efficient.

However, in the comparison between the Master and Undergraduate courses we have seen that the benefits of the methodology vary depending on the student population. Because Undergraduate students are the most proficient, we see how this issue is not correlated with the baseline knowledge. The differences between both courses are mostly related to the attitude of students: the time spent on campus and interacting with their fellow students, their commitment to the course and their motivation affect the results of Agile-PBL methodologies.

Moreover, Master students are more inclined to consider planning and Scrum an overhead, rather than a tool, and also abandon the usage of software version control tools, because they do not find a usage for that. In other words, they believe the tools provided by instructors try to solve problems that do not exist. For this particular population under study, PBL by itself does not seem to be enough. In these cases, we propose an approach based on PBL, but generating on purpose the specific problems that are found in a real-life situation in the design work flow.

That is, we propose a Project-and-Problems Based Learning (P^2BL) approach, that faces students with real-life problems that can only be solved by using the tools provided by professors. These problems might not arise during the semester, with just a dozen students, but are the reason for the development of those methodologies and tools. If students are not sufficiently motivated to embrace them with just a theoretical justification of their usage, we believe they will voluntarily adopt them when they suffer the problems they were designed to solve. This certainly constitutes an added overhead for teachers, that must design the scenarios so the problems (i.e., software conflicts, the need to recover older versions, the need to provide an accurate measure of the effort done and remaining...) arise naturally, but we expect the improvements in student progress to be worth the effort.

This new technique is being applied in the former year to the LSE Master course with the goal of improving the students results to the level of the LSEL Undergraduate course.

V. Conclusions

In this paper we have analyzed and evaluated the usage of Scrum-based agile methodologies in two Project-Based Learning courses, one belonging to a Master of Electronic Engineering course and the other belonging to a Bachelor on Telecommunication Engineering. We have seen that motivation and student satisfaction are higher when compared to a traditional course. However, there are still some open issues that negatively affect the implementation of Agile-PBL based methodologies, such as planning overhead or the accidental complexity that impedes instructors to dedicate time to real electronics design doubts and problems. We have also evaluated the differences between two different Agile-PBL courses, and showed that part-time students benefit less from these methodologies, mainly because they spend less time on campus and their commitment is lower. These students see some of the tools provided by instructors as an overhead, and are reluctant to use them. To this end, in courses where students exhibit these characteristics we propose to face them with problems that can only be solved via the usage of these tools.

Acknowledgment

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Exploring the use of Cadence IC in Education

Danijela Efnusheva, Josif Kjosev, and Katerina Raleva

***Abstract*—Microelectronics technologies and structures is electronics subfield, related to the study of integrated circuit design and fabrication. To familiarize with this widely applicable area, engineering students should gain practical experience, in addition to the theoretical knowledge attained on different microelectronics courses. Cadence IC is a world standard tool in this area, applicable not only in industry, but also in academic institutions. The academic environment of Republic of Macedonia has the ability to use this package through cooperation with foreign partners. Assuming that the access to the provided design kits is limited, the freely available NCSU CDK library from the North Carolina State University is integrated within the Cadence IC environment, and later used for educational purposes. The basic contribution of this paper is the systematization of the methodology for NCSU CDK library application by the students at FEEIT - Skopje, at both third cycle, and other levels of studies. Our general opinion is that the Cadence IC tool suite provides novel opportunities to academia and students in many educational and research activities.**

***Index Terms*—Cadence IC, CMOS inverter, integrated circuits, microelectronics, NCSU design kit, and ring oscillator.**

Original Research Paper
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I. Introduction

The process of designing integrated circuits is very demanding, especially when a complex circuit that contains a large number of transistors is going to be designed. In order to enable automation of this process, Electronic Design Automation (EDA) and Computed Aided Design (CAD) tools are used [1]. These environments are very complex and usually integrate several tools required to support different phases of the integrated circuit design flow. Cadence IC is a tool suite, commonly used for the given purpose. This environment is not only a standard in the electronics industry, but is also widely applied in many educational and research institutions around the world, [2], [3]. Despite its expensive license, academic institutions gain access to this set of tools via cooperation with various electronics companies. Universities can use Cadence IC tool suite for several purposes including education, science and industry. Actually, this paper presents the experiences in using Cadence IC tool suite within the microelectronics technologies and structures course, at the Faculty of Electrical Engineering and Information Technologies in Skopje.

The Cadence IC environment is used in many wide world universities for educational purposes. Therefore, there are a numerous tutorials and documentation about this software usability and operation, such as many laboratory exercises from a number of courses in the field of microelectronics, [4]. There are also many papers in the area of education, [2], [3], which share their experiences and provide opportunities for improving the process of learning Cadence IC as a tool suite which is commonly used in microelectronics, analog circuit design and other related courses in the electronics field.

Cadence IC enables integrated circuits design and fabrication with various technology processes, specified by the manufacturer. When a particular technology is selected, the Cadence IC environment, [4] is customized with appropriate configuration files, known as design kit. Actually, this paper describes the use of Cadence IC 5.1.41 set of tools along with NCSU Cadence design kit 1.5.1. This design kit is available free of charge from the University of North Carolina and is used to provide full-custom CMOS IC design through MOSIS. It includes several technology files which define the mask layers and their appearances and properties, as well as parameters used at library creation time which set the value of lambda, the technology code, and the availability of process-dependent layers, along with the SCMOS (Scalable Complementary metal-oxide-semiconductor) rules [5] for the given MOSIS process.

The procedure of downloading NCSU CDK 1.5.1 includes free registration on the web site: http://www.eda.ncsu.edu/wiki/NCSU_CDK_download and obtaining a link to a free version of this software on the user's e-mail address. After that, the user has the opportunity to select one of the two available versions of NCSU CDK: 1.5.1 or 1.6.0.beta. The first NCSU CDK version can be used in combination with several different versions of Cadence IC ranging from 4.4 to 5.1, while the second version is unstable and is still in development, mainly used in combination with Cadence IC 5.2.51 or 6.1 versions, [6].

Technology processes supported by NCSU CDK 1.5.1

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follow the SCMOS rules for design and verification, defined by the MOSIS IC fabrication service. The main idea of MOSIS is to provide a nearly process- and metric-independent interface to many CMOS fabrication processes available through MOSIS, in such a way that designers work in the abstraction of SCMOS layers and metric unit ("lambda"), [5], [6]. After the designer specifies the process and feature size of the design that should be fabricated, MOSIS maps the SCMOS design onto that process, generating true logical layers and absolute dimensions required by the process vendor. The designer can regularly submit exactly the same integrated circuit, but to a different fabrication process or feature size. In such case, MOSIS will alone handle the new mapping. On the other hand, using a specific vendor's layers and design rules will yield to a design which is less likely to be directly portable to any other process or feature size.

The general purpose of MOSIS is to combine designs from multiple customers (companies and universities), or diverse designs from a single company, on one mask set (Multi Project Wafer - MPW). This allows customers to share overhead costs associated with mask making, wafer fabrication, and assembly. The cost savings, along with the ability to use NCSU design kit and to support many technology processes, makes MOSIS attractive choice for integrated circuits design. According to [7], more than 50,000 integrated circuits have been processed through this service, since 1981.

The main idea of this paper is to present the experiences in using Cadence IC tool set and NCSU design kit for educational purposes. The paper is organized in five sections. In second section we describe the customizations of Cadence IC environment, which are required to enable the technology processes specified by NCSU CDK. In third section we explain the process of designing integrated circuits in Cadence IC, starting from schematic till layout. The results of the practical realization of CMOS inverter and ring oscillator in 0.25 µm TSMC MOSIS technology are presented in the fourth section. The paper concludes in the fifth section, which summarizes the experiences of using these tools within the microelectronics technologies and structures course at the Faculty of Electrical Engineering and Information Technologies in Skopje.

II. Cadence IC Environment Customization

Cadence IC is an environment which allows integrating in a single framework different applications and tools (both proprietary and from other vendors), allowing to support all the stages of IC design and verification. To invoke the Cadence IC environment, the command icfb& is entered at the command prompt in an UNIX based system (in this case Red Hat). This command opens the command interpreter window (CIW), which appears as a user interface to the complete Cadence IC environment. Through the CIW window the user can control the Cadence IC set of tools and as well perform several activities, including: opening new windows, tools startup, terminating sessions, reviewing the warnings, errors and other messages, changing the environment configuration etc., [8].

When the Cadence IC tool suite is initially invoked, several messages are written in the CIW window, ending up with the sentence: "Done loading NCSU_CDK customizations". This indicates that the Cadence IC environment loads all the configuration files specified by NCSU CDK, when it is launched. NCSU CDK 1.5.1 includes several technology processes that use special technology libraries. These libraries are named as NCSU_TechLib_xxxYY, where xxx is used for the manufacturer's name and YY indicates the minimal transistor length in microns (e.g. the library NCSU_TechLib_ami16 defines $\lambda = 0.8$ µm and minimal transistor length of 1.6 µm). NCSU CDK 1.5.1 includes several libraries for the following MOSIS processes, [6], [7]:

- NCSU_Techlib_ami06 - AMI 0.60u C5N (3M, 2P, high-res)
- NCSU_Techlib_ami16 - AMI 1.6u ABN (2P, NPN)
- NCSU_Techlib_hp06 - HP 0.60u AMOS14TB (3M, sblock, thin-ox cap)
- NCSU_Techlib_tsmc02 - TSMC 0.20u CMOS018 (6M, HV FET, sblock)
- NCSU_Techlib_tsmc02d - TSMC 0.18u CMOS018/ DEEP (6M, HV FET, sblock)
- NCSU_Techlib_tsmc03 - TSMC 0.30u CMOS025 (5M, HV FET)
- NCSU_Techlib_tsmc03d - TSMC 0.24u CMOS025/ DEEP (5M, HV FET)
- NCSU_TechLib_tsmc04_4M2P - TSMC 0.40u CMOS035 (4M, 2P, HV FET)

Cadence library manager displays the technology libraries for the MOSIS CMOS processes, included in the NCSU Cadence design kit. This window (shown in Figure 1) automatically opens, always when the Cadence IC environment is started.

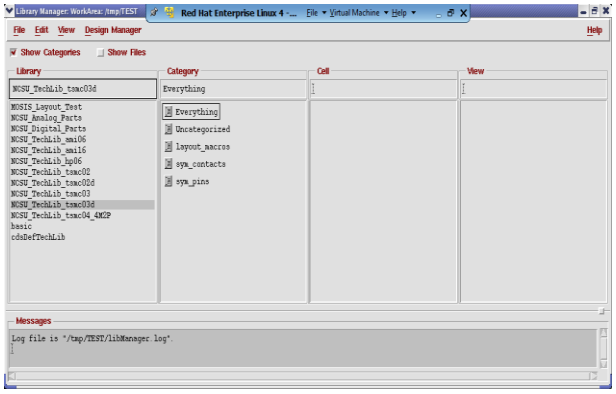

Fig. 1. Technology libraries in the Cadence Library Manager.

Figure 1 illustrates the library manager, showing all the libraries of the Cadence working directory, and their elements in different views (schematic, layout etc.), as well. For example, the NCSU_Analog_Parts library, which is used for analog circuits design includes basic electronic elements, such as: transistors, current sources, voltage sources, resistance, capacitance, etc.

III. Integrated Circuits Design Flow in Cadence IC

Cadende IC is an environment which includes a set of CAD tools, including: Composer Schematic, Composer Symbol, Spectre Simulator and Virtuoso Layout, [4], [8]. Each of these tools individually participates in a particular phase of the integrated circuits design flow in Cadence IC. To start a design in Cadence, one must first create a library where the design cells will be stored. Each library is associated with a technology file and it is the technology file that supplies color maps, layer maps, design rules and extraction parameters required to view, design, simulate and fabricate a circuit.

Cadence organizes its files in libraries, cells and cell views. A library (which actually appears as a directory in UNIX) contains cells (subdirectories), which in turn contain views (schematic, symbol, and layout). Each library contains a catalog of all cells, viewed along with the actual UNIX paths to the data files. Every cell in a library uses the same mask layers, colors, design rules, symbolic devices, and parameter values (which is the information contained in the technology file). A cell is the basic design object that forms an individual building block of a chip or system. Each cell has one or more views, which are files that store specific data for each cell. A cell view is the virtual data file created to store information in Cadence. A cell may have many cell views, signifying different ways to represent the same data of the cell (e.g. layout, schematic, etc).

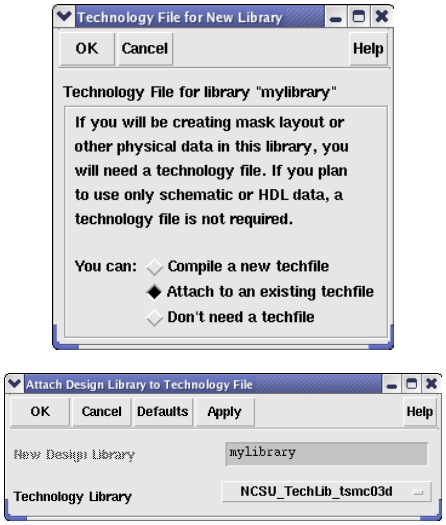

Fig. 2. Specification of technology file, while designing a library in Cadence IC.

The integrated circuit design flow begins by creating a schematic with the Composer Schematic tool. The created schematic is later used for automatic symbol creation with the Composer Symbol tool. The circuit schematic is then simulated with the Spectre simulator which allows different types of analyzes, such as transient, DC, AC etc. Once the circuit operation is verified, a layout is generated. Using the Virtuoso layout editor, the designer describes the detailed geometries and the relative positioning of each mask layer to be used in fabrication. The realized circuit layout has to match the actual circuit schematic.

The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built into the Layout Editor, called Design Rule Checker, is used to detect any design rule violations during and after the mask layout design. The designer must perform DRC and make sure that all layout errors are eventually removed from the mask layout, before the final design is saved. The layout is then extracted and a layout vs. schematic (LVS) comparison is run to ensure the cell layout exactly matches the schematic. All these verification tools are included in the Cadence Diva software. If some problems during the checks appear the designer returns back to the layout design phase. On the other hand, a netlist is created and finally the extracted layout is simulated (with Spectre) in order to observe the effect of parasitics that will be present in the fabricated chip. The post layout simulation results are closer to reality and will show weather the created design would work if is fabricated.

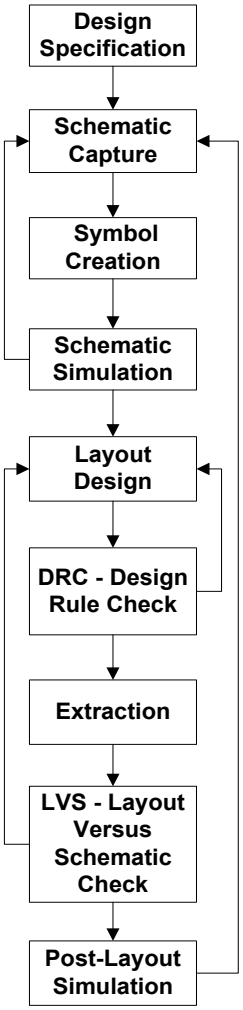

Fig. 3. Integrated circuit design flow in Cadence IC.

Due to the complexity of Cadence tools, approximately a month (eight hours weekly) is required for an engineering student to understand and learn their functionalities and capabilities for integrated circuits design with technologies supported by MOSIS.

IV. Integrated Circuit Design in 0.25 µm Technology for MOSIS

Best way to provide deeper understanding of Cadence IC environment capabilities is to start with integrated circuits design, using this tool. According to the numerous Cadence tutorials from many universities, [4], [8] it is almost a best practice to start designing a simple circuit, and then proceed with the creation of complex ones. This approach enables fast acquiring of the necessary knowledge about the Cadence tool and complete familiarization with the process of integrated circuits design. In order to design a particular circuit, one should first know the components it is consisted of, and then its characteristics, schematic, simulation capabilities etc.

In the continuation of this paper, we are describing all of the phases required for CMOS inverter design in Cadence IC. Using the NCSU_Techlib_tsmc03d library the CMOS inverter is realized within the 0.25 µm TSMC technology. This simple circuit is later used for ring oscillator design in the same MOSIS technology, [7]. Presenting this, we are describing the process of building a hierarchical design from already realized integrated circuits.

The experience with students at FEEIT-Skopje has shown that designing a simple integrated circuit lasts approximately a month (ten hours weekly). Therefore, we believe that in some cases is a good practice to build the basic logic circuits and then use them for developing hierarchical designs in the future. This approach can significantly accelerate the process of designing more complex integrated circuits.

A. CMOS Inverter

CMOS inverter is a simple circuit consisted of pmos and nmos transistors, input and output pins, and power sources (ground and high voltage), [8]. The process of designing an inverter integrated circuit begins with schematic creation, using the Composer Schematic tool. The pmos, nmos, vdd and gnd components are selected from the NCSU_Analog Parts library and then inserted into the scheme. These components are wired, as shown in figure 4, and thus complete schematic is created. The symbol of the circuit is automatically generated from its schematic, using the Composer-Symbol tool. Actually, for drawing the inverter symbol (triangle with a circle), Line and Rectangle tools are used.

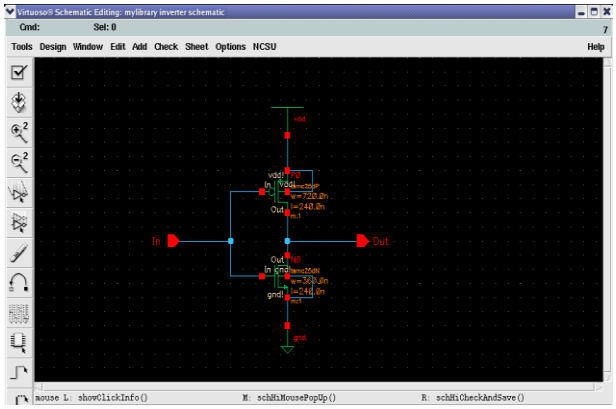

Fig. 4. CMOS Inverter schematic.

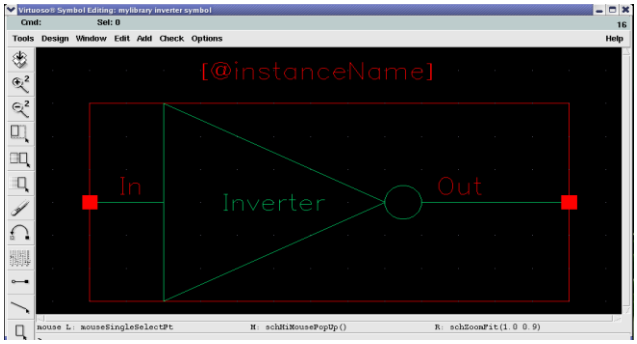

Fig. 5. CMOS Inverter symbol.

In order to simulate the CMOS inverter, a test scenario schematic is created into the Composer Schematic editor. The test scenario includes dc voltage generator and vpulse generator, selected from the NCSU_Analog_Parts library. For the vpulse generator, the voltages V1 and V2 are set to 0V and 2.5V, accordingly, while for the vdc generator the DC voltage is set to 2.5V. In CMOS digital circuits, the output nodes are typically loaded by purely capacitive loads, so a capacitor of 1pF is inserted in the schematic. The created test scenario is simulated using the Spectre simulator, which allows several types of simulations, including transient, DC, AC etc. Figure 7 shows the results of CMOS inverter transient analysis for duration of 6 µs.

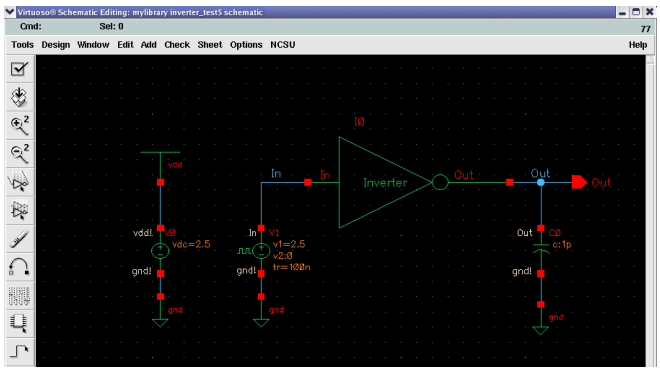

Fig. 6. CMOS Inverter test scenario.

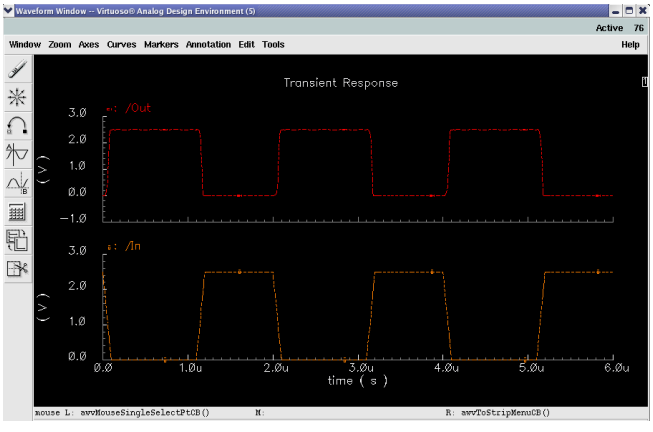

Fig. 7. Results of CMOS Inverter transient analyses.

Next thing to analyze are the characteristics of the output, such as rising and falling edge time, signal delay etc. All these signal properties are computed, using the embedded functions (RiseTime and Delay) of the Waveform calculator.

Additionally, DC and AC simulations are also done, but we are not discussing them here. However, the overall simulations results have shown that the CMOS inverter achieves the expected behavior.

Given that the functionality of the CMOS inverter is verified, the circuit layout design can start. The CMOS inverter layout will be designed in TSMC 0.25µm technology, whose specification is provided on the MOSIS website, [7]. The given web documentation states that this CMOS technology process has 5 metal layers and 1 poly layer, and is used for 2.5 volt applications.

In order to realize inverter layout with the TSMC 0.25µm MOSIS technology process, the designer must follow the SCN5M_DEEP rules, specified in [5]. These rules define the value of Lambda as 0.12µm, and thus limit the minimal length and width of a transistor to 0:24 µm and 0.36µm, respectively. In addition to this, the same rules identify the gridRes parameter (resolution of the grid layout) as Lambda/2, which equals to 0.06 mµ.

Considering the SCN5M_DEEP rules, the NMOS transistor length and width are specified as 0.24µm and 0.36µm, while the PMOS transistor length and width are set to 0.24µm and 0.72µm. The actual process of inverter layout design consists of: insertion of pmos and nmos transistors (pmos/nmos layout cell view, selected from the NCSU_Techlib_tsmc03d library), connecting the transistor layers (poly and metal1), and addition of I/O pins, voltage sources and contacts (metal1-poly) in the layout editor, as well.

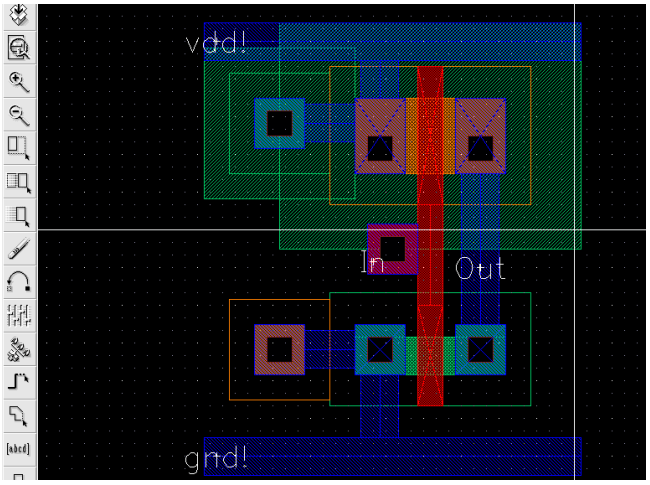

Fig. 8. CMOS Inverter layout.

Once the layout of the circuit is designed, the geometric rules check or DRC analysis can start. If this analysis is successful, the parasitic capacitances from the circuit can be extracted. The extracted circuit creates a novel cell view of the CMOS inverter, shown in Figure 9.

After the LVS check has finished successfully, it is considered that the layout and the schematic of the inverter circuit mach. However, it is still necessary to make additional circuit simulations in order to observe the parasitic effects that will remain in the manufactured chip. These analyses check whether the circuit will work properly after fabrication.

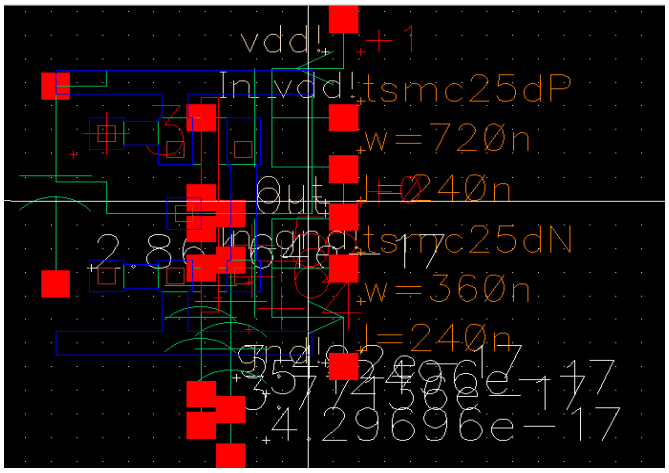

Fig. 9. CMOS Inverter extraction.

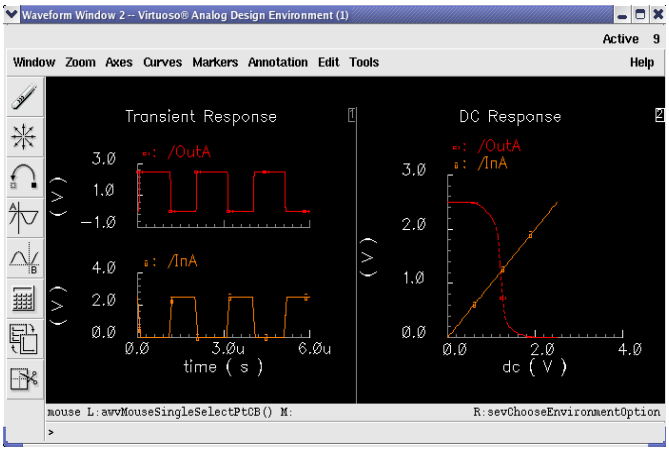

Fig. 10. Results of CMOS Inverter transient and DC post-layout simulation.

In order to perform post-layout simulations, some minor changes (removing the vdd and gnd contacts) in the CMOS inverter schematic and symbol are done, and several modifications in the test scenario schematic are also made. The results of these post-layout simulations (figure 10) verify that the extracted inverter circuit operates in similar way as the CMOS inverter schematic.

B. Ring Oscillator

The cell views of the CMOS inverter can be directly placed into other cell views of hierarchical designs. In order to show this, in the continuation we are presenting the process of designing a ring oscillator circuit, [9]. The ring oscillator is consisted of five CMOS inverters wired in a circular way, with coupled inputs and outputs. The complete ring oscillator schematic, realized in Cadence IC, is shown in figure 11. As can be seen on this picture, the ring oscillator output is connected to a noConn component, which is used to prevent any unconnected warnings. Additionally, some other components are also added in the Schematic editor (vdd, gnd and vdc - 2.5V voltage sources, selected from the NCSU_Analog_Parts library), and later used for simulating the ring oscillator circuit.

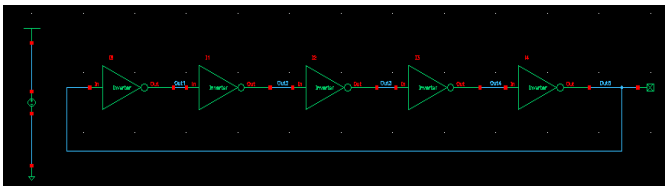

Fig. 11. Ring oscillator test scenario.

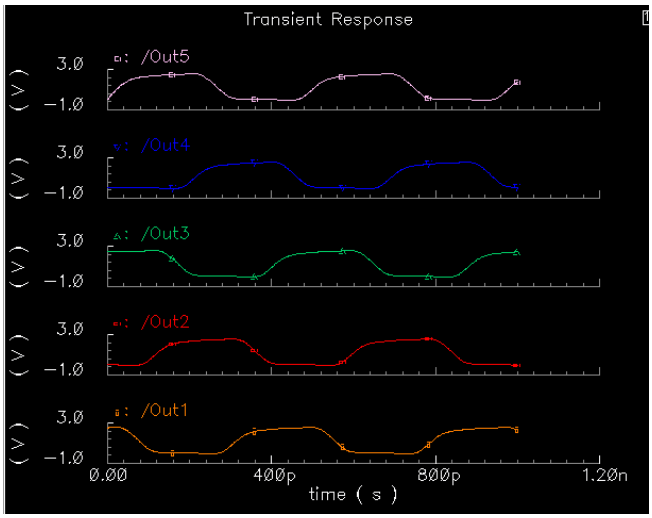

Fig. 12. Results of Ring oscillator transient analyses.

The previous figure presents the results of ring oscillator transient simulation for duration of 1ns. As shown in this figure, it can be considered that the given circuit achieves the expected behavior. This is additionally proven by computing the frequency and power consumption of the ring oscillator, using the special functions of the waveform calculator. However, the results of the last analyzes are not going to be discussed here.

The ring oscillator layout is designed in a similar way as its schematic. This process begins by adding the layout cell views of the five CMOS inverters in the Virtuoso layout editor. The inverters are then connected with metal1 layer, while the input of the first inverter and the output of the last inverter are connected with a metal2 path. The last connection is created, using M2_M1 contacts. Additionally, a RingOut PIN is added to serve as an output of the ring oscillator circuit.

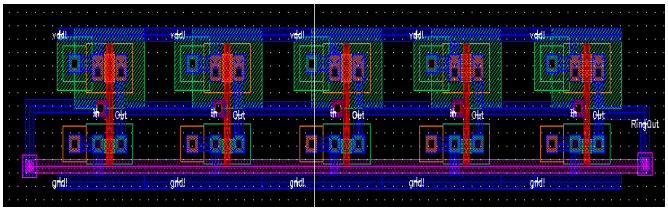

Fig. 13. Ring oscillator layout.

After the ring oscillator layout is created, DRC check, extraction, LVS check and post-layout simulations are performed. All of these design flow stages are successfully completed, with LVS analysis ending up with the message: "The net lists match". After that, post-layout simulations are performed, and the ring oscillator functionality is verified.

V. Conclusion

According to the complete flow of integrated circuits design in Cadence IC, shown by example, it can be said that this powerful environment is suitable for use not only by professionals but also by beginners. The structural approach of its tools organization and the availability of many written tutorials enable engineering students to easily adjust to it.

The experience in using Cadence IC tool suite within the microelectronics technologies and structures course, at the Electrical Engineering and Information Technologies Faculty in Skopje has shown that the process of studying this course would start by reading a professional literature, [10] - [13], which will help students learn the basics of microelectronic (for an average period of one month - 8 hours weekly). This would be followed by introducing students to the Cadence IC tool suite and NCSU design kit, as an integrated environment for integrated circuits design, supported by MOSIS (approximately one month - 8 hours weekly). Deeper knowledge would be acquired when the students will manage to design an integrated circuit with the Cadence IC tool. This can last for a month or two (around 40 hours per month) depending on the circuit complexity. However, the basic level of microelectronics, analog circuits design and other related electronics courses can be obtained through lab practice exercises and/or by completing a project work in Cadence IC.

The application of Cadence IC and NCSU CDK for educational purposes at FEEIT Skopje, expands the opportunities of the academic environment in our country, and increases the capabilities for collaboration with other companies, research and educational institutions from academia and industry, abroad.

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Tool-Based Curricula and Visual Learning

Dragica Vasileska, Gerhard Klimeck, A. Magana, and S. M. Goodnick

***Abstract*—In the last twenty years nanotechnology has revolutionized the world of information theory, computers and other important disciplines, such as medicine, where it has contributed significantly in the creation of more sophisticated diagnostic tools. Therefore, it is important for people working in nanotechnology to better understand basic concepts to be more creative and productive. To further foster the progress on Nanotechnology in the USA, the National Science Foundation has created the Network for Computational Nanotechnology (NCN) and the dissemination of all the information from member and non-member participants of the NCN is enabled by the community website www.nanoHUB.org. nanoHUB's signature services online simulation that enables the operation of sophisticated research and educational simulation engines with a common browser. No software installation or local computing power is needed. The simulation tools as well as nano-concepts are augmented by educational materials, assignments, and tool-based curricula, which are assemblies of tools that help students excel in a particular area.**

As elaborated later in the text, it is the visual mode of learning that we are exploiting in achieving faster and better results with students that go through simulation tool-based curricula. There are several tool based curricula already developed on the nanoHUB and undergoing further development, out of which five are directly related to nanoelectronics. They are: ABACUS – device simulation module; ACUTE – Computational Electronics module; ANTSY – bending toolkit; and AQME – quantum mechanics module. The methodology behind tool-based curricula is discussed in details. Then, the current status of each module is presented, including user statistics and student learning indicatives. Particular simulation tool is explored further to demonstrate the ease by which students can grasp information. Representative of Abacus is PN-Junction Lab; representative of AQME is PCPBT tool; and representative of ACUTE is SCHRED, which has 97 citations in research papers and is the most popular tool on nanoHUB.org.

Surveys were collected from three courses offered at Arizona State University. These courses were: EEE434/591, the Quantum Mechanics class offered in the fall 2007; EEE 101 Engineering Design, offered in the spring 2008; and EEE533 Semiconductor Device and Process Simulation, offered in the fall 2009. The study consisted of students participating in a voluntary Likert-scale survey that focused on: *Learning outcomes, Evidence of the learning, Pedagogical approach and Usability aspects.* In particular, the survey investigated how intuitive the tools are.

The results of the study identified differences in the way students perceived the nanoHUB.org simulation tools. Graduate and undergraduate students reported more positive experiences with nanoHUB.org simulations than freshman students did. Potential explanations for these differences are: a) freshman students have not fully developed graphical literacy skills; b) students may lack the prior knowledge required at the time they interact with the tool; and c) students may lack interests in the topic and have not yet seen the value of how these tools can be applied toward their own learning goals. A potential support to overcome some of these difficulties may be by embedding just-in-time instructional supports together with the simulation tools.

***Index Terms*—ABACUS, AQME, nanoHUB, tool-based curricula.**

Original Research Paper
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I. Introduction

Learning theorists [1] have demonstrated that people vary in the manner in which they absorb, process, and recall what they are taught. Verbal learners, a group that constitutes about 30% of the general population, learn by hearing. They benefit from class lectures and from discussion of class materials in study groups or in oral presentations, but chafe at written assignments. Experiential learners - about 5% of the population - learn by doing and touching, and clinical work, role-playing exercises, and moot court are their best instructional modalities. Visual Learners - the remaining 65% of the population - need to see what they are learning, and while they have difficulty following oral lectures, they perform well at written assignments and readily recall material they have read. Empirical research supports the conclusions that when students are matched with teaching methods that complement their learning styles, their absorption and retention is significantly enhanced. Moreover, variations in learning styles have been linked to gender: women tend to be more visually oriented than men, who are generally more kinesthetic, and consequently female students are systematically more prone to suffer the deleterious effects of learning style-teaching method mismatch than men.

In addition to regular student, we often encounter in the classroom students with learning disabilities. The term learning disability (LD) is used to refer to a range of neurological conditions that affect one or more of the ways

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that a person takes in, stores, or uses information [2]. Learning disabilities are specific, not global, impairments. For example, a person may have a LD which impacts on her ability to understand written information; the same information, delivered orally or visually, presents no problem. The term includes such conditions as dysgraphia (writing disorder), dyslexia (reading disorder), dyscalculia (mathematics disorder) and developmental aphasia.

Learning disabilities affect all areas of life to the extent that the affected mode is used in that area. They are most often noticed in school settings, where certain learning modes are employed more than others, causing the weaknesses caused by the LD to stand out. Learning disabilities are usually identified by school psychologists through testing of intelligence, academics and processes of learning. It is now well-known now that desktop-based computer technology plays an important role in the education of students with disabilities.

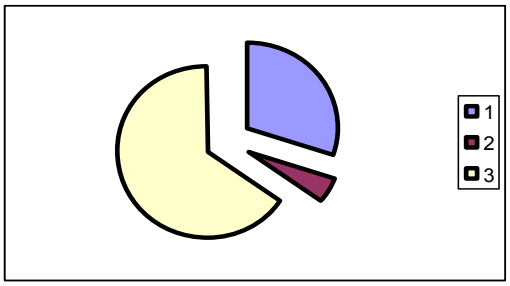

Fig. 1. 1- total % of verbal learners; 2- total % of experiential learners and 3- total % of visual learners.

It is also important to stress that visual memory is a part of memory preserving some characteristics of our senses pertaining to visual experience. We are able to place in memory information that resembles objects, places, animals or people. Some authors refer to this experience as "our mind's eye" through which we can retrieve from memory a mental image of the original object, place, animal or person. Eidetic imagery is perhaps the only kind that produces actual visual memory that can be looked at similarly as if looking at the actual picture. There are two kinds of memory related to eidetic imagery: photographic memory and iconic memory. The phenomenon of photographic memory is usually displayed by some individuals' exceptional skills in mental organization *and it is this type of memory that we will exploit in student/researcher learning via the use of the visualization and simulation software that has friendly graphical user interface and is deployed to the general public via www.nanoHUB.org*.

II. Tool-Based Curricula

Control of energy has become a common problem facing both the electronics industry in terms of thermal management and energy efficiency, not to mention solid state lighting, as well as in energy conversion of optical to electrical energy (and vice versa). The device scaling crisis has motivated researchers from all over the world to look for replacement of conventional field-effect transistor in digital applications as well as analog applications. Strained-Si devices have been proposed, alternative device technologies have also been explored. What will be the next device that will replace conventional silicon MOSFETs is not clear even to the Intel Corp. Many alternative structures such as nanowire transistors, carbon nanotubes, nanoribons, etc., graphene devices (these are some of the many choices being explored at the moment) have been proposed.

There is one common theme that describes all these alternative devices: they are small, so the atomic arrangement will affect the material properties, they operate more or less on quantum-mechanical principles, therefore requiring the latest developments in material science, great physics insight, and most importantly, they need state of the art modeling tools.

Several factors motivate us to focus on development of future generation software tools and integrate them into 21st Century Educational Courses and seminars. If we take, for example, the conventional silicon transistor, it consists of more then 60 elements which material properties we have to know to be able to predict its operation. Furthermore, as transistors get scaled into nanometer dimensions, quantum effects become more prominent and knowledge of Quantum Mechanics is essential. In addition, there is a continuous trend to scale the transistors to get faster devices and more functions on the chip. The conventional way of doing scaling no longer works and two general avenues are typically pursued by the industry: alternative materials and alternative device structures. Again, knowledge of the properties of the materials along, for example, various crystallographic directions becomes essential.

The above discussion suggests that new paradigms of learning are necessary for training students in the vibrant and constantly changing field of nanoelectronics. Since computers play more and more important role in person's everyday life, they have to be incorporated into the student learning process. Prof. Vasileska and Prof. Klimeck propose a novel methodology, the so-called tool-based curricula, to be used for training future engineers in the nanoelectronics field. This new methodology consists of assembling a set of tools, together with demos on how to use the tools, the objectives of the tool and what can be learned with them, assembly of solved problems, homework assignments including solve a challenge problem which is related to real world applications. Examples of such assemblies of tools and their capabilities are given in the following three subsections.

A. ABACUS

The purpose of the ABACUS tool-based curricula is that via simulations students get working knowledge for the operation of basic semiconductor devices. In order to understand the operation of bipolar devices, for example, it is crucial to understand the physical principles of the operation of a PN diode under forward and reverse bias conditions and in the presence of different generation/recombination processes including Shockley-Read-Hall generation/recombination and Auger generation/recombination (PN Junction Lab).

On the other hand, MOS capacitors are integral part of every MOSFET device, so understanding the operation of

MOS capacitors is crucial for the understanding of MOSFET devices. Several tools are developed and offered for this purpose with different levels of approximation listed below under a common name MOS Capacitors. One of them is based on the idealized delta-depletion approximation, the second one exploits the exact analytical model for semiclassical charge description, and the third tool is able to do either semiclassical or quantum-mechanical calculation of the charge self-consistently in the MOS Capacitor where appropriate.

MOSFET devices, that are a backbone of 99% of today's integrated circuits, can be analyzed using the MOSFET Lab. Various effects can be predicted such as punch-through (occurs when source and drain depletion regions touch), DIBL=Drain Induced Barrier Lowering (leads to finite output conductance), transistor breakdown caused by the impact ionization process, etc.

In summary, the following tools comprise ABACUS that is designed for the purpose of better understanding the operation of semiconductor devices:

- Crystal Viewer
- Periodic Potential Lab
- Piece-Wise Constant Potential Barrier Tool
- Bandstructure Lab
- Carrier Statistics Lab
- Drift-Diffusion Lab
- PN Junction Lab
- BJT Lab
- MOS Capacitor Lab (classical calculations)
- MOSFET Lab (classical calculations)

As one of the most popular labs from the ABACUS learning module is the PN-Junction lab. This lab not only describes the operation of a PN diode, the interplay of the drift and diffusion processes, and of the generation-recombination mechanisms, but it nicely illustrates the need for simulation for the case when modeling asymmetric junctions. Namely, if one looks at the electric field profile plot for a diode with $N_A=10^{16}$ cm^{-3} and $N_D=10^{18}$ cm^{-3}, then one finds that the depletion charge approximation underestimates the peak electric field by a large margin. The numerical solution, on the other hand, predicts the correct breakdown field. The peak electric field for the diode example considered here is shown in Fig. 2.

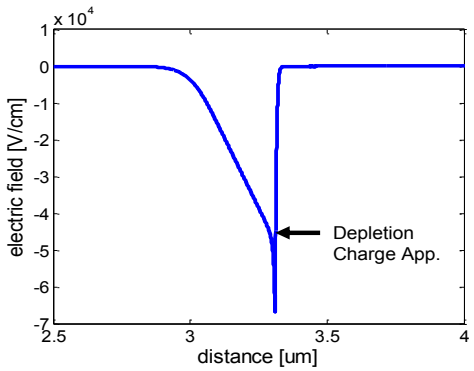

Fig. 2. Electric field profile in a pn-diode with $N_A=10^{16}$ cm^{-3} and $N_D=10^{18}$ cm^{-3} and equilibrium conditions.

The usage statistics of the PN Junction Lab is given in Tables 1-3.

TABLE I
OVERVIEW

Item	Average	Total
Simulation Users:	-	3,420
Interactive Sessions:	-	11,795
Simulation Sessions:	-	22,938
Simulation Runs:	-	33,015
Wall Time:	11.05 hours	10565.37 days
CPU time:	17.81 seconds	4.38 days
Interaction Time:	2.23 hours	1973.19 days

TABLE II
USERS BY ORGANIZATION TYPE

#	Type	Users	Percent
1	Educational - University	2,634	77.02
2	Unidentified	237	6.93
3	Educational - Unspec. Level	218	6.37
4	Industry	173	5.06
5	National Lab	45	1.32
6	Personal	39	1.14
7	Unemployed	27	0.79
8	Government Agency	25	0.73
9	Educational - Pre-College	24	0.7
10	Military	9	0.26
	Total Users	3,420	100

TABLE III
USERS BY COUNTRY OF RESIDENCE

#	Country	Users	Percent
1	United States	1,755	51.32
2	Czech Republic	242	7.08
3	India	200	5.85
4	Canada	126	3.68
5	Sweden	105	3.07
6	Turkey	86	2.51
7	Korea, Republic of	75	2.19
8	China	63	1.84
9	Italy	58	1.7
10	Germany	55	1.61
	Total Users	3,420	100

B. AQME

Every quantum mechanics book written by physicists, without any exception, is dominated by the discussion of the hydrogen atom and very little of the text is devoted to real world applications. Engineers need something different and that is very nicely captured by Prof. David K. Ferry from Arizona State University in his text "Quantum Mechanics for Engineers".

Namely, things that engineers are mainly concerned with are the differences between closed and open systems. Closed systems can be used to describe quantum mechanical size quantization effects in nanodevices in which there is constrain in the motion of the carriers in one or two or three directions in which case we talk about quasi-two-dimensional electron gas, quasi-one-dimensional electron gas and zero-dimensional electron gas. Bound states calculation lab is developed for this purpose to take into account quantization in one and two spatial directions.

Open systems are, on the other hand, very important to be properly explained because every functioning device is an open system. When describing open systems key thing to know is the energy dependence of the transmission coefficient because once that quantity is calculated one can use the Tsu-Esaki formula [3] and calculate the current.

Another quantity that has to be grasped by students studying semiconductor devices is the real electronic structure of a zinc-blende material of interest. For that purpose we have developed the Periodic Potential Lab that is based on the simple Kronig-Penney model and illustrates nicely how the interaction potential opens gaps in the free-electron dispersion curve. Students also have the opportunity to visualize realistic bandstructure of three-dimensional crystals by running the Bandstructure Lab tool that is based on the validity of the Empirical Pseudopotential method and tight-binding approximation.

In summary, the following tools comprise AQME devoted for understanding basic quantum-mechanical principles needed for understanding the operation of nano-electronic devices:

- Bound-States Calculation Lab
- Piece-Wise-Constant Potential Barrier Lab
- Periodic Potential Lab
- Bandstructure Lab
- SCHRED
- 1D Hetero
- Quantum Dot Lab
- Resonant Tunneling Diode Lab
- Coulomb Blockade Lab

Typical examples for the Bound State Calculation Lab are the investigation of the energy level spacing in rectangular, parabolic and triangular confinement. The lowest eigenenergies for these examples are plotted in Fig. 3.

The Piece-Wise Constant Potential Barrier Tool not only can be used to investigate transmission and reflection through three segment, 5 segment, 7 segment, 9 segment and 11 segment piece-wise constant barrier construct, but the tool very elegantly demonstrates the formation of energy bands and energy gaps under the option multiple identical barriers. This is illustrated very nicely on the example shown in Fig. 4. Only through such examples students can grasp the concept of formation of energy bands and energy gaps.

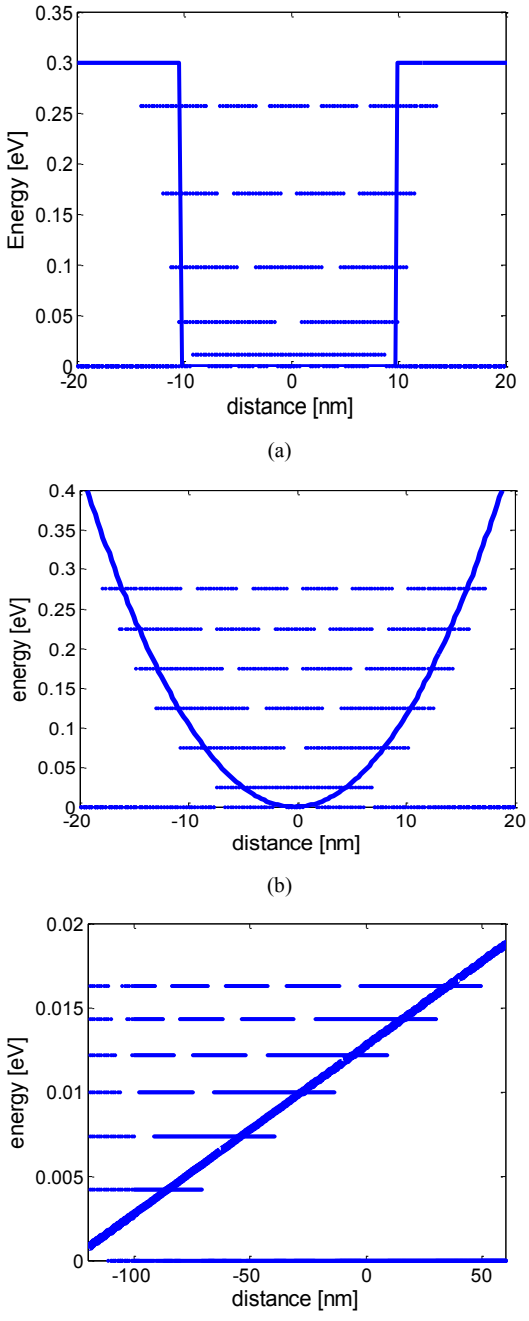

Fig. 3. Lowest energy eigenstates in a rectangular (a), parabolic (b) and triangular (c) confinement. Notice the differences in the energy level spacing. For rectangular confinement the energy level spacing increases with increasing energy, for parabolic it is constant and for triangular it decreases with increasing energy. These are typical confinement types that occur in nature. The wave functions are sine functions for square confinement, Hermite polynomials for parabolic confinement and Airy functions for triangular confinement.

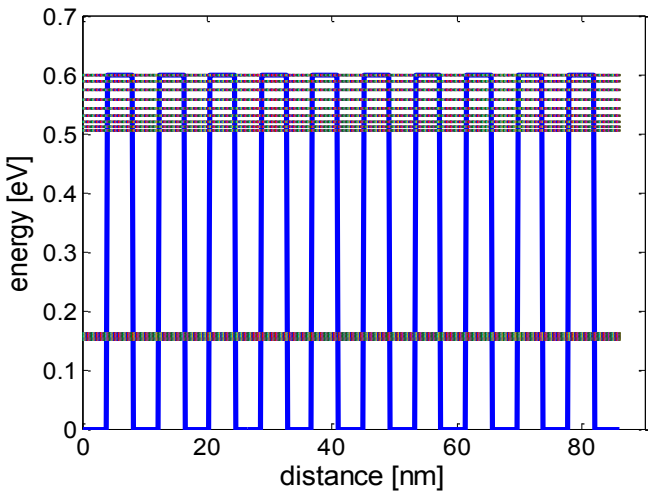

Fig. 4. Multiple-barrier case and formation of energy bands due to the interaction between the wells.

The PCPBT Tool Usage Statistics is given in Tables 4-6.

TABLE IV
OVERVIEW

Item	Average	Total
Simulation Users:	-	254
Interactive Sessions:	-	1,115
Simulation Sessions:	-	2,736
Simulation Runs:	-	3,851
Wall Time:	1 hours	114.35 days
CPU time:	29.26 seconds	22.24 hours
Interaction Time:	26.25 minutes	49.87 days

TABLE V
USERS BY ORGANIZATION TYPE

#	Type	Users	Percent
1	Educational - University	234	92.13
2	Unidentified	6	2.36
3	National Lab	4	1.57
4	Unemployed	3	1.18
5	Industry	3	1.18
6	Educational - Pre-College	2	0.79
7	Military	1	0.39
8	Government Agency	1	0.39
	Total Users	254	100

A critical insight here is the fundamental question of how many atoms are required to obtain a band structure. An analogous example is to start from isolated atom, then bring together two atoms, then three, etc., until n-atoms are used. Further complication can be that the atoms are not aligned on a line, but have their full 3D positions as in real crystals. This second case is examined by the band structure lab whose output is the energy versus wave vector dispersion along high symmetry points in the first Brillouin zone.

TABLE VI
USERS BY COUNTRY OF RESIDENCE

#	Country	Users	Percent
1	United States	142	55.91
2	Italy	17	6.69
3	India	16	6.3
4	Romania	8	3.15
5	Germany	8	3.15
6	Canada	7	2.76
7	China	4	1.57
8	Taiwan	3	1.18
9	Bangladesh	3	1.18
10	Egypt	3	1.18
	Total Users	254	100

C. ACUTE

Continuing technological advances make possible the fabrication of electronic devices with increasing structural and conceptual complexity, and in an expanding variety of material systems. In the field of Computational Electronics, advanced modeling and simulation techniques are created, developed and employed to assist in the invention, design and optimization of micro-, nano- and opto-electronic devices and circuits. Research in Computational Electronics draws upon knowledge from a variety of disciplines, predominantly solid state physics, quantum mechanics, electromagnetics and numerical algorithms, to achieve an accurate description of all aspects of device operation.

Device structure, material composition, and operating principles are all intimately related. For example, the characteristic length scale of devices such as resonant tunneling diodes and quantum dots which rely on coherent quantum effects is constrained to just a few nanometers. Most optoelectronic devices exploit heterojunctions between two or more different materials for confinement of both charge carriers and light; characteristic thicknesses of absorption or gain regions typically vary from around one hundred nanometers to several microns. Power electronic devices, on the other hand, may reach several millimeters in width due to their current-handling requirements, and are increasingly fabricated using materials other than silicon in a quest for superior thermal performance and breakdown voltage. The wide variety of possible applications, material selections, and realizable device structures make Computational Electronics a broad and exciting field.

On the nanoHUB we have created tool-based curriculum

that allows users to simulate semiconductor devices that range in behavior and can be explained with purely semiclassical concepts to devices that need fully quantum mechanical modeling to capture their behavior. The tools that comprise ACUTE are:

- Piece Wise Constant Potential Barrier Tool
- Periodic Potential Lab
- Bandstructure Lab
- PADRE Simulator
- Bulk Monte Carlo Lab
- QUAMC 2D – Monte Carlo Device Simulator
- SCHRED – 1D Schrödinger-Poisson solver
- 1D Hetero
- nanoMOS

The most popular tool on the nanoHUB is SCHRED that can be used, for example to qualitatively and quantitatively explain the semiclassical vs. quantum behavior of the carriers in the MOS capacitors which comprise MOSFET devices. The usage statistics of SCHRED is given in Tables 7-9, and SCHRED worldwide usage is illustrated in Fig. 5.

TABLE VII
OVERVIEW

Item	Average	Total
Simulation Users:	-	1,667
Interactive Sessions:	-	20,431
Simulation Sessions:	-	39,005
Simulation Runs:	-	47,153
Wall Time:	2.11 hours	3423.93 days
CPU time:	41.5 seconds	12.85 days
Interaction Time:	1.11 hours	1234.05 days

TABLE VIII
USERS BY ORGANIZATION TYPE

#	Type	Users	Percent
1	Educational - University	1,223	73.37
2	Unidentified	211	12.66
3	Industry	101	6.06
4	Educational - Unspec. Level	52	3.12
5	National Lab	40	2.4
6	Unemployed	17	1.02
7	Government Agency	11	0.66
8	Educational - Pre-College	10	0.6
9	Personal	10	0.6
10	Military	2	0.12
	Total Users	1,667	100

TABLE IX
USERS BY COUNTRY OF RESIDENCE

#	Country	Users	Percent
1	United States	762	45.71
2	Taiwan	149	8.94
3	India	87	5.22
4	China	49	2.94
5	France	36	2.16
6	Japan	29	1.74
7	Korea, Republic of	29	1.74
8	United Kingdom	27	1.62
9	Italy	27	1.62
10	Germany	24	1.44
	Total Users	1,667	100

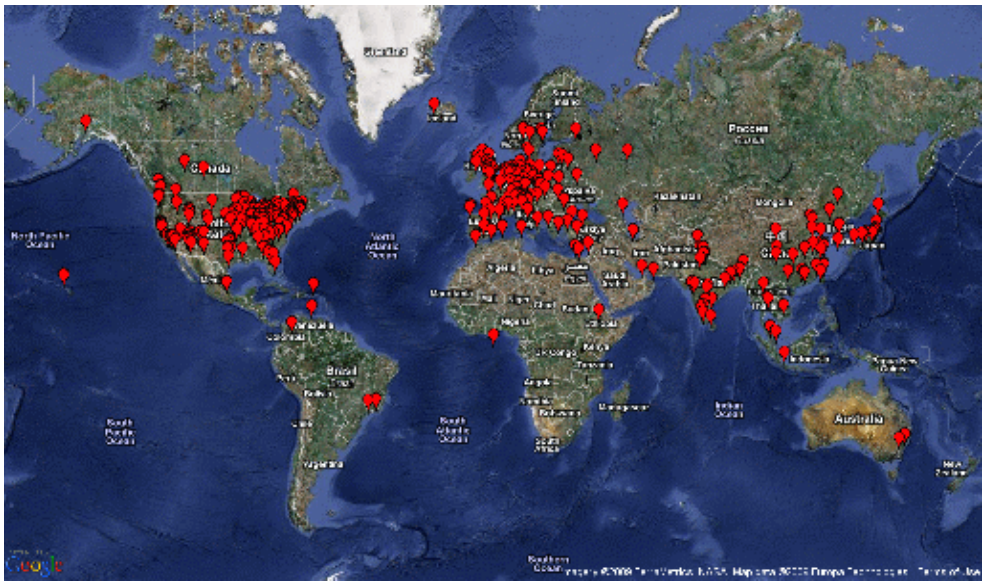

Fig. 5. World-Wide Usage of SCHRED.

III. Visual Environment Stimulating Student Learning

nanoHUB.org provides research-quality simulations that experts in nanoscience commonly use to build knowledge in their field. nanoHUB.org leverages an advanced cyber-infrastructure and middleware tools to provide seamless access to these simulations. As described on the nanoHUB.org website, key characteristics of nanoHUB.org simulation tools that make them good resources for incorporation into classroom environments are: a) they were produced by researchers in the NCN focus areas; b) they are easily accessed from a web browser powered by a highly sophisticated architecture that taps into national grid resources; and c) they provide a consistent interactive graphical user interface known as Rappture, which makes esoteric computational models approachable to non-experts. Rappture is a toolkit that allows the incorporation of a friendly graphical user interface with the simulation tools in nanoHUB.org [4]. An example of this interface is shown in Figure 6. In Figure 7 the results from a survey are summarized regarding the GUI and usability, in general, of nanoHUB tools. Three categories of students were being assessed: FS=freshman, US=undergradduate and GS=graduate students.

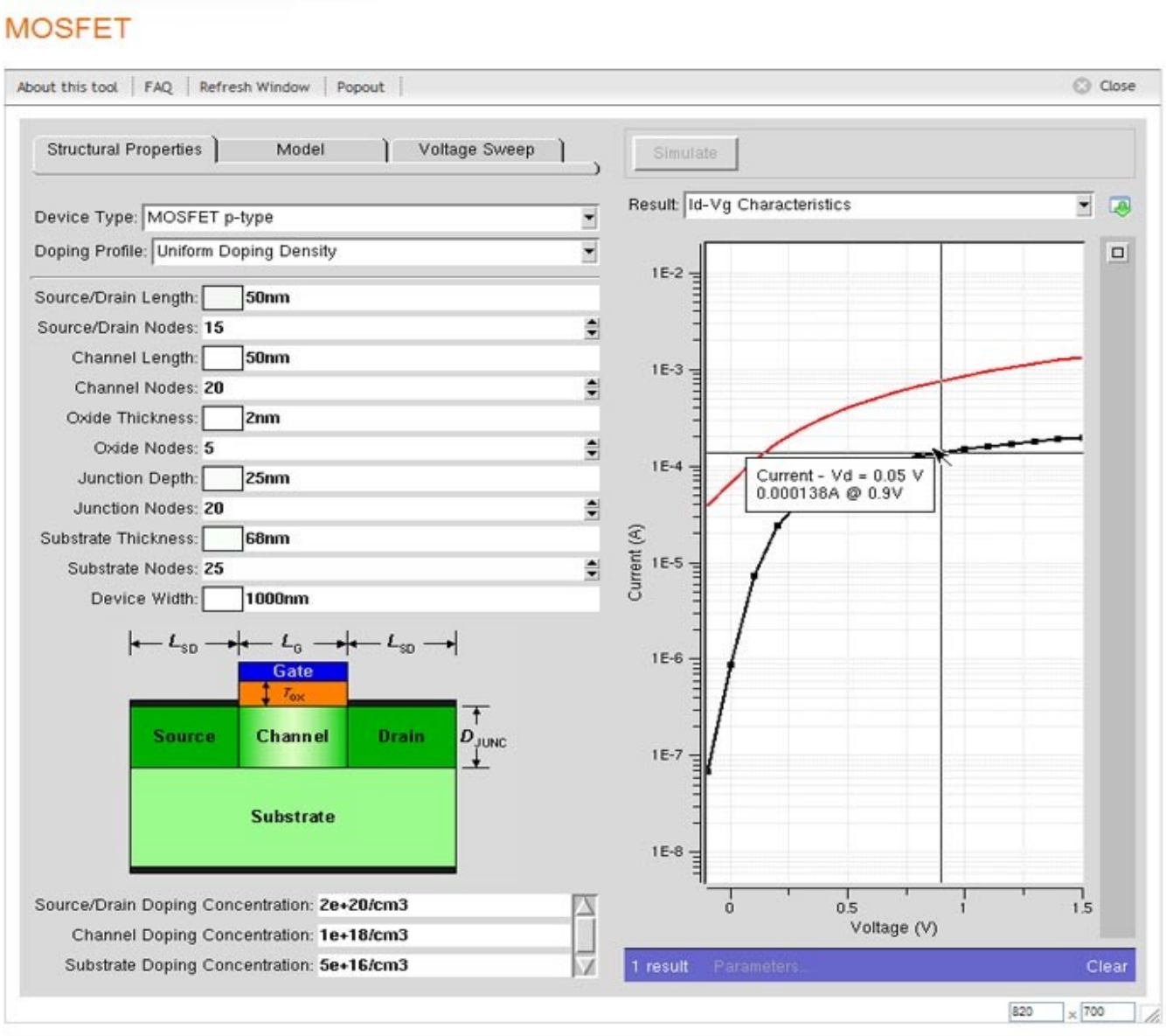

Fig. 6. MOSFET simulation tool interface.

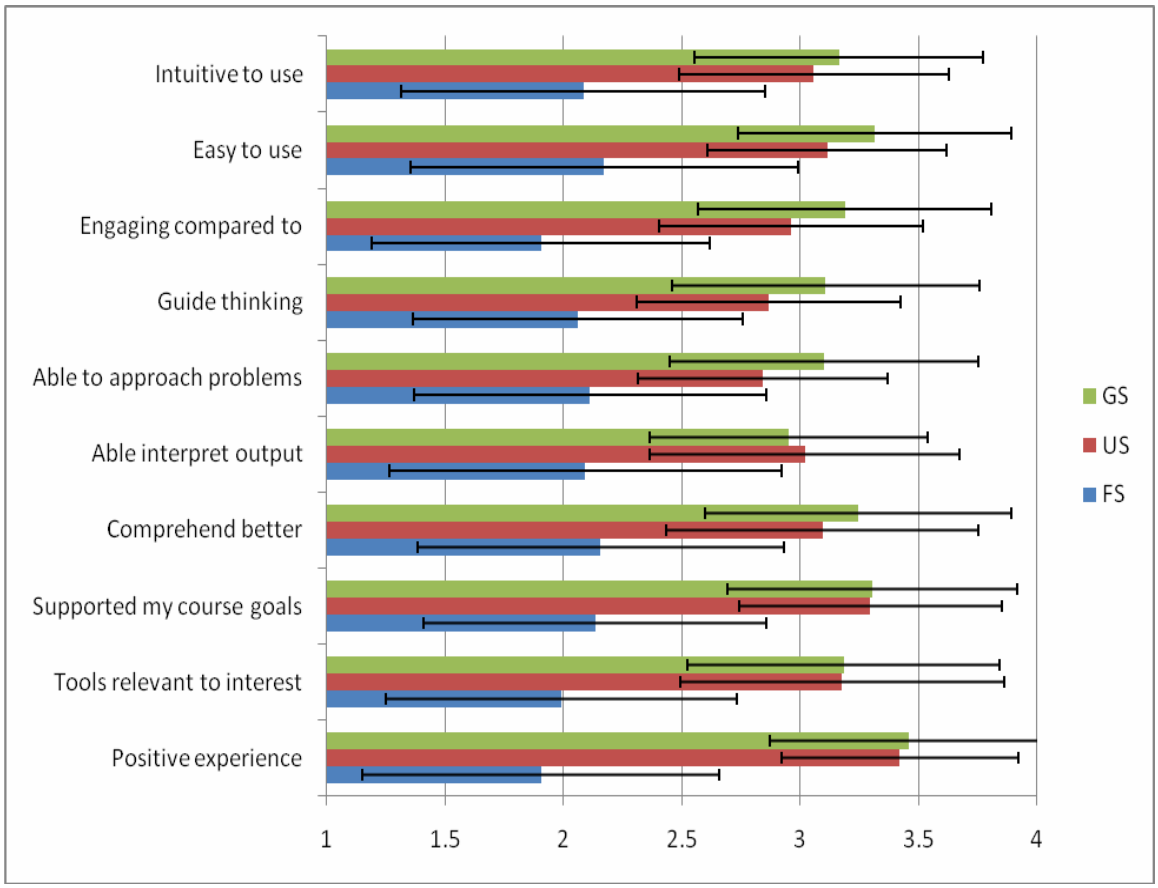

Fig. 7. Summary of responses from the student survey.

IV. Likert-Scale Responses on the Usage of nanoHUB Tools at ASU

The results presented in this section include surveys collected from three courses offered at Arizona State University. These three courses were EEE434/591 Quantum Mechanics class offered in the fall 2007, EEE 101 Engineering Design class offered in the spring 2008, and EEE533 Semiconductor Device and Process Simulation class offered in the fall 2009. Twenty students responded the survey for the course EEE434/591, ten students responded the survey for the course EEE 101 and seven students responded the survey for the course EEE533. In addition, three students from the course EEE533 were interviewed to gain an in-depth understanding of their experiences with the simulation tools.

The survey study consisted of students participating in a voluntary Likert-scale survey [5] focused on:

- *Learning outcomes:* identifying how relevant and positive is the use of simulation tools as part of the course (e.g. how simulation tools supported the goals of the course, how relevant is the topic as well as the course in general).
- *Evidence of the learning:* identifying how students learned with and from the simulation tools (e.g. better comprehension of concepts, ability to interpret the output, ability to transfer the learning to new situations).
- *Pedagogical approach:* identifying how useful simulation tools were to students for their learning (e.g. in helping them guide their thinking, in being more engaged with the task and in helping them study a certain phenomena).
- *Usability aspects:* in particular how intuitive the tools are.

For the survey utilized students responded in a scale from one to four: strongly agree, agree, disagree, and strongly disagree to each question. The assigned scores and our interpretation of the responses are as follows:

TABLE X
AVERAGE SCORES FOR THE STUDENT SURVEY DATA

Response	Score	Interpretation
Strongly agree	4	Strongly positive
Agree	3	Positive
Disagree	2	Negative
Strongly disagree	1	Strongly negative

Descriptive statistics was used to analyze the survey responses. In Figure 8 we report responses grouped by content, assessment, pedagogy and usability. In Figure 9 we report detailed scores of students' responses to individual questions.

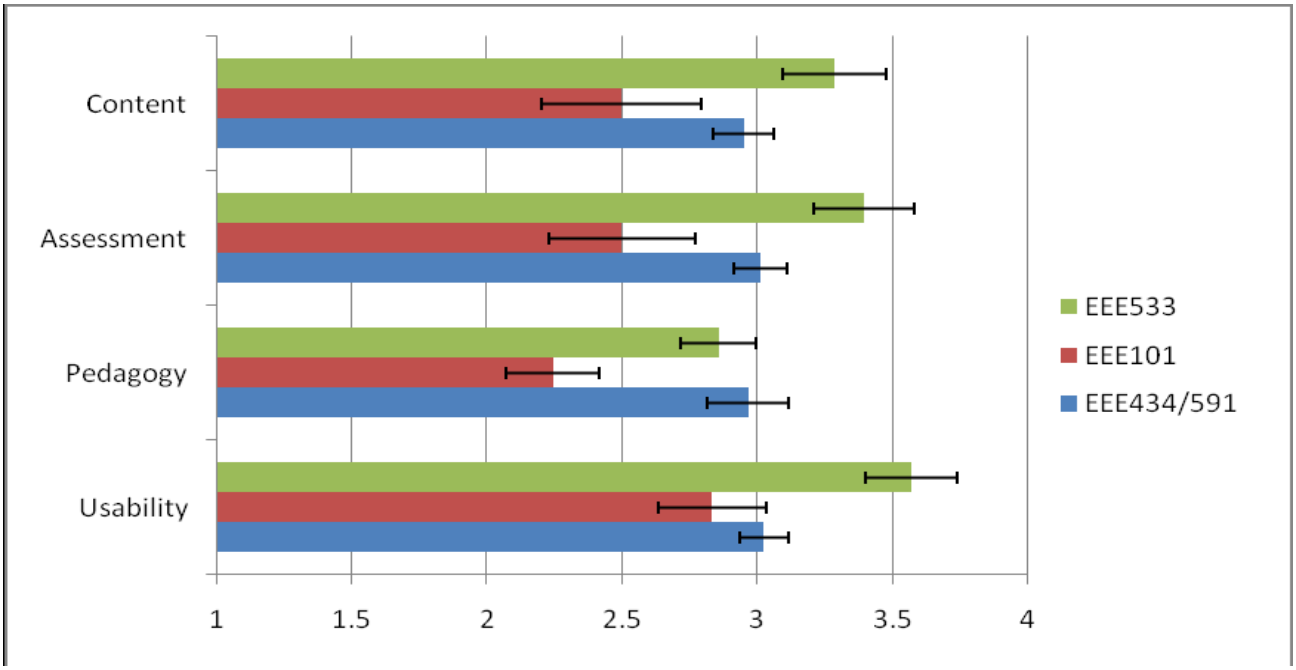

Fig. 8. Responses to survey grouped by content, assessment, pedagogy and usability.

Learning Outcomes (content) - This section focuses on the general experience students had, relevance of the content to whether students thought the simulation tools were relevant to their areas of interest as well as their level of satisfaction. Students from the courses EEE434/591 and EEE101 were positive in their responses of considering nanoHUB as a positive experience while students from the course EEE533 reported using nanoHUB as a very positive experience. Students from courses EEE434/591 and EEE101 reported inconclusive responses of perceiving nanoHUB.org simulation tools as highly relevant to their areas of interest and students from the course EEE533 reported positive responses to this same item. Students attending the EEE434/591 course found nanoHUB.org simulations supporting their goals and expectations of the course. Students attending the EEE101 course found the course as highly relevant to their areas of interest but did not find nanoHUB.org simulations supporting their expectations for the course. Students from the EEE533 course found the course as highly relevant to their areas of interest and found nanoHUB.org simulations as highly supporting their expectations for the course.

Evidence of Learning (assessment) - In this section we focused on how students perceived simulation tools as useful for their learning and their ability to transfer it to practical situations. While the students who attended the courses EEE434/591 and EEE533 could comprehend the concepts better by using the nanoHUB.org simulation tools as compared to lectures and readings only, students who attended the course EEE101 reported inconclusive responses on comprehending the concepts better by using the nanoHUB.org simulation tools as compared to lectures and readings only. Similarly, while students from the courses EEE434/591 and EEE533 did not have trouble interpreting the output of the simulation tools, students from the course EEE101 responded inconclusively to the same question. In the questions related to the transfer of knowledge such as confidence on students' ability to use concepts embedded in the simulation tools to approach new problems and students' increased awareness of practical application of the concepts, students from the courses EEE434/591 and EEE533 reported positive experiences while students from the course EEE101 reported inconclusive responses.

Instructional Approach (pedagogy) - In this section our focus is on identifying whether the simulation tools were a useful and engaging cognitive device for students' learning. Students from the courses EEE434/591 and EEE533 reported positive responses of using nanoHUB simulation tools to generate questions that guided their thinking, and also positively reported that using the nanoHUB made the course a lot more engaging for them compared to courses that only use lectures, homework, and readings. Students who attended the course EEE101 reported inconclusive responses that using nanoHUB simulation tools helped them generate questions that guided their thinking, and that using nanoHUB made the course much more engaging for them compared to courses that only use lectures, homework, and readings.

Usability – Students from groups EEE434/591 and EEE101 reported that nanoHUB simulations are intuitive as well as easy to use and students from the group EEE533 reported that nanoHUB simulations are very intuitive as well as easy to use.

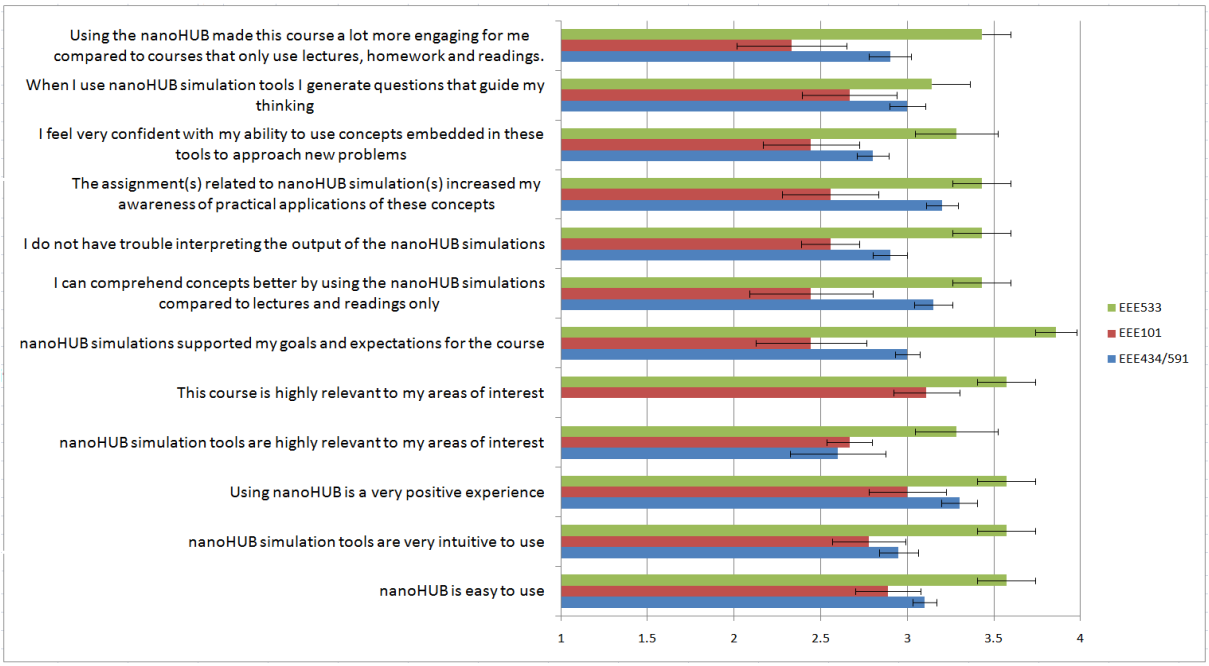

Fig. 9. Detailed Scores of Responses from the Student Survey.

V. Conclusion

Some conjectures about the factors that could explain the variance in the results of undergraduate and graduates can be derived from the open ended responses and the correlation analysis. From the correlation analysis of the survey items it was observed that an important factor of students' experiences with nanoHUB.org simulation tools is their perceived value of how the simulation tools can support their course goals, how are these related to their areas of interest, and how the tools can assist them in their learning process. Motivation was also observed as another equally important factor. For example, how students found using the simulation as a positive experience and how that experience was engaging for them.

From the analysis of the freshman students open ended responses, possible explanations of these students' differences of their perceptions of the simulation tools may be that they have not fully developed graphical literacy skills necessary to reason with the data outputted by the computational simulations. Another potential reason for this difference may be that students, at the moment they interact with the simulation tools, lack the prior knowledge required. Finally, it could also be related to a motivational factor since freshman students are still formulating their interests in various professional activities and have not yet seen the value of these tools toward their own goals, like the graduate students do.

These results can be supported with literature related to expert - novice differences. Some of the ways experts differ from novices is that experts are more capable of: a) noticing meaningful patterns of information, b) deeply understand the subject matter by organizing their content knowledge, c) place knowledge in a context of applicability, and d) flexibly and automatically retrieve relevant knowledge [6].

These novice learners may need additional supports to develop their learning process for skills that graduate students have already developed. These additional supports could take the form of introductory materials and guidance in the concepts, anticipated simulation results, and meaning of the results.

Additional research is needed to better understand what exact needs freshmen students have and how additional supports for learning can be provided. These supports could be provided by or embedded in nanoHUB.org.

Acknowledgment

Prof. Dragica Vasileska from Arizona State University would like to acknowledge the summer support from the Network for Computational Nanotechnology for two months each year in the last four years while working on development of educational tools and other course materials. Financial support from NSF Grant under grant No. NSF ECS 0901251 is also acknowledged.

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From Theory to Development: Role of Multiphysics Modeling and its Effect on Education in Electronics

Tejinder Singh

***Abstract*—Electronics engineering is a very rapidly growing field, as the time passes the requirement of more advance technologies increase. There are a lot of institutions and universities around the world that provide quality education to different fields of engineering. The courses that electronics engineers study need practical exposure as well to cope up with industrial demands. In this paper, the role of multiphysics modeling and its impact on engineering education is demonstrated. Finite element modeling (FEM) tools are very powerful tools and due to there huge advantages, electronics graduates should study these tools in their course curriculum to know how to tackle various types of physics problems and through examples it is demonstrated that how these tools can help shift from just theory to development process.**

***Index Terms*—Multiphysics modeling, FEM, electronics engineering, education sector, development.**

Original Research Paper
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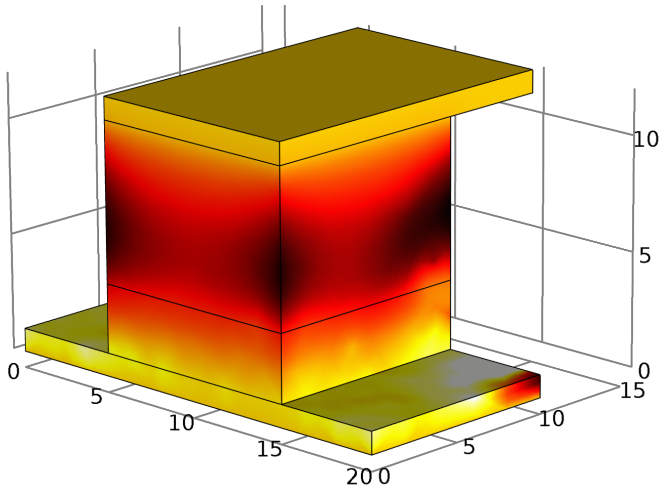

Fig. 1. Joule heating phenomena in memristor is demonstrated by thermal plot. The maximum joule heating problem in memristor can be clearly seen. It is due to the fact that when oxygen vacancies drift with mobility μ_v throughout length D of memristor, it generates heat in the undoped area.

I. Introduction

GRADUATE engineering or graduate research students usually face emerging class of challenges in designing that are vast in multiple disciplines of engineering and sciences. Streamlined computational methods and techniques that combine the can handle physics of various engineering domains, are required to precisely model the problems and accurately predict results before manufacturing or fabrication. Most of the engineering programmes offer field specific simulation and modeling courses on a very limited basis [1]. But as the requirement of engineers in different fields there is a need of one generic tool that can tackle multiphysics problems. As an example; electronics engineering graduates after their education choose an electronics industry [2]. Most of the industries have developed their own tools to train fresh graduates and to work upon. But with the high demand of advanced technologies, various physics solutions are required to design one specific solution, hence, companies are now opting for multiphysics modeling or finite element modller (FEM) to save costs and to reduce computing resources [3]. One tool can handle various physics problems. Instead of teaching very specific tools to electronics engineers, universities should focus and add multiphysics modeling in the course curriculum of graduate engineering students.

Basically, multiphysics environment or simply multiphysics modeling require the basic knowledge of the problem that one is going to solve as a prerequisite. Once, the basic equations of the problem is provided, then using finite element computation, the multiphysics modeller, thus ask for boundary conditions and finally computes those equations for specified boundary conditions. It takes a very less time if the basics are clear. Hence, the name of the paper: From theory to development perfectly suits for multiphysics modeling. These tools takes the theoretical inputs and do all the simulation and testing in between the frame of theory to actual development.

Few engineering curricula in some universities offers design and research experiences of multiphysics environment. An electrical or electronics graduate student may require finite element techniques to solve electric field problems as well as overall device level problems like mechanical stresses or chemical process if the system is on same chip/device. This paper presents the need of multiphysics modeling in electronics engineering graduate course curricula that should covers the most of the methods and techniques of multiphysics modeling.

Post-graduate students become active participants in multiphysics modeling than their theory counterparts because of the analysis by being challenged to tackle variety of physics problems that are related to high priority technological areas.

II. Multiphysics Modeling

Multiphysics handles various simulations that involve multiple simultaneous physical phenomena or multiple physics

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models. As an example; combining stress with RF electrical signals or combining fluid physics with electrical currents. Multiphysics modeling usually involves solving coupled physics systems of partial differential equations. In simple words, multiphysics environment computed partial differential equations for the given boundary conditions of a coupled physics problem of joule heating problem in memristor as shown in Fig. 1. Various modeling and simulations involves multi–coupled systems viz. magnetic and electric fields for electromagnetic circuits, fluid and gas for electronic sensors, or Ion drift or temperature rise in electronic components due to its continuous operation. Another example is the approximation of mean field for the electronic structure of various atoms, in the given example the electron wave functions and electric field are coupled.

A. Core Technologies

Multiphysics modeling or finite element modeller as the name suggests, computes partial differential equations for finite elements. Hence, to solve a problem, first the geometry is designed with proper material selection and then physics problem is selected. After applying boundary conditions to the geometry as per the chosen physics study, The modeller then perform *Meshing* of the geometry.

Meshing is one of the main process for any finite element modeller in which the modeling environment carefully creates very small finite elements of the geometry where the solution can be approximated. Fine or coarse meshing is as per users concerns. Higher the mesh elements, appropriate the result will be with the trade-off in computation speed because more finite elements need more degree of freedom to solve.

B. Studies

Different multiphysics modellers have almost similar material library and the type of studies. The basis of FEM is to solve equations as per the boundary conditions. Various physics modules are available in almost any FEM like: *Acoustic Wave modeling, Semiconductor physics, Fludic Flow, RF, MEMS, Structural Mechanics* and many more.

Physics modules are different from the study it will perform. The study basically depends on the chosen physics module and problem. Studies are basically: *Stationary, Time dependent* or *Frequency dependent*.

III. Importance in Education

As per the discussed benefits and technologies of multiphysics environment, it is required that multiphysics modeling should be included in the curriculum of electronics engineering, so that even fresh engineers when apply their knowledge in industry, they should know how coupled physics work and how to solve such kind of problems [4]. Further two case studies are presented, both are new technologies in the field of electronics. These case studies demonstrate that without multiphysics modeling it would be impossible to compute the parameters mathematically.

Case study I is on recently discovered memristor in which the current distribution, V–I characteristics and temperature effects are studied using multiphysics modeling and in case study II, RF performance, eigenfrequencies and stress distribution is analysed for RF MEMS switch.

IV. Case Study – I: Modeling of Memristor

Memristor is the recently discovered fourth missing circuit element. This case study is chosen because it perfectly links the aim of this paper with actual scenario. Memristor is theoretically postulated in 1971 by Leon Chua [5]. From 1971 till 2008 no–one discovered this missing circuit element, but in 2008 HP labs published a paper in *Nature* [6] that they have discovered the memristor, which shows the results as published by Leon Chua.

They have used multiphysics modeling to first design and test the theory and after the successful attempts, HP labs fabricated the memristor. After that the author of the original papers, studied the intrinsic constrains like temperature dependancy on memristor in which again they used FEM analyses [7].

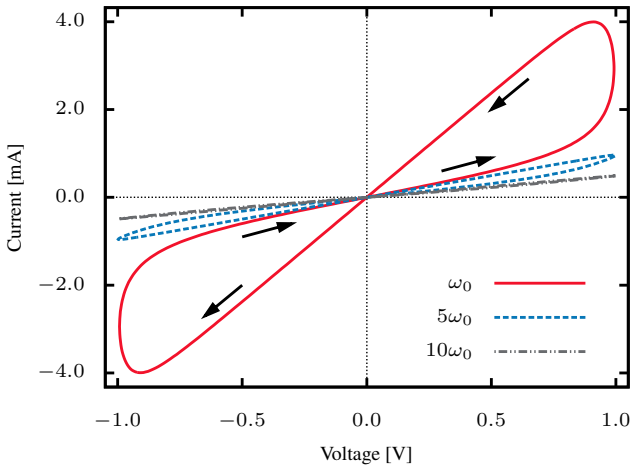

Fig. 2. Hysteresis loop of linear–ion drift memristor for frequencies: $\omega_0, 5\omega_0$ and $10\omega_0$ under the applied voltage bias of 1.0 V. The maximum current flows through the memristor at ω_0 is 4.0 mA

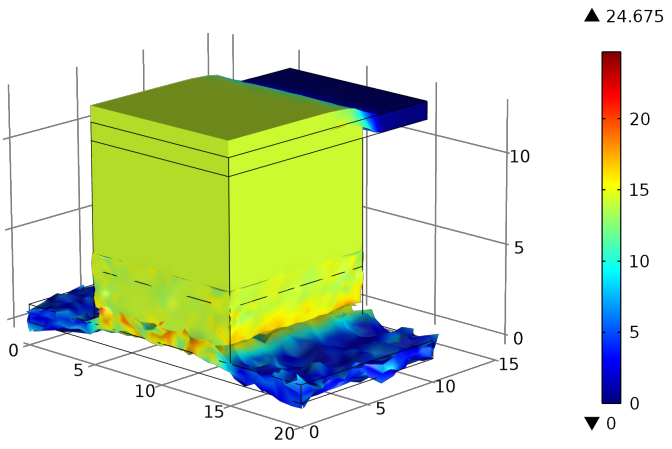

Fig. 3. Normalized current distribution in memristor due to the applied bias. The maximum current flows through the memristor is 24.675 A/m. Bottom deformed electrode is the positive electrode near doped region.

Linear–ion drift memristor is designed in multiphysics modeling with top and bottom plates are of platinum material and TiO_2 material is sandwitched in between. Its current distribution, temperature variation and V–I characteristics are extracted using FEM. Fig.2 shows the extracted V–I characters of designed memristor. Joule heating physics is used to determine the maximum temperature in memristor which is shown in Fig. 1. The darker the areas of the image, maximum temperature affects that areas. Thus from the analysis one can change material or other parameters to ensure the quality performance. Current distribution in memristor is shown in Fig. 3. In which current when bias is applied to memristor, current passes through it. The amount of current passes is shown in Fig. 3. The deformation of the surface depicts the normalised current distribution.

The solution for temperature distribution in the thin films can be computed using solving the Poisson equations as [7]:

$$\Delta T(r,z) = -Q/k_M, \qquad r \le R, \quad -H/2 \le z \le H/2 \tag{1}$$

where, k_M is th thermal conductance of the metallic cylinder, that is assumed to be isotropic, q is the heat source density generated in the uniform metal rod.

The external bias of voltage with respect to time $v(t)$ when applied across the device will move the internal boundary between the two regions viz. doped and undoped by causing the charged dopants to drift from positive to negative terminal [8]. The ohmic conduction and linear ion drift in a uniform field of length D with an average ion mobility μv, the voltage across it can be characterised by using

$$v(t) = \left(\mathcal{R}_{ON}\frac{w\,(t)}{D} + \mathcal{R}_{OFF}\left(1 - \frac{w\,(t)}{D}\right)\right) \tag{2}$$

$$\frac{\mathrm{d}w\,(t)}{\mathrm{d}t} = \mu_v \frac{\mathcal{R}_{ON}}{D} i\,(t) \tag{3}$$

which further yields the following equation for $w(t)$:

$$w(t) = \mu_v \frac{\mathcal{R}_{ON}}{D} q\,(t) \tag{4}$$

By plugging the equation (4) into (2) we can obtain the memristance of system, which is further $\mathcal{R}_{OFF} \gg \mathcal{R}_{ON}$ reduces to:

$$M(q) = \mathcal{R}_{OFF}\left(1 - \frac{\mu_v \mathcal{R}_{ON}}{D^2} q(t)\right) \tag{5}$$

In equation (5) the charge $q(t)$ is crucial to memristance. it becomes larger in value for higher dopant mobilities μ_v and quite smaller for thin–film thicknesses D.

V. Case Study – II: Modeling of RF–MEMS Switch

RF–MEMS (Microelectromechanical) switches are highly regarded for their excellent RF performance in microwave region. RF–MEMS switches have huge advantage as: compact structure, high RF performance, low–cost to manufacture over their semiconductor counterparts. RF–MEMS consists of a micro movable membrane for its switching operation under electrostatic force applied. Multiphysics modeling helps to determine the stress gradient in micro movable membrane to ensure its reliable operation, eigenfrequency analysis to determine its basic modes of frequency, RF performance and many other parameters in a single modeling environment.

RF–MEMS suffer from failures during switching due to fracture of membrane due to high stress prone areas if the stress distribution exceeds about 70% of its material's ultimate tensile strength [9], [10]. In this case study all the above said parameters are analysed using multiphysics modeling. The final design is the outcome of receptive testing and simulation of initial designs. Multiphysics modeling really saved a lot of time in designing and estimating the parameters, which seems

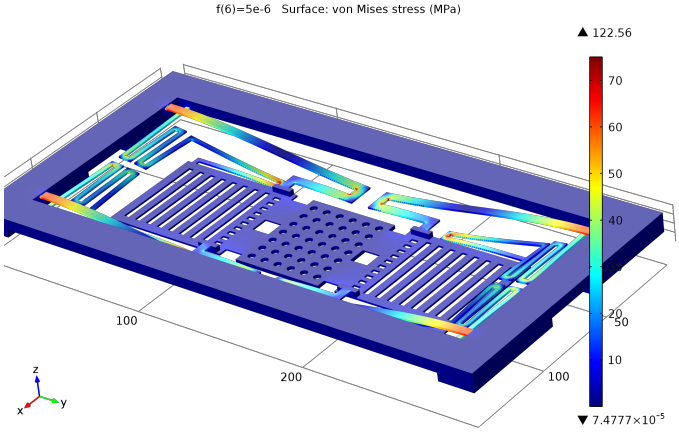

Fig. 4. Stress analysis in micro–membrane designed for RF–MEMS multiport switch. The analysis is done using multiphysics environment with structural physics module. The simulation is shown demonstrating the deflection corresponds to force applied in vertical -Z–direction. The results shows that the maximum stress of 122.5 MPa on the edges of flexures for 5 μN force applied.

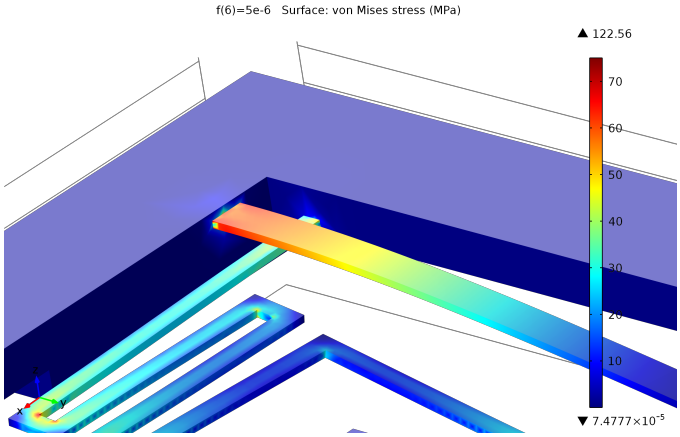

Fig. 5. Close–up view of stress prone area of Ti membrane. The flexures show maximum stress and thus the design can be further improved if required for different materials. The actual deformation is also shown in flexures.

Fig. 6. Vertical deflection of micro membrane in -Z–direction is demonstrated. Results shows that the flexures handle the inner movable membrane well. The design is made to reduce the bending of membrane from middle and after applying force, multiphysics modeling supports the arguments and the result can be seen from deflection and straight inner moveable membrane.

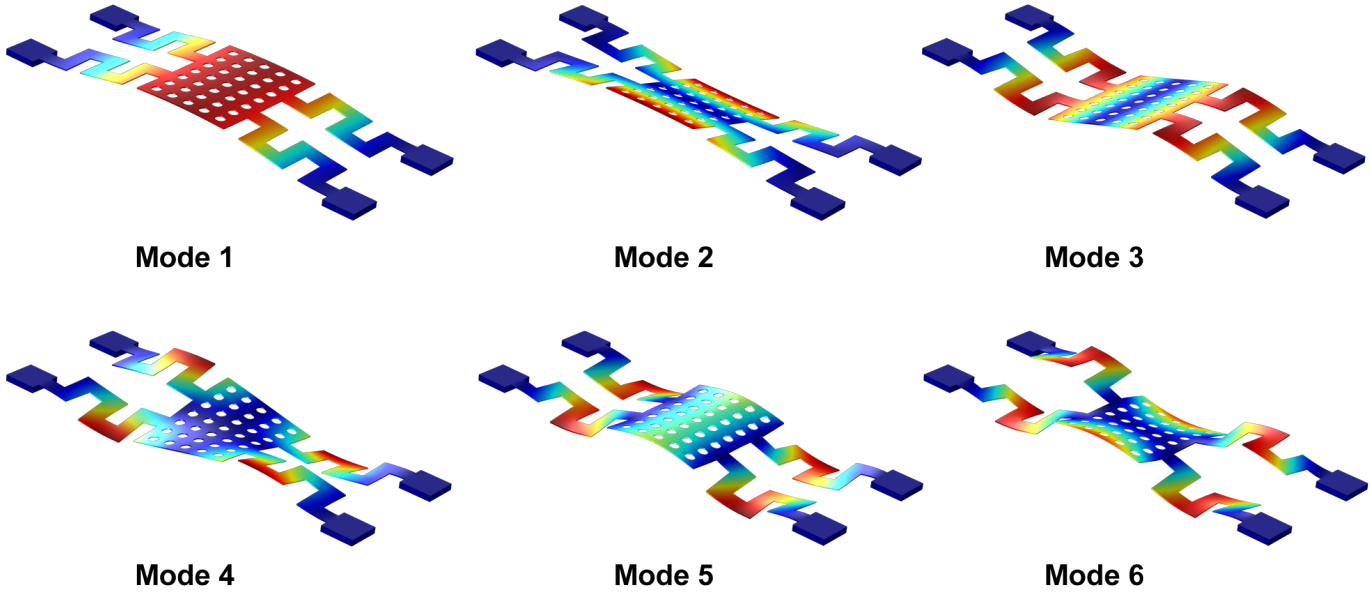

Fig. 7. First six modes with deformation of Au membrane is demonstrated that results from Eigenfrequency analysis in multiphysics environment.

impossible with mathematical analysis [11]. Fig. 4 shows the stress distribution in a Ti based micro membrane. Due to the complex, estimation of spring constant seems unfeasible and for multiphysics modeling its just a matter of few minutes.

Fig. 5 shows the close–up view of stress prone area of the membrane. Fig. 4 demonstrates the maximum stress is in the corners of membrane, while Fig. 5 shows the actual distribution of stress. During actuation, the middle part connected with flexures displaces to turn the switch ON or OFF according to the configuration. The vertical displacement of membrane in -Z direction or in downward direction towards electrodes is shown in the front view as given in Fig. 6. The RF performance is estimated in both ON and OFF state of switch that is given in Fig. 8. The membrane shows nominal stress and great RF performance over a range of frequencies in GHz. The insertion loss and return loss is also plotted. The eigenfrequencies or first six modes are shown in Fig. 7 are shown which is computed for a slightly different membrane designed for millimeter–wave frequencies [12].

The natural frequency of the membrane depends on the equivalent spring constant and the effective mass, the natural frequency f_0 is given as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_{\text{eff}}}{m}} \tag{6}$$

To determine the first mode of eigenfrequency f_1 for hybrid membrane, the component need to be computed first for Au and then for Poly-Si. Then the addition of these two factors can give best estimate of the desired frequency. The first mode of frequency f_1 can be determined by

$$f_1 = \frac{1}{2\pi}\left[\frac{15.418}{L^2}\right]\sqrt{\frac{EI_x}{\rho}} \tag{7}$$

To compute the parameters in ON state, Y_{11-x} will be used,

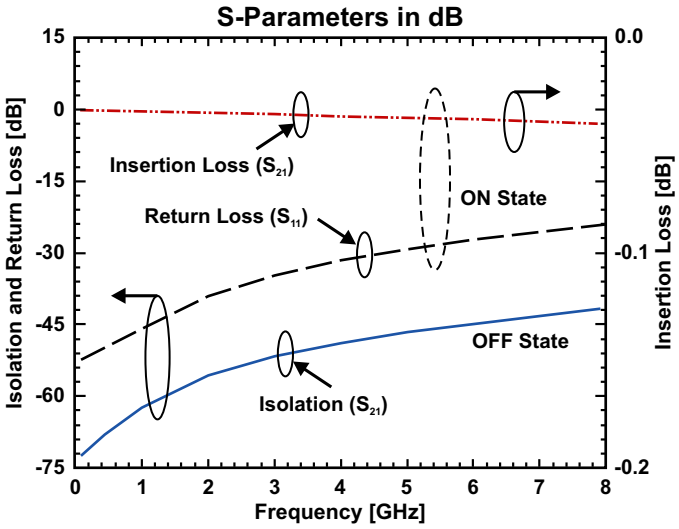

Fig. 8. RF performance measurements using the computation of S–parameters for the membrane shown in Fig. 4 results in isolation of 58 dB in OFF state of switch, insertion loss of 0.012 dB and return loss of 43 dB in ON state at 2 GHz.

where $x = 1$ for ON state and $x = 0$ for OFF state.

$$S_{11-x} = \left(\frac{Y_z^2 - Y_{11-x}^2 + Y_{21-x}^2}{(Y_{11-x} + Y_z)^2 - Y_{21-x}^2}\right) \tag{8}$$

where S_{11-x} is the return loss on ON or OFF state depending on the variable x, $Y_z = 1/Z_0$, $Y_{11-x} = j\omega C_{down}$ for $x = 0$ i.e., in OFF state and $Y_{11-x} = j\omega C_{up}$ for $x = 1$ i.e., in ON state. $Y_{21-x} = -j\omega C_{down}$ for $x = 0$ and $Y_{21-x} = -j\omega C_{up}$ for $x = 1$ i.e., in OFF and ON state respectively. To estimate isolation S_{21-0} and insertion loss S_{21-1}, plug the values in

$$S_{21-x} = \left(\frac{-2Y_{21-x}^2 Y_z}{(Y_{11-x} + Y_z)^2 - Y_{21-x}^2}\right) \tag{9}$$

Equation (8) and (9) helps determining the RF performance at specific frequency. For numerical calculations, frequency sweep seems unfeasible.

VI. Conclusion

From the case studies, it is clear that the capabilities of multiphysics modelling is tremendous for any cross–coupled physics problems. Although multiphysics environment provides a lot of modules to handle various problems, hence to learn different type of problem solving, there is need to put careful attention while learning the modeling methods. The learn curve might be steep for some, but once mastered it cam drastically reduce the designing and testing time. Electronics graduates can take huge advantage if multiphysics modeling is taught in their curricula. It can help fresh graduates to tackle numerous real world problems as they enter in the industry. As only engineers can develop better and advanced products that can serve the technical needs of humanity and it can all be possible with the quality education.

Acknowledgement

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Digital Controller Development Methodology Based on Real-Time Simulations with LabVIEW FPGA© Hardware-Software Toolset

Tommaso Caldognetto, Simone Buso, and Paolo Mattavelli

***Abstract*—In this paper, we exemplify the use of NI LabVIEW FPGA© as a rapid prototyping environment for digital controllers. In our power electronics laboratory, it has been successfully employed in the development, debugging, and test of different power converter controllers for microgrid applications. The paper shows how this high level programming language, together with its target hardware platforms, including Compact RIO and Single Board RIO systems, allows researchers and students to develop even complex applications in reasonable times. The availability of efficient drivers for the considered hardware platforms frees the users from the burden of low level programming. At the same time, the high level programming approach facilitates software re-utilization, allowing the laboratory know-how to steadily grow along time. Furthermore, it allows hardware-in-the-loop real-time simulation, that proved to be effective, and safe, in debugging even complex hardware and software co-designed controllers. To illustrate the effectiveness of these hardware-software toolsets and of the methodology based upon them, two case studies are presented.**

***Index Terms*—LabVIEW FPGA, inverters, digital control, real-time simulation.**

Original Research Paper
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I. Introduction

MOVING the first steps in digital control applications for power electronics is typically hard for many students. It requires the simultaneous use of theoretical knowledge and practical programming and experimental skills [1], [2]. Indeed, conventional integrated design environments for microcontroller, DSP, or FPGA boards are relatively complex and require considerable learning time. Besides, the peculiar nature of the control target, a switching converter processing significant amounts of electrical power, complicates the experiments, posing sometimes non negligible safety and logistic issues. At the same time, scientific research in the field of digital control applications has nowadays reached a certain maturity, so that original studies often present significant complexity, from both the theoretical and the practical implementation standpoint. As a result, the development of non trivial applications, for demonstration as well as for scientific research purposes, requires considerable efforts and relatively long times. All that, often, discourages students and prevents them from engaging the challenge altogether.

In order to simplify the approach to this field of study, both for students and for professional researchers, our power electronics laboratory has recently begun using National Instruments reconfigurable hardware platforms (RIO devices) programmed by NI LabVIEW. In particular, FPGA based platforms and the LabVIEW FPGA© module have been acquired and used as the main hardware-software toolset for all digital control applications.

The interest on digital computation platforms for the development of controllers and real-time simulation systems has increased significantly in recent years. This is also due to the needs, posed by smart grid applications, for the simulation of complex power systems [3]. In this field, popular state-of-the-art digital platforms are: the so called Real Time Digital Simulator (RTDS) [4], from RTDS Technologies, the RT-LAB [5], from OPAL-RT Technologies, and the Typhoon-HIL emulators [6], [7]. RTDS and RT-LAB are PC/FPGA based special purpose computers, while the Typhoon-HIL emulators are utralow-latency platforms based on application-specific digital processor cores. Compared to these state-of-the-art systems, the here identified hardware-software toolset, shows the following key features: relatively low cost, high performance, ease of use, off-the-shelf availability, affirmed and widespread use in other academic and industrial fields.

In particular, with respect to other commercial integrated design environments (IDEs), LabVIEW FPGA© features an extensive set of optimized and ready to use software drivers for a large variety of hardware components, including different types of A/D converters (ADC), D/A converters (DAC), and high speed digital I/O peripherals, which greatly simplifies the implementation of data paths and, in particular, of control applications [8]. Indeed, low level programming is no longer necessary, as the environment takes care of providing an easy access to all peripherals interfaced to the target processor and/or the FPGA chip. The loss of visibility on the low level operation of the front-end circuitry is more than compensated by its high performance capability. As a result, unless one is interested in very high data transfer rates, say above $100\,\mathrm{MSample/s}$, which is hardly the case for power electronic applications, the use of this tool determines no real performance limitation.

The programming language is in itself extremely user friendly and, apart from being often included in the typical

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student curriculum, is relatively easy to learn [8], [2]. The FPGA programming tool, in particular, is designed to appear as a particular function set, or palette, in no way different from the conventional LabVIEW programming language. Indeed, the basic data structures are the same and only a limited number of customized functions need to be studied to enable an effective FPGA chip programming. Not surprisingly, an inexperienced user is typically able to program both conventional software routines and hardware logic circuits after a limited training time. Furthermore, the developed software, thanks to its inherent orientation to modularity, is highly re-usable, which allows the laboratory to incrementally develop its own function set for the applications of interest and to maintain it for long times. Indeed, the updated programming software releases always come with a complete set of peripheral drivers, guaranteeing long term hardware/software compatibility.

Finally, properly combining hardware and software resources, it is possible to set-up hardware-in-the-loop (HIL) real-time (RT) simulations of the control applications under test. This step requires the availability of, at least, two hardware platforms, one used to virtually replicate the converter electrical behavior (the plant), the other to host the control software under test. This minimal set-up allows the developer to proceed with the implementation of the controller without needing to interact with the real plant, thus avoiding all the otherwise associated potentially hazardous situations, till the very last steps of the development.

In this paper, we present two examples of this novel research methodology and discuss how the use of the NI LabVIEW hardware-software toolset can effectively support the experimental research activities related to digital control in power electronics.

We begin, in section II, by presenting the hardware components of the considered toolset. Then, in section III, we describe some basic building blocks of the controlling software for a voltage source inverter (VSI). The HIL RT simulation of a grid-tied VSI controlled by the introduced software modules is discussed in section IV. Lastly, in section V, we present the results of the application of this approach to the study of a relatively complex scenario, tackling the timely topic of smart microgrid control.

II. Hardware & Software Toolset

The integrated design environment (IDE) discussed in this paper is made up of both software and hardware components. The software is represented by the LabVIEW© programming suite, a widely used software for control and automation applications. In particular, control functions have been generated with the LabVIEW FPGA© module, version 12.0.

A. Hardware Components

The hardware components considered throughout this paper are the so called general purpose inverter controller board, or GPIC board [9], and a particular configuration of the compact reconfigurable input output embedded control system, or cRIO [10], both from National Instruments, NI. The former is the platform upon which the controllers for the target converters are deployed. Its basic features are summarized in Table I. The latter, that hosts a more powerful FPGA, general purpose processor (GPP), and a freely configurable peripheral set, is used to virtualize the power converter(s) with coupling and filter networks, so as to implement HIL RT simulations. The cRIO configuration considered in this paper is presented in Table II.

TABLE I
Control Platform Characteristics (GPIC)

Feature	Parameter	Value
Processor	Model Processor Speed	PowerPC 400 MHz
Memory	Nonvolatile System	512 MB 256 MB
FPGA	Model # Slices # DSP48s	Xilinx Spartan-6 LX45 6822 58
Network	Network interface	IEEE 802.3 Ethernet
Communication	Port	RS-232, RS-485 CAN, USB
Peripherals	Channel	16 AI, 12-bit, ±10 V, 100 kHz 14 ch., 500 kHz gate drivers (1)

(1) Only the used subset of the NI 9683 mezzanine-card ports is reported.

TABLE II
Simulation Platform Characteristics (cRIO-9082)

Feature	Parameter	Value
Processor	Model Processor Speed	Intel Core i7-660UE 1.33 to 2.4 GHz
Memory	Nonvolatile System	32 GB (min.) 2 GB (min.)
FPGA	Model # Slices # DSP48s	Spartan-6 LX150 23038 180
Network	Network interface	IEEE 802.3 Ethernet
Communication	Port	RS-232, RS-485/422, USB VGA, CAN, MXI-Express
Peripherals	Channel	4 AO, 16-bit, ±10 V, 100 kHz 8 Digital Input/Output (1)

(1) Specs of the used digital (NI 9401) and analog (NI 9263) modules.

B. Software Components

The typical inverter control software has a multi-layer structure [11]. The lowest layer is the modulation software, that generates the logic signals for the inverter switch drivers. Upon that, a current controller is implemented, whose function is to allow the voltage source inverter to operate as a controlled current source. The implementation of this layer requires a feedback loop to be closed: a current sensor is used to provide samples of the inverter phase current, acquired at strategically placed instants during the modulation period. These are later processed by a digital regulator, in the simplest case, of

proportional integral, or PI, type. On top of the current control layer other loops are often implemented, that depend on the particular application, like, for example, a voltage control loop, a DC-link control loop, an injected power control loop (for some grid-tied inverters). These control functions require minimum delay and tight synchronization. Therefore, they are particularly well implemented on programmable logic devices, like FPGAs, where the control delay can be minimized and jitter free synchronization between the different control layers can be achieved.

As can be seen in Table I, the GPIC board is actually an heterogeneous computing platform, allowing the programmer to deploy control software both on an FPGA target and on a GPP target. A peculiar feature of the considered design environment is that the organization of the controller software, from the programmer point of view, is basically the same, irrespective of what is the target. In other words, the same data structures can be implemented, both when the controller runs on a GPP and when it is turned into the hardware configuration of an FPGA chip. It is the development environment that, almost transparently to the user, compiles the code differently, depending on the selected target. Clearly, this greatly simplifies the approach with hardware synthesized controllers. When the controller has to be deployed on an FPGA, the programmer can actually optimize the code performance and chip resource utilization, taking advantage of the specific FPGA building blocks provided within the IDE toolbox. These implement commonly used configurable fixed point arithmetic and logic functions, in some cases designed by the FPGA chip manufacturer, guaranteeing maximum data throughput. Therefore, it is wise to use them in place of the general purpose arithmetic functions, conceived to run on a GPP. The availability of a GPP on board the GPIC can be extremely useful to deal with the higher level control tasks of complex application scenarios, as it is described in the last section of this paper.

III. Implementation Example: Inverter Current Controller

The first example we would like to discuss is the implementation of a digital PI current controller for a grid-tied voltage source inverter. The considered inverter model, that replicates the physical hardware available at our laboratory, is shown in Fig. 1. The inverter and controller parameters are listed in Table III. The controller building blocks are represented by:

1) PWM modulator;
2) PI current controller;
3) Current reference generator.

All are meant to be deployed on the FPGA chip available on board the GPIC. In the following we discuss their implementation in more detail.

A. Controller Building Blocks

The software module for the PWM modulator is shown in Fig. 2. As can be seen, it is made-up of a single loop and a *case* structure. The latter is used to discriminate the ramp-up and ramp-down phases. Indeed, the modulator generates a symmetrical and centered triangular carrier, and compares

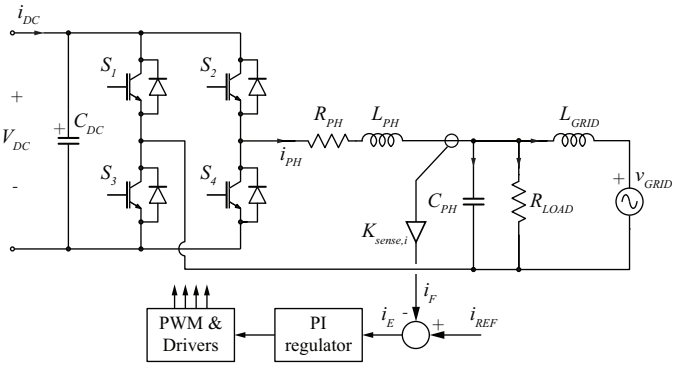

Fig. 1. Inverter model for real-time simulation and control design. The inverter is grid tied and a purely resistive load is considered.

TABLE III
System Parameters

Parameter	Symbol	Value	
Nominal input voltage	V_{DC}	400	V
Switching frequency	f_s	18	kHz
Filter inductance	L_{PH}	2	mH
Series inductor resistance	R_{PH}	1	Ω
Output filter capacitance	C_{PH}	1	μF
Current sense gain	$K_{sense,i}$	1	V/A
Line inductance	L_{GRID}	0.5	mH
Load resistance	R_{LOAD}	41	Ω
Grid voltage	v_{GRID}	230	V_{rms}
Current control bandwidth	BW_I	1.2	kHz
Phase margin	Φ_M	60	°
Carrier amplitude	$\pm A_r$	$\pm 2^7$	
A/D conversion delay	Δt_{AD}	10	μs
PI calculation delay	Δt_{calc}	1	μs

it with the modulating signal, thus generating the switch command that is sent to the `DO0` pin of the control board.

Even an inexperienced LabVIEW user can appreciate the simplicity of graphic programming and the easy way hardware resources are addressed within the program. This is further visible when we consider Fig. 3. Here, the acquisition of the current feedback signal is performed (note how the `AI0` channel of the GPIC board is accessed) and synchronized with the modulation code through a LabVIEW peculiar structure, more commonly used in FPGA programming, known as a

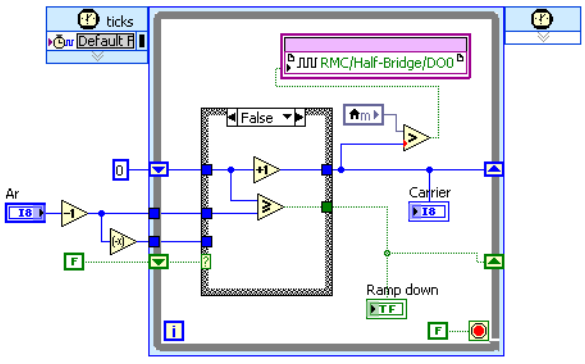

Fig. 2. PWM modulator software module.

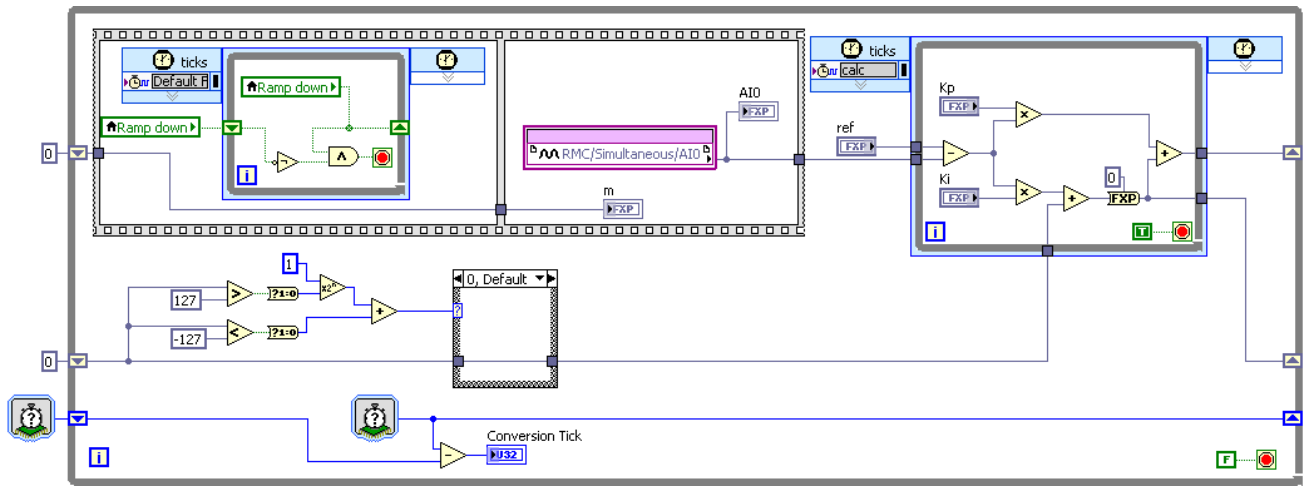

Fig. 3. Acquisition and control software module.

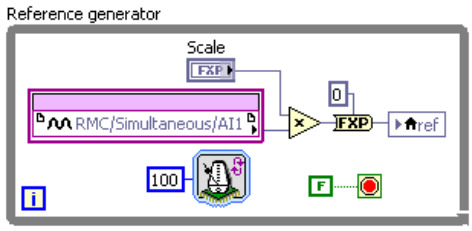

Fig. 4. Current reference generation software module.

frame. The current sample is then processed by a PI regulator, visible in the right hand side of the figure.

The reference generation software module is represented in Fig. 4. Its basic task is to define the phase relation between the grid voltage and the injected current. In its simplest form, shown in the figure, it calculates a properly scaled replica of the grid voltage waveform (acquired at `AI1` input of the GPIC board), so that only active power is injected into the grid.

It is worth noting that the code here presented is not strictly optimized and represents a *level 0* approach to FPGA programming in LabVIEW. It exemplifies well how, even without a deep knowledge of the underlying hardware, one can get an application running with limited effort. Besides, more sophisticated implementations are possible, where reactive power control is also guaranteed. Although we are considering a single phase converter, active/reactive power control can be implemented through the conventional d-q transformation approach, simply by creating a virtual *q-axis* in the synchronizing PLL algorithm. This solution is used in the application example discussed in section V.

B. User Interface

In a LabVIEW program, i.e. in a virtual instrument (VI), all inputs and outputs are organized and accessed via a user interface, called *front panel*. When the FPGA VI is launched from the IDE, the corresponding front panel is automatically reproduced on the development PC, enabling the user to set controls and view indicators. This allows the interaction with the FPGA VI at a typical rate of several updates per second, which is adequate to the purpose of monitoring the application during debugging. A more flexible interface can be set-up through the GPP on board the RIO device which, in addition, provides a deterministic access to the FPGA application. More specifically, in this case, access to controls and indicators is programmed by the user, employing the functions of a specific interface palette, and executed by the GPP. The GPP can be further programmed to generate stimulus signals, to acquire the system response, and to present data to the user (e.g., graphically via the front panel of its LabVIEW program). The communication between the development PC and the RIO device is, in any case, provided by an Ethernet link, as shown in Fig. 5.

IV. Software Debugging Through HIL RT Simulations

Taking advantage of the cRIO FPGA module, it is possible to create a numerical model for the converter shown in Fig. 1,

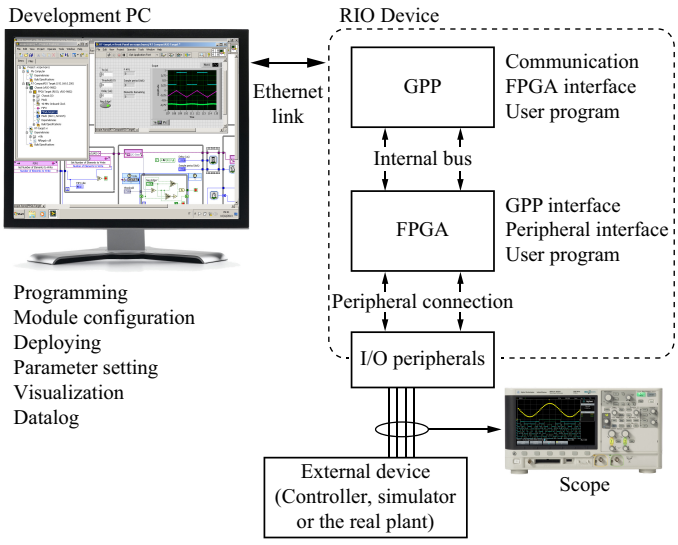

Fig. 5. Typical system configuration with user interface.

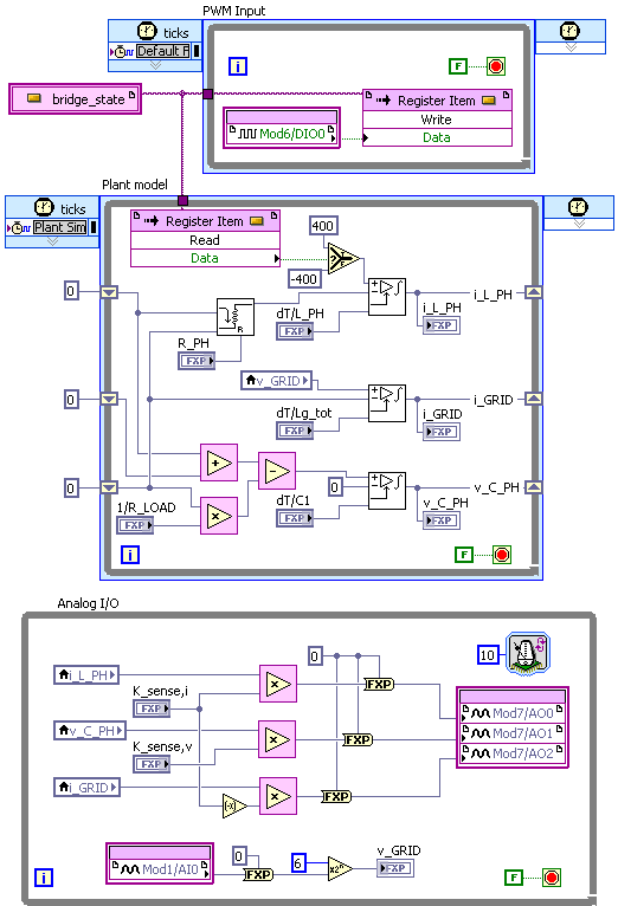

Fig. 6. FPGA implementation of the inverter model on the cRIO hardware. Top: digital input management – middle: network topology with discrete time integrators – bottom: analog inputs and outputs management.

comprising inverter (ideally modeled as a switched voltage source controlled by a logic signal), filter/coupling network and load. The filter/coupling network and load model is analytically formulated as the zero order hold discretization (or Euler discretization) of the continuous time network equations. The discrete time versions of the electrical variable relations are subsequently turned into a LabVIEW FPGA program, taking advantage of the optimized arithmetic functions available within the toolbox.

A view of the resulting program is given by Fig. 6. As we can see, an optimized digital integrator block is repeatedly used in the model definition. It is the digital counterpart of the continuous time integrator appearing in the original model. The topology of the coupling network is reflected in the way signals are routed in the block diagram of the LabVIEW program. It is worth underlining that, at this time, we do not have any automatic software tool capable of reformulating an electrical network into an FPGA compatible discrete time algorithm. The derivation of the model depicted in Fig. 6 is therefore done manually, by pencil and paper calculations, as it happens, for example, by coding with the traditional MATLAB/Simulink diagrams. Differently from ordinary coding, however, real-time simulation coding requires timing and synchronization issues to be accurately dealt with. This may represent, in view of more complex case studies, a possible limitation of our approach. Actually, what we do can be considered as the pencil-and-paper version of the modeling approach described in [6].

Referring once more to Fig. 6, let's point out in the following two of the challenges in obtaining precise and accurate simulation of power electronics, due to the digital nature of the simulation platforms [13].

- From Fig. 6, we see that the model input is represented by the PWM signal generated by the GPIC (DO0). The time resolution of the cRIO digital inputs is 100 ns, which is a relatively high value. To prevent jitter phenomena in the interpretation of the digital PWM inputs to the cRIO plant model, the time resolution of the GPIC PWM outputs should be larger than that. Indeed, in our implementation, the 7 bit carrier amplitude resolution and its 18 kHz frequency determine a 434 ns resolution, which prevents severe duty-cycle perturbations due to insufficient input resolution.
- The outputs of the model are the inverter phase current, the filter capacitor voltage and the grid current, AO0, AO1 and AO2 respectively. These are generated by a 16 bit DAC, whose update frequency is limited to 100 kHz. This is a rather low value, that negatively affects the quality of simulations. Indeed, the ratio of DAC update frequency over the sampling frequency is as low as 5, i.e., the analog signals are updated only five times for each sampling period. In the case of the inverter phase current, this causes significant sampling noise and triggers spurious controller dynamics. The ideal solution would be to use higher throughput DACs; for the time being, the current controller bandwidth is kept lower than the typical tenth of switching frequency, so as to increase the controller robustness to injected noise. It is worth noting that this hardware limitation has an impact on the model discretization step as well. The model is obviously solved by fixed step integration, therefore, frequency response warping can take place close to the Nyquist limit. This is the reason why, in principle, the discretization step should be kept as low as possible. Unfortunately, discretization steps lower than 10µs make little sense with the available DACs.

Despite the outlined issues, a typical outcome of the system's simulation is shown in Fig. 7. As can be seen, the obtained waveforms are acceptably smooth. The simulation represents the case when the inverter is controlled to deliver exactly the active power drawn by the resistive load. As a result, the current on the grid is practically zero. As a matter of fact, a small amount of reactive power is absorbed by the inverter output filter, which is provided by the grid, determining the small line current visible in the figure. The result proves that the model is capable of replicating the expected system behavior. By routine, HIL simulations are always cross checked with conventional simulations, e.g., based on MATLAB/Simulink© models, at least for short simulation times like those here considered. The results are not shown here because they appear identical to those of

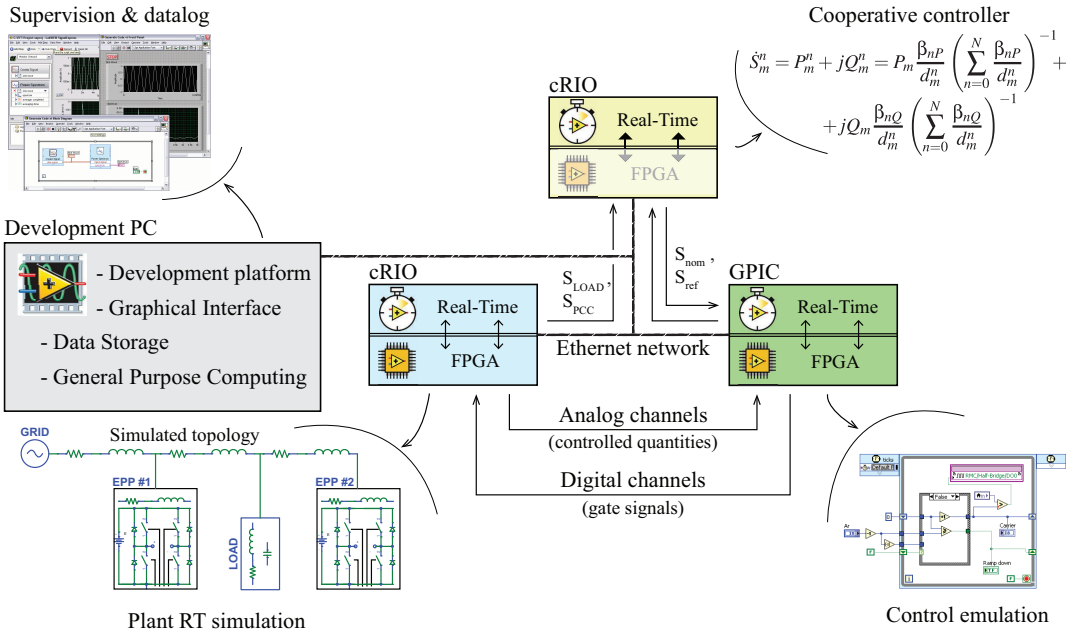

Fig. 8. Considered model for cooperative control test: real-time simulation system.

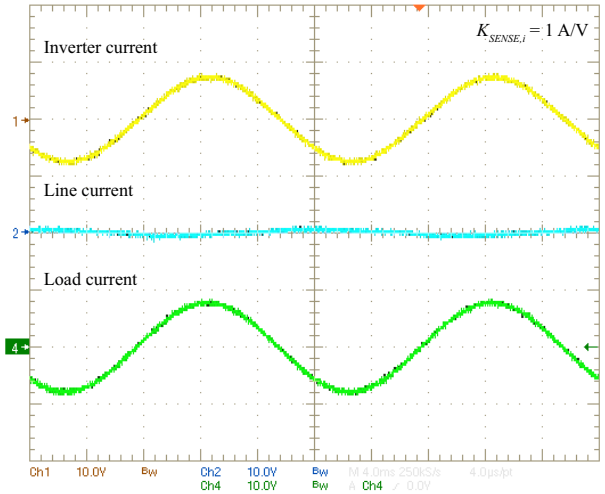

Fig. 7. HIL RT simulation of inverter current control – depicted waveforms: inverter current (yellow), line current (light blue), resistive load current (green) – horizontal: 4 ms/div; vertical: 1 A/div.

Fig. 7. After that, the controller running on the GPIC can be considered functional and the developed software/hardware control system can be embedded into the physical inverter.

As a final remark, it is interesting to note that the FPGA resource utilizations for the simple codes presented so far are 12% on the GPIC and 11% on the cRIO, without any specific code optimization.

V. A More Complex Scenario: Cooperative Control Low-Voltage Microgrid

The limited hardware considered in this paper is actually capable of sustaining more complex control application scenarios. To give a further example, we now propose a situation where *two* current mode controlled inverters operate in a

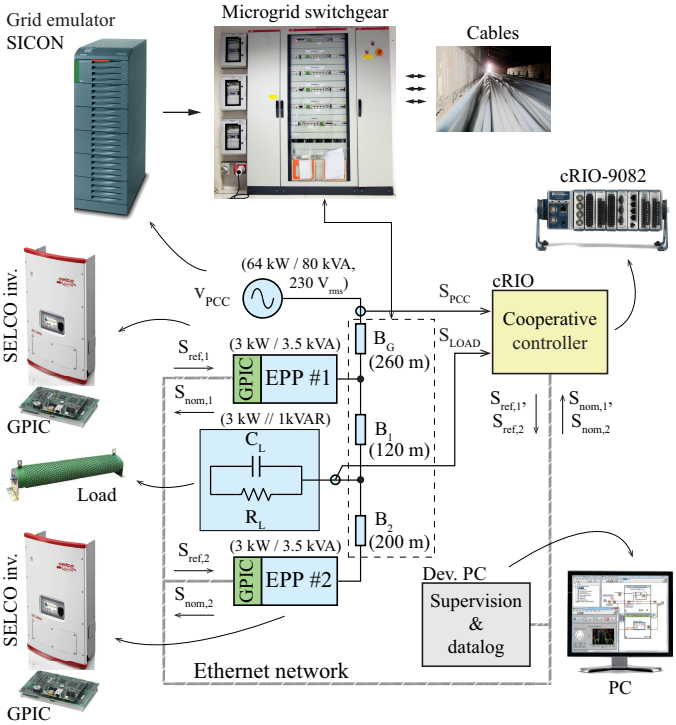

Fig. 9. Considered model for cooperative control test: experimental set-up.

centrally supervised microgrid. The purpose of the supervising strategy, which is described in detail in [15], is to coordinate the two inverters so as to minimize conduction losses on the grid. The basic idea is that the inverter that is placed closer to the load, which is known to the central supervisor, should supply the larger part of the needed active and reactive power.

A schematic representation of this case study is shown by Fig. 8, presenting a view of the hardware organization for the

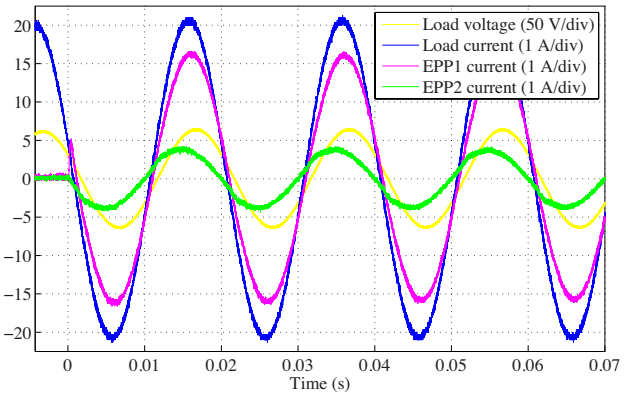

Fig. 10. HIL RT simulation test of the cooperative control strategy for a microgrid.

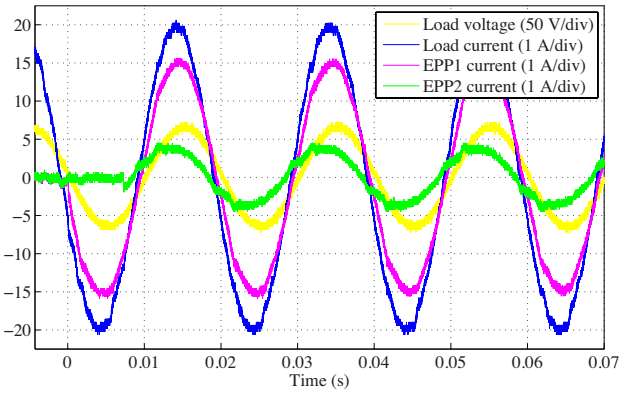

Fig. 11. Experimental test of the cooperative control strategy for a microgrid.

HIL RT simulation, and Fig. 9, illustrating the corresponding experimental set-up. The addressed system is actually a simple kind of grid-connected microgrid. It is composed of two inverters, also named electronic power processors (EPPs), connected by the distribution branches B_1 and B_2 to a linear load. The connection to the main grid is provided by the branch B_G, visible in Fig. 9. The set-up can be considered as a test bench for inverter control techniques and, as is discussed in the following, for optimum management algorithms for smart microgrids [14].

As can be seen, in this case the scenario is much more complex: not only two inverters are considered, but a new digital device comes into play, that is the centralized grid supervisor. Its task is to acquire the total load power absorption, to compute active and reactive power set-points for each inverter, and to periodically transmit them through the communication channel. Therefore, in addition to the local control for each inverter, here the study elaborates also on supervising control and communication channels.

The software development and debugging follows exactly the same line described above for the simple case of the basic current controller, comprising coding, HIL RT simulations and experimental tests. As far as code is concerned, the main distinctive features for the local inverter controllers (GPIC) required by this study are:

1) the activation of a communication channel (Ethernet) linking the GPIC devices to the central supervisor;
2) the use of d-q transformation to convert active and reactive power set-points into a suitable reference current signal which, in turn, requires
3) the implementation of a digital PLL that synchronizes each inverter to its local grid voltage.

It is worth noting that the communication channel is managed by the GPP on the GPIC device, so that it does not impact on the FPGA utilization, which is now higher, approximately equal to 50% of the total capability, due to the implementation of functionalities 2) and 3), but still far from saturation.

The centralized supervisor is implemented on a cRIO device, exploiting its on board real-time GPP to run the cooperative control algorithm. Being the computational burden not so light, the GPP has been used to take advantage of single precision floating point arithmetic. As mentioned above, the details concerning the supervising strategy, i.e., the logic based on which the supervisor determines the optimal power set-points for the microgrid inverters, are described in detail in [15]. Very basically, the optimization objective is to keep the grid losses to a minimum. From the inverter controller standpoint, this simply means that externally computed active and reactive power set-points are periodically received through the communication channel.

As a final remark on the cooperative control implementation, Ethernet networking has been used to implement the communication links as it is natively embedded in the controller hardware and supported by software. We would like to emphasize that this does not impair the capability of the illustrated set-up to validate any control strategy, nor reduce its flexibility to integrate other communication technologies, like, for example, power line communication (PLC).

We observe that the integrated multi-layer architecture of the controlling hardware, that hosts not only programmable logic circuitry, but a fully functional GPP as well, and seamlessly manages data exchange between the two computational layers, is what really enables a rapid development of this experiment. Thanks to that, for example, it is relatively easy to implement the required Ethernet communication links. Besides, all the system can be remotely monitored, as each device can be accessed from a conventional PC to perform, e.g., data logging and off-line processing.

As far as HIL simulations are concerned, we use, once again, a cRIO unit, whose FPGA runs the controlled plant model. This comprises the two inverters, a passive parallel connected R-C load and the interconnecting power network. The resulting FPGA occupation is nearly 50%. From this standpoint, minor improvements can be obtained optimizing the FPGA code of the model, but it is clear that, with our hardware, the set-up shown in Fig. 8 and Fig. 9 defines the manageable complexity level of the systems that can be simulated. To go further, we have recently acquired a much more powerful hardware platform, known as PXI, [12], whose FPGA boards offer about a tenfold increase in capacity and whose analog and digital peripherals allow multi-MHz update frequencies, solving all previously mentioned issues.

Fig. 10 and Fig. 11 show how the system operates in HIL RT simulations and in real life, respectively. The simulation

TABLE IV
COOPERATIVE CONTROL TEST PARAMETERS

Parameter	Symbol	Value	
B_G branch resistance	R_{B_G}	0.6	Ω
B_1 branch resistance	R_{B_1}	0.4	Ω
B_2 branch resistance	R_{B_2}	0.7	Ω
Load capacitance	C_{LOAD}	60	μF
Load resistance	R_{LOAD}	47/3	Ω
Grid voltage	v_{PCC}	230	V_{rms}
Current control bandwidth	BW_I	2	kHz
Phase margin	Φ_M	60	°
Reference update period	Δt_{update}	5	s

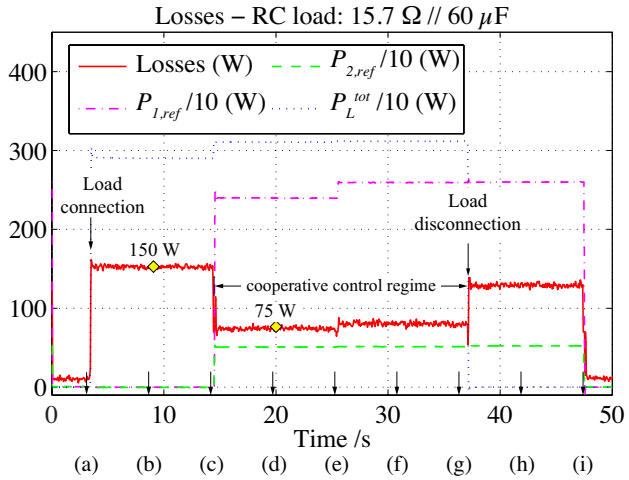

Fig. 12. Measured power losses for the experimental test.

parameters are summarized in Table IV; basically, the simulation and experiment start with disconnected inverters and the utility grid feeding the loads. The microgrid supervisor computes the optimal references and dispatches them at time $t = 0$. As a result, both inverters begin injecting the calculated active and reactive power as soon as the new power references are received, as is visible from the phase relation between load voltage, the yellow trace, and inverter currents, the purple and green traces. It is possible to see how the simulation correctly predicts the experimental results.

Lastly, Fig. 12 shows the power response of the experimental set-up while it undergoes a load connection and disconnection. It is noticeable the effect of the cooperative control of the power injected by the two inverters on distribution losses. In particular, due to the proposed algorithm, distribution loss decreases by 50% once the cooperative control regime establishes. Corresponding results were achieved from the HIL RT simulation of the experimental set-up.

VI. CONCLUSION

The application of LabVIEW FPGA© as a design environment allowing the rapid prototyping and the HIL RT simulation of digital controllers for power converters is discussed in this paper. Thanks to its user friendliness, the tool allows even inexperienced users to start programming FPGA chips after a relatively brief training phase. At the same time, it can be used to develop software applications for GPPs, thus allowing effective hardware/software co-design. To exemplify its usage, a digital current controller for a 3 kVA grid-tied inverter is considered, whose basic building blocks are illustrated. Exploiting two different hardware platforms, hardware-in-the-loop real-time simulations are possible and represent an effective means for safe and accurate controller debugging and tuning. The current controller can be embedded into more sophisticated inverter applications. As a final example, the centralized cooperative control of two current mode controlled inverters, connected to a microgrid, is presented. This example allows to verify how, applying the proposed methodology, different issues, typical of smart grid control, can be addressed, both in HIL RT simulations and in experiments. These include local inverter control, centralized or distributed grid optimization, communication channels.

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Solar Cybertech: A Competition of Digitally Controlled Vehicles Poweredby Solar Panels

O. García, J. A. Oliver, D. Díaz, D. Meneses, P. Alou, M. Vasić, J. A. Cobos

***Abstract*—Solar Cybertech is a conquest/subject at Universidad Politecnica de Madrid where student teams deal with electronics and renewable energies. The conquest is based in the design and construction of a vehicle powered by solar panels to complete a circuit that has different zones as a flat region, rising and falling slopes and a shaded region as well where different operating conditions are required. To optimize the energy consumed by the motors of the vehicles from the solar panels, a dc-dc converter is used. The control stage of the converter is digital and a maximum power point tracking algorithm has been used. Besides these objectives, this subject is intended to enhance the team work and cooperation as well as the application of the theoretical knowledge in a practical application.**

***Index Terms*—Solar panel, dc-dc converter, student competition.**

Original Research Paper
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I. Introduction

CYBERTECH started in the year 2001 in the Escuela Técnica Superior de Ingenieros Industriales (ETSII) of Madrid with a single event, with the objective of designing and implementing a robot that able to complete a circuit following a black line in the floor over a white floor. During the next years, more events were added, as well as the development of a robot to escape from a labyrinth in as less time as possible. Other new event added is the implementation of a bullfighter robot that has to interact with a robotic bull created by the organization.

Few years later, it was introduced in a new event, based on the growing interest in the renewable energies. This new event is based in the implementation of a vehicle capable of completing a circuit with several difficult zones in as less time as possible, using as the only power supply a solar panel.

The difficult zones of the circuit are:

- Rising slope (climbing the bridge).
- Shaded region (under the bridge).

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These different regions allow the implementation ofan 8-shaped circuit with two mechanical parallel guides to facilitate the races between two cars and having the circuits of both vehicles exactly the same length. Figure 1shows a photograph with the final circuit during the celebration of the competition where the different regions can be appreciated, that appear naturally when the bridge to close the 8 shaped circuit is placed.

Considering these difficulties in the vehicles operation, it is critic to optimize the energy flow obtained from a limited power source, a solar panel. To optimize the energy obtained from the panel a dc-dc converter has been added between the source and the load, a low voltage dc motor or motors used to power the vehicle.

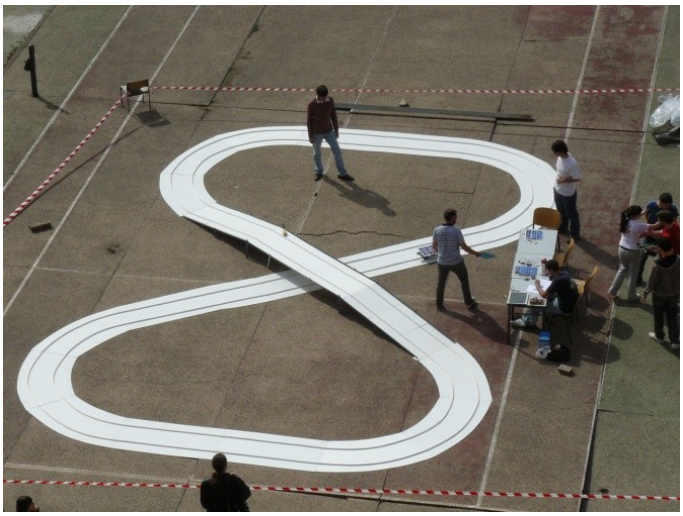

Fig. 1. Photograph of the Solar Cybertech circuit on a tennis courtyard during the competition.

To comply with the conquest objectives, to complete the circuit in as less time as possible, is necessary to maximize the power delivered by the solar panel.

For this reason the students have to implement a control algorithm that makes the dc-dc converter operate in the maximum power point tracking (MPPT).

Figure 2 shows the block diagram of the system used for the Solar Cybertech conquest.

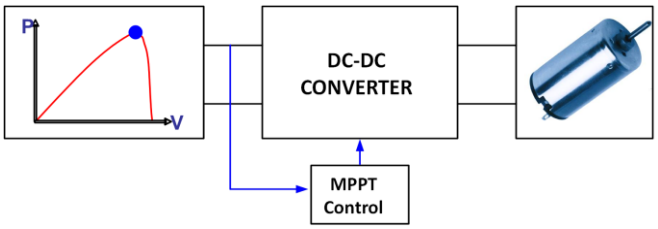

Fig. 2. Block diagram of the system.

II. TEACHING

With the new plan of studies, the Solar Cybertech conquest became part of the optional subjects of the industrial engineering grade, being two professors the responsible of the subject. As part of the subject the participant teams attend to theoretical lessons where they acquire the basic knowledge to carry out the conquest tasks as well as a set of conferences that deal about different aspects of the technology in other areas as the art or the environment conservation.

Each participant team in the subject and conquest has a supervisor, normally a student with a certain degree of experience that has been a participant in the previous years. This supervisor helps and controls the work of his assigned teams, two or three maximum to guarantee an adequate attention. Additional tasks are the technical supervision and advice in different aspects as the converter design, the control algorithm or in the design of the vehicle (Figure 3).

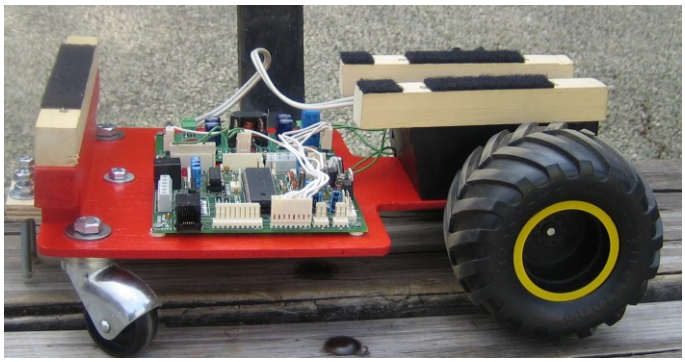

Fig. 3. Participant vehicle: structure, converter and control PCB.

The teams are formed by three to five students maximum, with the intention of a proper share of the amount of work between all of them and also to facilitate an adequate control of the work done by each student. Each team has to provide documentation before the competition with the proposed solutions to complete the conquest and to inform to their supervisors in the previous knowledge that has each group. As the final task, there is a final exam, which is also a condition to participate in the competition, as one of the parts of this exam is to complete one of the zones of the final circuit.

With this subject format it is intended, besides the team working and competitive improvement of the students, to provide the first contact with the electronic, developing a practical application, developing a prototype and doing experimental tests on it.

III. IMPLEMENTATION OF THE SOLAR CAR

As it has been commented, each participant team has to implement a vehicle, which from now will be called the solar car, which is based on a structure where the components of the blocks of Figure 2 are added. The different components are analyzed in the following subsections.

A. Solar Panel

The power supply of the solar car will be photovoltaic solar panels. The panels obtain the energy from the solar radiation, with the limitation that not always it is available, and not always the same level of power can be obtained.

The solar panels are implemented by the combination of solar cells. Each cell has the equivalent circuit shown in Figure 4.

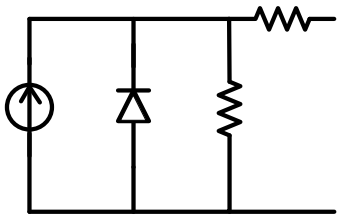

Fig. 4. Schematic circuit of a solar cell.

The selected solar panels for the contest can deliver a maximum power of 10W. The weight is 2Kg and the dimensions are 340x330 (cm). The open circuit voltage is 21.5V while the short-circuit current is 0.62A.

The solar panels have been characterized and the voltage-current and voltage-power are shown in Figure 5.

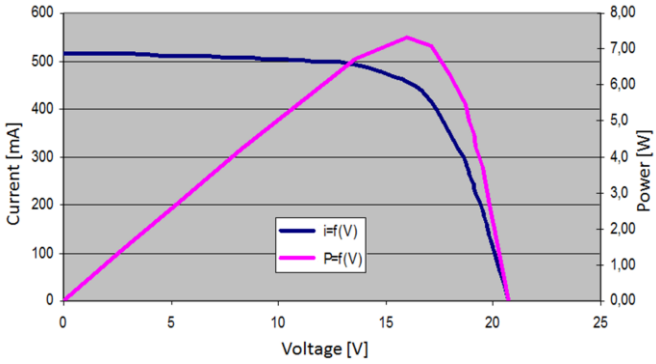

Fig. 5. Measured I-V and P-V curves for the 10W panel.

It can be seen in Figure 5 that, even in the best conditions, the maximum power is 80% of the nominal power in the maximum power point. Therefore, the design must optimize the efficiency and reduce the weight so the available power is enough for the solar car to complete the circuit, and to do it as fast as possible.

B. DC-DC Converter

To process the energy correctly and to obtain as much power as possible, a dc-dc converter controlled by PWM modulation will be used.

Due to the input voltage range obtained from the solar panels, with lower and higher values than the nominal operation voltage, the Flyback topology was chosen for the dc-

dc converter operation, as it is capable of producing higher and lower output voltages than the input voltage.

Forthe firstedition, the organization made the design of the converter as well as the PCB, shown in Figure 6, for the physical implementation as well as a tutorial for the soldering and assembly of the components in the PCB.

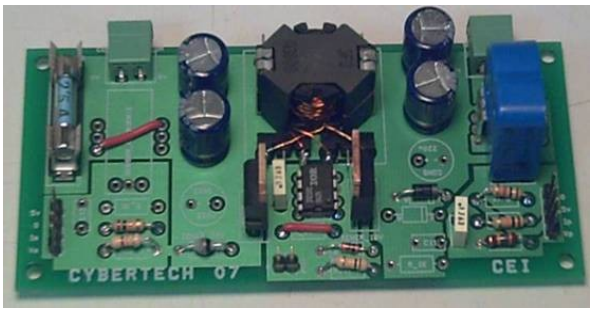

Fig. 6. PCB of the Flyback converter used in the first edition ofSolar Cybertech.

C. Converter control

The control of the dc-dc converter is of essential importance for the complete system due the following reasons:

- It has to find the peak power point of the solar panel.
- It adjusts the energy from the solar panel towards the dc motor of the car.

For the practical implementation it has been chosen a digital control implemented using a PIC18F442. The board with the microcontroller had been previously developed and given to the students by the Cybertech organizers.

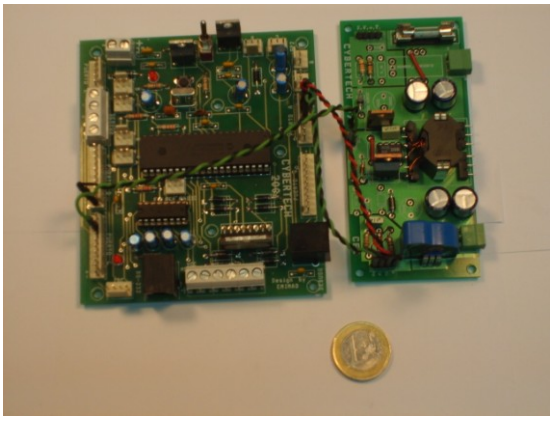

Fig. 7. Control PCB (left) and Flyback converter (right)used in the first edition of Solar Cybertech.

In order to implement the Maximum Power Point Tracking (MPPT) algorithm, it is necessary to measure two parameters, the input current and voltage. For the voltage measurement, a simple voltage divider is used, while the current is measured using a commercial current sensor.

The algorithm consists of constantly search the MMP by doing small incremental changes on the duty cycle. With these changes the algorithm is able to move the operation point along the power curve of the solar panel, having in mind two different zones. The first zone is for voltages higher than the V_{MPPT} (on the right side from the maximum power point), while the second one is for voltages lower than V_{MMPT} (on the left of the maximum power point). In each new working point it is necessary to measure the power and compare it with the previous measurement and decide if the panel voltage should be increased or decreased taking into account if the power has decreased or increased. Figure 8 illustrates the basic idea of the algorithm.

The procedure is the following: after each measurement the voltage and current measurement arestored, the duty cycle of the flyback converter is incrementally changed and the new output power is compared with the previous measurement. If the output power has increased and the working point is in the second zone (voltages higher than the V_{MMPT}, from x_n to x_{n-1} in Figure 8) it is necessary to increase the duty cycle. Similarly, if the working point is in the first zone, (from X1 to X2 in Figure 8), the duty cycle has to be decreased. In order to know in which part of the power curve we are, so we can define the sign of the duty cycle increment, the voltage measurement has to be saved together with its corresponding output power. If this information is not saved, the duty cycle will saturate in its minimum or maximum value and the output power will fall to zero.

The PWM signal that comes from the control board is sent to a driver which generates the proper control signals for the MOSFET of the flyback converter.

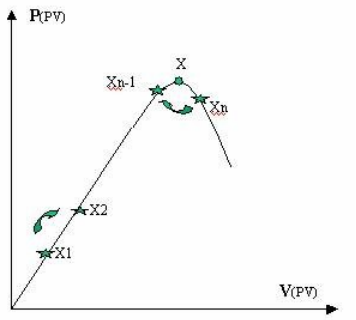

Fig. 8. V-P curve of a solar panel. MPPT algorithm representation.

D. DC motor

The dc motor receives the controlled power from the dc-dc converter and transmits it to the vehicle wheels through a set of gears. These gears decrease the nominal speed of the dc motor (3000 rpm) increasing the torque which is necessary for the vehicle to drive up the slope in one part of the test circuit.

The student teams were not limited with the number of dc motors. Each team decides for itself which dc motor will use and how will it connect to the vehicle.

In the first edition of the competition, there were 14 registered teams (approximately 70 students) and each constructed vehicle was able to complete the test circuit. Two teams were able to complete the test circuit including the shadowed part of the circuit as well. One team implemented a system and an algorithm for the solar panel orientation so that it always receives the maximal solar panel in each part of the test circuit. This team won the award for the best innovation given by the organization committee of the competition.

IV. 2ND EDITION OF SOLAR CYBERTECH

For the second Solar Cybertech competition, that was held in the last week of April, few modifications were introduced in order to enhance the learning and motivation of the students.

Instead to use a single solar panel, like in the previous year, it was possible to use different alternatives, which provide different output powers and have different sizes (mm x mm) and weight (g):

1. 10W/ 340x330/ 2000
2. 5W/ 270x270/ 800
3. 1.38W/ 75x116/ <10
4. 1.38W/ 75x64/ <10
5. 770mW/ 75x46/ <10
6. 550mW/ 75x116/ <10
7. 220mW/ 35x30/ 100
8. 100mW/ 67x35/ 50

The panels 1 and 2, 10W and 5W respectively, are complete commercial solutions, with several interconnected voltage cells and with a protecting glass. Their advantage is that these panels are quite robust, however, the main disadvantage is the increased weight due to the safety glass. Solutions from 3 to 6 are individual cells, which each team can combine in order to obtain a configuration that will provide desired voltage and power. Solutions 7 and 8 are complete solar panels with low weight, but with decreased output power.

Having in mind these characteristics, it is necessary to introduce some restrictions for solar panel selection:

- The maximal size is 330mm x 340mm
- The solar cells that can be combined are 3 to 6
- The maximal output power of one combination is 10W

For the cells between 3 and 6 it is necessary to put several panels in series due to the cell open circuit voltage of 0.55V, which is significantly lower for the proper functionality of the system

Having in mind that each solar panel has different electrical characteristics, the voltage of the peak output power varies among them. In the most of the cases, this voltage is different from the nominal output voltage of the dc-dc converter.

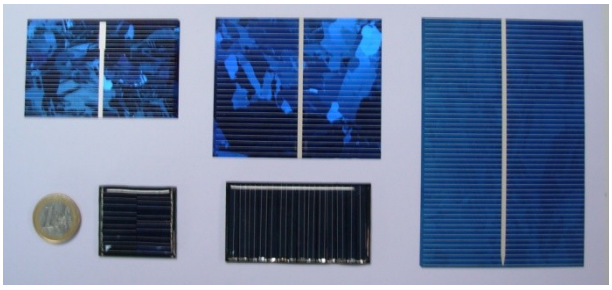

Fig. 9. Different types of solar panels used in the second edition of Solar Cybertech.

The new panel configurations have different voltages and, therefore, it is necessary to consider different topologies for the dc-dc converter:

- boost topology
- buck topology
- flyback topology.

The flyback topology is the most versatile, because it will operate correctly for any panel configuration and any dc motor selection. The buck topology is used when the minimum panel voltage is higher than the nominal voltage of the dc motor. Similarly, the boost topology is used in the opposite case.

Additional task was to design the dc-dc converter. For this task a new workshop was included and a design guide was created [1] to simplify this task.

The digital platform for the implementation of the control was another point where an improvement has been made. The board forthe first edition had high energy consumption (higher than 1W) because it was designed to include other functionalities of the microcontroller. Another drawback of this board was the high number of components which makes difficult the hardware debugging when something is not working.

To solve this, a new selected control board was Arduino, an open hardware platform, which has lower consumption and lower complexity than the previously used control board. The power consumption with Arduino was around 200mW (comparing to 1W with a PIC platform). The processor in this case is an ATMega 168. The employed board has an USB connection which is used as the power supply and programming cable at the same time.

Although Arduino is an open platform and the implemented programme is shared among users, it was impossible to find a library that generates a PWM signal of desired frequency (100 kHz) and also with a variable duty cycle. Therefore, it was necessary to develop this library.The code can be seen in Figure 11.

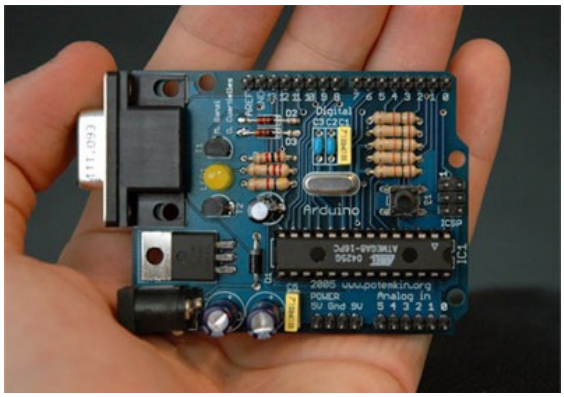

Fig. 10. Control board (Arduino) that was used in the second edition of Cybertech competition.

In the competition there were 10 teams (approximately 50 students) and all the teams were able to complete the test circuit. Four teams were able to finish the circuit passing the shadowed part of the circuit as well. The award for the best innovation was given to the team that implemented an additional system of gears activated by a servo-motor and a signal generated by simple light sensor (LDR). A photograph of the competition is shown in Figure 11, where two cars are at the beginning of the rising slope, one of the most challenging zones of the circuit.

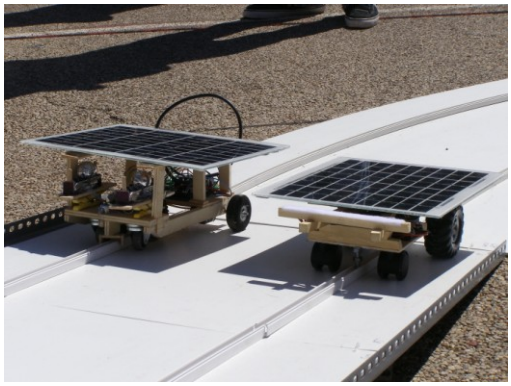

Fig. 11. Photograph of the Solar Cybertech competition.

All the information regarding the Cybertech competition can be found at the following link:
http://www.disam.upm.es/cybertech/

V. Teaching Experience

The experience obtained during the Solar Cybertech competition was very positive, due to the high motivation level of the participating students and their dedication. The students showed great interest in the buyinga solar panel in order to enhance their solar vehicle in their spare time.

This competition was made as a subject, serving to the students as an introduction to electronics, developing a practical application. Additionally, they obtained some basic knowledge regarding solar energy, switching power supplies, programming and usage of microprocessors. Finally, they had to deal with all the problems that can occur during the implementation of a complete system (from the control algorithm to the mechanical adjustment of the implemented vehicle).

Generally, the student teams were composed from the students who are specialized in electronics and automatics. It was common to find teams composed from the students from different areas of specialization, which in a natural way share the tasks. At the same time, this subject was very attractive for the students from the first years of studies in order to choose their area of specialization.

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- Pilar Montero Morales
- Beatriz Tato Eirín
- Pablo López Cenamor

```
#include "WProgram.h"
#include "pwmfast.h"


#ifndef cbi
#define cbi(sfr, bit) (_SFR_BYTE(sfr) &= ~_BV(bit))
#endif
#ifndef sbi
#define sbi(sfr, bit) (_SFR_BYTE(sfr) |= _BV(bit))
#endif


pwmfast::pwmfast(int pin)
{

  pinMode(pin, OUTPUT);
  _pin = pin;

}


void pwmfast::configurar()
{

  sbi(TCCR1A,COM1A1);
  sbi(TCCR1A,WGM11);
  cbi(TCCR1A,COM1A0);
  cbi(TCCR1A,WGM10);

  sbi(TCCR1B,WGM13);
  sbi(TCCR1B,WGM12);
  cbi(TCCR1B,CS12);
  cbi(TCCR1B,CS11);
  sbi(TCCR1B,CS10);
  cbi(TCCR1B,ICNC1);

}


void pwmfast::writePeriod(int T)
{

  sreg = SREG;
// Disable interrupts
  cli();
  ICR1 = T;
  SREG = sreg;
// Enable interrupts
  sei();

}


void pwmfast::writeDuty(int d)
{

  sreg = SREG;
// Disable interrupts
  cli();
  OCR1A = d;
  SREG = sreg;
// Enable interrupts
  sei();

}
```

Fig. 12. Library developed for Arduino platform in order to obtain a high frequency PWM signal.

References

[1] Tutorials written for the students: http://www.upmdie.upm.es/Cybertech_08/solar.html
[2] Arduino website: http://www.arduino.cc/
[3] Datasheet of ATmega168.

Single-Phase Full-Wave Rectifier as an Effective Example to Teach Normalization, Conduction Modes, and Circuit Analysis Methods

Predrag Pejović, Johann W. Kolar

***Abstract*—Application of a single phase rectifier as an example in teaching circuit modeling, normalization, operating modes of nonlinear circuits, and circuit analysis methods is proposed. The rectifier supplied from a voltage source by an inductive impedance is analyzed in the discontinuous as well as in the continuous conduction mode. Completely analytical solution for the continuous conduction mode is derived. Appropriate numerical methods are proposed to obtain the circuit waveforms in both of the operating modes, and to compute the performance parameters. Source code of the program that performs such computation is provided.**

***Index Terms*—Circuit analysis, circuit modeling, computer aided analysis, electrical engineering education, power engineering education, rectifiers.**

Original Research Paper
DOI: 10.7251/ELS1317123P

I. Introduction

Application of numerical computation tools in teaching practice is in increase, following increased application of numerical tools in engineering practice. This includes both application of specialized electronic circuit simulation tools [1], [2], and general purpose numerical computation tools [3]. However, wide application of simulation software did not replace the analytical approach completely, since the analytical approach provides deeper insight into circuit operation and provides better understanding, which is of interest for design engineers.

Analysis of single-phase rectifiers is inevitable part of every general electronics course [4, pp. 179–190], or power electronics course [5, pp. 82–100]. These circuits contain low number of elements, but expose rather complex behavior in the case some sort of filtering is applied. This makes the single-phase rectifiers an excellent example to teach some fundamental methods in nonlinear circuit analysis. A numerical approach to this problem could be found in [3, pp. 231–235]. On the other hand, analytical approach in teaching single-phase full-wave rectifiers with capacitive filtering is discussed in detail in [6] and [7]. These analyses are focused to the rectifiers supplied from an ideal voltage source. However, impedance of the supplying source might be significant in practice [5, page 82], especially if the rectifier is supplied by a small transformer.

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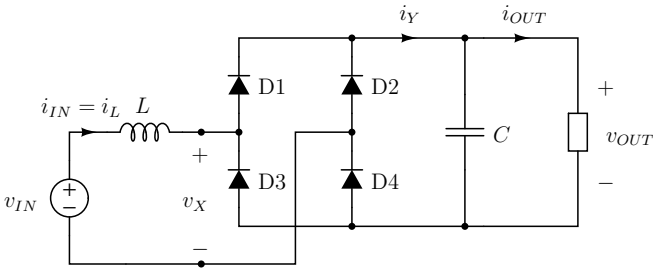

Fig. 1. The rectifier.

In this paper, analysis of the circuit shown in Fig. 1 is presented from an educational point of view. It is assumed that the supplying source might be represented as a series connection of an ideal voltage source and the source inductance L. The filtering capacitor is assumed to be large enough to neglect the output voltage ripple. This circuit is proposed as a nice example to teach circuit modeling, normalization, operating modes, conduction angle, and circuit analysis techniques. The approach has been successfully tested in teaching practice [8]. An approach to analyze this circuit is also presented in [5, pp. 91–95].

II. Preliminary Analysis, Normalization, and Analysis of the Discontinuous Conduction Mode

Let us assume that the rectifier of Fig. 1 is supplied by the voltage source

$$v_{IN} = V_m \sin(\omega t). \tag{1}$$

To simplify the analysis, let us also assume that the capacitance of the filter capacitor is large enough to justify the approximation that the output voltage is constant in time. At this time point, we are going to continue the rectifier analysis as if the rectifier output voltage V_{OUT} is known. Thus, the output part of the rectifier, consisting of the filtering capacitor and the load could be replaced by a constant voltage source of the voltage V_{OUT}, as depicted in Fig. 2, which would not cause any change in the remaining part of the circuit. The diode bridge operates such that for $i_L > 0$ diodes D1 and D3 are conducting, resulting in $i_Y = i_L$ and $v_X = V_{OUT}$. On the other hand, for $i_L < 0$ diodes D2 and D4 are conducting,

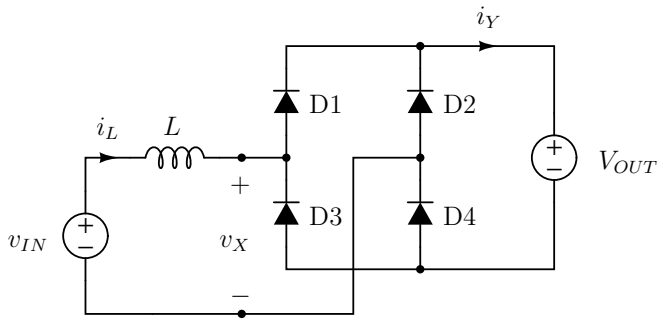

Fig. 2. Rectifier model applied in the analysis.

resulting in $i_Y = -i_L$ and $v_X = -V_{OUT}$. However, these two situations do not exhaust all of the conduction possibilities. In the case $i_L = 0$, input port of the diode bridge can stand any voltage in the range $-V_{OUT} < v_X < V_{OUT}$. An additional constraint that $di_L/dt = 0$ causes $v_X = v_{IN}$. The additional constraint requires that the inductor current is equal to zero over an interval of time. Thus, the result for the diode bridge input voltage v_X for $i_L = 0$ is obtained analyzing the remaining part of the circuit, not the diode bridge itself. In the case the inductor is replaced by a resistor, the additional constraint regarding the current derivative over time would not be necessary, but the result for v_X would be the same.

Thus, equations that characterize the diode bridge loaded with a voltage source could be summarized by the diode bridge input voltage equation

$$v_X = \begin{cases} V_{OUT}, & \text{for} \quad i_L > 0 \\ v_{IN}, & \text{for} \quad i_L = 0 \ \text{ and } \ \dfrac{d\,i_L}{d\,t} = 0 \\ -V_{OUT}, & \text{for} \quad i_L < 0 \end{cases} \tag{2}$$

and the diode bridge output current equation

$$i_Y = |i_L| \,. \tag{3}$$

It is worth to mention here that product $v_X\, i_L$ always provides a nonnegative value. Thus, the diode bridge rectifier behaves like a power sink, and there is no power that could be recovered from the diode bridge input terminals.

Assuming ideal filtering, the rectifier output current would contain only a DC component I_{OUT} equal to the average value of i_Y, while the AC component of i_Y would be taken by the filtering capacitor. In this manner, the rectifier output current for an assumed output voltage will be computed as the average value of i_Y.

Let us start the rectifier analysis from high output voltages, for $V_{OUT} > V_m$. In this case, the diodes in the diode bridge would be reverse biased during the whole period, resulting in $i_L = 0$, $i_Y = 0$, and $I_{OUT} = 0$. Thus, this situation to happen in practice would require an additional source to be connected at the rectifier output.

Lowering the output voltage slightly below V_m would cause the diodes D1 and D3 to start conducting at

$$V_m \, \sin(\alpha) = V_{OUT} \tag{4}$$

as illustrated in the first diagram of Fig. 3. It can be concluded that the conduction start angle α depends on two variables, the output voltage and the input voltage amplitude. Actually, the conduction start angle depends on the ratio of these two variables. Thus, to generalize the analysis it is convenient to introduce a normalization of the rectifier voltages and to replace all the voltages with their normalized equivalents according to

$$m_Z = \frac{v_Z}{V_m} \tag{5}$$

i.e. taking the amplitude of the input voltage as the normalization basis. In this manner, the conduction start angle is obtained from

$$\sin(\alpha) = \frac{V_{OUT}}{V_m} = M_{OUT}. \tag{6}$$

Equation that governs the inductor current in this half-cycle is

$$L\,\frac{d\,i_L}{d\,t} = V_m \, (\sin(\omega t) - M_{OUT}) \tag{7}$$

which can be transformed to

$$\frac{\omega L}{V_m}\,\frac{d\,i_L}{d\,(\omega t)} = \sin(\omega t) - M_{OUT}. \tag{8}$$

To simplify the notation further, normalization of currents naturally arises as

$$j_X = \frac{\omega L}{V_m}\, i_X \tag{9}$$

followed by the normalization of time

$$\varphi = \omega t \tag{10}$$

which effectively replaces the time variable with the phase angle variable. In this manner, the inductor equation in this half-period is simplified to

$$\frac{d\,j_L}{d\,\varphi} = \sin(\varphi) - M_{OUT} \tag{11}$$

having the solution

$$j_L(\varphi) = j_L(\alpha) + \int_{\alpha}^{\varphi} (\sin(\theta) - M_{OUT}) \; d\,\theta. \tag{12}$$

Since $j_L(\alpha) = 0$, the inductor current is given by

$$j_L(\varphi) = \cos(\alpha) + M_{OUT}\,\alpha - \cos(\varphi) - M_{OUT}\,\varphi \tag{13}$$

which is plotted in the second and the fifth of the diagrams of Fig. 3, and remains positive while $\varphi < \beta$, where $j_L(\beta) = 0$, i.e.

$$\cos(\alpha) + M_{OUT}\,\alpha - \cos(\beta) - M_{OUT}\,\beta = 0. \tag{14}$$

This situation could also be explained graphically, applying volt-second balance on the inductor voltage waveform, as depicted in the first diagram of Fig. 3. According to that explanation, the inductor current flows until the integral of the inductor voltage over time is different than zero. When the integral reaches zero, the inductor current reaches the initial current, zero in this situation. In the case

$$-m_{IN}(\beta) < M_{OUT} \tag{15}$$

all of the diodes in the diode bridge would remain reverse biased over the phase angle interval $\beta < \varphi < \alpha + \pi$, when diodes D2 and D4 would start to conduct since

$$-m_{IN}(\alpha + \pi) = M_{OUT} \tag{16}$$

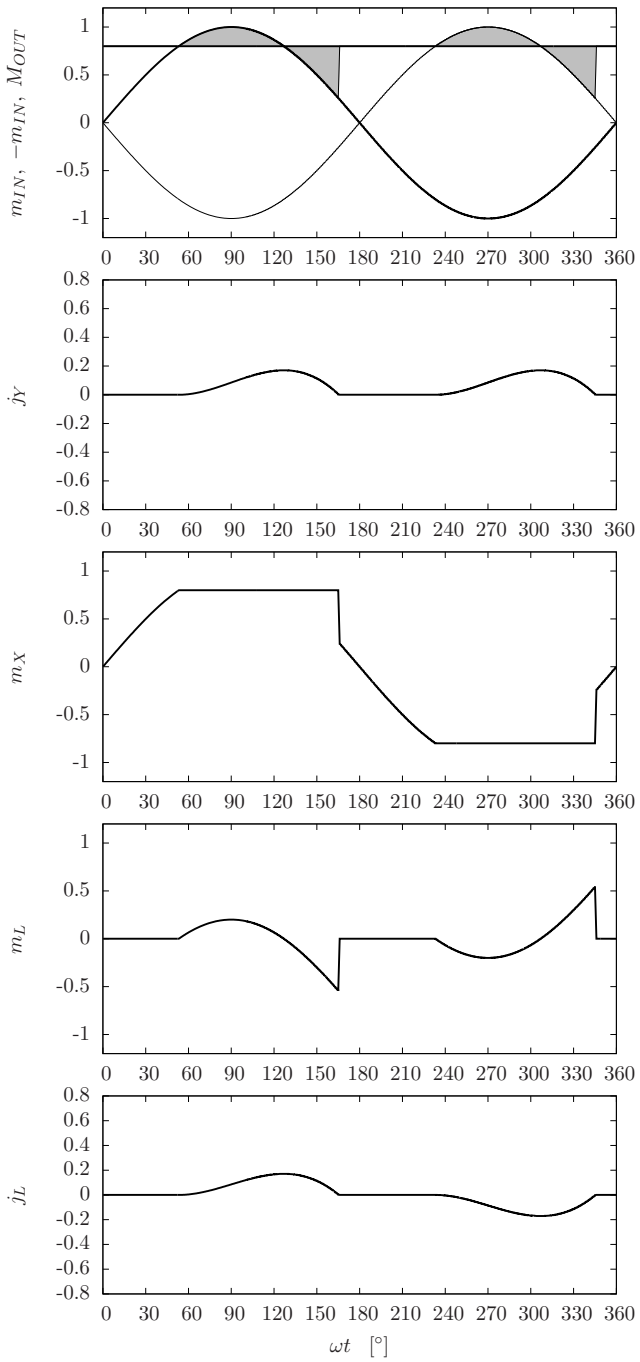

Fig. 3. Waveforms of the rectifier voltages and currents in the discontinuous conduction mode for $M_{OUT} = 0.8$.

as depicted in the first diagram of Fig. 3.

Operating mode when the inductor current stops and remains zero over a time interval is referred to as the discontinuous conduction mode. Thus, diagrams of Fig. 3 represent waveforms of the rectifier voltages and currents in the discontinuous conduction mode. Time intervals when j_L and j_Y are equal to zero could be observed. Conducting diodes are labeled on the waveform of m_X.

Equation (14) that determines phase angle β when the inductor current flow stops does not have a closed form solution. This is the limiting factor for obtaining an analytical solution for the discontinuous conduction mode. Thus, the solution should be obtained numerically.

Analysis of the rectifier performed this far covers only one half-period of the rectifier operation, for $\alpha < \varphi < \alpha + \pi$. Applying symmetry, both of the circuit and the input voltage, we may conclude that in steady state

$$j_L(\varphi) = -j_L(\varphi + \pi). \tag{17}$$

The same conclusion applies for all variables at the AC side of the rectifier, including m_L and m_X, as it can be observed from the last three diagrams of Fig. 3.

Phase angle interval when $j_L < 0$ is named the conduction angle, and it is determined by

$$\gamma = \beta - \alpha. \tag{18}$$

In the case the rectifier operates in the discontinuous conduction mode, $\gamma < \pi$. For $\gamma = \pi$, the converter switches to the continuous conduction mode, which would result in entirely different behavior of the rectifier.

III. Analysis of the Rectifier in the Continuous Conduction Mode

In the case

$$-m_{IN}(\beta) > M_{OUT} \tag{19}$$

the inductor current continues to decrease after it reached zero, taking negative values. This situation corresponds to the rectifier operating in the continuous conduction mode. Applying symmetry arguments, we may conclude that $\gamma = \pi$ in this case. Extending the definition of α to the phase angle when the inductor current starts to grow from zero, we have

$$j_L(\alpha + \pi) = j_L(\alpha) = 0 \tag{20}$$

and even more important, equation (13) for the inductor current applies over the whole half -period $\alpha < \varphi < \alpha + \pi$. Applying (13) in (20), in the continuous conduction mode we have

$$\cos(\alpha) + M_{OUT}\,\alpha - \cos(\alpha + \pi) - M_{OUT}\,(\alpha + \pi) = 0 \tag{21}$$

which reduces to

$$\cos(\alpha) = \frac{\pi}{2} M_{OUT}. \tag{22}$$

This is one of the differences between the conduction modes, in the discontinuous conduction mode the inductor current starts to grow from zero at the phase angle determined by (6), while in the continuous conduction mode this angle is determined by (22). At the boundary between the modes both of the equations for α apply, resulting in the conduction starting angle α at the boundary between the modes

$$\tan(\alpha_{MC}) = \frac{2}{\pi} \tag{23}$$

and the corresponding normalized output voltage

$$M_{OUT\,MC} = \frac{2}{\sqrt{4 + \pi^2}} \approx 0.5370. \tag{24}$$

After the conduction starting angle is determined by (22), the inductor current is from (13) obtained as

$$j_L(\varphi) = M_{OUT}\left(\frac{\pi}{2} + \arccos\left(\frac{\pi}{2} M_{OUT}\right)\right) - \cos(\varphi) - M_{OUT}\,\varphi \tag{25}$$

during the half-period $\alpha < \varphi < \alpha + \pi$. During the other half-period, the input current waveform could be computed applying (17).

Waveforms of the voltages and currents for the rectifier operating in the continuous conduction mode at $M_{OUT} = 0.5$ are presented in Fig. 4. The diagrams are plotted applying the same scale as applied in the diagrams of Fig. 3, to illustrate increased magnitudes of currents in the continuous conduction mode. In the first diagram of Fig. 4, it should be noticed that condition (19) applies. Volt-second balance over the half-period is highlighted in the same diagram.

The rectifier output current is obtained as the average of the diode bridge output current j_Y, which in terms of j_L reduces to

$$J_{OUT} = \frac{1}{\pi}\int_{\alpha}^{\alpha+\pi} j_L(\varphi)\, d\varphi = \frac{2}{\pi}\sin(\alpha). \tag{26}$$

Such integral is harder to compute for the discontinuous conduction mode, due to the difficulties in obtaining the upper limit of integration, β.

Substituting the value of α obtained from (22), dependence of the output current on the output voltage in the continuous conduction mode is obtained as

$$J_{OUT} = \frac{1}{\pi}\sqrt{4 - \pi^2 M_{OUT}^2} \tag{27}$$

meaning that the rectifier output characteristic in the normalized output plane (J_{OUT}, M_{OUT}) is a circle with the radius equal to $2/\pi$, $M_{OUT}^2 + J_{OUT}^2 = (2/\pi)^2$. Applying the rectifier output characteristic (27), the rectifier short circuit current is obtained as

$$J_{OUT\,SC} = \frac{2}{\pi} \approx 0.6366 \tag{28}$$

while the output current when the rectifier changes its operating mode is

$$J_{OUT\,SC} = \frac{4}{\pi\sqrt{4 + \pi^2}} \approx 0.3419. \tag{29}$$

The RMS value of the rectifier input current is analytically obtained as

$$J_{IN\,RMS} = \frac{\sqrt{3}}{6}\sqrt{6 + (\pi^2 - 24)\, M_{OUT}^2} \tag{30}$$

which is an important parameter to design the input transformer.

Normalized value of the rectifier output power is

$$P_{OUT} = M_{OUT}\, J_{OUT} = \frac{M_{OUT}}{\pi}\sqrt{4 - \pi^2 M_{OUT}^2} \tag{31}$$

and this curve exposes maximum at

$$M_{OUT\,PMAX} = \frac{\sqrt{2}}{\pi} \tag{32}$$

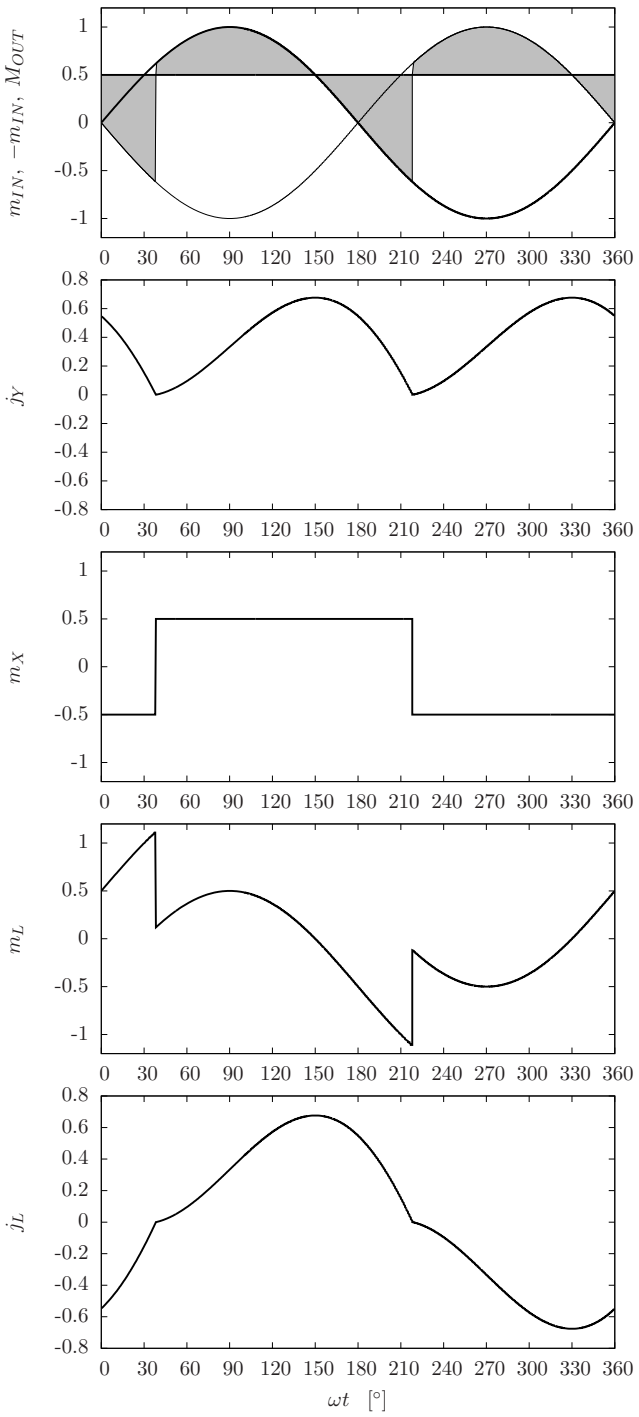

Fig. 4. Waveforms of the rectifier voltages and currents in the continuous conduction mode for $M_{OUT} = 0.5$.

which is within the continuous conduction operating range. The maximum of the DC power that the rectifier could supply to the load is

$$P_{OUT\,MAX} = \frac{2}{\pi^2}\,\text{p.u.} \approx 0.2026\,\text{p.u.} \tag{33}$$

Since the commutation angles α and β are available in closed form for the continuous conduction mode, many analytical results for the parameters that characterize the rectifier operation are available in closed form. To obtain values of

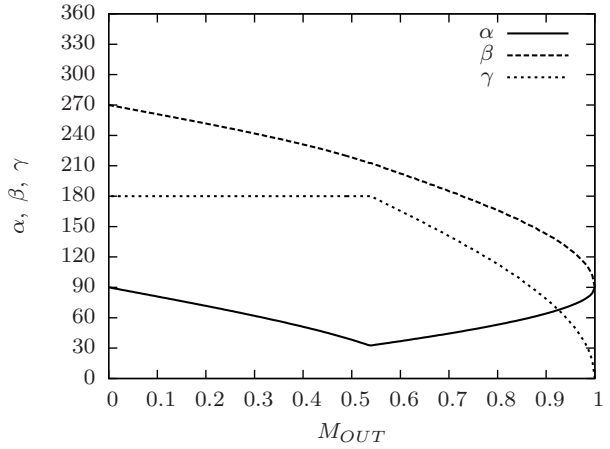

Fig. 5. Dependence of α, β, and γ on M_{OUT}.

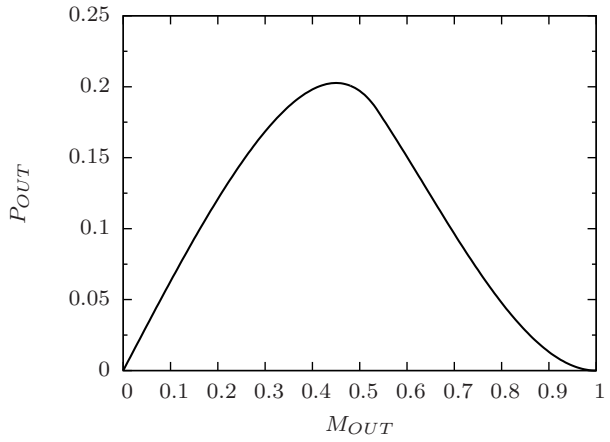

Fig. 7. Dependence of the rectifier output power on the output voltage.

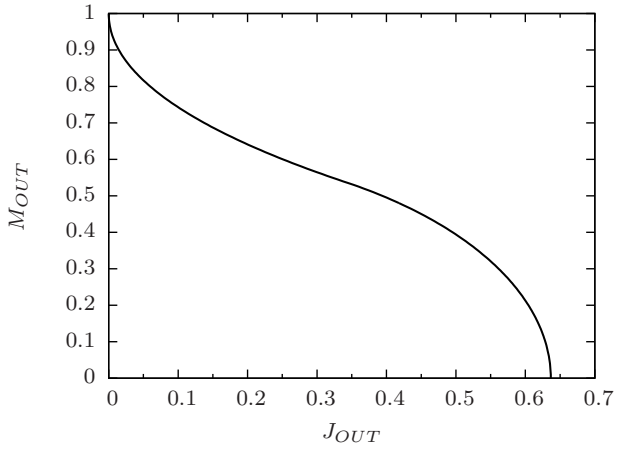

Fig. 6. Dependence of the rectifier output voltage on the output current.

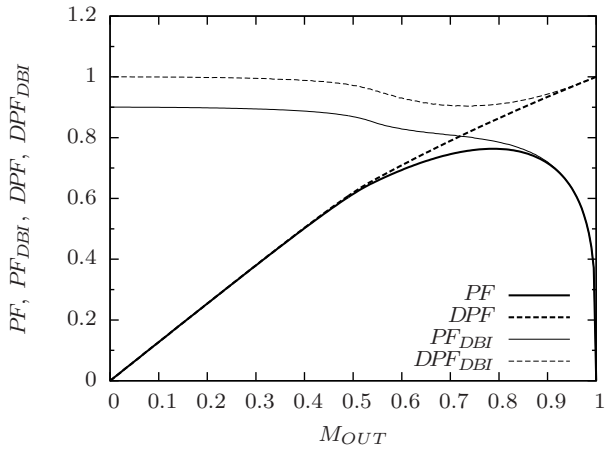

Fig. 8. Dependence of power factors and displacement power factors on the output voltage.

these parameters for the rectifier operating in the discontinuous conduction mode, numerical methods should be applied.

IV. Numerical Simulation of the Rectifier Operation

After the analysis of the rectifier is performed, numerical implementation of the model is a straightforward procedure. A GNU Octave program that "plays a cartoon" illustrating the rectifier operation for the whole range of the output voltage values is given in the Appendix. Source code is available at http://tnt.etf.bg.ac.rs/~oe3ee/singlephase.m, while Python version of the same program (PyLab) is available at http://tnt.etf.bg.ac.rs/~oe3ee/singlephase.py. Some of the diagrams that the program provides as a result are presented here.

In Fig. 5, dependence of the phase angle when the inductor current becomes positive, α, the phase angle when the inductor current falls to zero, β, and the conduction angle γ on M_{OUT} are presented. Transition between the modes could clearly be observed in the diagrams $\alpha\,(M_{OUT})$ and $\gamma\,(M_{OUT})$.

Dependence of the rectifier output voltage on the output current is presented in Fig. 6. The diagram of Fig. 6 is obtained by numerical computation, but in the continuous conduction mode matches the analytical result (27). Dependence of the output power on the output voltage is presented in Fig. 7. The curve is obtained applying numerical computation, but in the continuous conduction mode matches the analytical result (31) and reaches maximum according to (32) and (33).

Other parameters, like the total harmonic distortions of the input current and the voltage at the rectifier input, as well as the RMS value of the input current, may be computed. As an illustration, values of the power factor and the displacement power factor at the ideal voltage source, PF and DPF, as well as at the diode bridge input terminals, PF_{DBI} and PF_{DBI} are presented in Fig. 8. This diagram may be applied as an illustration while introducing definitions of power factor and the displacement power factor, since differences between these two parameters are clearly observable on an example encountered in practice.

V. Conclusions

In this paper, a single-phase full-bridge rectifier supplied by a source with finite leakage inductance is proposed as an effective example to teach circuit modeling, normalization, operating modes, and various techniques of circuit analysis. Discontinuous conduction mode is analyzed, and it is shown why an analytical closed form solution cannot be obtained. On the other hand, an analytical solution is derived for the continuous conduction mode. During the circuit analysis, appropriate normalization is introduced to generalize the results. A numerical method to compute the rectifier waveforms in both of the operating modes is presented, and a GNU Octave program that illustrates the circuit behavior and may be used for educational purposes is provided. Diagrams of various parameters that characterize the rectifier operation, provided by numerical computation, are presented. The circuit analyzed in the paper is simple and reach in phenomena of educational interest that it might be used as a laboratory example, as well.

VI. Appendix

```
np = 180 * 2; # could be adjusted if the simulation is too slow
step = 0.005; # could be adjusted if there are too many points

np2 = 2 * np;

i = 1 : np2;
wt = 2 * pi / np2 * (i - 0.5);
deg = wt * 180 / pi;

minp = sin(wt);
co = cos(wt);

Mboundary = 2 / sqrt(4 + pi^2);

counter = 0;
for Mout = 1 - step : -step : step
    counter = counter + 1;
    mout(counter) = Mout;
    if Mout > Mboundary
        dcm(counter) = 1;
        colour = 'b';
        alpha = asin(Mout);
        a(counter) = alpha * 180 / pi;
        nalpha = find(wt > alpha, 1) - 1;
        jl0 = cos(alpha) + Mout * alpha;
        for i = 1 : np
            j(i) = jl0 - co(nalpha + i) - Mout * wt(nalpha + i);
        end
        nbeta = find(j < 0, 1);
        b(counter) = nbeta / np * 180 + a(counter);
        j(nbeta : np) = zeros(1, np - nbeta + 1);
    else
        dcm(counter) = 0;
        colour = 'r';
        alpha = acos(pi / 2 * Mout);
        a(counter) = alpha * 180 / pi;
        b(counter) = a(counter) + 180;
        nalpha = find(wt > alpha, 1) - 1;
        jl0 = cos(alpha) + Mout * alpha;
        for i = 1 : np
            j(i) = jl0 - co(nalpha + i) - Mout * wt(nalpha + i);
        end
    end
    jl(1 : np) = j;
    jl(np + 1 : np2) = -j;
    jl = circshift(jl', nalpha)';
    mx = minp .* (jl == 0) + Mout * ((jl > 0) - (jl < 0));
    ml = minp - mx;
    jy = abs(jl);
    jout(counter) = mean(jy);
    pout(counter) = Mout * jout(counter);



    figure(1)

    subplot(2, 2, 1)
    plot(deg, jl, colour)
    axis([0 360 -1.1 1.1])
    set(gca, 'xtick', 0 : 360 : 30)
    xlabel('wt [deg]')
    ylabel('jl')

    subplot(2, 2, 3)
    plot(deg, ml, colour)
    axis([0 360 -1.5 1.5])
    set(gca, 'xtick', 0:360:30)
    xlabel('wt [deg]')
    ylabel('ml')

    subplot(2, 2, 4)
    plot(deg, mx, colour)
    xlabel('wt [deg]')
    ylabel('mx')
    axis([0 360 -1.5 1.5])
    set(gca, 'xtick', 0 : 360 : 30)

    subplot(2, 2, 2)
    plot(deg, jy, colour)
    xlabel('wt [deg]')
    ylabel('jy')
    axis([0 360 -1.1 1.1])
    set(gca, 'xtick', 0 : 360 : 30)

    pause(0.5)

    xin = measure(jl, minp);
    pin(counter) = xin(1);
    pf(counter) = xin(3);
    dpf(counter) = xin(4);
    thdi(counter) = xin(5);
    jrms(counter) = xin(8);
    xpcc = measure(jl, mx);
    pinpcc(counter) = xpcc(1);
    pfpcc(counter) = xpcc(3);
    dpfpcc(counter) = xpcc(4);
    thdv(counter) = xpcc(6);
end

figure(2)
plot(mout, jout)
xlabel('Mout')
ylabel('Jout')

figure(3)
plot(jout, mout)
xlabel('Jout')
ylabel('Mout')

figure(4)
plot(mout, pin, 'r', mout, pinpcc, 'g', mout, pout, 'b')
xlabel('Mout')
ylabel('Pin, Pinpcc, Pout')

figure(5)
plot(mout, pf, 'b', mout, pfpcc, 'r')
xlabel('Mout')
ylabel('PF [blue], PFpcc [red]')

figure(6)
plot(mout, dpf, 'b', mout, dpfpcc, 'r')
xlabel('Mout')
ylabel('DPF [blue], DPFpcc [red]')

figure(7)
plot(mout, thdi)
xlabel('Mout')
ylabel('THDi')

figure(8)
plot(mout, thdv)
xlabel('Mout')
ylabel('THDv')

figure(9)
plot(mout, a, 'b', mout, b, 'g', mout, b - a, 'r')
xlabel('Mout')
ylabel('alpha [blue], beta [green], gama [red]')



function x = measure(i, v)

    n = size(i, 2);

    I = fft(i);
    V = fft(v);

    irms = sqrt(mean(i .* i));
    vrms = sqrt(mean(v .* v));

    ilrms = sqrt(2) * abs(I(2)) / n;
    vlrms = sqrt(2) * abs(V(2)) / n;

    p = mean(i .* v);

    s = irms * vrms;

    pf = p / s;

    dpf = cos(angle(I(2)) - angle(V(2)));

    thdi = sqrt(irms^2 - ilrms^2) / ilrms * 100;
    thdv = sqrt(vrms^2 - vlrms^2) / vlrms * 100;

    x = [p s pf dpf thdi thdv irms ilrms vrms vlrms];
```

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Model-driven Techniques for Data Model Synthesis

Drazen Brdjanin and Slavko Maric

***Abstract*—This article presents a survey of model-driven techniques for data model synthesis. During an extensive research, we identified more than 70 research papers in the field and more than 15 different graphical notations used for the source model representation. We have classified the proposed approaches into four distinct groups: function-oriented, process-oriented, communication-oriented and goal-oriented. Their contributions are presented in chronological order and evaluated based on several main criteria. Although the idea of model-driven design of the data model is more than 25 years old, the survey shows the richness and diversity of ideas, but only a small number of implemented automatic generators.**

***Index Terms*—Communication-oriented, data model, function-oriented, goal-oriented, model-driven, process-oriented, survey.**

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I. Introduction

THE data model constitutes one of the most important artifacts in the information system design process, as well as the crucial component of software system models. Consequently, the automatization of data model design has been the subject of research for many years.

Since Chen's eleven heuristic rules [1] for the translation of information requirements specified in a natural language into an E-R diagram, a lot of research has been done in the field of natural language processing (NLP) on extracting knowledge from requirements specifications and automating data model design. At present, a natural language is the most frequently used way for requirements specifications and the majority of approaches to automated data model design are NLP-based approaches. Their effectiveness and limitations are usually deeply related to the source language, and their utilization is questionable for languages with complex morphology. Currently, there are several non-NLP-based alternatives to automated data model design, such as approaches taking models (graphically specified business/software requirements) as the basis for automated data model design instead of requirements specifications expressed in a natural language.

The first papers that focused on the model-driven design of the data model appeared in the second half of the 1980s. The first papers reporting the model-driven tools for (semi)automatic data model synthesis were published in the mid-1990s. However, although the idea of model-driven design of the data model is more than 25 years old, the fully automatic model-driven synthesis of the data model is still the subject of intensive research. In the existing literature there are only a small number of papers presenting the implementation of the automatic model-driven generator of the target data model with the corresponding evaluation results, while the great majority of papers only present modest achievements in (semi)automated, or even manual, data model synthesis.

In the related literature there are no papers presenting the systematic literature review (SLR) in the field of model-driven synthesis of the data model. Several existing papers [2]–[5] give only a partial overview of the field by focusing on some particular source notation or by presenting a wider overview of techniques for synthesizing different (not only data) models and taking different source (not only graphical) specifications as the base. Jilani et al. in [3] present a comparative study of seven approaches to the synthesis of UML diagrams based on data flow diagrams (DFD), but this study is not focused on data model synthesis and does not cover all existing approaches taking the DFD as a starting point. Franch et al. in [2] present the classification of the combined usage of the i^* notation with other notations and modeling frameworks. However, only two of all identified papers address the synthesis of data models based on i^*. Loniewski et al. in [4] present the SLR of the use of requirements engineering techniques in model-driven software development. However, they are not exclusively focused on the model-driven synthesis of the data model, and only a few papers, out of approximately 70 identified, belong to the target group of model-driven approaches to data model synthesis. Yue et al. in [5] present the SLR of transformation approaches between user requirements and analysis models, but this review is focused on the textual specification of user requirements as a starting point.

Inspired by the lack of an appropriate review of the existing model-driven techniques for data model synthesis, we have conducted an extensive survey of the related literature and identified more than 70 papers addressing the model-driven synthesis of the data model. In this paper we present the results of this survey and provide a classification of the identified techniques based on the primary focus, i.e. the orientation of a source notation. The contribution of the related papers within each classification group is presented in chronological order and evaluated based on several main criteria.

The article is structured as follows: after the introduction, the second section presents the taxonomy of source notations and the corresponding classification of the existing papers; the subsequent sections briefly present all categories and their main representatives; the seventh section presents the comparative study of the existing approaches; the final section concludes the paper.

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II. Classification of existing approaches

We conducted an extensive survey of the related literature and identified more than 70 primary sources (articles, conference papers, PhD theses) addressing the model-driven synthesis of the data model (MDSDM). Based on the primary focus of a source notation, all identified papers can be classified into four main groups: (i) *function-oriented*, (ii) *process-oriented*[1], (iii) *communication-oriented*[2], and (iv) *goal-oriented*. The corresponding paper distribution is given in Table I, while the taxonomy of source notations is presented in Fig. 1.

TABLE I
Distribution of papers according to source notation classification

Source notation	Function-oriented (FOM)	Process-oriented (POM)	Communication-oriented (COM)	Goal-oriented (GOM)
Number of papers	22	36	10	11

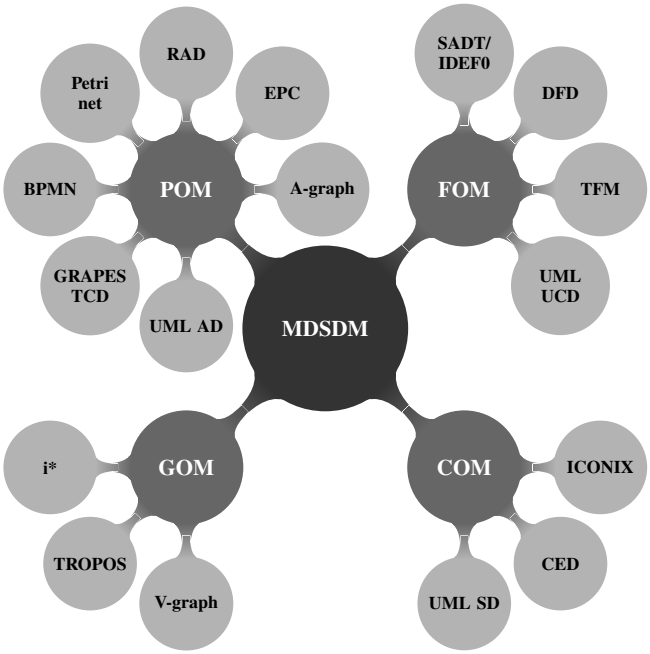

Fig. 1. Taxonomy of source notations in MDSDM.

The chronological overview of the identified MDSDM approaches is given in Fig. 2. The approaches are grouped by a source notation and then aggregated in accordance with the introduced classification. Different marks are used to differentiate the source model completeness and the level of automatization for the identified papers. The arrows are used to emphasize the related papers presenting the improvements in the same approach.

[1]The main criterion for the differentiation between the process-oriented and function-oriented notations is the capacity for the explicit representation of a workflow.

[2]Although some communication-oriented notations might be considered as process-oriented, the main reason for making a separate category lies in the fact that the given notations are focused on the interaction between the process participants.

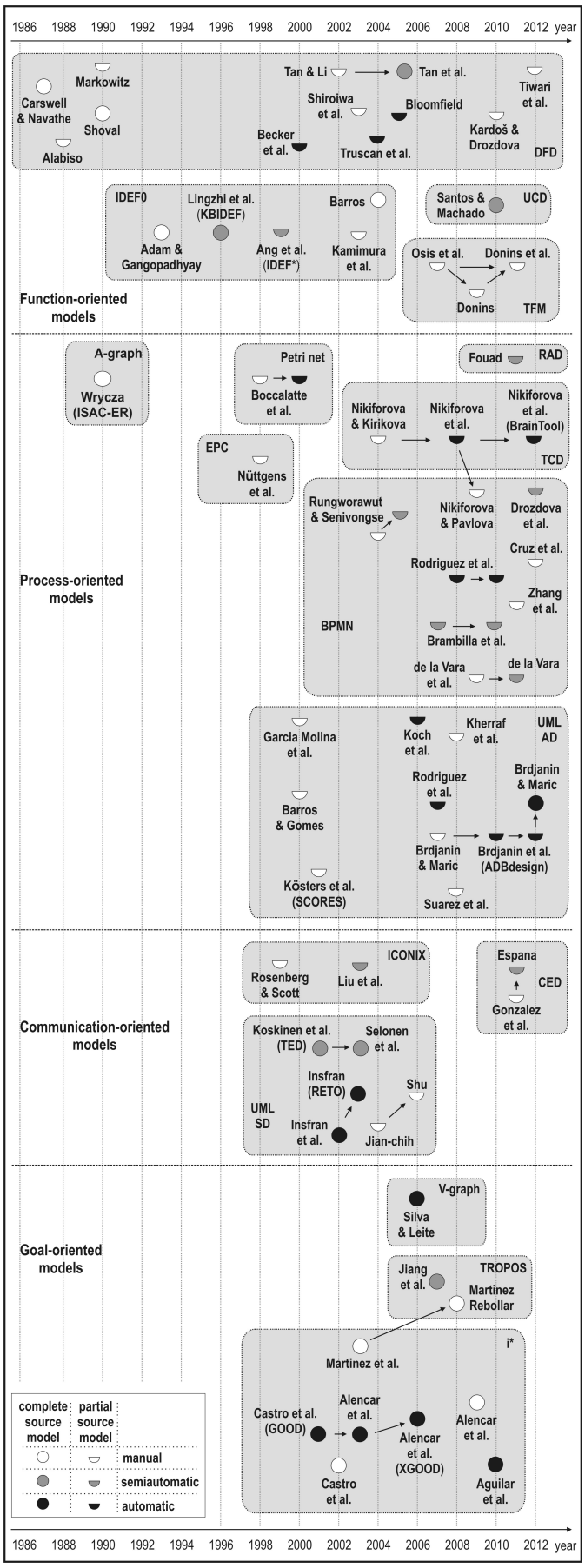

Fig. 2. Chronological overview of MDSDM approaches.

III. Function-oriented models as starting point

The first ideas about the MDSDM based on function-oriented models (FOMs) appeared in the second half of the 1980s, but the initial implementations of (semi)automatic generators did not occur before the mid-1990s.

The chronological overview of the identified approaches is presented in Fig. 2 (together with other categories).

Our survey shows that FOMs, used as a basis for the MDSDM, have been represented by four different notations (Fig. 1): DFD, SADT/IDEF0, TFM (Topological Functioning Model) and UML UCD (Use Case Diagram).

Since the Carswell & Navathe's SA-ER proposal [6] in 1987, the DFD [7] (including its modifications) has been a function-oriented notation commonly used ($>50\%$) as a starting point for the MDSDM. Among the 13 identified papers [6], [8]–[19], there is no paper that presents an automatic generator taking a complete model of functional system requirements represented by the DFD-hierarchy. Just one paper [13] presents a semiautomatic generator taking a complete source model represented by the DF Net hierarchy, while four papers [12], [15]–[17] present the automated generation of the data model based on an incomplete source model, i.e. a single DFD.

The SADT/IDEF0 is used in five papers [20]–[24]. Only two papers [21], [22] report the (semi)automated generation of the target data model. The TFM [25] is used in several papers [26]–[28], but all of them present only manual data model derivation from the TFM. The UML UCD is used in [29] for semiautomated data model synthesis.

The survey of the MDSDM approaches, taking FOMs as a starting point, implies:

- the majority of approaches ($>65\%$) take an incomplete model of functional requirements, i.e. a single diagram, as a basis for data model synthesis;
- the target data model is mainly represented by the UML class diagram ($>60\%$), but some other notations are also used (e.g. IDEF1/IDEF1X in [20]–[22], E-R in [6], [9], [23], NIAM in [10] and OODM in [11]);
- since the great majority of approaches ($\sim 90\%$) are based on guidelines and informal rules, the automatization level is very low ($\sim 60\%$ is manual, while less than 20% is automatic);
- the percentage of the evaluated approach is very low – only one [13] approach ($<5\%$) was evaluated based on a controlled experiment, while all others were not evaluated at all, or were just shown by some illustrative examples without any quantitative and/or qualitative evaluation;
- the semantic capacity of FOMs has not been sufficiently identified to enable the automatic synthesis of the target data model, since the existing approaches, which automatically generate the data model, do not generate an adequate data model structure regarding the proper number of classes, their associations and association end multiplicities.

IV. Process-oriented models as starting point

Process-oriented models (POMs) constitute the largest category of models being used as a starting point for the MDSDM. Although the first data model synthesis based on the POM (A-graph) was proposed by Wrycza [30] in 1990, the boom of these approaches was influenced by the appearance and development of metamodel-based notations, particularly the UML AD (UML activity diagram) in the late 1990s/early 2000s, and the BPMN (Business Process Model and Notation) a few years later, as well as the ATL [31] and QVT [32] transformation languages.

The survey shows that POMs, used as a basis for data model synthesis, have been represented by seven different notations (Fig. 1): UML AD, BPMN, GRAPES-BM/TCD, Petri Net, RAD (Role Activity Diagram), EPC (Event-driven Process Chain) and A-graph. The chronology of the identified approaches is presented as a part of Fig. 2.

The UML AD is used in 14 papers [33]–[46]. Only one paper [46] presents an automatic data model generator (named ADBDESIGN) based on the complete source model, i.e. a source model containing a finite set of UML ADs representing all business processes in a domain; several papers [36]–[38], [42]–[45] present the automated, mainly ATL- and QVT-based, data model generation based on the incomplete source model, but with a modest *precision* (measure showing the percentage of correct automatically generated concepts) and *recall* (automatically generated percentage of the target model), while the others present manual data model derivation.

Although the BPMN is used in 12 papers [47]–[58], there is no paper presenting an automatic generator of the data model based on the complete source model. There are two QVT-based proposals [50], [53], but with modest achievements in the automated generation of the analysis level class diagram, as well as several proposals [48], [49], [52], [56], [58] for the semiautomated generation.

There are also several related papers [59]–[63] proposing the usage of the TCD notation (a part of the GRAPES-BM language) as a starting point for data model synthesis, initially through the intermediate model, while the final release [63] presents the BRAINTOOL generator, which generates the data model directly from the TCD. However, like the majority of all proposals, they do not consider the complete source model, and the proposed approach is also not evaluated.

Among the remaining papers proposing data model synthesis based on Petri nets in [64], [65], EPC in [66], A-graph in [30], and RAD in [67], only two sources [65], [67] present software tools for the (semi)automated generation of the data model based on the incomplete source model.

The survey of the MDSDM approaches based on POMs implies:

- only two ($\sim 5\%$) papers [30], [46] take the complete source model, while others just consider a single diagram as a basis for data model synthesis;
- the target data model is predominantly represented by the UML class diagram ($>90\%$), while the E-R is used only in [30], [64], [65];

- the majority of proposed approaches are based on guidelines ($\sim 30\%$) and informal rules ($\sim 40\%$), but the development of transformation languages (ATL and QVT) has made an important contribution to the formalization and automatization of the MDSDM approaches in the recent years, so the participation of (semi)automatic techniques is significant ($\sim 60\%$);
- a small percentage ($\sim 10\%$) of approaches were evaluated based on a controlled experiment [56], [67] or a single case study [45], [46], while all others were not evaluated at all, or just illustrated by some examples without any quantitative/qualitative evaluation;
- only one paper [46] presents an automatic data model generator based on the complete source model, but the generated data model can be considered just as an initial data model, i.e. an analysis level data model;
- the semantic capacity of POMs has not yet been sufficiently identified to enable the automatic synthesis of the complete target data model, since the existing approaches still do not have a significant recall in the automated generation of some types of associations and class members.

V. Communication-oriented models as starting point

Communication-oriented models (COMs) constitute a smaller category of models used for data model synthesis. The survey shows that COMs, used as a starting point for data model synthesis, have been represented by three different notations (Fig. 1): UML SD (Sequence Diagram), ICONIX (Robustness Diagram) and CED (Communicative Event Diagram). The chronology of the identified approaches is presented in Fig. 2.

The UML SD [68] was identified in six (60% of this category) sources [69]–[74] as a source notation for data model synthesis. According to [72], transformations from sequence to class diagrams can be classified as *strong*, which implies that the source model possesses a semantic capacity only for the semiautomatic synthesis of the target data model, as in [69], [72]. The semantic capacity of the UML SD can be augmented by the specialization of the standard notation, and the process of data model synthesis can be automatic, as in the RETO tool [70], [71]. The process of data model synthesis in other two studies [73], [74] is manual. Among the remaining proposals for data model synthesis based on the CED [75] in [76], [77] and the ICONIX [78] in [78], [79], the semiautomatic synthesis of the data model is proposed in [77], [79], while others propose the guidelines for manual data model synthesis.

The survey of the MDSDM approaches based on COMs implies:

- the majority (60%) of papers take the incomplete source model as a basis for data model synthesis;
- the target data model is exclusively represented by the UML class diagram;
- although the majority (70%) of papers are based on guidelines and informal rules, the majority (60%) of papers still present (semi)automated techniques for data model synthesis;
- only one (10%) proposal [77] was evaluated based on a controlled experiment, while all others were not evaluated;
- only one primary study [71] presents an automatic data model generator based on the complete source model, but with a modest recall of some association types and without proper evaluation.

VI. Goal-oriented models as starting point

Goal-oriented models (GOMs), as the main artifacts produced in the early phases of goal-oriented requirements engineering processes, constitute the fourth category of models used for data model synthesis. The survey shows that GOMs, used as a starting point for data model synthesis, have been represented, as depicted in Fig. 1, by the i^* notation [80] and some i^*-originated notations like TROPOS [81], [82] and V-graph [83]. The chronology of the identified approaches is presented in Fig. 2.

i^* models were identified in eight ($> 70\%$ of the entire category) papers [81], [84]–[90] as a basis for data model synthesis. Most of the identified papers present the automatic synthesis of the data model to some extent, while only two papers [81], [84] present manual data model derivation. Most of the papers reporting automated data model synthesis are mutually related and present improvements in the same approach and the same tool named GOOD/XGOOD [85]–[88]. Other proposals based on TROPOS models in [91], [92] and V-graph in [93] are also mainly automated to some extent, but not evaluated.

The survey of the MDSDM approaches based on GOMs implies:

- since i^* and i^*-originated notations enable the representation of functional and non-functional requirements by a unique diagram (but with difficult "readability"), all identified papers take the complete source model as a basis for data model synthesis;
- the target data model is exclusively represented by the UML class diagram;
- the large majority ($> 90\%$) of papers are based on guidelines and informal rules;
- the majority ($> 60\%$) of papers present (semi)automated techniques for data model synthesis, but the recall might be estimated as insufficient; and
- there is no evaluated approach at all.

VII. Comparative analysis

All papers were analyzed according to the following criteria (results are presented in Fig. 3):

- ***Source notation*** – a notation used for the source model representation;
- ***Source model completeness*** – a source model might be considered as **complete** or **partial** (complete/partial representation of requirements);

- ***Target notation*** – a notation used for the data model representation;
- ***Level of automatization*** – data model synthesis might be considered as **manual** (not supported by any software tool), **semiautomatic** (supported by a tool, but the designer's assistance is still required) or **automatic** (without designer's assistance);
- ***Level of formalism*** – data model synthesis might be driven by **guidelines** (synthesis is generally described without rules for data model synthesis), **informal rules** (rules specified in a natural language) or by **formal rules** (rules formally represented by a transformation language, formal algorithm, predicate logic, etc.);
- ***Approach evaluation*** – an approach might be considered as **evaluated** (based on a **controlled experiment** or a **case study**) or **not evaluated**.

The analysis implies that POMs and FOMs are predominantly ($> 70\%$) used as a basis for the MDSDM. Three notations (UML AD, DFD, BPMN), belonging to these two categories, are used in half of all identified sources. The DFD, as a traditional function-oriented notation, still constitutes the subject of research in the field of MDSDM, but it loses the precedence to the newer, metamodel-based notations UML AD and BPMN, as well as the goal-oriented notations.

Most of the papers ($\sim 70\%$) do not take the complete source model, but only incomplete, i.e. the partial model of business or system requirements, as a basis for data model synthesis. The incompleteness of the source model is a typical characteristic of all categories, except for approaches having GOMs as a basis for data model synthesis, since all of them are based on the i^* notation, which captures "all" requirements by a single diagram.

The UML class diagram is used for the representation of the target data model in a large majority ($>85\%$) of all identified papers. Other notations were mainly used in some approaches before the adoption of the UML standard.

Data model synthesis is mainly ($\sim 80\%$) informally specified, equally by guidelines and informal rules, while just one-fifth of all papers specify data model synthesis in some formal way. Consequently, the level of automatization is rather low – a half of all papers present only manual data model derivation, while the other half present (semi)automated data model generation to some extent. The development of transformation languages (ATL and QVT) has made a significant contribution to the formalization and automatization of data model synthesis in the recent years, so the participation of automatic techniques ($\sim 35\%$) is growing.

A deeper analysis implies that the semantic capacity of graphically represented business/software requirements (regardless of their orientation) has not yet been sufficiently identified to enable the automatic synthesis of the complete data model, since a large majority of the existing approaches still do not have a significant recall in the automated generation of class associations, association end multiplicities and class members.

Apart from the low level of formalism and automatization, the insufficiently identified semantic capacity of models representing business/software requirements constitutes also the main cause for the almost complete absence of evaluation of the proposed approaches. More than 90% of the analyzed approaches are not evaluated at all, while the evaluation in the evaluated papers was mainly focused on the approach usability, but not on the qualitative/quantitative measures for the implemented tools and generated data models.

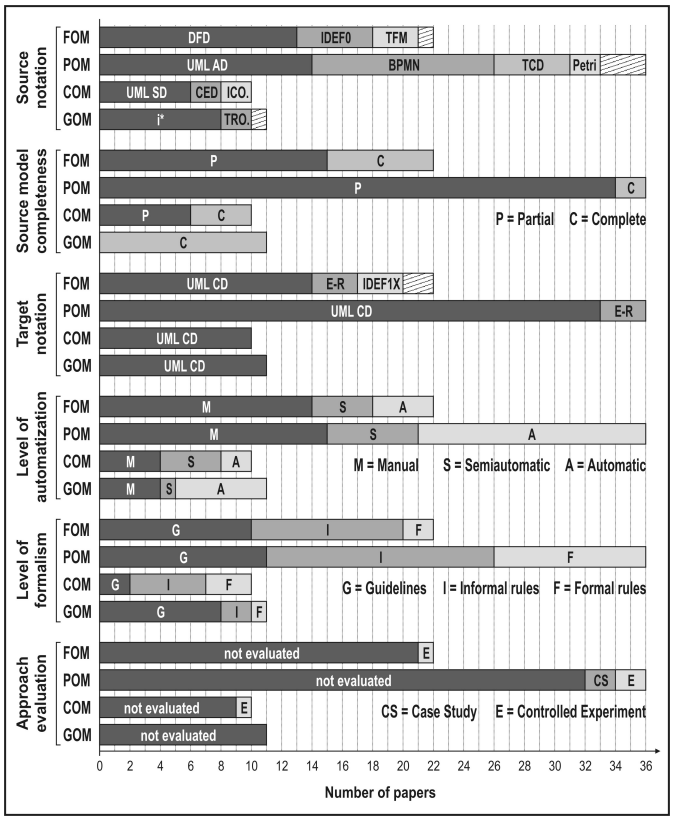

Fig. 3. Main characteristics of MDSDM approaches.

VIII. Conclusion

In this article we presented the results of the survey of model-driven techniques for data model synthesis. During the extensive research, we identified more than 70 research papers in the field and more than 15 different notations used for the source model representation.

Apart from the unique classification into four distinct groups: function-oriented, process-oriented, communication-oriented and goal-oriented, we gave the chronological overview of all identified papers classified according to the introduced classification, as well as the results of the evaluation based on several main criteria.

Although the idea of model-driven design of the data model is more than 25 years old, the survey shows that only a small number of papers present the implemented automatic model-driven generator of the data model and the corresponding evaluation results.

The main reason for the modest achievements in the automated model-driven design of the data model lies in the insufficiently identified semantic capacity of graphically represented business/software requirements for the automatic synthesis of the complete target data model.

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Control Strategy for Cascaded Medium – High Voltage STATCOM

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***Abstract*—Control strategy is researched for cascaded medium high static synchronous compensator to provide synthetic compensation ability of reactive power, harmonics and asymmetric currents. Basing on selective harmonic compensation strategy, a reference current detection method utilizing the combination of synchronous reference frame transformation and discrete Fourier transformation is proposed. The tracking control of instruction current is implemented by multi-carrier pulse width modulation (PWM). In allusion to the multi-carrier PWM, the capacitor voltage balancing control at the dc side is realized by a type of software based on the energy balance principle of the inverter bridge. The proposed control strategy is convenient for engineering implementation given its low calculation burden and simplicity. The effectiveness of the proposed control strategy is proven by both simulation and experimental results.**

***Index Terms*—control strategy, reference current detection, static synchronous compensator, tracking control of instruction current, voltage balance control at the dc side.**

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I. Introduction

STATIC synchronous compensator (STATCOM) is the most advanced equipment for reactive power and harmonic current compensation. Compared with other types of STATCOM, cascaded STATCOM, which is based on the series connection of the H-bridge cells, excels for its physical consistency, fewer components, better quality of output current and low difficulty in controller designing especially when the cascaded level becomes large [1]. Given its characteristics, cascaded STATCOM is suitable for high- or medium-voltage power systems.

When used in power systems that have harmonic distortion and asymmetry, the optimal goal of STATCOM is to compensate all reactive currents, harmonic currents, and unbalanced currents, so that the system will need only to provide the positive fundamental active current. To achieve this goal, an appropriate reference current detection method is needed.

The frequently used detection methods were divided into two types in [2]. The first type is the fundamental wave extraction methods (indirect extraction methods). An example of this type of method is the method based on synchronous reference frame transformation [3]. These methods extract the positive fundamental active current component (i_{lb}) from the load current (i_l); subsequently, the compensate currents (i_f) will be equal to ($i_l - i_{lb}$). These methods are usually used for full compensation. The second type of detection method is the harmonic direct extraction methods. These methods extract the reactive currents, harmonic currents and unbalanced currents directly from the load currents. Therefore, this type of method is usually used for selective harmonic elimination. The main function of STATCOM is reactive compensation. Thus, if we utilize fundamental wave extraction method for full compensation, then the installed capacity of STATCOM should be increased. Harmonic energy is mainly concentrated in low frequency band, and the bandwidth of STATCOM is limited because of limited control frequency. Therefore, the output compensating current probably cannot suppress the harmonic components of the load current in high frequency band. Accordingly, the harmonic direct extraction method will be a better choice. The discrete Fourier transformation (DFT) algorithm [4] is one example of the harmonic direct extraction method. However, the ordinary DFT algorithm is complex and needs large storage space. Another direct extraction method based on multiple synchronous rotating reference frames was presented in [5]. When we use this method, the harmonic component to be compensated should be calculated individually. Thus, more calculation work and more resources are needed with more selective harmonic currents to be compensated. This disadvantage can negatively influence the practical effect of the method.

Another problem of cascaded STATCOM is the imbalance of the dc capacitor voltages [6], [7]. The imbalance is caused by the following: different switching patterns for different

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H-bridges [8]; parameter variations of active and passive components inside H-bridges; and control resolution [9]. The voltage balance control at the dc side plays an important role in the output performance and reliability of STATCOM. The imbalance of dc capacitor voltages will degrade the quality of the voltage output; in severe cases, this imbalance could lead to the complete collapse of the power-conversion system [10]. This imbalance will also cause excessive voltages across devices and an imbalance of switching losses. Currently, the capacitor voltage control strategy used for cascade STATCOM mainly has two forms: additional hardware devices and software control algorithm. In normal cases, the software method is used to ensure capacitor voltage balance because hardware requires an increase in complex and expensive equipment. A software method using angular deviation control is proposed in [11]. However, the controllable angle range is very small, so the pulse generator must have high accuracy. By adding an active component, the balance of H-bridge capacitor voltages is realized in [12], but the controller is complex and the parameters are difficult to set.

Aiming at the above-mentioned problems, this paper focuses on the control strategy for cascaded STATCOM. The reference current detection method and voltage balance control strategy at the dc side are discussed as the main part. The validity of the proposed method is verified through simulation and experiment.

II. Reference Current Detection Method

The STATCOM equipment in this paper is mainly used for three three-phase three-wire systems. Thus, the zero sequence components of the three-phase load currents can be ignored, and the load currents can be described as follows:

$$\begin{cases} i_{\mathrm{la}} = \sum_{n=1}^{\infty}\left[i_{\mathrm{ln}+}\cos(n\omega t+\theta_{n+}) + i_{\mathrm{ln}-}\cos(n\omega t+\theta_{n-})\right] \\ i_{\mathrm{lb}} = \sum_{n=1}^{\infty}\left[i_{\mathrm{ln}+}\cos(n\omega t+\theta_{n+}-2\pi/3) + i_{\mathrm{ln}-}\cos(n\omega t+\theta_{n-}+2\pi/3)\right] \\ i_{\mathrm{lc}} = \sum_{n=1}^{\infty}\left[i_{\mathrm{ln}+}\cos(n\omega t+\theta_{n+}+2\pi/3) + i_{\mathrm{ln}-}\cos(n\omega t+\theta_{n-}-2\pi/3)\right] \end{cases}, \quad (1)$$

where $i_{\mathrm{ln+}}$ and $\theta_{\mathrm{n+}}$ respectively stand for the amplitude and initial phase angle of the positive sequence component; $i_{\mathrm{ln-}}$ and $\theta_{\mathrm{n-}}$ respectively stand for the amplitude and initial phase angle of the negative sequence component; ω stands for the fundamental angular frequency; n stands for the harmonic order. The three-phase load currents can be transformed into dq vector forms by using abc–dq transformation.

$$\begin{bmatrix} i_{\mathrm{ld}} & i_{\mathrm{lq}} \end{bmatrix}^{\mathrm{T}} = \mathrm{T}_{\mathrm{abc\text{-}dq}}\begin{bmatrix} i_{\mathrm{la}} & i_{\mathrm{lb}} & i_{\mathrm{lc}} \end{bmatrix}^{\mathrm{T}} \quad (2)$$

$$\mathrm{T}_{\mathrm{abc\text{-}dq}} = \frac{2}{3}\begin{bmatrix} \cos\omega t & \cos(\omega t-2\pi/3) & \cos(\omega t+2\pi/3) \\ -\sin\omega t & -\sin(\omega t-2\pi/3) & -\sin(\omega t+2\pi/3) \end{bmatrix} \quad (3)$$

Substituting (1) into (2), we obtain (4) as follows:

$$\begin{cases} i_{\mathrm{ld}} = \sum_{n=1}^{\infty}\{i_{\mathrm{ln}+}\cos[(n-1)\omega t+\theta_{n+}] + i_{\mathrm{ln}-}\cos[(n+1)\omega t+\theta_{n-}]\} \\ i_{\mathrm{lq}} = \sum_{n=1}^{\infty}\{i_{\mathrm{ln}+}\sin[(n-1)\omega t+\theta_{n+}] - i_{\mathrm{ln}-}\sin[(n+1)\omega t+\theta_{n-}]\} \end{cases}. \quad (4)$$

The obtained d axis component i_{ld} and q axis component i_{lq} stand for the active component and reactive component of the load currents, respectively.

According to (4), the n-th positive sequence components in the abc frame become $(n-1)$-th components in the dq frame, and the n-th negative sequence components will become $(n+1)$-th components. Thus, the $(6k\pm1)$-th characteristic harmonic components in the abc frame will become the $6k$-th component in the dq frame (k=1,2,…). Taking advantage of these characteristics, we may firstly obtain the $6k$-th component of i_{ld} and i_{lq} which is gained through abc–dq transformation, then use a resonance regulator which is tuned at the frequency $6k\omega$ to track the $6k$-th component. By using this method, each couple of harmonics at $(6k\pm1)\omega$ can be compensated with only one regulator, thus allowing the required number of regulators to be halved. This approach is better compared with methods using a regulator for each harmonic, such as the method based on multiple synchronous rotating reference frames.

When using this method, the reference current can be obtained through the detection algorithm utilizing the combination of synchronous reference frame transformation with DFT. Firstly, the three-phase load currents in the abc frame become i_{ld} and i_{lq} in the dq frame through abc–dq transformation, then we can use the DFT algorithm in the dq frame to obtain the $6k$-th harmonic components of i_{ld} and i_{lq}.

Calculating the harmonic components in the dq frame by using the ordinary DFT algorithm, which is based on full period sampling, is complex and requires much time because all the sample values in one power cycle are needed to calculate the Fourier coefficients. To reduce the computational effort and to improve real-time performance, the recursive discrete Fourier transform (RDFT) algorithm can be used.

Supposing a periodic signal $X(t)$ with angular frequency ω and period T exists, after discrete sampling with a sampling period τ, we obtain N sample points in one power cycle. The signal $X(t)$ can be described as follows with the DFT formula:

$$X_n(k\tau) = A_n\cos(n\omega k\tau) + B_n\sin(n\omega k\tau), k = 0,1,2,...,N-1 \quad (5)$$

$$A_n = \frac{2}{N}\sum_{m=0}^{N-1}[X(m\tau)\cos(n\omega m\tau)] \quad (6)$$

$$B_n = \frac{2}{N}\sum_{m=0}^{N-1}[X(m\tau)\sin(n\omega m\tau)]. \quad (7)$$

When we use the RDFT algorithm, only the latest sample values, the sample values before one power cycle and the calculated results of the last cycle are needed [13]. The Fourier coefficients of each harmonic component can be calculated according to the following formula:

$$A_n(i) = A_n(i-1) + \frac{2}{N}\{X(i\tau) - X[(i-N)\tau]\}\cos(n\omega i\tau) \quad (8)$$

$$B_n(i) = B_n(i-1) + \frac{2}{N}\{X(i\tau) - X[(i-N)\tau]\}\sin(n\omega i\tau). \quad (9)$$

By using the recursive algorithm, we obtain a significant reduction of the computational effort.

The RDFT algorithm is based on the sampling period, so the calculation result will be refreshed once each sampling cycle. By using high-performance digital signal processor and high speed AD sampling, the sampling frequency can be higher than 10 kHz. Thus, the refresh speed of the calculation result is very fast. When the system is in steady state, i.e., $X(i\tau)=X[(i-N)\tau]$, the calculation result will remain unchanged. When the load currents change, the calculation results can show an error. If the fundamental current changes, the correct calculation results will be obtained after a delay time of one power frequency cycle. If only the harmonic component changes, then the delay time will be shorter. Therefore, this method can work correctly even for the fast variable load.

Fig. 1 shows the schematic of the reference current detection algorithm based on synchronous reference frame transformation and DFT. In Fig. 1, i_{ldnr}, i_{ldni} and i_{lqnr}, i_{lqni} stand for the Fourier coefficient of the real part and imaginary part of i_{ld} and i_{lq}, respectively; i_{ld0} and i_{lq0} stand for the dc component of i_{ld} and i_{lq}; i_{ldn} and i_{lqn} (n=2,6,…,24) stand for the n-th component of i_{ld} and i_{lq}; u_{dc} stands for the average voltage value of all the capacitors at the dc side; U_{dc}^* stands for the reference value of the capacitor voltage; u_e stands for the error between U_{dc}^* and u_{dc}; i_{dcd} stands for the reference value of fundamental active current.

Only the characteristic harmonic components below the 25-th component are taken into account in Fig. 1. The three-phase load currents are processed with the proposed detection algorithm, and the reference currents (i_{Fd}^*, i_{Fq}^*) in the dq frame are finally obtained.

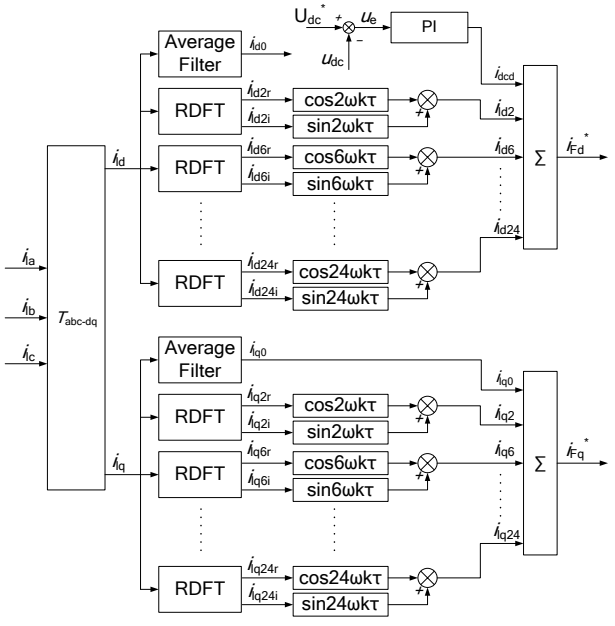

Fig. 1. Proposed reference current detection algorithm.

If the three-phase load currents are unbalanced, a fundamental negative sequence current will occur, which will become a 2-th harmonic component in the dq frame. Therefore, the 2-th component is also calculated in Fig. 1, except for the 6k-th harmonic components. When the load currents only have the characteristic harmonic components below 25-th, the system will need only to provide the positive fundamental active current if we consider the 2-th harmonic component.

By using this reference current detection method, the STATCOM will be able to provide more flexible compensation. Selective compensation can be easily realized by choosing the compensate components in Fig. 1 according to the actual need. The amplitude of reference currents can also be easily limited to avoid exceeding the power rating, and the amplitude of different compensate components can be limited to different values according to the importance degree.

The detection method presented in this paper is based on synchronous sampling. Thus, a voltage-phase synchronizer based on software phase-locked loop technology is necessary. By using this technology, the sample points in one power frequency cycle will remain constant.

III. Tracking Control Strategy of Instruction Currents

Fig. 2 shows a control system that uses the proposed detection method. The variables i_{Fa}, i_{Fb}, i_{Fc} stand for the three-phase output currents of the STATCOM; i_{Fd}, i_{Fq} are the output currents in the dq frame; i_{ed}, i_{eq} are the tracking errors in the dq frame; k_{in} (n=2,6,…,24) are the amplitude gain of the resonance controller; ω_c is the cut-off frequency of the resonance controller; $\omega_n=n\omega$, u_{Fdn}^*, u_{Fqn}^* are the n order reference voltage in the dq frame; u_{Fdsum}^*, u_{Fqsum}^* are the sum of the reference voltage in the dq frame; u_{sa}, u_{sb}, u_{sc} are the three-phase grid voltage; L stands for the connected air-core reactor inductance.

The control system contains a dc link voltage control loop (see Fig. 1), two fundament current control loops and two sets of selective harmonic control loops. The traditional proportion-integral (PI) controller is used in the dc link voltage control loop, which gives the fundamental active reference current. The two fundamental current control loops also use the PI controller. The selective harmonic control loops use resonance controller instead. Given the grid voltage disturbance and current coupling, the grid voltage feed-forward and output current decoupling control strategies are adopted in the control system.

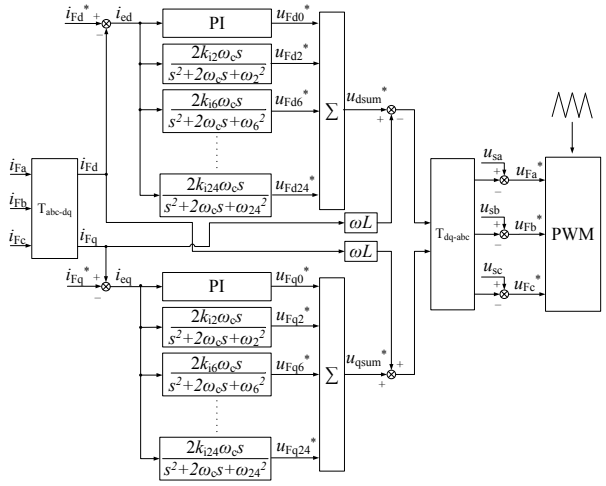

Fig. 2. Control strategy based on the proposed detection algorithm.

The obtained u_{Fa}^*,u_{Fb}^* and u_{Fc}^* in Fig. 2 are the voltage commands, i.e., the final modulation waves in the abc frame. The three-phase modulation waves are applied to a digital PWM block on the basis of the sine-triangle comparison modulation technique to generate the switching pulse for the STATCOM inverter. The multi-carrier PWM method, which is widely used in multi-level converters, can be used here for the cascaded STATCOM. Taking the single-phase three H-bridges as an example, the principle of the multi-carrier PWM method is shown in Fig. 3. The main modulation wave must be split into sections, then each section should be assigned to a different power unit.

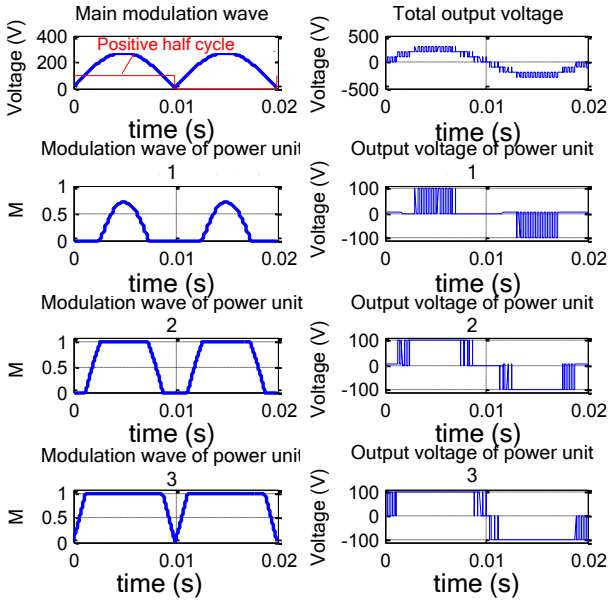

Fig. 3. Multi-carrier PWM.

IV. DC Voltage Balance Control Strategy

The dc link voltage control loop in Fig. 1 is used to control the total real power into the STATCOM to regulate the total dc voltage of all H-bridge units. However, this approach is not enough. Clustered balancing control (to balance the phase leg voltages) and individual balancing control (to balance the capacitors in each phase leg) are also needed. Clustered balancing control can be realized through zero sequence injection [14] or negative sequence injection [15]. Limited by space, this paper provides a discussion only on individual balancing control.

In allusion to the multi-carrier PWM used in this paper, a software individual balancing control strategy is proposed. The software strategy is based on the energy balance principle of the inverter bridge, as shown in Fig. 4.

In Fig. 4, when the capacitor voltage u_c and the current i_{dc} are in the same direction, the capacitor is charged and the voltage increases. When the capacitor voltage u_c and the current i_{dc} are in the reverse direction, the capacitor is discharged and the voltage drops. Shadows A and B stand for the energy absorbed and released by the capacitor, respectively. Given the differences in losses, the capacitance parameters and pulse width of each H-bridge, the energy absorbed and released by the capacitor is not equal in each cycle, so the capacitor voltage of each H-bridge will be imbalanced. The above-mentioned charge and discharge process can be adjusted by the software method, thus solving the voltage imbalance problem.

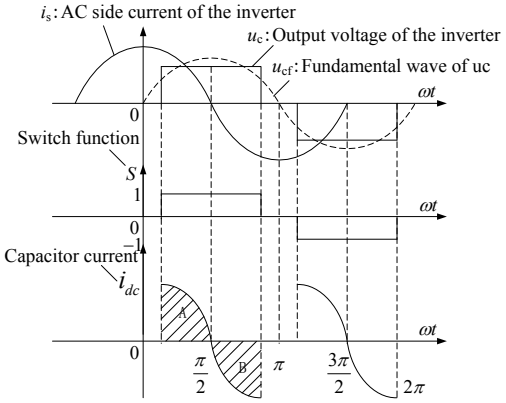

Fig. 4. Energy balance principle of the inverter bridge.

In this paper, the multi-carrier PWM method is adopted to realize the tracking control of instruction currents. As shown in Fig. 3, the modulation wave of each power unit is different, so the charging and discharging time of each dc capacitor will likewise be different. Given these characteristics, the imbalance problem of the dc-link capacitor voltage is even more serious. To solve this problem, a simple and practical software method is presented in this paper. Take phase A for example, when the main modulation signal u_{Fa}^* and the output current i_{Fa} are in the same direction, the dc capacitors of phase A will be charged, but their charging time are different because of their different modulation waves. When u_{Fa}^* and i_{Fa} are in the reverse directions, the dc capacitors of phase A will be discharged, but their discharging time will be different. Thus, we can control the charging and discharging time by changing the distributive rule of modulation signal according to the capacitor voltages. The individual capacitor balance algorithm is made up of a sequence of steps, which are executed every control cycle (see Figs. 5 and 6). In Figs. 5 and 6, x=a, b or c; $temp0$ and $temp1$ are two temporary variables; n is the number of cascaded power units in each phase; the capacitor voltages of each power unit are stored in array $u_{cx}[n]$; the modulation signal for each power unit is stored in array $pwmo_x[n]$; the serial number of each power unit is stored in array $id_x[n]$ according to the order of capacitor voltages.

By using this method, the capacitor with lower voltage will have longer charging time or shorter discharging time, and the capacitor with higher voltage will have shorter charging time or longer discharging time. Thus, the voltages of all the capacitors will become balanced.

The distributive rule of the modulation signal will be changed immediately when the charging and discharging state changes or when the order of capacitor voltages changes. This method is based on the sample time and has a good dynamic response. Furthermore, this method does not require other controllers and will never be out of control.

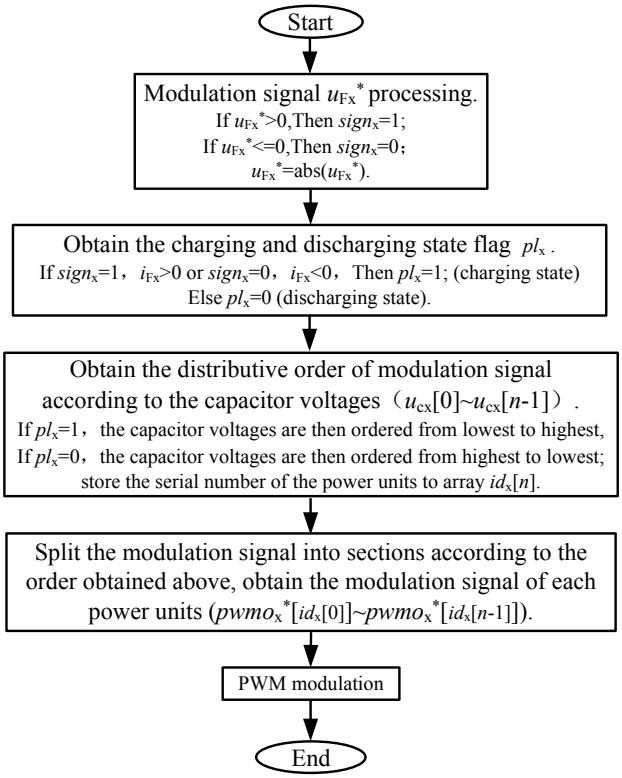

Fig. 5. Flow diagram of proposed individual balancing control strategy.

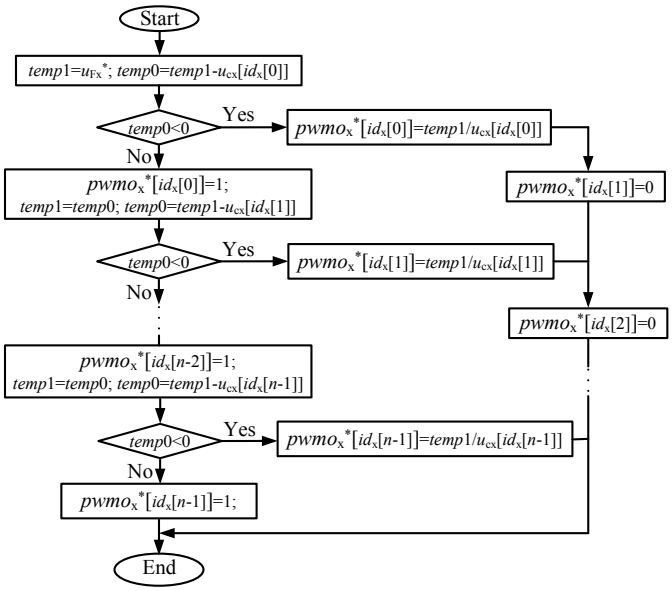

Fig. 6. Flow diagram of the modulation signal distribution process.

V. Results and Analysis

A. Simulation Verification

A simulation model is built in MATLAB. The system voltage is 6 kV, and the fundamental frequency is 50 Hz. The number of cascaded H bridges of each phase is 8, and the star connection method is adopted. The dc link capacitor of each power unit is 3000 μF. The reference voltage of the dc link capacitor is 750 V, and the sampling frequency is 10.8 kHz. To verify the synthetic compensation ability for STATCOM when using the control strategy proposed in this paper, the load current is designed to contain 150 A active currents, 100 A reactive currents, 20 A harmonic currents and 10 A unbalanced currents. Simulation results are shown in Figs. 7 to 11.

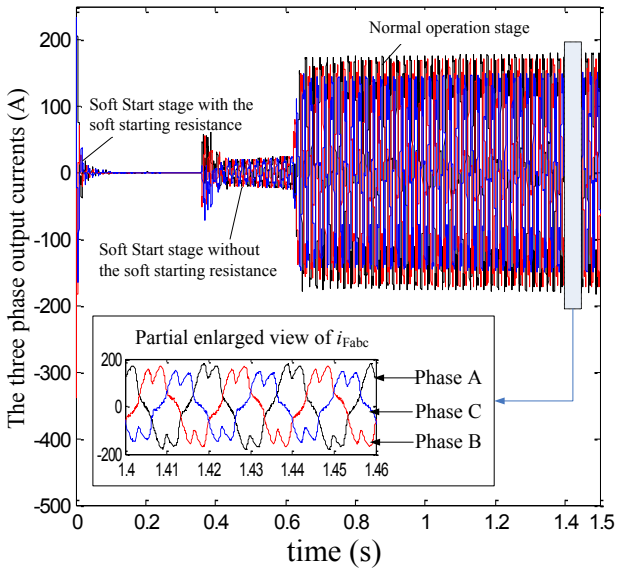

Fig. 7. Waveforms of three-phase output currents.

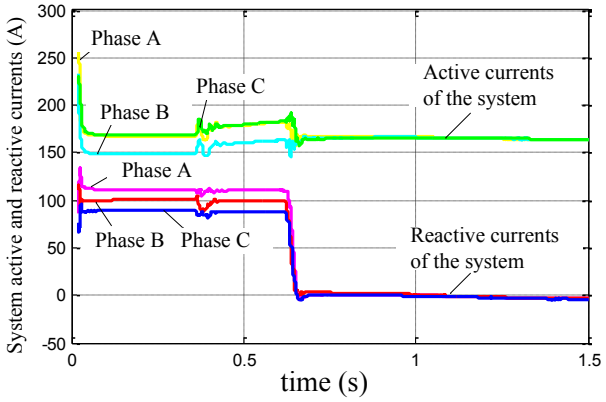

Fig. 8. System active and reactive currents.

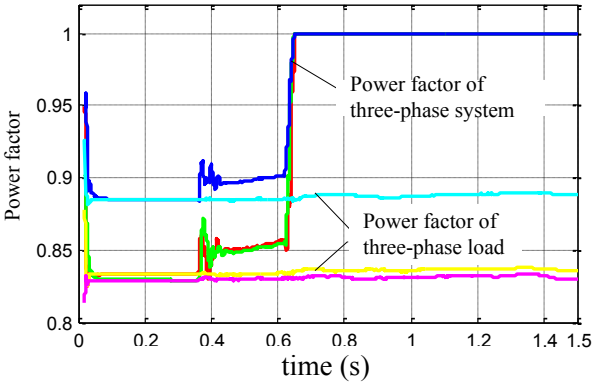

Fig. 9. System power factor.

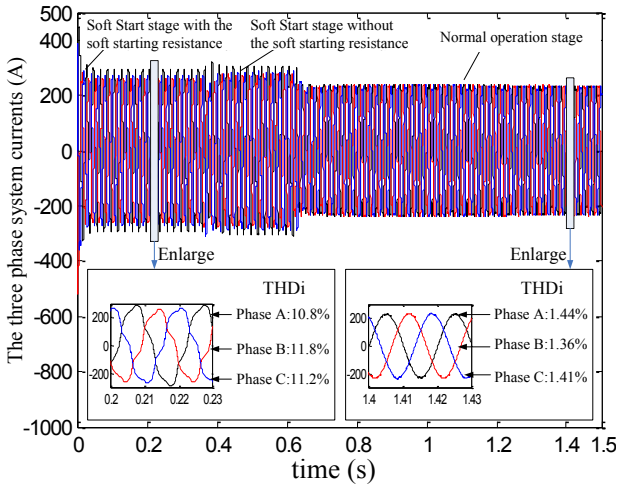

Fig. 10. Waveforms of three-phase system currents.

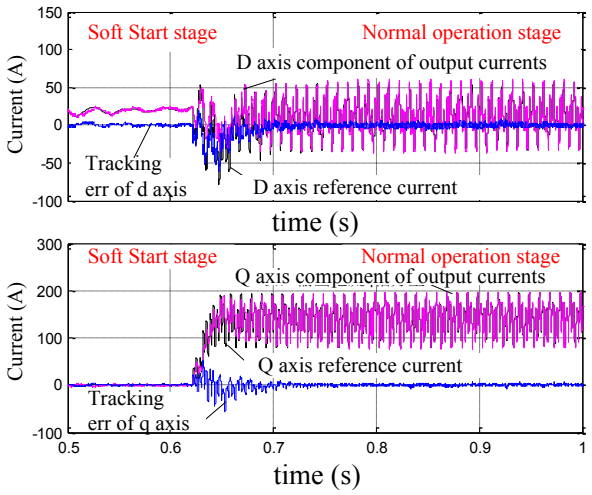

Fig. 11. Reference current, output current, and err.

From Figs. 8 to 10, we can see that the three-phase active currents and reactive currents provided by the system are changed from unbalanced to balanced, and the reactive currents are restricted to almost zero after the STATCOM runs properly (see Fig. 8). The system power factor values are improved from below 0.9 to 1(see Fig. 9). The total harmonic distortion (THD) values of the system currents are also significantly restricted (see Fig. 10). From these data, we can denote that the STATCOM has synthetic compensation ability. Thus, the proposed reference current detection algorithm is accurate.

Fig. 11 shows the reference current of the *d* axis and *q* axis, the *d* axis and *q* axis component of the output currents and the tracking err. According to Fig. 11, the tracking err in the normal operation stage is very small. Thus, the performance of the tracking control strategy used in this paper is very good.

The dc voltage balance control strategy is also verified in the simulation process. The modulation waves of each power unit in phase A, which is obtained by using the balance method presented in this paper, are shown in Fig. 12. All the dc capacitor voltages fluctuate slightly around the reference voltage, as shown in Fig. 13, which shows that the control strategy is very effective.

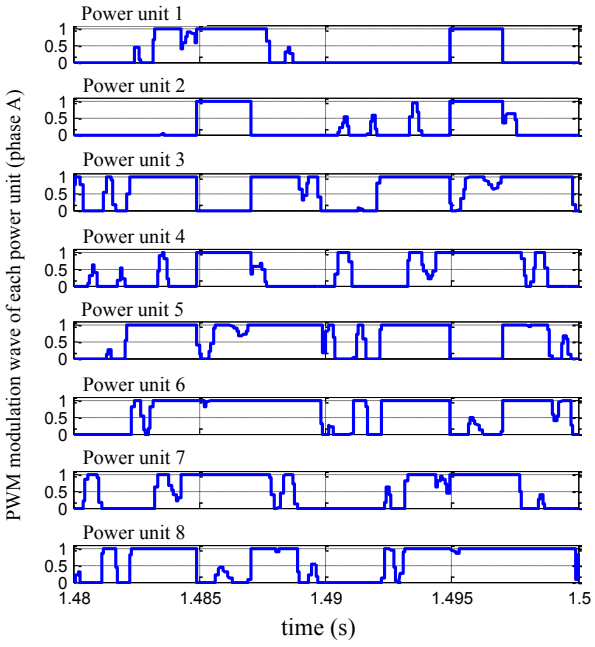

Fig. 12. PWM modulation wave for each power module.

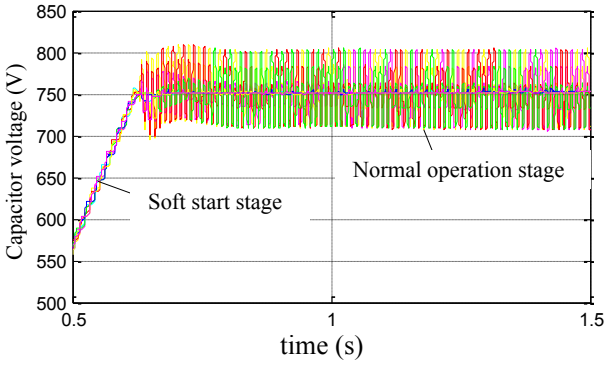

Fig. 13. Capacitor voltage of each power module (phase A).

B. Experiment Verification

Verification is carried out in the laboratory platform. Taking account of the difficulty of setting up a real load in medium- or high-voltage environment, we use two same capacity (3MVar) STATCOMs in the experiment. The two STATCOMs are connected to the point of common coupling of a 6 kV power system. One STATCOM works as a load, and the other works as a compensator. The STATCOM working as a load can send out various currents flexibly in open loop state, thus imitating the real load. The currents mainly contain two components, namely, fundamental reactive current (may be inductive, may be capacitive) and harmonic currents (may contain a variety of characteristic harmonic currents). The STATCOM working as a compensator will detect the load currents in real time and will then compensate the load currents by using the method proposed in this paper.

We made a performance test for reactive compensation. One STATCOM worked as a load and sent out inductive reactive currents, which changed between 70 A (light load) and 250 A (heavy load) every 5 s. Fig. 14 shows the current waves of the two STATCOMs (measured from the same phase but with an opposite direction). After the reactive compensation test, we made a performance test for harmonic compensation. This time, the load currents also sent out 30 A harmonic currents (contained a variety of characteristic harmonic currents), except for the inductive reactive currents, which changed between 50 A and 100 A every 5 s. Fig. 15 shows the current waves of the two STATCOMs.

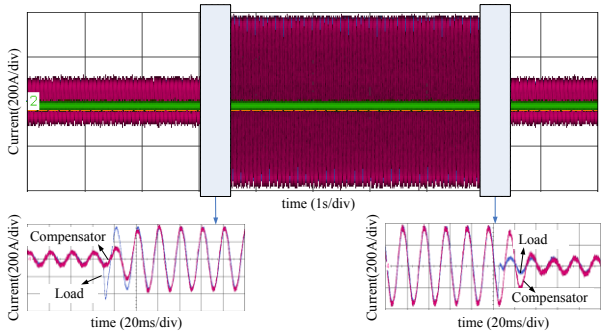

Fig. 14. Performance test for reactive compensation.

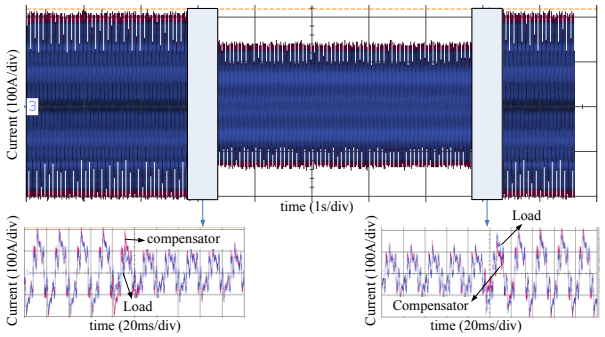

Fig. 15. Performance test for harmonic compensation.

From Figs. 14 and 15, we can see that the current waves of the two STATCOMs are almost the same in steady state. Therefore, the reactive and harmonic load currents are compensated by the STATCOM, which worked as a compensator fairly well. Figs. 14 and 15 also show that only about one power cycle is needed after the step change of the load currents, good compensation effect will be achieved again. Thus, we can denote that the dynamic performance of the STATCOM in this paper is good.

VI. Conclusion

The main contribution of this paper is the development of a new reference current detection algorithm based on selective compensation strategy for STATCOM. This algorithm allows the simultaneous compensation of two characteristic harmonics with only one regulator, yielding a significant reduction of computational effort compared with other methods. By using this method, the STATCOM can provide synthetic compensation ability, and the compensation will be very flexible.

This paper also proposed a software method to realize the individual balancing control of capacitor voltages at the dc side. Compared with other methods, the proposed method does not require other controllers and will never be out of control.

Theoretical analysis and experimental research show that the proposed control strategy is characterized by its simple structure, small calculation time and good dynamic performance. In conclusion, the proposed strategy is suitable for practical application of engineering and has wide application prospects.

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Study on New Smart Transformer Terminal Unit Based on ARM and GPRS Network

Na Wu, Yinjing Guo, Yongqin Wei, Aying Wei

***Abstract*—Distribution transformer is one of the most important power equipments in distribution network, whose running state exercises a great influence on the stability of the network. Transformer Terminal Unit (TTU) is an effective device to monitor the running state of transformers in the distribution automation system. In this paper, we study a new smart TTU which uses ARM7 series chip as processor, equipped with ATT7022B based electric meter module and GPRS module for remote data transmission control. We focus on the corresponding hardware, software design and the measurement principle of harmonics of TTU. The new TTU can measure the electric parameters of the distribution transformer precisely. Taking advantage of the powerful ARM processor, it can analyze harmonic of the power line effectively. Due to the always-on-line feature of GPRS, TTU can achieve reliable communication with the remote terminal and the master station. Compared with other similar units, the new unit outperforms in terms of real-time, precision and reliability, which can fully meet with the high-speed development of distribution automation system.**

***Keywords*—ARM, GPRS, ATT7022B, Transformer Terminal Unit (TTU).**

Original Research Paper
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I. Introduction

DISTRIBUTION transformers are widely used in distribution networks. But at present, most of distribution transformers are not equipped with intelligent monitoring devices with the ability of communication. In recent years, some efforts have been made to distribution transformers in terms of non-oiling, combination and maintenance-free at home, therefore some automation equipments for transformers in the distribution system have come forth. Unfortunately due to the limited economic strength of China, it is impossible to set uniform provision for distribution transformers and most of the existing automation equipments are high-cost that are unsuitable to be used universally for enormous distribution transformers. With the in-depth development of distribution automation, Transformer Terminal Unit (TTU) has a very broad market demand [1].

TTU is an important component of distribution automation system. It is the remote terminal which is installed in the bottom of the system and used for monitoring the real-time operation parameters of the distribution transformers [2]. Under the market demand of distribution transformers, it is therefore desirable to design a monitoring device which can collect the data precisely, meanwhile it can communicate with the remote terminals and monitoring center reliably [3].

The remainder of this paper is organized as follows: Section 2 summarizes the research situation of TTU in China and abroad. In section 3, we propose the structure of transformer monitoring system and introduce the function of TTU in the system. The overall design of TTU is consequently given in section 4. Section 5 discusses the detailed hardware design of each part of TTU. Section 6 is the software design of TTU, and we focus on the algorithm of harmonic analysis and the flow chart design of the main program. Section 7 presents the analysis of harmonic detection results. Section 8 is the conclusion of the paper.

II. The Development and Research of TTU

In traditional design of TTU, single chip microcomputers such as 8031 or 8051 are mostly used as the CPU. This kind of single chip has many disadvantages such as slow data processing rate, small memory capacity, relatively simple interface circuit and more complicated hardware design of data acquisition. Most of the analog acquisition modules in traditional TTU design are as follows. Voltage and current signal firstly flowed into the corresponding sensors, then the filter circuit, sample hold circuit, multiplex switch, A/D conversion, and finally entered into the CPU. The communication module mostly adopts RS-485 Bus or other wired communication mode. All of them need laying so much

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communication line resulting in increasing the investment of hardware inevitably. Moreover most designing of TTU did not consider harmonic analysis function of the distribution line. Thus many scholars have made some improvement in the designing of TTU in recent years, where outstanding contributions are summed up as follows: New single chip microcomputers such as MSP340, SCM F449 and F2012 are adopted as CPU [4]. Double CPU structure is used in reference [5]. Powerful ARM is used as the microprocessor in [1] [6] [7], but the data acquisition circuit and communication circuit of them are designed in the traditional way. In [2] [3] [9], the design of communication circuit is only the way of GPRS wireless communication, and no improvement has been made in other ways. In [8], only data acquisition circuit has been made for certain improvement, and the electric energy meter chip is adopted. The contribution of [9] is the harmonic analysis circuit in the design of TTU. Through analysis of all literatures above, it's obvious that not all aspects are considered comprehensively in the design of TTU.

For these reasons shown above, this paper designed a new intelligent transformer terminal unit (TTU) in distribution network. This device adopted ARM7 series chip as processor, which would improve the processing speed of the system greatly. GPRS wireless communication mode is chosen in communication module, which saves the investment in communication line enormously. Electric energy metering chip ATT7022B is used in the design of data processing module, which simplifies the hardware design of the data acquisition circuit and the harmonic analysis function is considered in the design too. This device combined many functions in one, realized the real-time data acquisition and control, alarm in time and solved the problem of remote data transmission between distribution transformers and master station effectively.

III. The Structure and Function Division of Distribution Transformer Monitoring System

The distribution transformer monitoring system is composed of Transformer Terminal Unit (TTU), GPRS wireless communication network and master station. TTU is installed in the transformer, which mainly accomplishes data collection, analysis and record, pops up alarm information in time when the transformer has abnormal events, receives the command from the master station and implements it. GPRS wireless communication network is the bridge of data transmission between the master station and transformers. Master station receives the real-time data of transformers through GPRS wireless communication network, implements further data processing and saving, consequently issues control command. Therefore the system can achieve a comprehensive monitoring and control for distribution transformers. At the same time, it can provide users with a visual interface and let dispatches obtain monitoring performance of far transformers in time for never leaving home. The structure of transformer monitoring system is shown in Figure 1.

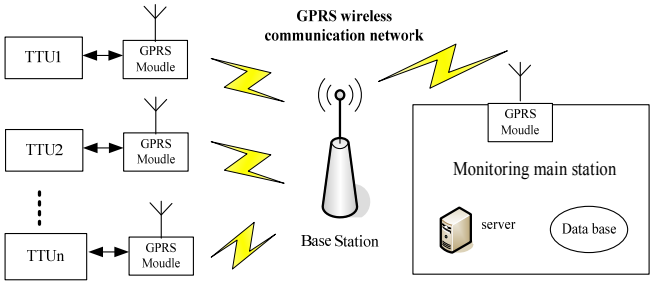


Fig. 1. The structure of transformer monitoring system.

IV. Overall Design of TTU

A. The Main Function of TTU [10]

(1) Measurement capabilities: TTU can online measure three-phase voltage, current, harmonic current, active power, reactive power, electric energy, power factor, etc.

(2) Recording capabilities: TTU can online record all measured values of the parameters mentioned above which includes minimum value and maximum value.

(3) Statistical capabilities: TTU can online make a statistical investigation of blackout time in one year, voltage qualified rate, switching times of capacitor, etc.

(4) Analysis Functions: TTU can complete online and offline analysis of current curves, voltage quality, harmonic distortion rate, etc. and give corresponding governance methods.

(5) Protection Functions: TTU can provide an alarm signal in real time. It has perfect communication function and operation record function, and can record all the operation events for analysis.

(6) TTU can control the switching of capacitors accurately, keep the three-phase low-voltage balance of transformer and adjust the power factor to the optimal state.

B. The General Structure Design of TTU

According to the monitoring system structure introduced above and the main function of TTU, the hardware architecture of TTU is shown in Figure 2.

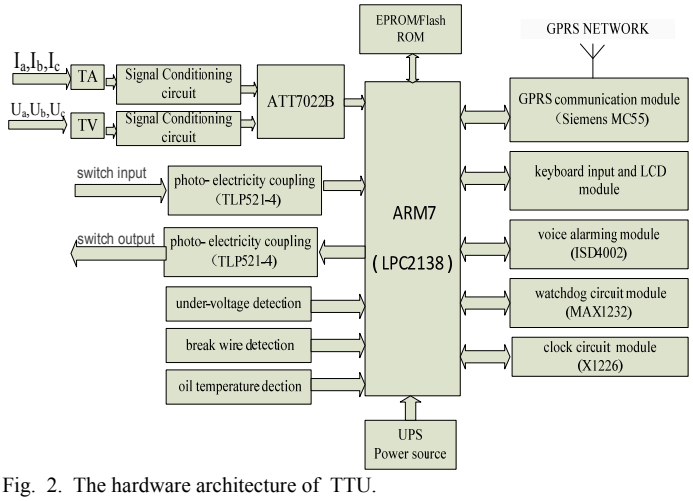


Fig. 2. The hardware architecture of TTU.

In the hardware architecture of TTU, chip LPC2138 based on ARM7TDMI-S is the core of the system. It consists of such modules as analog input module, electric energy measurement

circuit, switch input circuit, switch output control circuit, the keyboard and LCD display circuit, GPRS wireless communication circuit, voice alarm circuit, clock circuit, watchdog circuit, uninterruptible power supply (UPS), etc.

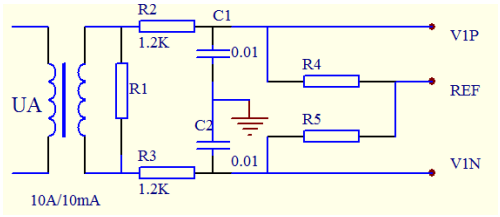
V. Hardware Design of TTU

A. Design of Analog Input Module

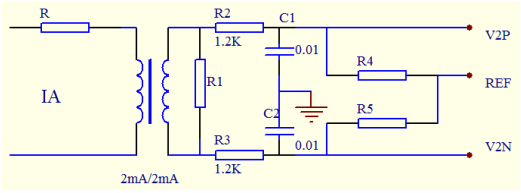
Analog input module is responsible for voltage and current collection from three-phase transformer. It has two parts of the signal conditioning circuit and chip ATT7022B for electric energy metering.

（1） *Current and Voltage Signal Conditioning Circuit*

In the three-phase current signal collections, phase current I_A is changed into suitable voltage signal for measuring range of chip ATT7022B by 10A/10mA current transformer and resistance. 1.2kΩ resistance and 0.01uF capacitance constitute the anti-aliasing filter and the voltage signal after filtering flows into the current input channel of ATT7022B. The principle of three phase voltage signal collections is the same as three phase current collection circuits. Because the voltage transformer adopts 2mA/2mA current-mode voltage transformer, voltage U_A needs to be changed into 2mA current signal by the resistor R_1 firstly [11]. The current and voltage conditioning circuits are shown in Figure 3.



(a) Conditioning circuit of A-Phase voltage.



(b) Conditioning circuit of A-Phase current.

Fig. 3. Circuit diagrams of current and voltage conditioning.

（2） *ATT7022B Electric Energy Metering Chip*

After the processing of signal conditioning circuits, three phase voltage and current enter into the electric energy metering chip ATT7022B. ATT7022B is a three-phase power special measurement chip which has high precision and anti-pilfering electricity function. The chip is used to measure parameters of voltage, current, active power, power factor and frequency, etc, and monitor the running status of three-phase power line. Because of the open phase threshold register of ATT7022B, bit0, bit1and bit2 in measurement register 0x2C would give a status flag of three-phase voltage-absent when the detected voltage effective value in the register is lower than that of open phase threshold register. Thus it can reliably judge whether the power transmission line is lack of a phase or a power outage occurs. ATT7022B can also judge whether the voltage and current phase sequence are normal by detecting the sequence of zero-crossing point of voltage and current signal [12]. The schematic diagram of the interface circuit between ATT7022B and LPC2138 is shown in Figure 4.

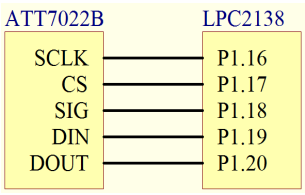


Fig. 4. Schematic diagram of the interface circuit between ATT7022B and LPC2138.

B. Design of Switch Input Module

Switch input signal of TTU mainly includes remote signal and remote pulse signal. Remote signal indicates the position status of the circuit breaker of the distribution transformer and the action status of protection and automatic devices. Remote pulse signal is to read the pulse signal of multi-function electric meter. Switch input signal must be converted to 3.3V logic signal by the isolation of the optocoupler firstly and then enters into I/O port of LPC2138. The circuit of the switch input module is shown in Figure 5.

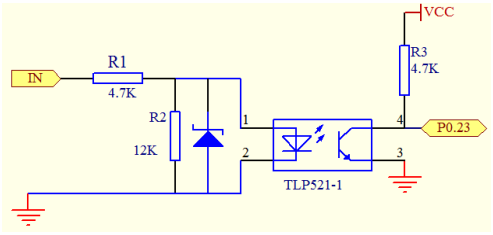


Fig. 5. Circuit diagram of switch input.

C. Design of the Central Processing Module

The central processing module and peripheral circuit can realize data collection and data processing of all kinds of analog quantities and switching values. At the same time it can control the module sending and receiving short message and dialing the alarm telephone number. Because of the distribution monitoring function, the historical data and statistical data must be saved timely, besides it needs a memory bank to save a large number of control parameters. So a piece of AT241024 EEPROM is extended in the system, which storage space can achieve 1M byte.

D. Design of GPRS Wireless Communication Module

GPRS wireless communication module in the system is composed of MC55 produced by Siemens Company, which is the minimum size of three-frequency module in the market. In addition to the original function of GSM module, MC55 supports packet service functions, which embeds TCP/IP protocol stack of high reliability and usability. So it is very suitable for wireless communication as a terminal module [13].

Such functions of MC55 as power on and off, working mode and working condition, etc. are controlled by LPC2138. Serial port 0 of MC55 and serial port 1 of LPC2138 are used to realize the TCP/IP network communication in the system. LPC2138 realizes commands and data control with MC55 through AT command.

MC55 has 50 pins which can be divided into the function modules as following: power charging management module, double serial ports module, double audio interface module and SIM card interface module. The SIM card interface module provided by MC55 can drive SIM holder directly. The CCIN pin of MC55 is designed for testing SIM card. When the SIM card is inserted, the output level of CCIN is high and MC55 is on work, otherwise the output level of CCIN is low and MC55 is closed. CCIN pin controls the switch of MCU through the electrical level in order to prevent the damage of MC55 when SIM card is pulled out in the process of work. In order to guarantee the electromagnetic compatibility, the distance between SIM card and MC55 is no more than 200mm [13]. The interface circuit between MC55 and SIM card is shown in Figure 6.

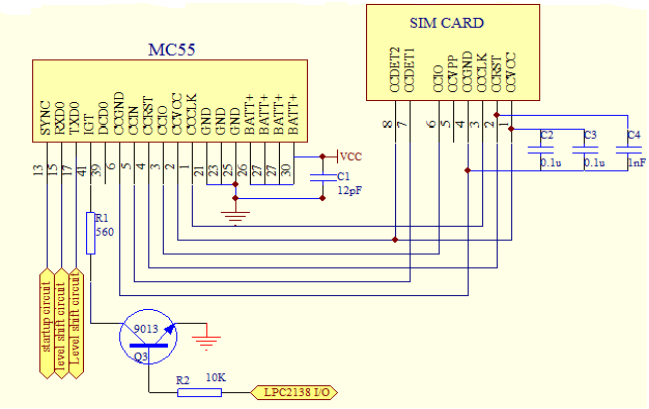


Fig. 6. Diagram of interface circuit of MC55 and SIM card.

The typical voltage of MC55 is 2.65V when the serial-port sending and receiving data, while the voltage of ARM7 is 3.3V. So direct connection between them may cause data error, and two electric level conversion circuits are designed, which respectively convert 5V to 2.5V, 2.5V to 5V. Two bipolar junction transistors are used in each conversion. Electric level conversion circuits of MC55 are shown in Figure 7.

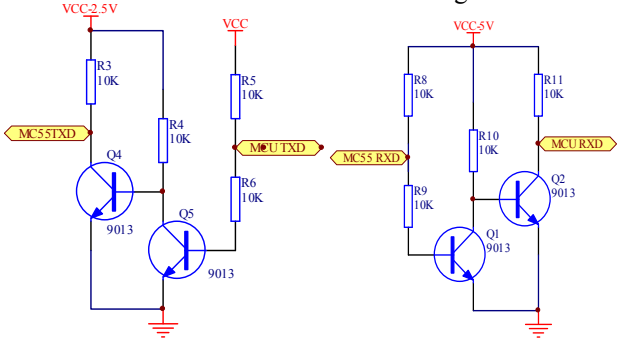


Fig. 7. Diagram of electric level conversion circuits.

E. Design of Other Major Modules

(1) Design of the keyboard and LCD module

In the distribution automation system, we can realize the function of data acquisition through remote communication. But on many occasions, users need to understand real-time situation of the transformer directly. Thus, the Liquid Crystal Display function is extended, which provides a great convenience for users. So it is very helpful to field maintenance and detection for distribution transformer [9]. The Liquid Crystal Display module MS12864R is used to display Chinese and graph. We can control the content of Liquid Crystal Display and modify the field parameters of TTU by the key module. Six keys are designed in the key module. Input signal of the key is detected by the interrupt pin GPIO of ARM, and the interrupt signal of the key is provided by the chip 74LS14.

(2) Design of the Alarm Module

Once the transformer has been stolen, broken line fault or power failure occurs, alarm module will immediately detect out them and report to operators on duty through GPRS short message or voice alarm and store the alarm data into the database in the end. In the electronic map of master station, the corresponding emergency alarm will keep flashing, which will display the time, location and type of the alarming. So it is very convenient for the staff of the scene to arrive at the alarm point in time.

The design of the power module and clock module circuit is no longer described.

VI. Software Design of TTU

A. Algorithm Selection

Due to the electric energy metering chip completing the collection of three-phase voltage and current, and calculating parameters such as voltage, current, power, electric energy and so on, the software design of the measurement module is relatively simple. Here only the algorithm of harmonic analysis is introduced [14].

In power system, the equation of voltage and current is as follows.

$$u(t) = \sum_{k=1}^{\infty} U_k \sin k\omega t \tag{1}$$

$$i(t) = \sum_{k=1}^{\infty} U_k \sin(k\omega t - \theta_k) \tag{2}$$

As periodic function, voltage and current signal can be decomposed into the Fourier series as follows.

$$x(t) = A_0 + \sum_{n=1}^{\infty} (A_n \cos n\omega t + B_n \sin n\omega t) \tag{3.a}$$

or

$$x(t) = A_0 + \sum_{n=1}^{\infty} (C_n \sin n\omega t + \psi_n) \tag{3.b}$$

In the formula, $\omega = 2\pi f$ is the corresponding angular frequency, n=1, 2⋯ is the harmonic order. A_0 is the DC component which is the average value of one cycle in the periodic function. A_n and B_n are the coefficient of Fourier series, which are the rectangular coordinate component of N harmonics. The corresponding n harmonic vector is as follows.

$$\psi_n = \arctan(\frac{B_n}{A_n}),$$

$$C_n = \sqrt{A_n^2 + B_n^2},\ C_n < \psi_n = A_n + jB_n,$$

$$A_0 = \frac{1}{T}\int_0^T x(t)dt,$$

$$A_n = \frac{2}{T}\int_0^T x(t)\cos n\omega t dt,$$

$$B_n = \frac{2}{T}\int_0^T x(t)\sin n\omega t dt \quad (4)$$

After discretization, there is the following formula.

$$A_n = \frac{2}{N}\sum_{k=0}^{N-1} x_k \cos\frac{2\pi}{N}nk \quad (5)$$

$$B_n = \frac{2}{N}\sum_{k=0}^{N-1} x_k \sin\frac{2\pi}{N}nk \quad (6)$$

In the formula above, n = 0, 1, 2, … , N – 1 is the harmonic order, k = 0, 1, 2,…, N – 1 is the sampling number, and x_k is the sampling value at k time.

But in the actual measurement, the functional relationship between the formula (1) and (2) is unknown, we can get the limited length sequence, whose cycle is N, through the voltage and current sampling circuits. According to the theory of digital signal processing, the Discrete Fourier Transform (DFT) is expressed as follows.

$$X(n) = \sum_{k=0}^{N-1} x(k)e^{-j2\pi k\frac{n}{N}}(0 \le k \le n-1) \quad (7)$$

In the equation, $X(n)$ is the size of the n times harmonic component.

From the equation (4), (6), (7), we can get the following equation.

$$\frac{2}{N}X(n) = A_n - jB_n \quad (8)$$

So the amplitude of each harmonic, the phase angle between the same harmonic, etc. can be got by Discrete Fourier Transform (DFT) in actual measuring system. But DFT needs extensive calculation, so Fast Fourier Transformation (FFT) is used in the system.

B. Flow Chart of Software Design

The working process of the main program of TTU is as follows. The system is powered on and initialized firstly, that is setting the value of each control register of the ARM which includes system clock, I/O port, UART, SPI, I^2C, SSP, interrupt timer, etc. Then it carries out a self-checking on the special chips including memory, real-time clock, LCD module, electric energy metering chip ATT7022B, etc. If there is some abnormal chip, the system would alarm, otherwise continue to run the main program.

The main program flow chart is shown in Figure 8. It judges whether the circuit breaker of the transformer circuit has acted or not firstly. If the circuit breaker has acted, the system would alarm, or go into the acquisition of voltage, current and other parameters, and perform harmonic analysis. According to the acquisition parameters, we can diagnose whether the transformer working properly. If there is a fault of transformer, the system would alarm, or go into the next round of data collection.

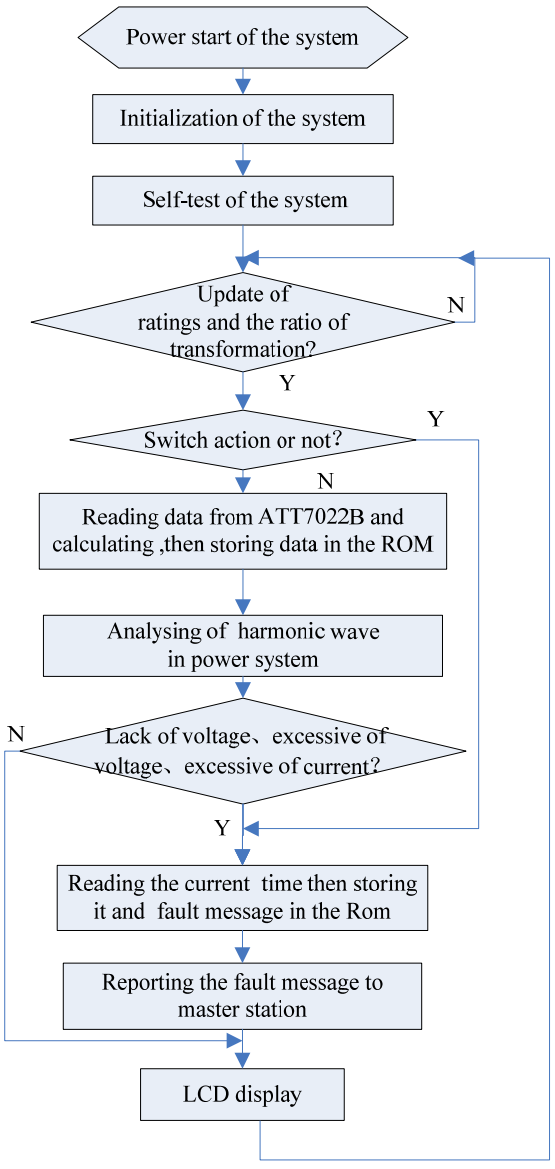


Fig. 8. The flow chart of the main program.

Subroutine contains such modules as data acquisition module subroutine, display subroutine, fault alarm subroutine, harmonic detection subroutine, GPRS communication module subroutine, etc.

VII. Analysis of Experimental Results of Harmonic Detection

Harmonic source generator is adopted in order to output harmonic signal. If each harmonic of the harmonic source are set in table I, each harmonic phase can be given freely. After harmonic signal sampled (each cycle by 128 points) and calculated by FFT, each harmonic content rate can be got, which will be compared with the set value. Measurement value of harmonic percentage is shown in table II.

TABLE I
HARMONIC PERCENTAGE OF SETTING

Harmonic frequency of setting	3	5	7	9	11	13	15
Harmonic ratio of setting（%）	2.5	4.0	3.5	1.8	1.0	0.9	0.7

TABLE II
HARMONIC PERCENTAGE OF MEASUREMENT

Harmonic frequency of measurement	3	5	7	9	11	13	15
Harmonic ratio of measurement （%）	2.491	3.982	3.488	1.789	0.990	0.902	0.697

VIII. Conclusion

Facing the demand of users, in this paper we design an easy-to-use distribution transformer monitoring terminal with powerful functions by use of advanced techniques. Compared with similar products, the proposed system has completed not only all basic functions of TTU but also the harmonic detection which reduced the harmonic harm to distribution transformer and utility grid. We achieve the data acquisition and processing and some other management functions of distribution transformer by GPRS wireless communication mode, which has the outstanding advantages in terms of cost-effective, fully functional, easy maintenance management, etc. This new system has been put into running for more than a year in distribution department of Jining Power Supply Company in China. Operation practice shows that the system has achieved satisfactory results in the control accuracy, reliability, real-time and harmonic analysis so that it has a satisfied promotion and application value.

With the development of microelectronics technology and communication technology, the TTU designed in this paper can also be further improved and the below development directions can be taken. Double CPU structure such as ARM+DSP can be used and other parts of the hardware design can adopt new chips in the market, etc. The functions of TTU can also be further enhanced to collect the information of distribution transformer as much as possible and it can better promote the development of intelligent distribution network.

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