Strained Silicon Layer in CMOS Technology

Tatjana Pešić-Brđanin, Branko L. Dokić

Abstract— **Semiconductor industry is currently facing with the fact that conventional submicron CMOS technology is approaching the end of their capabilities, at least when it comes to scaling the dimensions of the components. Therefore, much attention is paid to device technology that use new technological structures and new channel materials. Modern technological processes, which mainly include ultra high vacuum chemical vapor deposition, molecular beam epitaxy and metal-organic molecular vapor deposition, enable the obtaining of ultrathin, crystallographically almost perfect, strained layers of high purity. In this review paper we analyze the role that such layers have in modern CMOS technologies. It's given an overview of the characteristics of both strain techniques, global and local, with special emphasis on performance of NMOS biaxial strain and PMOS uniaxial strain. Due to the improved transport properties of strained layers, especially high mobility of charge carriers, the emphasis is on mechanisms to increase the charge mobility of strained silicon and germanium, in light of recent developments in CMOS technology.**

Index Terms—**Strained silicon layers, uniaxial strain, biaxial strain, CMOS technology.**

Review Paper
DOI: 10.7251/ELS1418063P

I. Introduction

IN the last 30 years, the primary characteristic of improving performance of CMOS technology has been scaling the dimensions of the components. Continuous reduction in size of devices and simultaneously increase of the size of chips has led to the production of highly complex integrated circuits with ultra large scale of integration. The realization of such complex high-speed integrated circuits is enabled by using CMOS technology with critical dimensions of components of a few nanometers. Numerous factors influence the increase of speed of MOS transistor operation; the most important is the time of the carriers transport through the channel under the gate, which can be reduced by shortening the gate length. However, the other demands of designing integrated circuits with ultra large scale of integration, such as, for example, the increase in density on the chip and reducing the size of the chip, have led to the scaling of other transistor dimensions. Fig. 1 shows the trend of reducing the gate length that has led to the emergence of new technologies [1]. Reducing the gate length caused a simultaneous scaling of other technological parameters, in order to meet the required performances of integrated circuits regarding high speed and low power consumption, or the desired degree of integration. However, with recent CMOS technologies, in which the gate length is less than 90 nm, this performance improvement becomes more difficult due to physical limitations in miniaturization of MOS transistors.

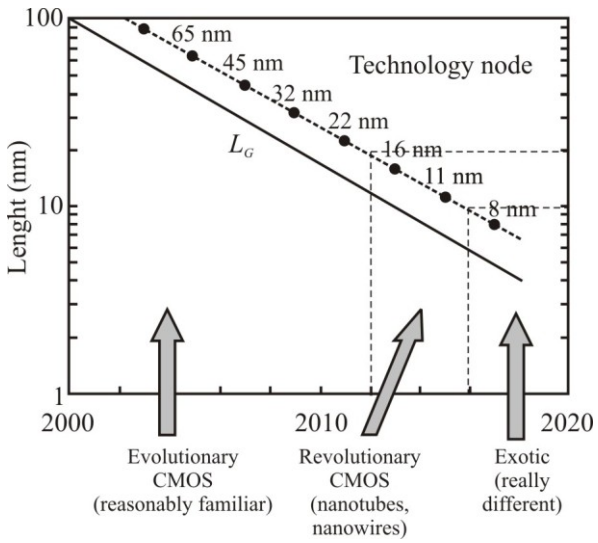

Fig. 1. Technology and gate length evolution [1].

With the scaling dimensions, at the same time, new process technologies were developed, especially ultra high vacuum chemical vapor deposition (UHV-CVD), and molecular beam epitaxy (MBE), which enabled the obtaining of ultrathin, crystallographically almost perfect, strained layers of high purity. Due to the low temperature processes ($<600\,^{\circ}\mathrm{C}$), diffusion of impurities is very weak. This allowed obtaining of super abrupt pn junctions with much greater difference in concentration of ingredients on both sides of the joint than in the case of other epitaxial growth techniques. Using the metal-organic CVD (MO-CVD) growth techniques, the

Manuscript received 15 December 2014.

Tatjana Pešić-Brđanin is with the Faculty of Electrical Engineering, University of Banja Luka, Banja Luka, Bosnia and Herzegovina (phone: +387-51-221-829; fax: +387-51-211-408; e-mail: tatjanapb@etfbl.net).

Branko L. Dokić is with the Faculty of Electrical Engineering, University of Banja Luka, Banja Luka, Bosnia and Herzegovina (phone: +387-51-221-824; fax: +387-51-211-408; e-mail: bdokic@etfbl.net).

homogeneous and heterogeneous layers are created with controlled concentration and thickness up to 50 Å, while using the MBE technology obtained layers were even less than 10 Å of thickness [2]. With these new technological processes, and great progress in lithographic techniques, new structures of MOS transistors with ultrathin layers of germanium or SiGe alloys on silicon substrates were reached. Compared to conventional, these new structures are characterized, above all, with a significantly higher speed operation, as well as improved current-voltage performances. The operations of these transistors, however, are characterized by a number of new physical phenomena (quantum effects, transport across the heterojunction, ballistic transport, tunneling etc.), which must be taken into account in optimization of such structures and specifications of their electrical characteristics [3,4].

One of the new technological structures of MOS transistors, the structures with strained silicon in channel region, thanks to advances in the local strain technique, are used in CMOS technology (e.g., logic circuits in 90 nm CMOS technology) [5]. The increase of the carrier mobility, which is implemented by appropriate silicon strain, provides higher speed of the carriers, respectively higher current drive, under the same conditions of polarization and a fixed oxide thickness. On the other hand, it means that with the same current conditions in the channel, thicker oxides and/or lower voltages supply could be used, which leads to relaxation of compromise between the current, consumption and the effects of short channels. Therefore, the strain technique and a corresponding increase in carrier mobility are considered as factors required for future CMOS technologies [6,7].

This paper provides an overview of the principles and application techniques of strained layers, with special emphasis on the physical mechanisms to increase mobility due to strain, in modern and future CMOS technologies.

II. Phisical Mechanisms for Mobility Enhancement

One way to improve the performance of MOS transistor is the possibility to change the properties of materials. The property of silicon to exhibit modified characteristics of transport parameters while strained [8,9] is used for this purpose. Measurements which were performed on Hall structures in strained silicon layer at room temperature showed a large electron mobility, which in the case of a very low temperatures (0.4 K) reaches extremely high values, up to 500 000 cm^2/Vs [10]. The increase in electron mobility in strained silicon layers is supported by theoretical studies [11,12].

A. Electron Mobility Enhancement

The silicon layer straining is technologically commonly performed by the growth of silicon on the SiGe substrate. Fig. 2 schematically shows the crystal structure of the silicon and the relaxed layer of $Si_{1-x}Ge_x$. Since the lattice constant of $Si_{1-x}Ge_x$ composition is higher than the silicon lattice constant in the balance state, the pseudomorph layer of silicon which has grown on the relaxed $Si_{1-x}Ge_x$ layer (or virtual substrate) is under biaxial strain. The distance of silicon atoms assimilate to the higher atomic distance in the SiGe layer, thereby increasing the lattice constant of silicon a_{Si} in the growing level. The lattice constant of the SiGe composition, and hence the strained silicon, is approximately a linear function of the germanium content (or the value of the x in the $Si_{1-x}Ge_x$ composition). As the germanium lattice constant is about 4% higher than the lattice constant of silicon, it will, for example, $Si_{0.75}Ge_{0.25}$ virtual substrate cause an increase in lattice constants of strained silicon which has grown on the composite layer for approximately 1% [9].

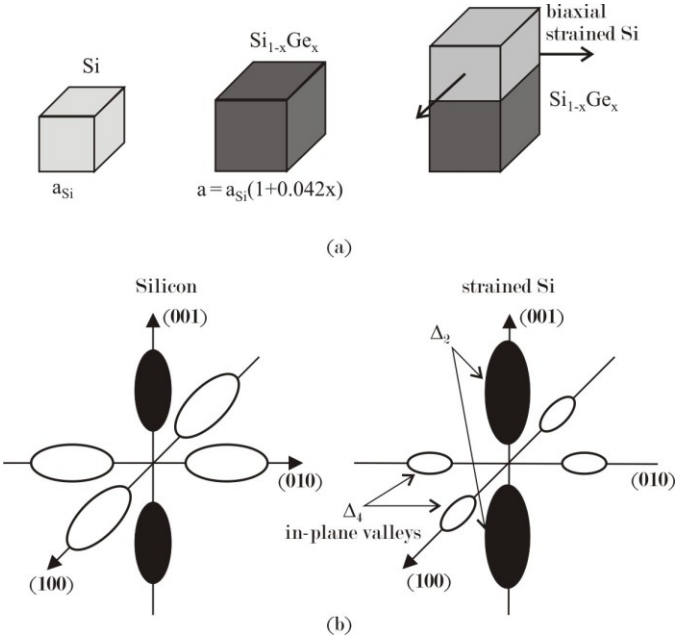

Fig. 2. Schematic illustration of balance silicon structure in SiGe composition (a) and conduction zones of unstrained and strained silicon (b).

The strain leads to the shape degeneration of six equipotential valleys in conduction zone by reducing the value of the energy minimum in the two transverses (Δ_2), compared to the values of the energy minimum in four longitudinal directions (Δ_4) [13] (Fig. 2). The result is an effective anisotropy of the electron effective mass; transversal mass ($m_t = 0.19 m_0$) appears, and it is smaller than the longitudinal mass ($m_l = 0.916 m_0$). m_0 is the electron mass. Table 1 shows the values of the electron effective mass depending on the crystallographic planes and directions for silicon and germanium [14].

The difference of the effective mass causes different physical properties in Δ_2 and Δ_4 valleys. The conductive electron mass in parallel MOS interface is smaller in Δ_2 the plane than in the Δ_4 plane, and, therefore, the electron mobility is greater in the Δ_2 plane, than in the Δ_4 plane. Also, as the inverted layer thickness and the subzone energy are determined by effective mass in the direction normal to MOS interface, an inversion layer is thinner and the subbands energy is lower in Δ_2 plane, and so the effective mass is higher.

The effect of strain on the electron mobility can be reflected by changing the subbands energy, i.e. the energy levels in the conduction zone. The increase of the energy of the sublevels results in increased mobility through two mechanisms: increasing the average value of mobility in Δ_2 plane due to a large number of electrons with higher mobility and modification of the bottom of the conduction band leads to a reduction of dissemination of holders on the phonons, which, in total, increases the electron mobility even when the electric field has low values [13].

TABLE I
ELECTRON EFFECTIVE MASS DEPENDING ON THE CRYSTALLOGRAPHIC PLANES AND DIRECTIONS FOR SILICON AND GERMANIUM

	Plane	Channel direction	Effective mass ($\cdot m_0$) m_x	m_y	m_z
Silicon	(100)	⟨001⟩	0.19	0.19	0.916
		⟨011⟩			
	(110)	⟨001⟩	0.19	0.553	0.315
		⟨110⟩	0.553	0.19	
Germanium	(100)	⟨001⟩	0.153	0.153	0.12
		⟨011⟩	0.085	1.12	
	(110)	⟨001⟩	0.601	0.082	
		⟨110⟩	0.082	0.601	

Unlike the conduction band, the structure of the valence band is similar for silicon and germanium. The energy minimum and maximum are located in the same crystallographic directions. Band structure of germanium is less anisotropic when compared to silicon, so its effective mass is lower. Germanium structure reacts to strain in a similar way as silicon structure, with improved response to the strain inversion.

There are several empirical phrases to assess the width modification of the band gap zone of strained silicon. For strained silicon, a narrowing of the band gap zone depending on the percentage of germanium in the relaxed $Si_{1-x}Ge_x$ layer can be calculated:

$$E_{g\,st} = E_g - 0.4 \cdot \mathrm{x} \quad \text{(eV)} \tag{1}$$

where E_g is the silicon bang gap energy, and $E_{g\,st}$ is the strained silicon bang gap energy.

Of particular importance is the electron mobility model which has to include the functional mobility dependence for strain, temperature, ingredients concentration in the channel and polarization. Fig. 3.a shows the experimental results for mobility enhancement factor, which is defined as the mobility ratio of strained and unstrained silicon. The findings for the two models of mobility, derived mainly from the theory of phonon diffusion, are also shown [3,15,16].

Figure 3.b shows the dependence of effective mobility on the effective electric field at a room temperature, with and without strain. It shows that the mobility enhancement factor is almost unchanged in a wide range of values for the external electric field.

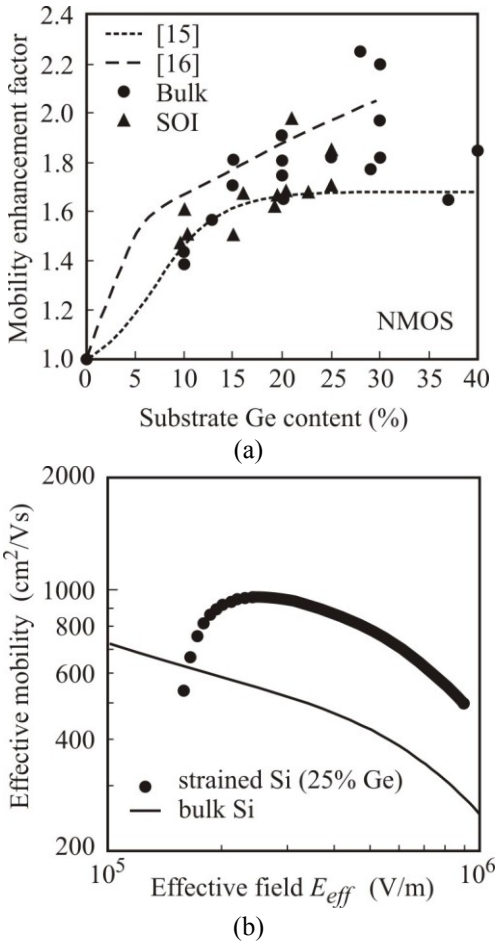

Fig. 3. Mobility enhancement factor as a function of Ge content in SiGe substrates for NMOS transistor (a) and effective field dependence of electron mobility in biaxial strained Si NMOS (b).

B. Hole Mobility Enhancement

Unlike the electron mobility enhancement, the physical mechanisms of change of the hole mobility in PMOS transistors due to strain have not been fully explained. Also, it has been shown that the effects of the uniaxial and biaxial strain on the hole mobility are completely different. With the biaxial strain, the hole mobility enhancement due to strain is a consequence of the decrease of the hole effective mass in the occupied zones of the valence zone, suppression of inter-subband scattering and increase of the availability of subbands with a smaller effective mass, i.e. higher mobility.

Figure 4.a shows the experimental results for hole mobility enhancement factors for biaxial strained PMOS transistor, and the results obtained by theoretical models. It can be noted that a large percentage of germanium significantly increase the hole mobility. The dependence of hole mobility enhancement factors on the effective electric field indicates to the fact that the maximum hole mobility enhancement factor is at a lower

values E_{eff}, Figure 4.b. As mobility at large values E_{eff} is significant for most practical applications, it is necessary to use a biaxial strain silicon layers with a high content of germanium. Recent studies have shown that, when uniaxial compression along $\langle 110 \rangle$ PMOS channel direction is applied, the hole mobility enhancement factors is higher, even for less strain, and it does not decrease significantly with increasing values E_{eff} [17-20].

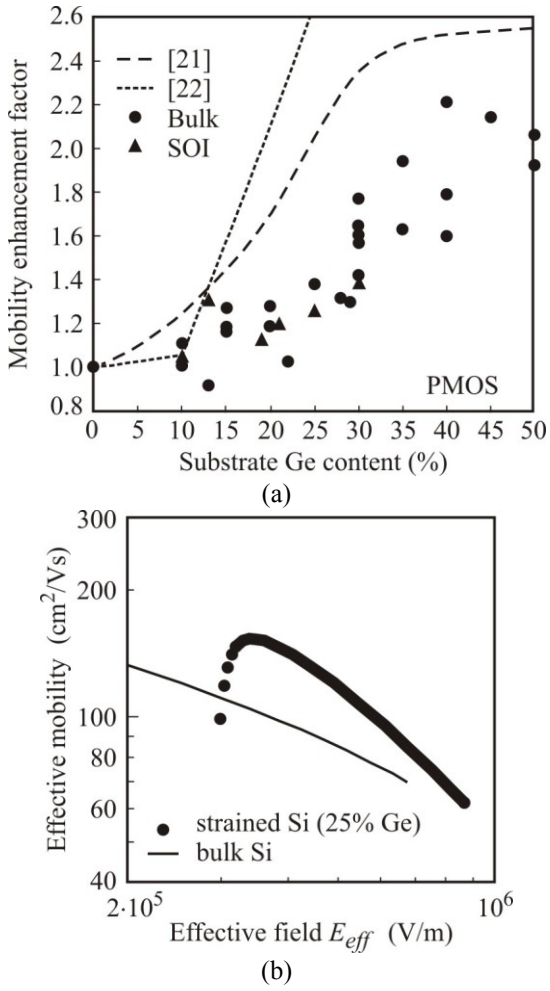

Fig. 4. Mobility enhancement factor as a function of Ge content in SiGe substrates for PMOS transistor (a) and effective field dependence of hole mobility in biaxial strained Si NMOS (b).

By measuring the piezoresistivity at (100) surface of PMOS channel during uniaxial compression parallel to the channel direction and strain by stretching parallel to the channel width, the hole mobility enhancement has been shown. Fig. 5 shows these complex dependencies of hole mobility on strain for PMOS transistor. It can be seen that, for less strain, compression at $\langle 110 \rangle$ surface increases the hole mobility. Also, for higher strain, the hole mobility is increased by biaxial strain, as by compression, and stretching. It can be concluded that the uniaxial compression at $\langle 110 \rangle$ surface and biaxial stretching are the most effective in terms of increasing the hole mobility for PMOS transistors.

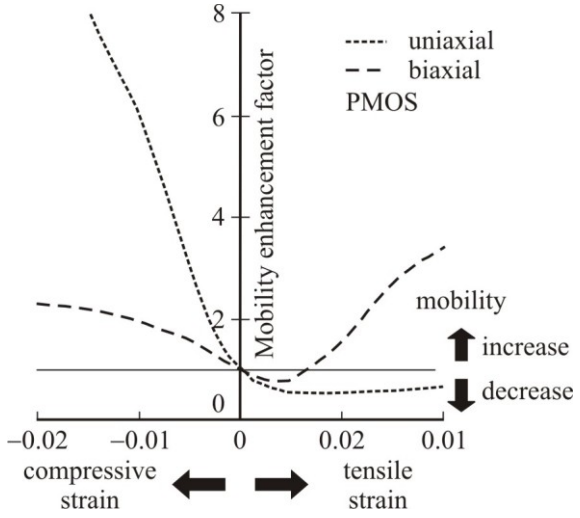

Fig. 5. Hole mobility enhancement factor for PMOS transistor with uniaxial compressive and biaxal tensile strain [23]. The value of E_{eff} is taken to be 1 MVcm^{-1}.

III. MOS Structures with Strained Layers

The strain is widely accepted as a promising technique which improves CMOS performances through a significant increase of mobility, even from 90 nm CMOS technology. In recent years, substrate and/or process-induced strained channels are successfully integrated in MOS transistors, for the purpose of increasing the channel mobility. Technologically, so far, the biaxially strained layer showed the best results in the case of long channels transistor (over 100% improvement in mobility). However, the contact resistance of the source and drain, saturation velocity, self-heating of relaxation for strained layer complicate the improvement of performances in nano devices.

The advantage of the uniaxial strain access is that it is installed during production of CMOS circuits. However, the scalability and the geometrical dependence are the main problems. The lateral dimensions of the transistors affect the efficiency and strength of strain in the strained layer. It is shown that the process-induced strain layers increase the mobility of both types of carriers and the power drain in NMOS and PMOS transistors. The strain in the channel can be obtained through the individual process steps and the use of strained silicon substrate.

A. Global Strain Technology

The structure of MOS transistor with biaxially strained silicon layer, which has grown on a relaxed SiGe substrate, has been intensively explored in recent years. Also, there have been research on the structures with strained silicon layer on insulator (***S**train-**S**i **O**n **I**nsulator* - SSOI) [24], where strained/relaxed layers are formed on the buried oxide, and the structures where the strained silicon layer is directly linked to the buried oxide (***S**train-**S**i **D**irectly **O**n **I**nsulator* - SSDOI) [25]. Common structures and substrates using biaxial strained layers are shown in Fig. 6. The technology for production of

MOS transistor on substrates on which strained layers are formed is called a "Global strain technology".

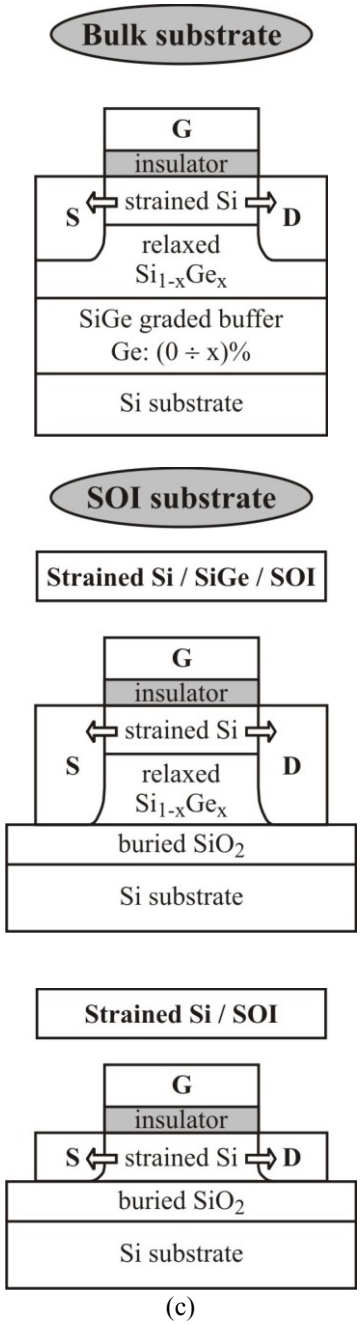

Fig. 6. Cross-sections of typical MOS structures using biaxial strain [3].

As for MOS transistors using silicon substrates from the global strain technology, the research and development of optimized components are implemented on 45 nm and 32 nm CMOS technology. Many research groups have achieved a improvement of current activation in the range of 10-25% with a global strained silicon layer, and gate lengths smaller than 100 nm [25,26]. Also, there has been success in the design of CMOS circuits with gate lengths of 25 nm and the integration of strained silicon layers with gate oxides with high dielectric constant and a metal gate [27].

Main advantages of global strain technology are in obtaining uniformly strained layers with more strength and possibility of implementing standard CMOS process steps with minimal modifications. On the other hand, there are certain difficulties relating to the limited improvement of PMOS transistor performances with small and medium silicon strain, the occurrence of defects and dislocations at the boundary surfaces, increased production costs and an increase of current leakage at compounds. In transistors with ultra short gate lengths, special attention must be paid to the reduction of the parasitic resistance of the source and drain [3,25].

B. Local Strain Technology

In order to eliminate the limitations of the global strain technology, special attention is paid to the local introduction of structures and materials that will cause strain in the channel of MOS transistors. This process can be conducted in two ways:

- The source and drain of the transistor are formed by epitaxy growth of SiGe composition. These buried SiGe layers, which introduce uniaxial compression in the channel area, are applied in the case of PMOS transistors. Recently it has been shown that NMOS transistor with a layer that is strained by stretching, in which the source and drain formed by selective growth of SiC instead of SiGe, can be implemented (Fig. 7) [28].
- A thin layer of SiN can be applied on the MOS structure, which introduces strain in the channel. In many cases, the SiN layers with stretching are applied for NMOS transistor, while the SiN layers with compression are applied for PMOS transistor (Fig. 7) [29].

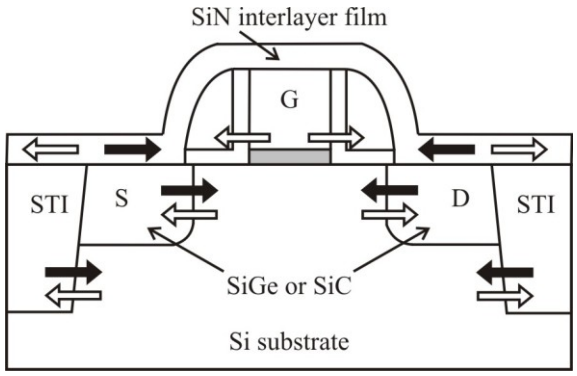

Fig. 7. Illustration of a device structure using different local strain techniques. STI means Shallow Trench Isolation. Black and white arrows indicate compressive and tensile strain, respectively [3].

Beside the above mentioned methods, the strain can be also used for the other parts of the structure, such as, for example, the field insulation, the gate electrode, ... Since the mentioned methods are used in the production of logical LSI circuits for technologies less than 90 nm, the local strain technology has a growing practical importance in CMOS technology [5,30].

The basic advantages of the local strain technology are the possibility of using standard CMOS process with slight modifications and low cost, and acquiring the uniaxial strained PMOS transistors with excellent performance with relatively low strain. However, as in any strain technology, what presents a problem is the process of relaxation of strained layers, which occurs due to the advanced processes in a technological sequence or the component geometry, and a great attention is

devoted to this issue at a moment [3,30].

IV. Influence of Strain on Electrical Characteristics

The content of germanium in the SiGe composition used for the source and drain can change the channel compression of 255 MPa to 1.8 GPa, which causes different levels of strain. Fig. 8 shows the output characteristics of PMOS transistor depending on the content of germanium in SiGe S/D pockets. The improvement of drain current with increase of the germanium share is noticeable.

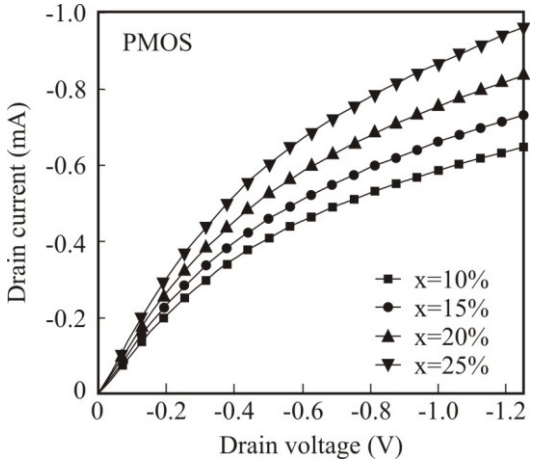

Fig. 8. Drive current enhancement in strained SiGe (S/D) PMOS [31].

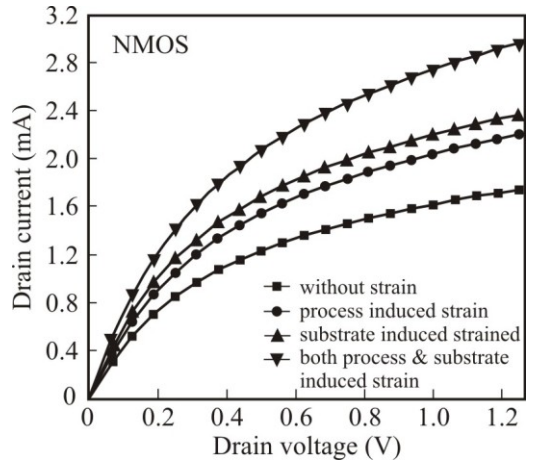

Fig. 9. Drive current enhancement in strained SiGe (S/D) NMOS [31].

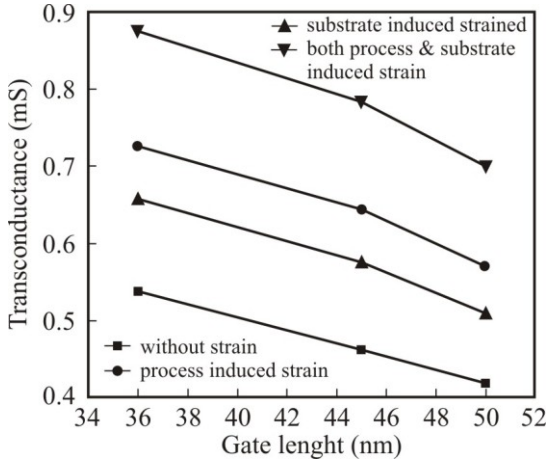

Fig. 10. Transconductance enhancement in strained-Si NMOS [31].

It is particularly interesting to consider the electrical characteristics due to the combined strain, the uniaxial (process-induced) and biaxial (substrate-induced). The combined strain effects for SS NMOS with variable gate lengths (minimum 45 nm) are given in [31], and the performance improvement for more than 62% compared to the conventional NMOS has been shown. Figs 9 and 10 show the combined strain effects on the electrical characteristics of SS MOS.

V. Conclusion

Today, modern CMOS technologies cannot be imagined without the strained layers. These layers will, in the future, for the new CMOS technology nodes, have a much more important role, given the limitations of improvements in the standard CMOS technology and the requirements to maintain high current drive. This role imposes the need to develop methods that strain layers can make more compatible with other innovations that are introduced into the standard CMOS process, regardless of whether it is a new material (e.g. for gate of dielectrics), or new structures (i.e. multi-gate structures). Therefore, future research can move in two directions: the optimal design of strained structures and their implementation, on the one hand, and the robustness of the processes and structures to changing performance, with a high level of reliability, on the other hand.

References

[1] http://www.intel.com/content/www/us/en/silicon-innovations/silicon-innovations-technology.html

[2] D. Harame, J. Komfort, J. Kressler, E. Crabbe, J. Sun, B. Meyerson, T. Tice, “Si/SiGe epitaxial-base transitors – Part I: Materials, physics and circuits”, *IEEE Transactions on Electron Devices*, vol. 42, pp. 455-468, 1995.

[3] S Takagi, *Strain-Si CMOS Technology* in *Advanced Gate Stacks for High-Mobility Semiconductors*, Springer Berlin Heidelberg, 2007, ch. 1.

[4] D.A. Antoniadis, "MOSFET scalability limits and "new frontier" devices," *2002 Symposium on VLSI Technology, Digest of Technical Papers*, pp. 2-5, June 2002.

[5] S. Thompson, et al., "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 um^2 SRAM cell," *2002 International Electron Devices Meeting, IEDM*, pp. 61-64, Dec. 2002

[6] 2010 Edition of the ITRS, http://public.itrs.net/

[7] C.K. Maiti, N.B. Chakrabarti, S.K. Ray, Strained Silicon Heterostructures*: Materials and Devices*, IEE Circuits, Devices and Systems Series, 12, The Institution of Engineering and Technology; 2001.

[8] C. K. Maiti, L. K. Berra, S. Chattopadhyay, “Strained-Si heterostructure field effect transistors”, *Semiconductor Sci. Technology*, vol. 13, pp. 1225-1246, 1998.

[9] M. Currie, “Strained silicon: Engineered substrates and device integration”, *Proceedings of 2004 International Conference on Integrated Circuit Design and Technology*, pp. 261-268, 2004.

[10] K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu, B. S. Mererson, “Extremely high electron mobility in Si/SiGe modulation-doped heterostructures”, *Applied Physics Letters*, vol. 66, pp. 1077-1079, 1995.

[11] Z.-Y. Cheng, M. Currie, C. Leitz, G. Taraschi, E. Fitzgerald, J. Hoyt, D. Antoniadas, “Electron mobility enhancementin strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates”, *IEEE Electron Device Letters*, vol. 22, pp. 321-323, 2001.

[12] S. Dhar, H. Kosina, V. Palankovski, S. Ungersboeck, S. Selberherr, “Electron mobility model for strained-Si devices”, *IEEE Transactions on Electron Devices*, vol. 52, pp. 527-533, 2005.

[13] K. Rim, J. Hoyt, J. Gibbons, “Fabrication and analysis of deep submicron strained-Si N-MOSFET`s”, *IEEE Transactions on Electron Devices*, vol. 47, pp. 1406-1415, 2000.

[14] S. Richard, F. Aniel and G. Fishman, “Band diagrams of Si and Ge quantum wells via the 30-band k p method”, *Phys. Rev. B*, vol. 72, pp. 245316-7, Dec. 2005.

[15] S. Takagi, J.L. Hoyt, J.J. Welser, J.F. Gibbons, “Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal–oxide–semiconductor field-effect transistors”, *Journal of Applied Physics*, vol. 80, pp. 1567-1577, 1996.

[16] M. Rashed, W.–K. Shih, S. Jallepalli, T.J.T. Kwan, C.M. Maziar, "Monte Carlo simulation of electron transport in strained $Si/Si_{1-x}Ge_x$ n-MOSFETs," *1995 International Electron Devices Meeting, IEDM,* pp. 765-768, Dec. 1995.

[17] T. Mizuno, N. Sugiyama, H. Satake, S. Takagi, “Advanced SOI-MOSFETs with strained-Si channel for high-speed CMOS electron/hole mobility enhancement,” *2000 Symposium on VLSI Technology, Digest of Technical Papers*, pp. 210-211, Dec. 2000.

[18] K. Rim, S. Koester, M. Hargrove, J. Chu, P.M. Mooney, J. Ott, T. Kanarsky, P. Ronsheim, M. Ieong, A. Grill, H.-S.P. Wong, "Strained Si NMOSFETs for high performance CMOS technology," *2001 Symposium on VLSI Technology, Digest of Technical Papers*, pp. 59-60, June 2001.

[19] K. Rim, J. Chu, H. Chen, K.A. Jenkins, T. Kanarsky, K. Lee, A. Mocuta, H. Zhu, R. Roy, J. Newbury, J. Ott, K. Petrarca, P. Mooney, D. Lacey, S. Koester, K. Chan, D. Boyd, M. Ieong, H.S. Wong, "Characteristics and device design of sub-100 nm strained Si N- and PMOSFETs," *2002 Symposium on VLSI Technology, Digest of Technical Papers*, pp. 98-99, June 2002.

[20] S. Takagi, T. Mizuno, T. Tezuka, N. Sugiyama, T. Numata, K. Usuda, Y. Moriyama, S. Nakaharai, J. Koga, A. Tanabe, N. Hirashita, T. Maeda, "Channel structure design, fabrication and carrier transport properties of strained-Si/SiGe-on-insulator (strained-SOI) MOSFETs," *2003. IEDM Electron Devices Meeting,* pp. 3.3.1-4, Dec. 2003.

[21] R. Oberhuber, G. Zandler, and P. Vogl, “Subband structure and mobility of two-dimensional holes in strained Si/SiGe MOSFET’s,” *Phys. Rev. B*, vol. 58, pp. 9941-8, Oct. 1998.

[22] H. Nakatsuji, Y. Kamakura, K. Taniguchi, "A study of subband structure and transport of two-dimensional holes in strained-Si p-MOSFETs using full-band modeling," *2002. IEDM International Electron Devices Meeting,* pp. 727-730, Dec. 2002.

[23] M. Uchida, Y. Kamakura, and K. Taniguchi, “Performance enhancement of pMOSFETs depending on srain, channel direction, and material,” *Proc. Int. Conf. Simul. Semcond. Process Devices*, pp. 315-318, 2005.

[24] S. Takagi, T. Mizuno, N. Sugiyama, T. Tezuka, A. Kurobe, “Strained-Si-on-Insulator (Strained-SOI) MOSFETs – Concepts, Structures and Device Characteristics,” *IEICE transactions on electronics*, vol. 84, pp. 1043-1050, 2001.

[25] K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders, G. Walker, Y. Zhang, M. Steen, M. Ieong, "Fabrication and mobility characteristics of ultra-thin strained Si directly on insulator (SSDOI) MOSFETs," *2003. IEDM International Electron Devices Meeting,* pp. 3.1.1-4, Dec. 2003.

[26] J.-S. Goo, Q. Xiang, Y. Takamura, H. Wang, J. Pan, F. Arasnia, E.N. Paton, P. Besser, M.V. Sidorov, E. Adem, A. Lochtefeld, G. Braithwaite, M.T. Currie, R. Hammond, M.T. Bulsara, M.-R. Lin, “Band offset induced threshold variation in strained-Si NMOSFETs,” *IEEE Electron Device Letters,* vol. 24, pp.568-570, 2003.

[27] K. Rim, E.P. Gusev, C. D'Emic, T. Kanarsky, H. Chen, J. Chu, J. Ott, K. Chan, D. Boyd, V. Mazzeo, B.-H. Lee, A. Mocuta, J. Welser, S.L. Cohen, M. Leong, H.-S. Wong, "Mobility enhancement in strained Si NMOSFETs with HfO2 gate dielectrics," *2002 Symposium on VLSI Technology,* pp.12-13, June 2002.

[28] K.W. Ang, K. J. Chui, V. Bliznetsov, A. Du; N. Balasubramanian, M.-F. Li, G. Samudra, Y.-C. Yeo, "Enhanced performance in 50 nm N-MOSFETs with silicon-carbon source/drain regions," *2004 IEDM IEEE International Electron Devices Meeting,* pp. 1069-71, Dec. 2004.

[29] H.S. Yang et al., “Dual stress liner for high performance sub-45nm gate length SOI CMOS manufacturing,” *2004 IEDM IEEE International Electron Devices Meeting,* pp. 1075-77, Dec. 2004.

[30] K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, “Past, Present and Future: SiGe and CMOS Transistor Scaling”, *The Electrochemical Society Transactions*, vol. 33, pp. 3-17, 2010.

[31] S. S. Mahato, T. K. Maiti, R. Arora, A. R. Saha, S. K. Sarkar and C. K. Maiti, “Strain Engineering for Future CMOS Technologies,” *International Conference on Computers and Devices for Communication (CODEC-06)*, 2006.