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Fast carrier recovery in FHSS systems with DDS based Costas loop

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***Abstract*—Owing to fast change of carrier frequency, the usage of coherent demodulation methods in Frequency-Hopping Spread Spectrum (FHSS) communication systems is limited by the coherent state acquisition performed by the local oscillator. To get around this difficulty, it is needed to implement the circuit within the FHSS system that is able to rapidly generate a coherent carrier. The work presented in this paper proposes a realization of Costas loop based on a combination of Direct Digital Synthesis (DDS), (Temperature-Compensated) Voltage-Controlled Oscillator ((TC)VCXO), and Phase-Locked Loop (PLL), which in particular enables a short period (less than 100 μs) required for a local oscillator to reach the coherent state. The implemented model is thoroughly described with measurements results also provided.**

***Index Terms*—Costas loop, DDS, PLL, carrier, FHSS.**

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I. INTRODUCTION

THE carrier signal synchronization is prerequisite for an application of a coherent demodulation method. In coherent communication systems, the technique of carrier synchronization is what drives the receiver structure. In general, there are two types of carrier synchronization techniques.

First type relies on a closed-loop phase which automatically tracks the carrier phase and use error feedback control to minimize the error in the received signal. Costas loop is most commonly used type of a closed-loop for carrier recovery [1]-[4]. This loop is not only adequate for a phase-based tracking of a suppressed carrier, but also for a demodulation of received signals. Therefore, the term 'Costas demodulator' is quite broad. Costas loop can be either analog or digital.

Second type relies on an open-loop phase with direct estimation of a phase error. Open-loop phase and frequency synchronization schemes are based on either the Maximum Apriori (MAP) or Maximum Likelihood (ML) parameter estimation principles. These are general feedforward techniques where the signal parameter is actively estimated and then treated as statistic for a detection algorithm [5].

The feed-forward compensation algorithm with direct phase offset estimation using in-phase and quadrature-phase demodulator outputs is presented in [6]. The feedback compensation algorithm with carrier synchronization that compensate a phase offset using the feedback loop, and signal conversion to baseband performed by the receiver, is described in [7]. Lately, turbo synchronization time and frequency based methods have emerged. Turbo synchronization using an iterative Expectation-Maximization (EM) algorithm used to estimate carrier phase, frequency offset or timing within a turbo receiver is proposed in [8]. More specifically, carrier phase estimation within a turbo receiver in BPSK (Binary Phase Shift Keying) and QPSK (Quadrature Phase Shift Keying) systems is described in [9]. Turbo decoders involve significant mathematical operations which restricts their use in FHSS systems. Previously mentioned techniques use either feedback-loop with very small noise bandwidth or feed-forward schemes which use training-sequences or symbol sequences in order to perform the time and frequency synchronization. These techniques might have relatively long acquisition time, and are not adequate for carrier synchronization in systems with short data packets.

Previous analysis demonstrates that fast carrier recovery has not been prioritized research activity. The fact that FHSS systems almost exclusively use incoherent demodulation methods proves our statement. Unlike the related work, this paper proposes a solution based on Costas loop, which enables fast carrier recovery. Proposed and implemented solution has the potential to be used for coherent demodulation in FHSS systems.

II. PROPOSED MODEL

Costas loops are being used in analog and digital communication systems for carrier synchronization. Moreover, Costas loop can be used for carrier recovery from double-sideband suppressed carrier signals. A circuit scheme of classical Costas loop used for coherent demodulation of BPSK

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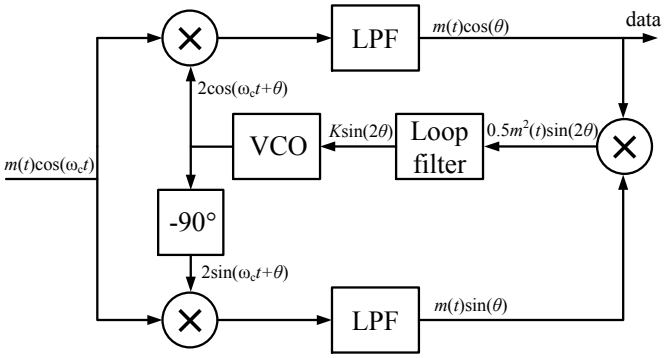

Fig. 1. A classical circuit scheme of Costas loop.

signals is shown in Fig 1.

The input signal is RF BPSK modulated signal $m(t)\cos(\omega_c t)$, which is a product of the transmitted data $m(t)=\pm 1$ and the high frequency carrier $\cos(\omega_c t)$, where $\omega_c = 2\pi f_c$, and f_c denotes input signal carrier frequency. The sinusoidal voltage-controlled oscillator (VCO) signal is represented by $2\cos(\omega_c t+\theta)$, where θ is an implicit time function representing the portion of total signal phase not included in $\omega_c t$. On the upper branch the input signal is multiplied by the output signal of VCO, and signal $m(t)\cos(\theta)$ is obtain at the output of low-pass filter (LPF). On the lower branch the input signal is multiplied by the VCO signal, shifted by –90°, and then low-pass filtered obtaining the signal $m(t)\sin(\theta)$. Signal of form $0.5m^2(t)\sin(2\theta)$ is obtained after both branches being multiplied together. This signal is then filtered by the loop filter in order to provide control signal $K\sin(2\theta)$, which is used to adjust VCO frequency to the frequency of the input signal carrier. By reducing the phase error to zero, the VCO signal is synchronized with the carrier, and demodulated data are obtained on the upper branch. Thorough analysis of Costas loop with the noise influence on the loop performance can be found in technical literature.

The proposed Costas loop is based on direct digital frequency synthesis (DDS) and voltage-controlled crystal oscillator (VCXO), as shown in Fig. 2. The VCO and phase shifter in the classical model given in Fig. 1, is replaced by DDS and VCXO. The VCXO or temperature-compensated voltage-controlled crystal oscillator (TCVCXO) is used as a reference clock for DDS. The TCVCXO is more temperature stabile than VCXO resulting in a lower frequency mismatch between the input signal carrier and DDS output signal. Therefore, this configuration has a lower acquisition time. In addition, DDS allows faster frequency change when used as a local oscillator (LO). It can output two signals whose frequencies and phase difference can be adjusted with very high resolution (order of mHz and less than degree, respectively). Due to high frequency and phase resolution, in-phase and quadrature-phase signals can be provided by a single DDS chip.

The main advantage of this model of Costas loop is the ability to generate very fast and precisely both in-phase and quadrature-phase signals in complete DDS operating range.

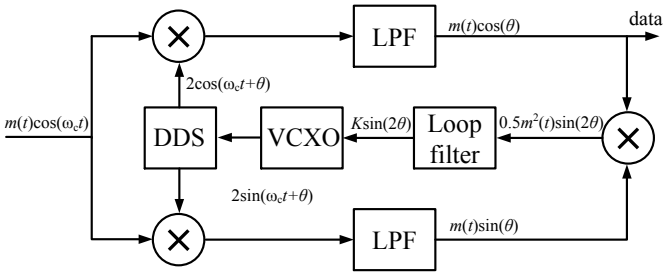

Fig. 2. A circuit model of Costas loop based on DDS and VCXO.

This allows the usage of Costas loop in reconfigurable radio and FHSS systems. In-lock state of the Costas loop is achieved when there is no frequency and phase mismatch between input signal and DDS output signals.

Considering fixed frequency scenario, the mean acquisition time T_{acq} consists of phase recovery time T_p and frequency recovery time $T_{\Delta f}$ [10]. For the second order PLL, it is given by

$$T_{acq} = T_p + T_{\Delta f} = \frac{4}{\omega_n} + \frac{4.2(\Delta f)^2}{B_L^3}. \quad (1)$$

where ω_n denotes PLL's natural frequency, B_L is PLL's bandwidth, and Δf is initial frequency mismatch. One can see that the frequency recovery time is proportional to the square of frequency mismatch. Phase and frequency recovery (locking) times as a function of frequency difference between the input signal carrier and local carrier are given in Fig 3.

Practical VCOs can have frequency mismatch of several kHz or MHz, which would have negative impact on frequency acquisition time. When there is no input signal, TCVCXO will oscillate at the frequency of crystal oscillator. Due to its relatively high temperature stability (0.28-2 ppm), DDS can be set very close to nominal frequency of the input signal carrier. This way, during the acquisition process, TCVCXO will reduce the frequency mismatch very fast, while phase recovery time would depend on natural frequency ω_n. For example, considering TCVCXO with frequency stability of ±1 ppm and

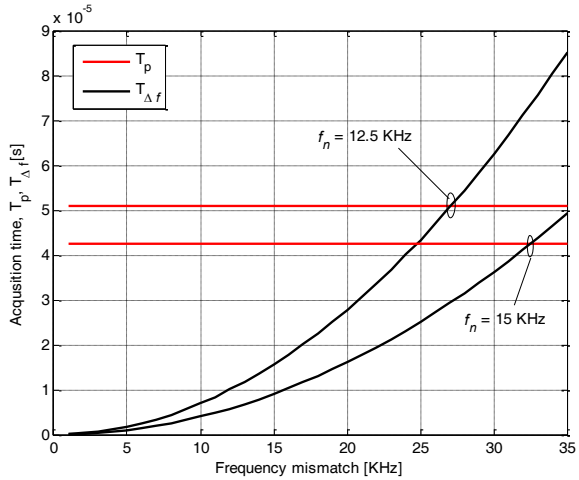

Fig. 3. Phase and frequency acquisition times.

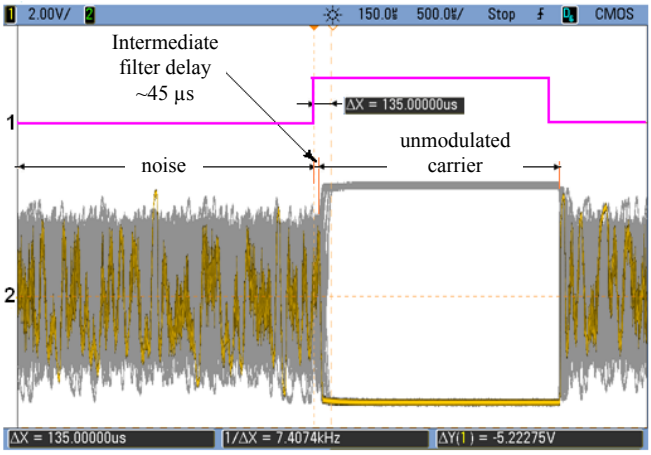

Fig. 4. Coherent state acquisition in Costas loop.

nominal frequency of 100 MHz, maximal frequency difference between the input signal carrier and local carrier is Δf = 200 Hz. For the second order PLL with natural frequency $f_n \approx$ 12.5 KHz, damping factor $\xi \approx 0.7$, and $B_L = \omega_n/2(\xi+1/4\xi) \approx \pi f_n$ = 39.2 KHz, time need to reduce frequency error can be assumed negligible, while mean phase acquisition time is 51 µs. Frequency recovery time gets higher with the increase of frequency difference, and becomes the same as phase recovery time for Δf = 27 KHz. With further increase of input signal carrier and local carrier frequency mismatch, the frequency recovery time becomes larger than phase recovery time.

The above analysis is referred to the fixed frequency scenario. In frequency agile systems, such as FH radios, where an agile local carrier is required, maximal frequency mismatch is equal to overall available bandwidth. In this case, if VCO is used as a local oscillator, frequency acquisition time would be very high. However, in the model with DDS and TCVCXO, the frequency acquisition time is negligible compared to the time needed for phase recovery. Using higher natural frequency, thus allowing additional noise, one can reduce the loop-locking time. However, more noise power is causing abrupt change of phase of local carrier during the transmission, which further causes change of polarity of demodulated signal. Therefore, PLL should have greater natural frequency during

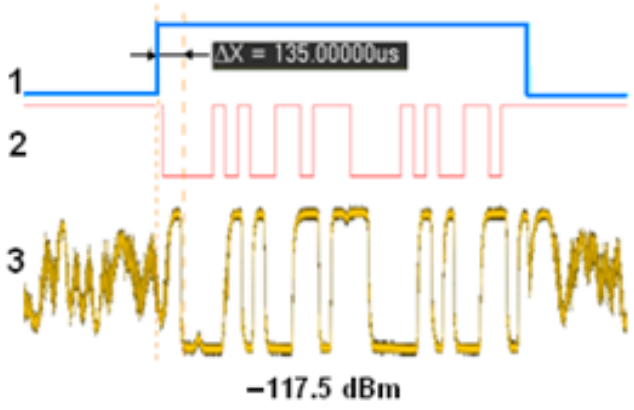

Fig. 5. The control signal (1), sequence (2) and demodulated signal (3).

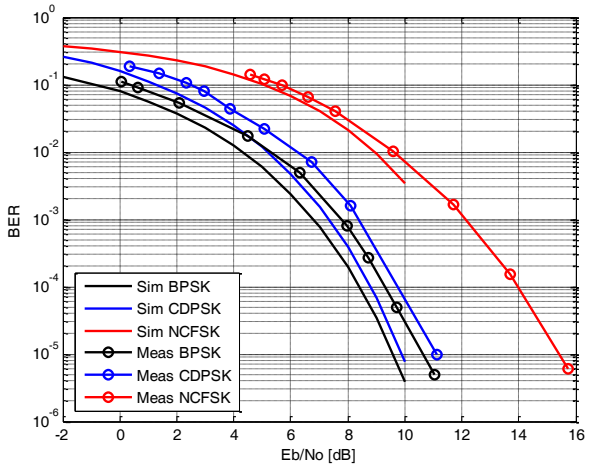

Fig. 6. BER as a function of E_b/N_0.

the acquisition and a lower natural frequency afterwards. However, a proper moment of switching from one value of natural frequency to another is not an easy task, especially at low signal-to-noise ratios, which may be the subject of a future research.

III. Measurements Results

Fig. 4 shows PLL coherent state acquisition time with natural frequency $f_n \approx$ 12.5 KHz and damping factor $\xi \approx 0.7$. In order to measure the time period of interest, an input burst on-off keying (OOK) signal is used, as well as the VCXO. Signal 1 in Fig. 4 represents the modulating signal, whereas signal 2 represents in-phase component of demodulated signal in Costas loop. As notable from the figure, carrier demodulation is finalized within 135 µs. Reducing this value by the 45 µs delay of an intermediate frequency filter, one gets the coherent acquisition time of Costas loop. Given the aforementioned parameters and the frequency mismatch between the local and received signal of Δf = 1 KHz, the time needed to acquire coherent state (acquisition time) is less than 100 µs.

Fig. 5 shows demodulated signal when RF signal level is set to -117.5 dBm. The modulating signal is given in a form of the short pseudo random (PN) sequence, making the receiving RF signal in a form of a burst signal, which is quite typical for radars and FHSS systems. For proper demodulation of first receiving bits from the PN sequence, it is required that the phase loop is in its coherent state. This means that the transmitter should start emitting the carrier before information data (or sequence) is being sent.

Minimal carrier emitting time corresponds to loop-locking time (acquisition of coherent state), which is less than 100 µs, as stated before. It is demonstrated that the fast carrier generation at the transmitter is feasible [11], while keeping the phase noise and spurious signals at low level.

Theoretical and measured bit-error-rate (BER) as a function of signal-to-noise ratio (E_b/N_0) for BPSK, Coherent Differential PSK (CDPSK), and incoherent Frequency Shift Keying (FSK) is shown in Fig. 6. Measured BER for BPSK modulated signal is slightly worse relative to the theoretical

BER for BPSK modulated signal (≤ 1dB). Nonetheless, Fig. 6 illustrates that coherent demodulation of BPSK modulated signal significantly outperforms incoherent demodulation of FSK modulated signal. As we already stated, to reduce the acquisition time, it is required to broaden the loop bandwidth (larger ω_n). However, this leads to an increased power of the noise. The trade-off between the time of the coherent state acquisition and BER might be in usage of the coherent detection of the differential PSK (CDPSK) signal, whose theoretical and measurements results are presented in Fig. 6. Due to the difficulties observed in carrier phase tracking in FHSS communication system, incoherent FSK and Binary Frequency Modulation (BFM) are mainly deployed. Using BPSK modulation technique in these systems, however, requires extremely fast acquisition time at the beginning of each hop interval.

IV. Conclusion

In this paper a model of the Costas loop based on direct digital synthesis and phase-locked loop has been proposed and analyzed. Results of the measurement have confirmed a high performance of the model in terms of acquisition time and bit-error-rate at low signal-to-noise ratios. The proposed model has showed a very fast carrier recovery time (less than 100 μs), and when combined with CDPSK modulation, it allowed coherent demodulation in FH radios. CDPSK had up to 3-4 dB better performance by means BER relative to NCFSK. Finally, the proposed model of carrier synchronization can be applied in reconfigurable radio systems.

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Modeling Method of Finite Element Modeler and Electromagnetic Solvers for Education and Research in RF MEMS

Tejinder Singh, Wael M. El-Medany and Kamal J. Rangra

***Abstract*—Field of electronics engineering is the most captivating among students, researchers and academicians now-a-days. With the passage of time the requirement of advance tools for engineering is increasing. Many institutions and universities around the globe provide quality education to various engineering domain. Students although study theory courses but they also need exposure that how theory can be related to actual devices. Simulations play an important role for relating theoretical components to the virtual practical environment. Students of Radio Frequency (RF) domain and especially students that are studying Microelectromechanical Systems (MEMS) as courses, due to the extreme complexity of these devices, students need multiple tools to simulate the performance parameters. This paper highlights the most prominent tools that are used in the industry to design and implement RF MEMS structures. The role of Electromagnetic (EM) solvers and Finite Element Modeller (FEM) and its impact on electronics engineering education is demonstrated. Modeling approach of these tools are also explained. These tools and due to there huge advantages, electronics graduates should study these tools in their course curriculum to know how to tackle various types of RF problems and through case studies, it is demonstrated that how these tools can aid shift from just theoretical study to virtual practical environment.**

***Index Terms*—EM solver, FEM, electronics engineering, education, simulation environment.**

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I. Introduction

MANY a times, graduate engineering students or graduate research students face variety of challenges in designing and modeling the problems that are spanned in multiple disciples of engineering and applied sciences [1]. Streamlined computational methods and techniques that combine the technologies and that can handle engineering problems are required to precisely model the issues and accurately predict results before manufacturing or fabrication [1], [2]. Most of the electronic engineering programmes offer domain specific simulation and modeling methods on a very limited basis.

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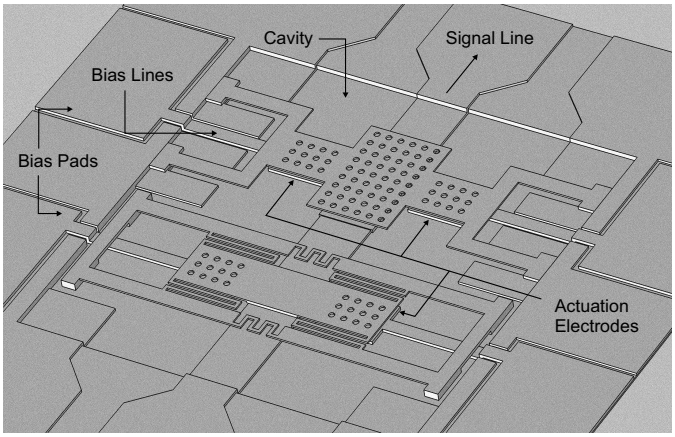

Fig. 1. T. Singh [5] proposed the RF MEMS switch based on series-shunt configuration, both membranes are incorporated inside the cavity. Bias pads demonstrate the actuation signal routing beneath the membranes. [Copyright © 2014, Springer Science, NY]

Our primary focus is on group of graduates that are into RF MEMS/antenna designing. RF MEMS [3] is a very fast growing field of research. Students usually face challenges in modeling and simulating RF MEMS systems [4]. We have encountered many questions on technology forums and through emails, students that just entered into this industry wonder that which tools are most prominent for simulating these micro structures.

Fabricating RF MEMS devices [6], [7] is a cumbersome process, hence simulations is the best bet to get approximate near to actual response. Theoretically it said that RF MEMS systems show excellent performance like high isolation and low insertion loss. But, to model the response, complex mathematical derivations need to be solved prior to check performance. EM solvers, provide comprehensive solution to all these RF or microwave related issues. Including, radiation field analysis, near and far fields, *S*, *Y* and *Z* parameters to name a few. If taught as core curriculum with hands on experience with these tools, fresh grads can usher in the industry. FEM on the other hand solves multi domain physics problems and provide solutions as per the requirement. Hence, companies are now opting for multi-physics modeling or finite element modeller (FEM) [8], [9] to save costs and to reduce computing resources. One tool can handle various physics problems. By this way, students not only learn their field specific solvers, instead they also get experience to couple various

physics problems that may include, particle trajectories, flow analysis, damping analysis, stress or fracture analysis, doping concentration, charge flow and many more. Universities should focus on these issues and add finite element modeling in the course curriculum of graduate engineering students [2], [10].

Basically, FEM environment require the basic knowledge of the problem that one is going to tackle as a prerequisite. Once, the governing equations of the problem is provided, then using FEM computation methods, the FEM, thus ask for boundary conditions and finally computes those governing equations for specified boundary conditions [1], [4], [11], [12]. It takes a very little time if the basics are strong and clear. EM solvers are a boon to RF engineers, couples with FEM is just icing on the cake. These tools takes the theoretical inputs and do all the simulation and testing in between the framework of theory to actual development.

Engineering curricula in good universities offer design and research experience of various tools to better teaching and practical exposure. An electronics graduate student may require FEM techniques to solve electric field issues as well as overall device level issues like mechanical stresses or chemical process if the system is on same chip or base. This paper presents the need of these tools as an electronics engineering graduate course curricula that should covers the most of the methods and techniques relating to theory courses [11], [12].

Mostly, graduate engineering students become active participants in concept based learning than their theory counterparts. More generally, These tools not only teach them how to solve physics problems but also make them understand in very efficient manner. The introduction of the concept (need of simulation methods as a course) is explained in introduction followed by a section on impact of research tools on education and core technologies behind these tools. The statements are supported by our prior research work, by providing two case studies, in which Section IV, covers RF performance simulation using commercially available EM solvers followed by Section V, that reports the use of FEM on the design and analysis of RF MEMS. We have provided simulation process flow in Section III as well. The concluding remarks are given in Conclusion section.

II. Impact of Research Tools on Education and Core Technologies

There are many industrial grade tools for simulation depending on the problems. Now-a-days, tools are developed that we can also couple the physics from different domains for analysis [4], [13]. Modeling tools provides an environment for engineers in which they can design, analyse/simulate, compare the results and optimise various factors depending on the type of application [14]. Students after their engineering education, definitely look for engineering jobs. It is always advantageous for students to learn and practise these tools in whichever field they want to pursue their careers [15].

Our primary focus of this paper if for the graduates, who are studying antennas, RF engineering, microwave engineering, microelectromechanical systems or micro systems course in their curriculum, can get advantage to implement the theoretical designs and concepts in these tools. Thus by this methodology and practise graduates not only learn in an efficient manner, but also can understand better and comply with the industry requirements. Many a times, students face the issues that what to do with the mathematical formulas, that they are studying as theory [15]. Even in our classes, during lecture delivery, we show them the simulations that how those mathematics come into picture when we solve real world problems.

Universities might not have industrial grade testing labs or research centres, but either a lab related to the research tools or simulations along with lecture delivery can make students learn and understand in an efficient way. As, we have implemented this methodology from last few months, we have seen that students now learn and understand mathematical concepts in better way. They remember the things if we relate it to real world problems.

In this paper, we provided two case studies, that clearly relates the use of engineering tools, specially EM solvers and FEM in the field of Antennas, microwave theory and the most prominent research area RF MEMS.

A. Aid of Simulation Tools

As discussed in the previous section, we have designed an RF MEMS switch and relating the computed parameters from mathematical formulas to implementing in EM solver and FEM to check how accurate these tools are and how these tools can save abundant of time.

Solving partial derivatives and many other complex mathematical equations are not practical for engineering field. Such tools provide, ready to use solving algorithms and provide the results that are very close to the actual solutions. Simulations act as a mid way in between theory to development. It plays a very crucial role, providing ample space to optimise and check the solution to the problem.

In RF industry, performance and size of the devices are limiting factor especially for RF MEMS [16], [17]. For RF MEMS Switches, scattering parameters are analysed to check its RF performance. Other that that we are interested in how E field and H field of RF signal travels in the RF MEMS switches or subsystems. Then there comes the analysis of current density, J, temperature, leakage, resistant, capacitance, inductance, q-factor to name a few. That can be easily simulated in commercially available EM solvers like Ansys HFSS, Sonnet, CST Microwave Studio, EM3D and many more. These are many different types of EM solvers available in the market based on requirements.

Then to check the issues like stress gradient, voltage requirement, spring constant, switching time, damping, fracture analysis etc, finite element modeller are used. FEM like COMSOL or Ansys Workbench provides sophisticated solution in a close proximity to the real world fabricated designs. FEM divides the problem into finite elements of very small or desired size called the *Mesh* and solve the governing equations relating to that particular problem.

Fabricating RF MEMS switches and subsystems needs million dollar machinery, time, knowledge and engineering. Hence, these tools before going into actual experiment or

fabrication run, provides relatively exact solutions. That saves time and money, thus increase productivity.

Students, if they would be knowing the tools before entering into industry, they can perform better and their initial performance in industry would be impactful on peers.

Briefly, in the following sections, we have presented the Series-Shunt based RF Switch, we have analysed the RF performance and Stress distribution. The comprehensive study of the RF MEMS switch is given in [5]

III. Simulation Process Flow and Design Properties

Till now, We have discussed that simulation represent an invaluable link between theory and practice in modern engineering. In this section, the simulation process flow is demonstrated.

A. Process Flow using Ansys HFSS

1) Geometry: Geometry can be created in 3D environment layer by layer. After setting the units to appropriate scale, one can start designing the geometry of product (RF MEMS Switch as used in this case). Geometry can be imported or exported in variety of formats to exchange with different simulation tools.

2) Material Assignment: After creating the geometry, material has to be assigned to different layers, as an example, bulk of Silicon (Si), is used mostly followed by a deposition of dielectric layer of different material. Once the material selection is complete, one can proceed to next section.

3) Ports Excitation: I/O Ports have to be assigned. We have to design the CPW lines to characterise it for 50 ohm for ease in coupling with coaxial cables. In this case study, typically for RF MEMS Switch, we have used Port 1 and Port 2 as input and output port with Wave Port assignment to both ports.

4) Analysis Setup: After setting up the model, we have to setup analysis. We have provided a linear frequency sweep of DC to 40 GHz with step size of 0.1 GHz to simulate RF performance of the designed switch. We have used smaller step size to get precise results. Although, less the step size, can affect computation time. Although, this tool provides the provision of High performance computing concept, such that we can use all the licenses available with us to get results in less time. Parts of the projects is usually simulated by using the computation power of different machines and then it automatically combine the results in host machine.

5) Checking the Results: After the completion of analysis, results can be plotted using Rectangular 2D plot option. Then, we can easily check the performance of switch while plotting S11 as Return loss [dB] and S21 as Isolation [dB] of the switch.

B. Process Flow using COMSOL Multiphysics

Although, Multiphysics environment provides, realistic approach to solve various physics problems. We can couple the physics to get best of both worlds. But, just to highlight the advantage of EM solver, we have simulated RF performance in Ansys HFSS and mechanical modeling in COMSOL Multiphysics. RF performance can also be simulated using COMSOL Multiphysics only. But, from our experience, it takes much more time to compute the same problem, thus we have chosen HFSS as our dedicated EM Solver.

1) Geometry: We have to check the mechanical issues like stress gradient, spring constant and pull-in voltage required to deflect the beam for particular gap height, g_0. We have to set the units to micrometers. In this, we need only metal membrane instead of complete geometry to ease the computational load. Hence, we imported membrane only in multi physics environment to start investigating the issues further.

2) Material Assignment: In COMSOL, huge library of materials is already provided with details like Poisson Ratio, Elasticity, Permittivity, Permeability, Density, Young's modulus, thermal coefficient and many more. We then assigned "*Au*" material from category MEMS, as the only material for this switch membrane.

3) Physics: We have chosen, Electromechanics (emi) physics and stationary study for this particular problem. This physics allows to compute pull-in voltage and deflection of membrane.

4) Boundary Conditions: For this model, we have assigned inner membrane as Linear Elastic Material, while the fixed constraints are bottom side anchors of membrane. Then, we have to choose Boundary Load and we have applied boundary load as Contact Pressure as a predefined variable followed by Prescribed Mesh Displacement. At last, we have applied boundary conditions: Voltage Terminal and Ground Terminal.

5) Mesh: COMSOL Multiphysics offer physics controlled mesh depending on the complexity of geometry or we can optimise the mesh to reduce computation time. for this model, we have chosen Mapped mesh and Swept the mesh in complete geometry.

6) Solver: COMSOL offer variety of solvers, but we have optimised the solver for our model. We chose Full couples solver and under Method and Termination section, we chose Nonlinear method to select Automatic (Newton). Finally under "Direct" option, we chose PARDISO solver.

7) Computation and Results: After setting up the model, we computed it and plotted the results as desired in Results section. In that section, we can plot 3D, 2D or 1D results depending on the requirement.

The correctness of simulation results with experimental results can be seen from the work of [3], [18], in which researchers have fabricated the designs and compared the performance.

IV. Case Study I - RF Performance Estimation using EM Solvers

The most critical parameter for any RF system or device is to analyse its RF performance. RF performance is the most important factor that primarily shows the performance of MEMS that it is intended for. The isolation loss, return loss and insertion loss of the RF MEMS switch is simulated using commercially available EM solver Ansys HFSS. RF performance of the switch is observed between frequencies 1 to 40 GHz. Fig. 2 shows the peak isolation S_{21}, of 75 dB at 28 GHz in OFF state, although the switch has very large

bandwidth of 30 GHz, i.e., it can be used for K–Ka band applications. From the results, the performance of switch is excellent for said frequency bands. Two bandwidths a and b are considered, Bandwidth a is 30 GHz and has the complete frequency range of K and Ka band that shows more than 60 dB of isolation and bandwidth, b is 7 GHz narrow bandwidth that shows excellent isolation of above 70 dB from 25 GHz to 32 GHz. The solution to the RF problems thus can easily be solved by using EM solver as demonstrated [19].

Numerically the S–parameters S_{11}, S_{21} in both switching states can be computed using the Y and Z–matrix data from EM solver and by plugging the values in equations given below. To determine the ON state parameters, Y_{11-x} is required, where $x = 1$ for switch in ON state and $x = 0$ for switch in OFF state.

$$S_{11-x} = \left(\frac{Y_z^2 - Y_{11-x}^2 + Y_{21-x}^2}{(Y_{11-x} + Y_z)^2 - Y_{21-x}^2} \right) \quad (1)$$

where S_{11-x} is the ON or OFF state return loss depending on the variable x, $Y_z = 1/Z_0$, $Y_{11-x} = j\omega C_{down}$ for $x = 0$ i.e., in OFF state and $Y_{11-x} = j\omega C_{up}$ for $x = 1$ i.e., in ON state. $Y_{21-x} = -j\omega C_{down}$ for $x = 0$ and $Y_{21-x} = -j\omega C_{up}$ for $x = 1$ i.e., in OFF and ON state respectively. Isolation S_{21-0} and insertion loss S_{21-1} can be analysed by using

$$S_{21-x} = \left(\frac{-2Y_{21-x}^2 Y_z}{(Y_{11-x} + Y_z)^2 - Y_{21-x}^2} \right) \quad (2)$$

For the switch in ON state, the return loss, S_{11} and insertion loss, S_{12} is computed. Fig. 3 shows the return loss of 24 dB and Fig. 4 shows low insertion loss of 0.13 dB at 28 GHz with markers for complete 30 GHz bandwidth for K and Ka bands.

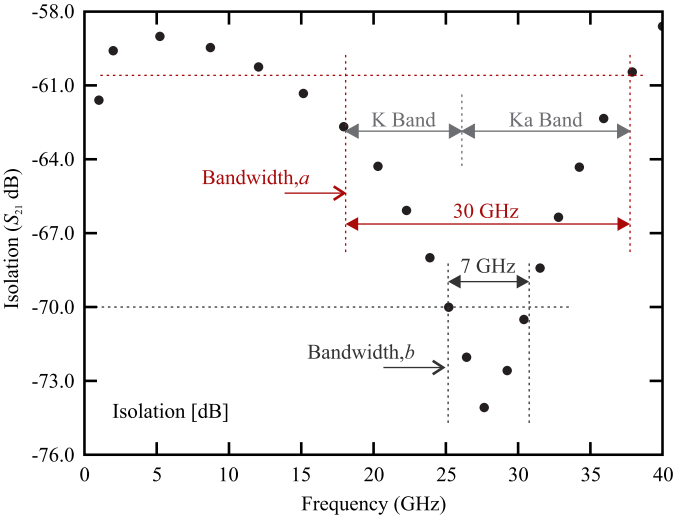

Fig. 2. Simulation of Isolation [dB] performance for combined switch in series–shunt configuration. The simulation is done for frequency sweep of 1–40 GHz and results in maximum peak isolation of 75 dB at 28 GHz. Two bandwidths are considered for this switch, Bandwidth (a) 30 GHz is very large with above 60 dB of isolation and bandwidth (b) 7 Ghz has excellent isolation of above 70 dB. Parameters are for the RF MEMS switch shown in Fig. 1, courtesy T. Singh [5]

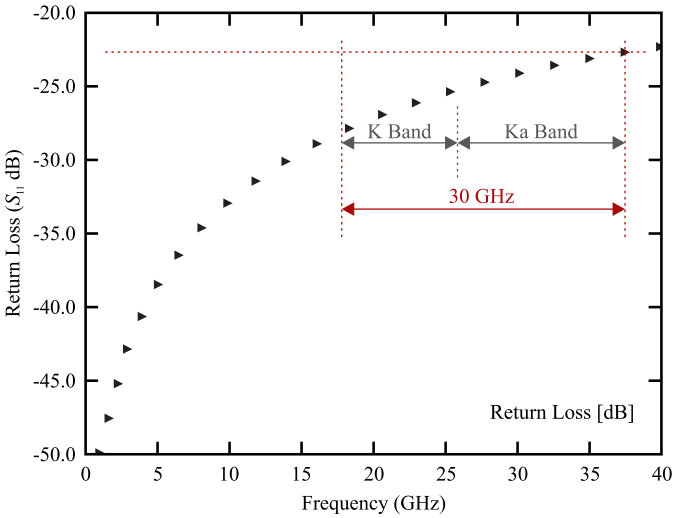

Fig. 3. Return loss [dB] for switch in series–shunt configuration. The simulation results are analysed for frequency sweep of 1–40 GHz and demonstrates the maximum peak return loss of 50 dB at 1 GHz and 24.5 dB at 28 GHz.

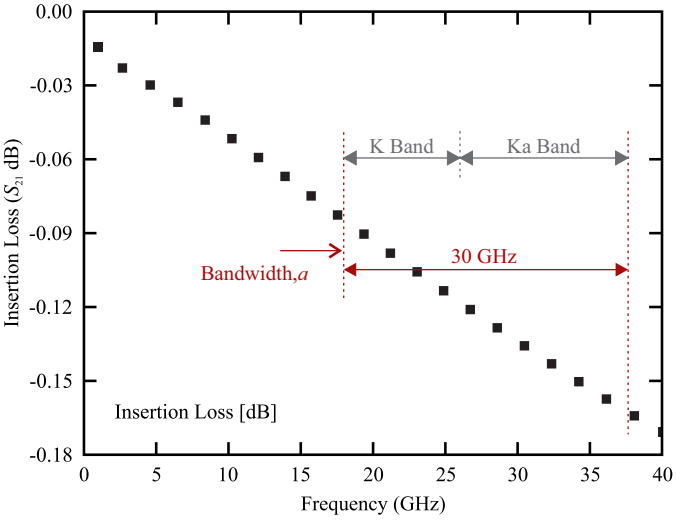

Fig. 4. Insertion loss [dB] simulation for complete switch in series–shunt configuration. The simulation is carried out for frequency sweep of 1–40 GHz and demonstrates the maximum peak insertion loss of 0.015 dB at 1 GHz and 0.13 dB at 28 GHz.

V. Case Study II - Finite Element Modeling for RF-MEMS

RF MEMS switches or subsystems are highly regarded for their better RF performance in microwave regime than their semiconductor counterparts. RF MEMS switches have huge advantage including; excellent isolation, low insertion loss, negligible power consumption, very compact structure, low cost of manufacturing [20]. But these tiny intelligent devices suffer from reliability issues including stiction and high voltage requirements [13], To overcome these problems, researchers and designers has to model and analyse the issues first and then optimise the design accordingly. In this case study, we have reported that how FEM is useful in estimating the stress gradient to help determining how the membrane of RF MEMS can handle stress for reliable operation [5].

The design and modeling parameters are reported in [5], [20]. We have presented the stress analysis for two different membranes. We have also reported the spring constant estimation and pull-in voltage analysis of these switches by using FEM. Although, RF performance is analysed by EM solver and is given in the previous section. There is a need of FEM (Finite Element Modeling) to check various parameters before fabrication of devices [16]. For this proposed switch, the spring constant, stress and pull-in voltage required for actuation is analyzed as discussed in [5], [20]. COMSOL Multiphysics is used as finite element modeler for analyzing the parameters [17], [20]. This section deals with the coupled physics, electrostatic + magnetic problem solving. Analytical calculations of spring constant for complex structures are not possible, because the formulas presented till now are for simple beams or for beams with simple meanders. The complex geometries can be better analyzed using FEM. To calculate the spring constant and stress in membranes, sweep of force is applied over the area of electrodes. Both the membranes are analyzed one by one for the same force and displacement sweep.

As the membranes are made of gold, the gold can withstand stress of 100 MPa and it fails for values higher than that. The effective stress can be seen in membranes from Fig. 5 and 6 respectively. The von Mises stress analysis is mandatory to check the maximum stress level. If the maximum stress increases for a given gap height from the stress a material can withstand, then it is an alert for failure in design. But the redesigned membranes can withstand stress for assigned gap height and have margin to take twice of more stress. The ohmic membrane is designed to reduce the spring constant and stress. The side view of ohmic membrane is shown in Fig. 7. It depicts that the sides of membrane are not making any contact with signal line and it helps to keep the inner membrane straight for better contact and better switching speeds. It increases the reliability of switch as well. The spring constant for ohmic and capacitive switch membranes are shown in Fig. 8

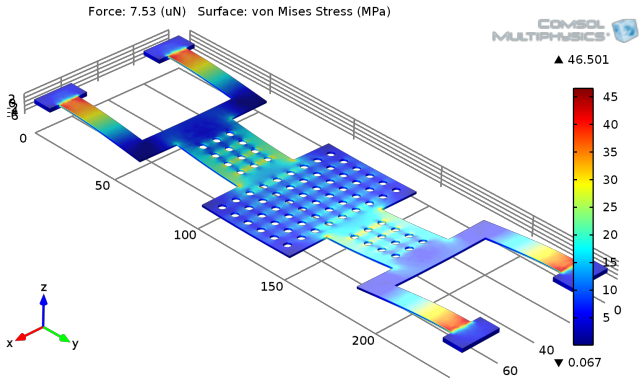

Fig. 5. Capacitive / Shunt switch membrane stress analysis for 2.5 μm gap height, showing maximum stress of 46.5 MPa. [Copyright ©2014, Springer Science, NY]

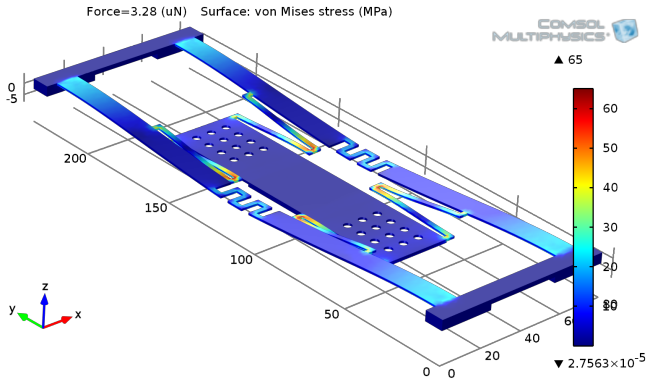

Fig. 6. Results by T. Singh [5] Ohmic / Series switch membrane stress analysis for 3 μm, showing maximum stress of 65 MPa. [Copyright ©2014, Springer Science, NY]

The actuation voltage is analyzed by plotting a curve of applied voltage vs. deflection of beam. The voltage required for desired gap height is shown in Fig. 9. The ohmic switch membrane works properly on 3 μm gap and capacitive switch membrane on 2.5 μm. The pull–in voltage required is same for both membranes as shown in plot.

Theoretically, determining the fundamental mode of operation is also required for certain analysis. The equation of motion of the thin metal beam that is under harmonic force is considered. In single degree of freedom, the harmonic motion of the mass-spring system is fundamentally modelled with the 2$^{\text{nd}}$ order differential equation as

$$m_{\text{eff}}\frac{\mathrm{d}^2x}{\mathrm{d}t^2}+\gamma_{\text{eff}}\frac{\mathrm{d}x}{\mathrm{d}t}+k_{\text{eff}}x=F_e \tag{3}$$

where m_{eff} is the beam's effective mass, γ_{eff} is the effective coefficient of damping of dielectric material, F_e is the electrostatic force and k_{eff} is the effective spring constant. m_{eff} is of gold material, effective mass of inner movable beam i.e., 8.52 ng. Effective spring constant k_{eff} is composed of k' and k''. According to [3] the component of biaxial residual stress k'' can be neglected due to the crab type flexures design, perforation i.e., holes are added to release the biaxial residual stress in membrane. γ_{eff} can be estimated by computing Eq. 3 by fitting all the remaining values.

The spring constant is simulated for the membrane and shown in Fig. 8. For the serpentine flexures, the numerical values of spring constant can be analysed by using

$$k'\approx\frac{48GJ}{l_a^2\left(\dfrac{GJ}{EI_x}l_a+l_b\right)n^3}\quad\text{for } n\gg\frac{3l_b}{\dfrac{GJ}{EI_x}l_a+l_b} \tag{4}$$

where n is the number of meanders in the serpentine configuration, $G=E/2\,(1+v)$ is the torsion modulus, $I_x=wt^3/12$ is the moment of inertia, and the torsion constant is usually

Fig. 7. Vertical defection in ohmic switch membrane showing deflection in Z–direction, from this side–view image, the straight contact over signal line and contact area on electrodes can be seen.

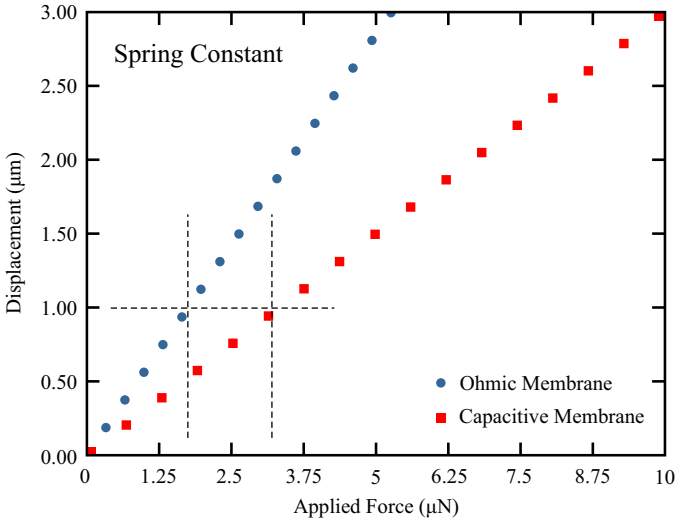

Fig. 8. Spring contact analysis for ohmic and capacitive switch membranes for displacement sweep of 0.3 – 3.3 μm vertical displacement in Z–direction

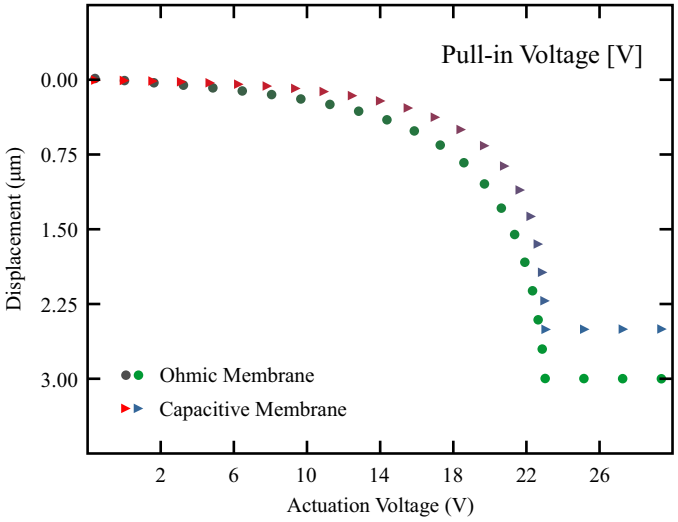

Fig. 9. Simulation of actuation voltage requirement by series and shunt membranes. The voltage is simulated for the maximum 3.5 μm displacement. The maximum voltage required are optimized to use same potential for different gap height of 2.5 μm for series and 3 μm for shunt membrane.

given by

$$J = \frac{1}{3}t^3 w \left(1 - \frac{192}{\pi^5}\frac{t}{w}\sum_{\substack{t=1,\\ i=odd}}^{\infty}\frac{1}{i^5}\tanh\left(\frac{i\pi w}{2t}\right)\right) \quad (5)$$

The effective spring constant k_{eff} can be determined by plugging material values like Young's modulus E and moment of inertia I_x in Eq. 4. The combined spring constant k_{eff} for the membrane is 1.5 N/m for ohmic and 2.7 N/m for capacitive membrane.

The natural frequency of the membrane depends on the equivalent spring constant and the effective mass, the natural frequency f_0 is given as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_{\text{eff}}}{m_{\text{eff}}}} \quad (6)$$

Next higher mode of eigenfrequency f_1 can be determined by using

$$f_1 = \frac{1}{2\pi}\left[\frac{15.418}{L^2}\right]\sqrt{\frac{EI_x}{\rho}} \quad (7)$$

where; ρ is the mass density (mass/length), L is length of membrane

VI. Assessment Results

To check the understanding of concepts by introducing simulation environment to students, we have conducted a survey of 3 Grad classes and 2 Undergrad classes. While, teaching the subject RF MEMS theoretically, we have presented the simplistic flow of simulation and explained its use among students. They students first of all became more attentive in the class, and whatever they have learned using tools i.e., results computed using simulation environment were more regarded by students. A simple exercise of comparing the simulation results with analytical results provides a good method of learning among students. They started relating the numerical concepts in correct manner. By teaching using simulations, brain become more attentive to see the actual working of analytical equations on products/designs. Students tend to learn and understand things faster.

We have conducted a survey by demonstrating few simple electromagnetic related problems and their computed solutions by numerically and using computationally, and finally found that more than 90% of undergrad and grad students wanted faculty to teach using these kind of tools for their better understanding. We then taught about a simple physics problem numerically or analytically in one section consisting more than 60 students with their average academic standing of grade A. Simultaneously, we taught about same physics problem by introducing simulation tools to the students with average academic standing of grade B.

After that session, we conducted a test based on that problem and found the score of test of students taught using simulation tools scored way better than other section. Students enjoyed learning about the concepts if taught using computational tools.

VII. Conclusion

The role of EM solvers and finite element modeller for researchers in RF MEMS domain is discussed by citing two case studies from our previous research work. Our primary focus in this paper is to relate the industrial requirements to the electronics engineering students. Students who are working or want to work in antennas or RF MEMS industry can take advantage, if they would learn these tools in their course curriculum. The capabilities of these tools in solving engineering problem is demonstrated in both case studies. It is clear that the capabilities of these tools are tremendous for any cross-coupled physics problems. The learn curve might be steeper for some, but once mastered it cam drastically reduce the designing and testing time. As only engineers can develop efficient and advanced products that can serve the needs of humanity and it can be possible with the quality engineering education.

APPENDIX – I

Design parameters and material parameters are given in Table I and in Table II respectively for the RF MEMS switch designed for Case study in this paper. These parameters are for the design elaborated in depth by T. Singh [5]

TABLE I
SPECIFICATIONS OF THE RF MEMS SWITCH

Component	Length μm	Width μm	Depth μm	Material
Substrate	412	412	200	Quartz
Substrate Dielectric	412	412	0.5	HfO_2
CPW (G S G)	126	31.5	1	Gold
Cavity	245	245	3	–
Series Membrane	235	80	1	Gold
Shunt Membrane	245	80	1	Gold
Electrode $\times 4$	35	40	1.5	Gold
Series Contact Pad	35	31.5	0.5	Gold
Meanders width	A (10)	B (3.5)	C (2.5)	Gold
Signal Line Dielectric	80	31.5	0.25	HfO_2

In value column, first value is for ohmic membrane and second is for capacitive unless otherwise specified. The parameters are given in Table. II. Some parameters are given in the specification table as shown in Table. I.

TABLE II
RF MEMS SWITCH – MATERIALS PROPERTIES

Parameter	**Notation**	**Value**
Young's Modulus	E	70 GPa
Density	ρ	$19,300$ Kg/m^3
Poisson's Ratio	ν	0.44
Dielectric Constant	ε_r	25
Spring Constant	k	$1.5, 2.7$
Initial Gap	g_0	$2.5, 3.0$ μm
Holes Radium	r_0	3.8 μm
Mean Free Path	λ	70 nm
Mass of Membrane	m	$8.52, 11.3$ ng

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Cost Effective Implementation of Fixed Point Adders for LUT based FPGAs using Technology Dependent Optimizations

Burhan Khurshid and Roohie Naaz

***Abstract*—Modern day field programmable gate arrays (FPGAs) have very huge and versatile logic resources resulting in the migration of their application domain from prototype designing to low and medium volume production designing. Unfortunately most of the work pertaining to FPGA implementations does not focus on the technology dependent optimizations that can implement a desired functionality with reduced cost. In this paper we consider the mapping of simple ripple carry fixed-point adders (RCA) on look-up table (LUT) based FPGAs. The objective is to transform the given RCA Boolean network into an optimized circuit netlist that can implement the desired functionality with minimum cost. We particularly focus on 6-input LUTs that are inherent in all the modern day FPGAs. Technology dependent optimizations are carried out to utilize this FPGA primitive efficiently and the result is compared against various adder designs. The implementation targets the XC5VLX30-3FF324 device from Xilinx Virtex-5 FPGA family. The cost of the circuit is expressed in terms of the resources utilized, critical path delay and the amount of on-chip power dissipated. Our implementation results show a reduction in resources usage by at least 50%; increase in speed by at least 10% and reduction in dynamic power dissipation by at least 30%. All this is achieved without any technology independent (architectural) modification.**

***Index Terms*— FPGA, LUT, FPGA primitives, Technology mapping, Boolean Network.**

Original Research Paper
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I. INTRODUCTION

FIELD programmable gate arrays provide an alternative approach to application specific integrated circuits (ASIC) implementation [1] with features like large-scale integration, design verification post production, lower non-recurring engineering (NRE) costs, reconfigurable design approach etc. [2, 3]. FPGAs also offer an attractive platform for development of novel systems for rapid system prototyping and low to medium volume productions [1, 4, 5, 6]. Most of the modern day FPGA devices contain programmable logic blocks that have look-up table (LUT) as the basic programmable logic element [7, 8]. A k-input LUT is a digital memory that can implement any Boolean function of k variables. The k inputs in an LUT address 2k storage elements that store the truth table of the Boolean function. LUT based FPGAs account for a significant part of the commercial FPGA market [9, 10].

Since their genesis in 1985 [10], FPGAs have evolved enormously with state-of-art devices having in-built full custom processing elements like multipliers, DSP blocks, fast carry chains, high speed clocking, I/O resources etc. [11, 12, 13]. These blocks are highly optimized in terms of speed or area thereby facilitating efficient realization of complex functions [14, 15]. One of the major changes in the FPGA architecture has been the introduction of 6-input LUT as a logic element [11, 16]. With this FPGA primitive, the logic implementation would lead to higher logic densities resulting in a minimal-depth circuit and hence higher speed - a trend towards which the current FPGAs are oriented [17, 18, 19].

Perhaps the biggest issue with 6-input LUTs is their under-utilization while implementing a particular logic function, since many logic functions do not require six inputs [10]. This leads to low logic density and thus slower structures. Although many FPGA vendors have designed these elements with dual output capabilities [17, 18], their usage in implementing a Boolean function still remains far from the optimum.

Another issue is regarding the technology mapping of Boolean networks representing a combinational function. Logic synthesis in FPGAs has a well-defined flow that starts with design entry and proceeds through phases like synthesis, translation, mapping and place and route (PAR). Technology mapping is one of the most important phases in the FPGA computer aided design (CAD) flow that is directly concerned with selecting the circuit elements that will implement a given Boolean network [1, 7]. For LUT based FPGAs the target circuit element is the *k*-input LUT. Technology mapping is always cost driven. The goal is to produce a minimum-cost circuit that implements a desired Boolean function [1, 7, 8]. The cost of the circuit is typically a measure of its area, speed, power or a combination of these and accordingly there are algorithms that drive the technology mapping process towards area optimization [19, 20, 21, 22, 23, 24], delay optimization

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[25, 26, 27, 28, 29, 30], power optimization [31, 32, 33, 34, 35, 36], or area and delay optimization [37, 38, 39, 40, 41].

Modern day commercially available tools from leading vendors like Xilinx and Altera have fully automated technology mapping. The technology mappers in these tools take the native generic circuit (NGC) file from synthesis and create a native circuit description (NCD) file as per the desired cost function. The NCD file contains the physical description of design in terms of the components in the target device. Thus the mapping process is fully automated and the designer has no control over the selection of circuit elements that will implement the given function.

In this paper, we aim at tackling these two issues. The contributions of this paper are:

i) We re-design the initial Boolean network for RCA based adders for area, speed, and power optimality. Achieving area and power optimality for Boolean networks with inputs greater than four is NP-hard [31, 42, 43], however, since the basic cell in RCA based fixed point adders is very simple our approach simultaneously addresses the area, speed and power issues and a complete utilization of 6-input LUTs is assured. We do not particularly use any of the algorithms listed previously but our approach uses a combination of techniques like node decomposition, exploiting re-convergent nodes, logic replication etc.

ii) Since design entry is the only manual phase in the FPGA design flow, we try to control the mapping of the Boolean networks at the design entry step only. This involves modifying the coding style and writing VHDL codes for optimized Boolean networks based on direct instantiations of the targeted circuit elements. This is in contrast to the conventional coding styles that are typically behavioral and rely completely on the synthesizer to map the Boolean network by inferring the logic.

We have compared our implementation results against various adder designs listed in [44]. Our implementation results show a reduction in resources usage by at least 50%; increase in speed by at least 10% and reduction in dynamic power dissipation by at least 30%. We have also compared our implementation against the Xilinx IP adder v 11.0 and a subsequent improvement in performance is observed.

The rest of the paper is organized as follows. Section II discusses some basic terminology used in this paper. Section III discusses the basic technology mapping of the Boolean network corresponding to the RCA cell on LUTs. In section IV we redesign the initial Boolean network to ensure proper utilization of the 6-input LUT. Synthesis and implementation is carried out in section V. Conclusions are drawn in section VI. References are listed at the end.

II. Definitions and Terminology

A *Boolean network* is a directed acyclic graph (DAG) with *nodes* corresponding to logic gates, primary inputs and primary outputs and directed edges corresponding to wires connecting the gates. Since the Boolean networks considered in this paper are simple full-adder circuits, we will use actual gates for nodes. Further the term *network* will be used to refer to a Boolean network representing a combinational function and the term *circuit* will be used to refer to a Boolean network representing a circuit net-list i.e. a network of connected LUTs.

A node in a network may be driven by zero or more predecessor nodes known as *fan-in* nodes and may drive zero or more successor nodes known as *fan-out* nodes. The primary inputs (PIs) of the network are nodes without any fan-in. Similarly primary outputs (POs) are nodes without any fan-out. A network is said to be *k-bounded* if the number of fan-ins of each node does not exceed *k*.

The *level* of a node is the length of the longest path from any PI to the node. The node itself is counted in the path length. In this paper we have considered buffered inputs and outputs so that PIs and POs also contribute to the network *depth* which is defined as the largest level of a node in the network. The delay and area of a mapped circuit is measured by the depth and number of LUTs respectively.

A *cone* of a node v, C_v, is a sub-graph consisting of the node v and some of its non-PI predecessors, such that any node in this cone has a path to the node v that lies entirely in C_v. Node v is referred to as the *root* of the cone.

III. Mapping the Basic RCA Cell

Addition is one of the basic operations in digital signal processing (DSP) systems. It is used as a primitive operation in various arithmetic circuits like multipliers, multiply-adders etc. In order to maximize the performance of the adder circuit various technology independent (architectural) approaches have been used. However, this work focuses on carrying out the technology dependent optimization of the conventional ripple carry adder on LUT based FPGAs.

Technology mapping using LUTs is a two step process. In the first step, the entire network is partitioned into suitable sub-networks. The individual nodes within each sub-network are then covered with suitable cones. The logic implemented by each cone is then mapped onto a separate LUT and an optimal LUT net-list is obtained. In the second step, the net-list for the entire network is constructed by assembling the individual net-lists. The overall goal is to have a circuit implementation that uses minimum possible LUTs and has minimum possible depth.

The basic cell in an RCA network is a full adder. Fig. 1 shows the Boolean network for a full adder circuit. The network is partitioned into two sub-networks corresponding to sum (S) and carry (C), by dividing it at fan-out nodes. Each sub-network is separately mapped into a circuit of LUTs by covering the individual nodes with suitable cones. A straight forward approach would be to cover each node within a sub-network with a separate cone. The sub-network is then traversed in post-order depth-first fashion and each cone is assigned to a separate LUT as shown in Fig. 2(a). The number at the lower-right corner of each LUT indicates the level of the LUT assuming each LUT has a delay of one unit. The overall depth of the circuit at PO nodes S and C is four (including the buffers at PIs and POs). The total number of LUTs needed is six. The number of LUTs may be reduced by decomposing the 3-input OR gate in the carry sub-network. The decomposed node is included in two separate cones and the sub-network is

again traversed in post-order depth-first fashion to have a circuit implementation of Fig. 2(b). The number of LUTs is now reduced to three. However, an optimal implementation may be obtained by exploiting the reconvergent PI nodes in the carry circuit. Reconvergent nodes share the same inputs and can be exploited to reduce the number of PIs to a sub-network. This is shown in Fig. 2(c) where the reconvergent paths are included within the LUTs and the circuit is implemented with a single LUT for each sum and carry sub-network. The number of LUTs utilized is two and the overall depth including the buffers at PIs and POs is three. An n-bit adder implemented using the optimized circuit of Fig. 2(c) will have an overall depth of n+2 and will require 2n LUTs.

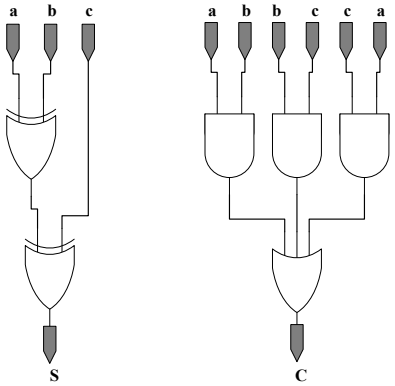

Fig. 1. Basic RCA cell.

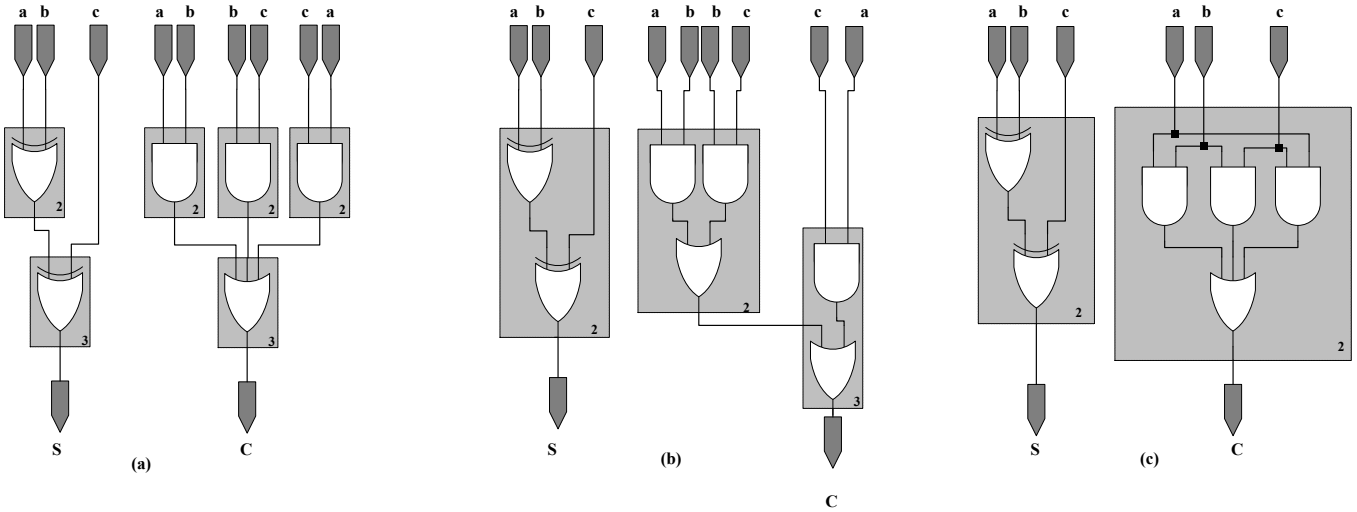

Fig. 2. Mapping of the RCA cell. a) Direct Mapping. b) Mapping using node decomposition c) Mapping exploiting reconvergent nodes.

The following instantiations were used in the design entry phase to map the circuit in Fig. 2(c).

```
    begin
    -- Optimal mapping for sum output
       L_1 : LUT3_L generic map (INIT => X"96")
          port map (S, c, b, a);
    -- Optimal mapping for carry output
       L_2 : LUT3_L generic map (INIT => X"E8")
          port map (C, c, b, a);
end Behavioral;
```

IV. Optimal Mapping for 6-Input LUT

The circuit in Fig. 2(c) may be an optimal circuit for a 3-input LUT but when the target element is a 6-input LUT, it leads to severe under-utilization of the resources resulting in a low-density circuit. Since most of the modern day FPGAs have 6-input LUTs as their basic logic element, it is compelling to devise a method that utilizes this circuit element efficiently. We counter this issue by considering two RCA cells simultaneously and restructuring the initial Boolean network so that the circuit obtained after transformation utilizes the targeted 6-LUT efficiently. Fig. 3(a) shows the Boolean network that corresponds to two full adder cells. The network may be partitioned into three separate sub-networks corresponding to two sum bits S(0) and S(1) and a carry bit C(1). The reconvergent nodes in the carry sub-network are exploited to reduce the number of inputs and a circuit implementation similar to Fig. 2(c) is obtained. This is shown in Fig. 3(b). However, an optimal 6-input LUT implementation may be achieved by replicating the logic at fan-out node Z as shown in Fig. 4(a). The replicated nodes are shown by shaded portions. Node replication ensures that the sub-networks S(1) and C(1) have the same inputs. The covering process covers the individual networks with suitable cones and each cone is mapped onto a separate LUT. Sub-networks S(1) and C(1) share the same inputs and are implemented using a single 6-LUT with dual outputs. The overall circuit is shown in Fig. 4(b). The depth of the circuit is three and the number of LUTs utilized is two. An n-bit adder implemented using this circuit will have an overall depth of (n/2)+2 and will utilize only n LUTs. Thus the implementation based on Fig. 4(b) is theoretically 50% more efficient than the one based on Fig. 2(c). Fig. 5 shows an 8-bit adder unit constructed using the optimized circuit of Fig. 4(b).

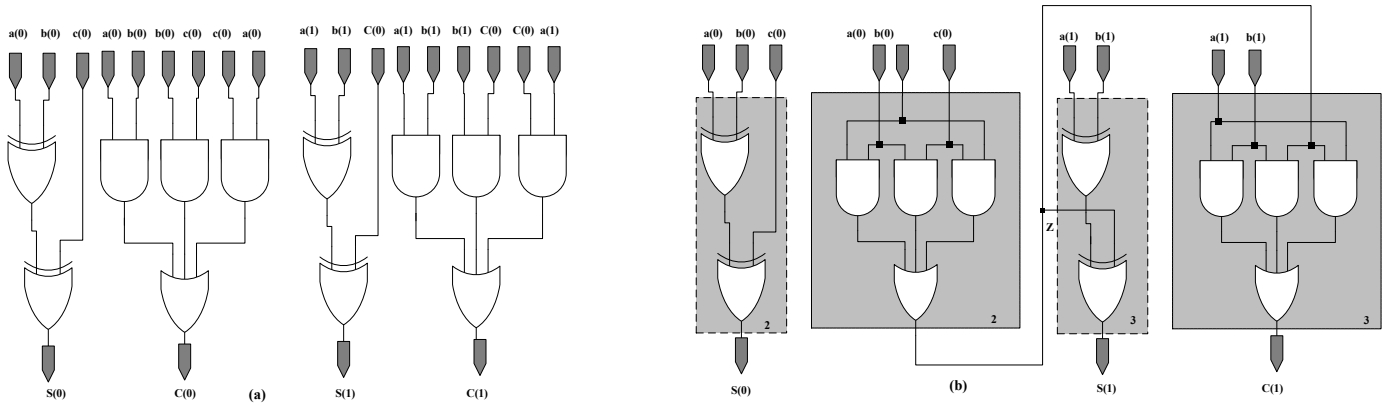

Fig. 3. a) Logic diagram for a 2-bit RCA adder. b) Mapping using 3-input LUTs.

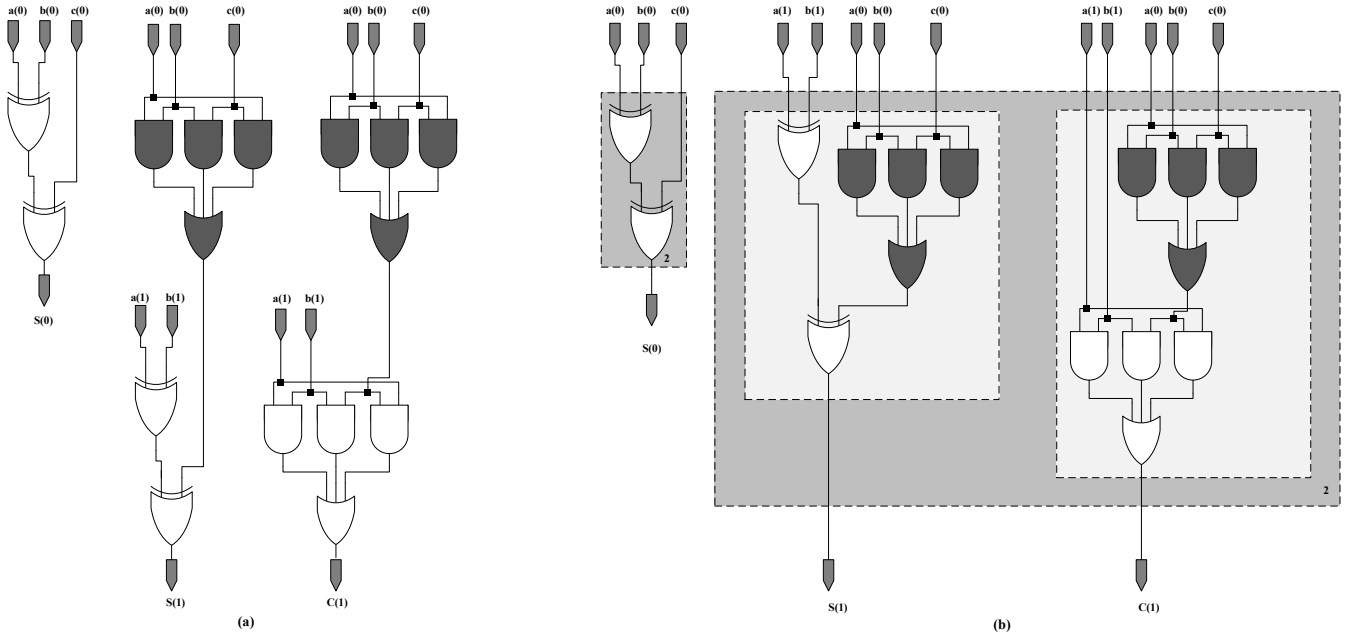

Fig. 4. a) Logic replication at node Z. b) Optimal 6-input LUT implementation.

The following instantiations were used in the design entry phase to map the circuit in Fig. 4(b).

```
begin
-- Optimal mapping for S(0) output
   L_1: LUT3_L generic map (INIT => X"96")
      port map (S(0), c(0), b(0), a(0));
-- Optimal mapping for S(1) and C(1) output
   L_2: LUT6_2 generic map ( INIT => X"E81717E8FFE8E800")
      port map (C(1), S(1), c(0), b(0), a(0), b(1), a(1), '1' );
end Behavioral;
```

V. Synthesis and Implementation

A. Methodology

The implementation in this work targets the XC5VLX30-3FF324 device from Xilinx Virtex-5 FPGA family. The implementation is carried out for an input word-length varying from 8 to 64 bits. The parameters considered are area, timing and dynamic power dissipation. Area is considered in terms of the number of occupied slices. Timing analysis may be static or dynamic. Static timing analysis gives information about the delay associated with the critical path and the maximum frequency at which the design may be operated. Dynamic timing analysis verifies the functionality of the design by applying test vectors and checking for correct output vectors. Dynamic timing analysis is done post implementation and PAR. The quality of dynamic timing analysis depends on the number of test vectors used. An important result from dynamic timing analysis is the switching activity information (toggle rates, signal rates etc.). This information is captured in the value charge dump (VCD) file and helps in determining accurate power measurements. Dynamic power dissipation is related to the charging and discharging of various node capacitances along different switching elements. To ensure a fair comparison, similar test benches have been used for all the implemented designs i.e. the input statistics remain same in each case. The initial design entry is done using VHDL through direct instantiation of the primitives rather than writing inferential codes and letting the synthesizer decide how to infer the logic. This ensures a fairly controlled mapping. The constraints relating to synthesis and implementation are duly provided and a complete timing closure is ensured in each case. The design synthesis and implementation is carried out in Xilinx ISE 12.1 [45] and the simulator database is then analyzed for speed and area metrics. Power metrics are obtained from Xpower analyzer.

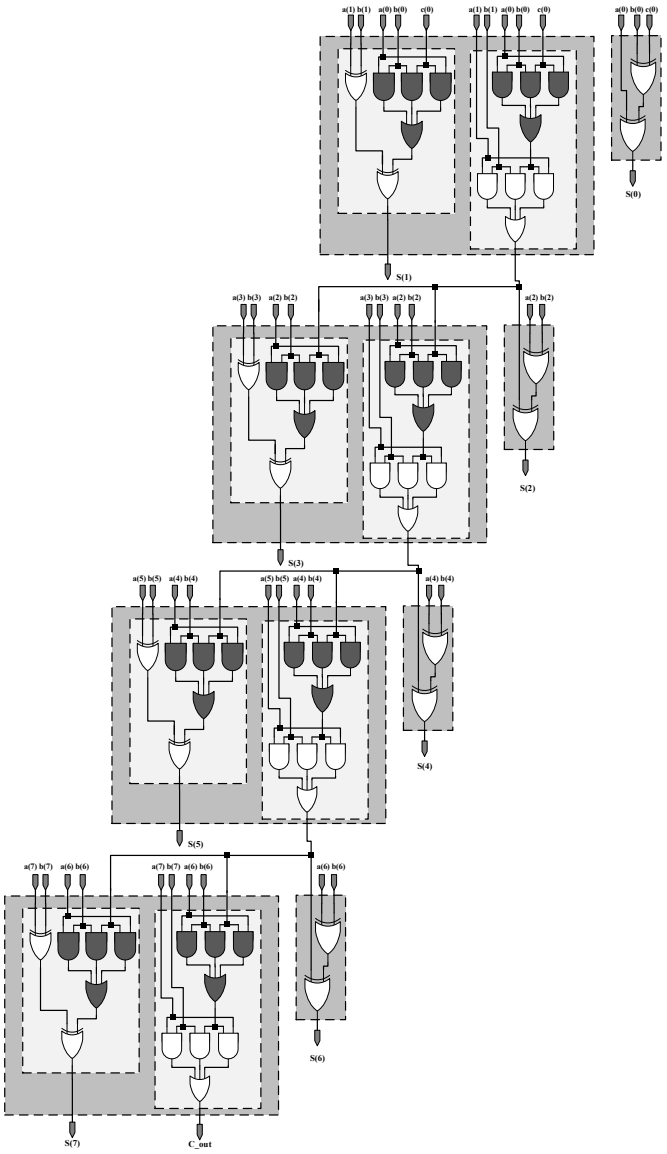

Fig. 5. 8-bit adder structure based on technology optimized binary adder cell.

B. Experimental results

We have compared our implementation results against the various fixed point adder designs in [44] and the Xilinx IP adder v 11.0.

TABLE I
RESOURCE UTILIZATION FOR DIFFERENT ADDERS ON XC5VLX30 FOR 16 BIT INPUT WORD-LENGTH

Adder Design	No. of occupied slices
Carry chain adder (CCA) [44]	9
Carry select adder (CSA) [44]	7
Carry skip adder (CKA) [44]	7
Carry look ahead adder (CLA) [44]	16
Sign magnitude adder (SMA) [44]	15
Xilinx IP adder v.11.0	4
3-input LUT based adder (LUT_3)	7
6-input LUT based adder (LUT_6)	**3**

Table I gives the comparison of resource utilization for various adder designs. The comparison is carried out for an input word-length of 16 bits. It is observed that technology mapping using LUTs results in a subsequent reduction of the on-chip resources being utilized. The most area efficient structure is obtained using 6-input LUT because of its ability to implement sum and carry sub-networks in a single LUT. Further analysis is carried out for different adders for varying word-lengths. The results are plotted as a function of word-length and appear in Fig. 6.

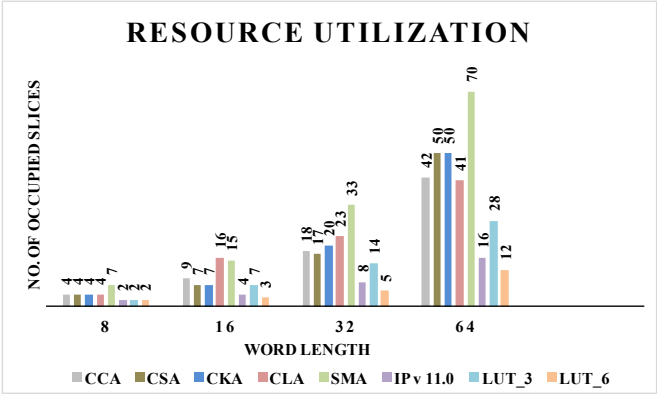

Fig. 6. Resource utilization for different adder structures.

Technology mapping using LUTs also reduces the depth of the implemented circuit resulting in shorter critical paths. Table II provides a comparison of the critical path delay for various adders for an input word-length of 16 bits.

TABLE II
CRITICAL PATH DELAY FOR DIFFERENT ADDERS ON XC5VLX30 FOR 16 BIT INPUT WORD-LENGTH

Adder Design	Critical path delay (ns)
Carry chain adder (CCA) [44]	7.872
Carry select adder (CSA) [44]	7.64
Carry skip adder (CKA) [44]	7.872
Carry look ahead adder (CLA) [44]	9.165
Sign magnitude adder (SMA) [44]	12.16
3-input LUT based adder (LUT_3)	7.148
6-input LUT based adder (LUT_6)	**6.969**

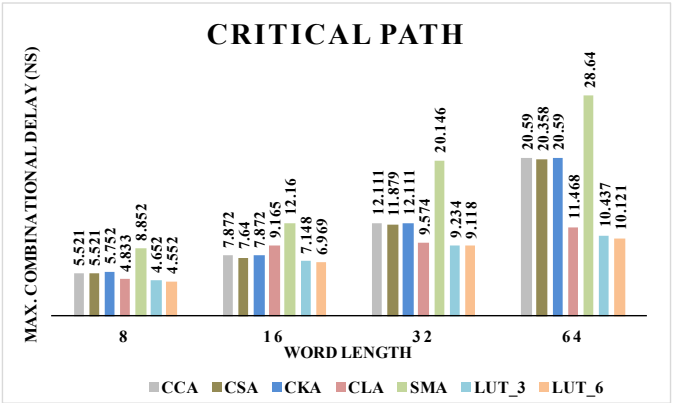

Fig. 7. Critical path delay variation for different adders.

Fig. 7 gives the variation in critical path delay for different adders as word-length is varied from 8 to 64 bits. We have also compared the maximum clock frequency for the 6-LUT

based adder and the Xilinx IP adder v 11.0. The results are shown for different word lengths in Table III.

TABLE III
MAX CLOCK FREQUENCY FOR IP BASED AND TECH. MAPPED DESIGNS

Word length	Max. Clock frequency (MHz)	
	Xilinx IP v 11.0	LUT_6
8	355.493	498.008
16	266.028	378.5011
32	211.372	287.7934
64	145.65	210.32

Finally dynamic power dissipation for different structures is considered. The dynamic power dissipation is a function of the input voltage (V^2), the clock frequency (f_{clk}), the switching activity (α), the total capacitance seen by a particular node (C_L) and the number of elements used (σ). The capacitance C_L, which needs to be driven at each toggling node, varies with the type, fan-out, and capacitance of the logic and routing resources used in the design. The use of LUTs ensures that the high activity switching nodes remain hidden. This reduces the charging and discharging of the capacitances associated with these nodes, resulting in reduced dynamic power dissipation. In addition, there is also a reduction in the number of elements (σ) being utilized which reduces the power dissipated in the logic. The analysis is done for a constant supply voltage and at maximum operating frequency for each structure. To ensure a reasonable comparison the test vectors provided during post route simulations are selected to represent the worst case scenario for data coming into the adders. Same test bench is used for all the synthesized structures. The design node activity captured in the VCD file along with the power constraint file (PCF) is used for power analysis in the Xpower analyzer tool. Table IV shows the comparison of dynamic power dissipation for various adders for an operand length of 16 bits.

Further analysis is carried out by plotting the total dynamic power dissipation as a function of input word-length for different adders. The result is shown in Fig. 8.

TABLE IV
DYNAMIC POWER DISSIPATION FOR DIFFERENT ADDERS ON XC5VLX30 FOR 16 BIT INPUT WORD-LENGTH

Adder Design	Dynamic power dissipation (Watt)
Carry chain adder (CCA) [44]	0.03608
Carry select adder (CSA) [44]	0.03604
Carry skip adder (CKA) [44]	0.03604
Carry look ahead adder (CLA) [44]	0.03625
Sign magnitude adder (SMA) [44]	0.03631
Xilinx IP adder v.11.0	0.026
3-input LUT based adder (LUT_3)	0.0193
6-input LUT based adder (LUT_6)	**0.01136**

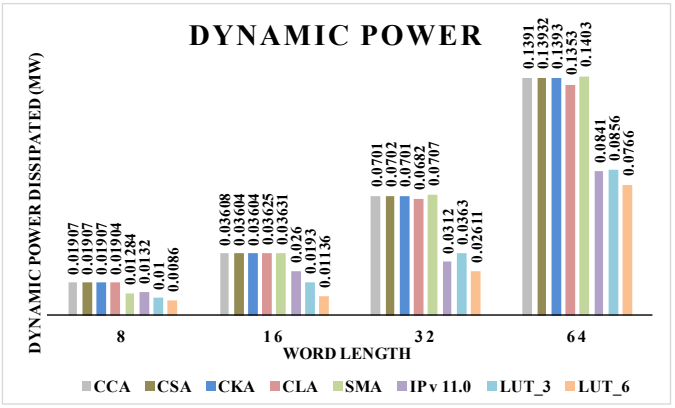

Fig. 8. Variation in Dynamic power dissipation with word-length.

VI. CONCLUSION

This paper implemented RCA based fixed-point adders by considering their mapping on LUT based FPGAs. The paper in particular targeted the 6-input LUT that is an inherent basic logic element in most of the modern day FPGAs. The optimization techniques used in this paper are purely technology dependent. Further hardware implementations presented in this paper were based on the primitive instantiations rather than the conventional inferential approaches. This ensured a controlled mapping of the optimized Boolean networks. The analysis and the experimental results presented in this paper clearly indicate that a considerable improvement in performance is achievable by technology dependent optimizations. No such analysis has been reported so far. By using a coding strategy based on instantiations the on-chip FPGA components can be used in a manner that fully utilizes their potential. This paper deliberately ruled out any technology independent (architectural) modification that may be carried out at the top level of the design. The idea was to present a clear cut analysis that will provide an insight about the performance speed-up that may be achieved by utilizing the huge primitive support provided by FPGA families through technology dependent optimizations. The future discourse will focus on achieving performance speed up in larger circuits like multipliers, multiply-accumulators etc. Also a combination of technology independent and technology dependent optimizations can lead to enormous improvement in performance and will encourage hardware intensive processing using FPGAs as a platform.

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Vector-Controlled Induction Motor Drive with Minimal Number of Sensors

Evgenije M. Adžić, Vlado B. Porobić, Marko S. Vekić, Zoran R. Ivanović, and Vladimir A. Katić

***Abstract*—This paper proposes an improved and robust induction motor drive control method which uses minimal number of sensors, providing only dc-link current measurement as a feedback signal. The proposed dc-link current sampling scheme and modified asymmetrical PWM pattern cancel characteristic waveform errors which exist in all three reconstructed line currents. In that way, proposed method is suitable for high-quality and high-performance drives. Comparison between conventional and proposed current reconstruction method is performed using hardware-in-the-loop (HIL) test platform and digital signal processor (DSP).**

***Index Terms*—Induction motor drive, Vector control, Sensorless control, Single current sensor.**

Original Research Paper
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I. Introduction

Controlled induction motor drives are main driving force behind all automation systems in industry. They are used in a wide range of industry applications where they significantly contribute to improved efficiency and reliability of automation processes [1]. Due to economical and reliability reasons most automation systems use induction motor drives where motor torque and speed are controlled without shaft-sensor [2]. Speed information is then determined indirectly, by measuring terminal currents and voltages [2-5]. Elimination of shaft-sensor not only reduces cost of the drive, but it also significantly increases whole system reliability. This is especially important in high-power range applications. Industry trends to provide more robust and reliable drives operation imposed necessity for drives with minimal number of sensors.

This paper proposes solution in the field of induction motor control, case where number of sensors is reduced to minimum. Only one sensor which measures the dc-link current of the converter is used. Control algorithm includes method for motor terminal current reconstruction in a way to achieve motor current and speed control. Analysis of recent relevant literature, confirms that most of the problems are recognized and solved in a way which allows their application in low-performance drives [6]-[10]. In this situation, authors usually do not consider quality and performance of implemented control algorithms.

Quality of controller is of major importance in general purpose applications having in mind their wide distribution and energy savings that can be achieved, while dynamic performances are usually put in the background. Recent developments in the electrical vehicle industry, has discovered a need to reduce the number of sensors to minimum, i.e. only one current sensor in the converter dc-link [11]. In that way, current reconstruction method becomes important also in high-performance applications. Priority in designing high-performance drives is not the cost of the drive, but accomplishing a highly accurate, stable and fast response.

Application of the current reconstruction method in a vector controlled induction motor drives proves to be significantly lower in quality and performances compared to drives using direct line current measurement. This is mainly consequence of the usual inaccuracy in reconstructed current waveforms, which is explained in details in [12]. Application of the conventional current reconstruction mechanism with two dc-link current samples in different time instants during the same switching period in combination with PWM current ripple generates error reflected in abrupt changes in reconstructed line current waveforms. This error reflects further in dq-current components in vector control algorithm, which can be observed in increased torque and speed oscillations. Moreover, in shaft-sensorless drives, accuracy in estimated speed is significantly reduced. Stability is seriously jeopardized in situations when current and speed controllers are tuned in optimal way characteristic for high-performance drives.

Conventional approach to overcome this problem employs low-pass current filters in control structure. This paper presents original solution for conventional current reconstruction method improvement, which avoids dynamic reduction, but in the same time eliminates the error and contributes to better control characteristics.

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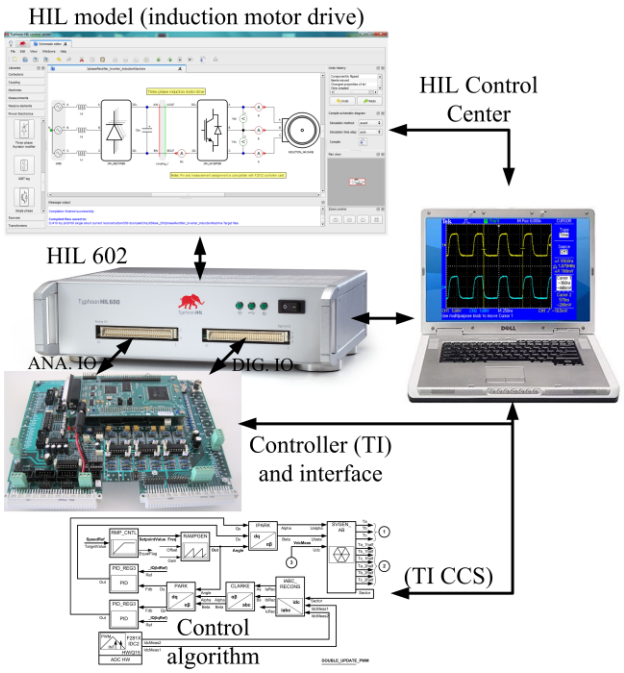


Fig. 1. Block diagram of experimental setup used for control algorithm verification.

II. Description of Experimental Setup

In order to validate effectiveness and reliability of the proposed current reconstruction method, hardware-in-the-loop (HIL) emulator was used for representing the power stage of induction motor drive. The core of the HIL platform is programmable FPGA based processor dedicated for processing power electronics circuits, with fast analog/digital input/output interface and supporting software tool-chain [13]. Beside schematic configurator and compiler, software tool-chain includes oscilloscope function for observing desired system variables and flexible debugging of the connected controller.

This approach provides real-time execution with *0,5 μs* emulation time-step and digital signals (e.g. PWM) sampling period of *20 ns* for more accurate system emulation. This feature allows the connection of real hardware controller with PWM frequency up to *100 kHz*. Controller interfaced with the HIL system is based on TMS320F2812 digital-signal processor. In all performed experiments, PWM frequency was set to *2 kHz*. Fig. 1 shows the experimental setup used for evaluation of the induction motor drive with minimal number of sensors. Motor nominal data and parameters of the related equivalent scheme are given in Table I.

III. Vector Control with the Measurement of Line Current and Speed

A. Rotor-flux oriented sensored control structure

In the early stages of the control algorithm development, current and speed controllers are set in the framework of conventional rotor-flux oriented vector control structure using directly line current and speed sensor information. This approach defines relevant framework for testing and comparison of proposed algorithm with only one dc-link sensor in a feedback path. In this stage, control algorithm uses measured line current and rotor speed as depicted in Fig. 2. Core of the control algorithm represents the flux model (*FLUX_MOD*) which is used to estimate the values of rotor flux angle (*Theta*) from the stator current vector components (*IDs* and *IQs*) and from the measured speed (*Wr*) [14].

TABLE I
Tested Motor Data

Symbol	Quantity	Value
P_n	Nominal power	1,1 kW
p	Number of poles	4
f_n	Nominal frequency	50 Hz
n_n	Nominal speed	1410 rpm
U_n	Nominal voltage	380 V
I_n	Nominal current	2,9 A
	Winding connection	Y (star)
J	Moment of inertia	0,00247 kgm^2
R_s	Stator resistance	9,137 Ω
R_r	Rotor resistance	6,422 Ω
$L_{\gamma r}$	Stator leakage inductance	18,89 mH
$L_{\gamma s}$	Rotor leakage inductance	17,28 mH
L_m	Magnetizing inductance	320,3 mH

B. Stator current controller tuning

PI current controllers for d- and q-axes are tuned using Dahlin's algorithm [15] which defines fast aperiodical step response of controlled current components, *IDs* and *IQs*, i.e. motor flux and torque. A proportional and integral gain for current controllers in discrete domain are:

$$K_{pi} = \frac{1 - e^{-\lambda T_i}}{K_{it}\left(e^{\frac{T_i}{T_\sigma}} - 1\right)\left(1 + \left(1 - e^{-\lambda T_i}\right)\right)} \qquad (1)$$

$$K_{ii} = K_{pi}\left(e^{\frac{T_i}{T_\sigma}} - 1\right)$$

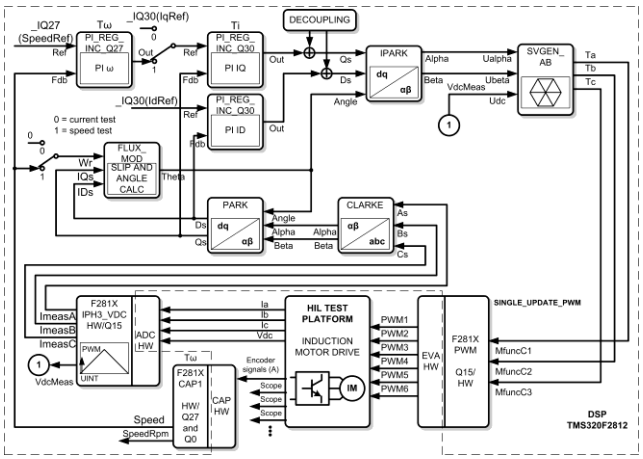


Fig. 2. DSP implementation of classical structure of rotor-flux oriented control for induction motor drive.

In Eq. 1 parameter λ defines desired dynamic of aperiodical step response, T_i represent current loop sampling period, and K_{it} is total gain in a direct path of current control loop. Total gain K_{it} equals:

$$K_{it} = \frac{u_{dc}}{\sqrt{3}} \frac{1}{R_s} \frac{1}{I_b} \tag{2}$$

where are: u_{dc} – dc-link voltage, R_s – stator winding resistance, and I_b – selected current base value. Independent design of current and speed controller is enabled by selecting the parameter λ to satisfy the condition:

$$\frac{1}{\lambda} \leq \frac{T_\omega}{5} \tag{3}$$

where T_ω represents the speed control loop sampling period. Used values for current controllers in d- and q-axes are given in Appendix section.

Dynamic response of stator current controller is given in Fig. 3. where it can be noticed that d-axis reference current was maintained on the constant value, i.e. i_d^{REF}=*0,32 p.u.*, while q-axis reference current was periodically step-changed between values *0* and *0,48 p.u.* d- and q-current references, i_d^{REF}=*0,32 p.u.* and i_q^{REF}=*0,48 p.u.*, together defines nominal current amplitude for considered motor. Fig. 3 proves that aperiodical response, without overshoot, was achieved with settling time of *19 ms* which is approximately equal to expected value of $5/\lambda$=*16,7 ms*. Fig. 4 shows corresponding response of motor line currents and electromagnetic torque. For rotor flux value defined with i_d^{REF}=*0,32 p.u.* and i_q^{REF}=*0,48 p.u.* motor develops nominal electromagnetic torque T_{en} = *7,45 Nm* in steady-state. Torque oscillations around *4,7%*·T_{en} are consequence of PWM current.

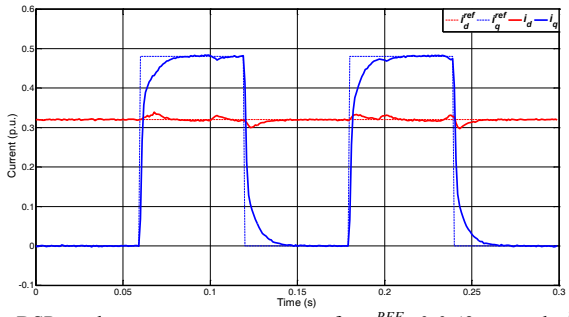


Fig. 3. DSP results: q-current step response for i_q^{REF}=*0-0,48 p.u.* and i_d^{REF} = *0,32 p.u.*

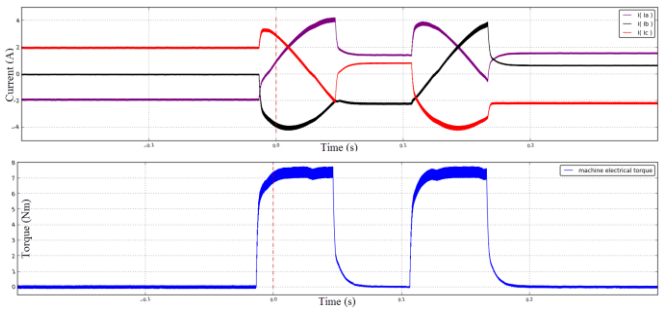


Fig. 4. HIL results: corresponding line current and electromagnetic torque response for i_q^{REF}=*0-0,48 p.u.* and i_d^{REF}=*0,32 p.u.*

Designed current controllers are used for all other experiments throughout this paper.

C. *Rotor speed controller tuning*

Speed controller parameters are selected in a way to obtain fast aperiodical step response. Detailed design procedure, suggested for high-performance motor drives in [16], gives following proportional and integral gains for speed controller:

$$K_{p\omega} = 0{,}2027 \frac{2J}{T_\omega} \frac{\omega_b}{K_m}$$

$$K_{i\omega} = 0{,}03512 \frac{2J}{T_\omega} \frac{\omega_b}{K_m} \tag{4}$$

In Eq. 4 J represents motor moment of inertia, ω_b is adopted base value for angular frequency, and K_m is the gain in the direct path of speed control loop model obtained from the torque equation of vector-controlled induction motor:

$$K_m = \frac{3}{2} p \frac{{L_m}^2}{L_r} i_{sd} I_b \tag{5}$$

Used parameters of speed controller are given in the Appendix. Fig. 5 shows dynamic speed response after setting step reference value ω_r^{REF} = *0,1 – 0,4 p.u.* (*300 – 1200 rpm*). Motor was loaded with *20%* of rated torque *1,5 Nm*. Recorded HIL results in the same conditions are shown in Fig. 6. It could be noticed that speed has aperiodical transient response with settling time *0,2 s*, as expected for optimal method and parameters given with Eq. 4. Current response in field coordinates in the Fig. 5, proves that decoupled control of motor flux and torque was successfully achieved. Designed speed controller is used for all other experiments in the paper.

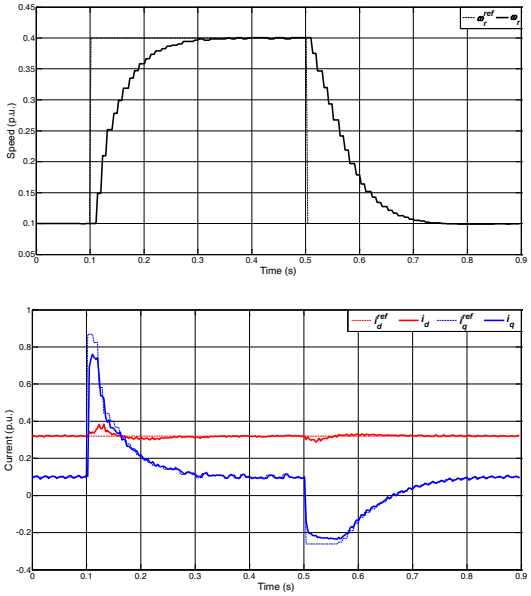


Fig. 5. DSP results: motor speed and dq-currents response for step reference ω_r^{REF} = *0,1 / 0,4 p.u.*

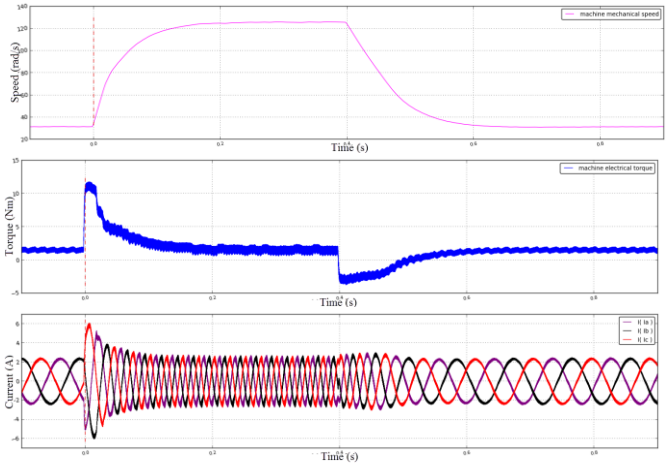


Fig. 6. HIL results: corresponding motor speed, electromagnetic torque and stator currents step response for ω_r^{REF}=0,1-0,4 p.u.

IV. Shaft-Sensorless Vector Control with Line Current Measurement

A. Rotor-flux oriented sensorless control structure

In a base speed region rotor-flux oriented vector control without speed sensor shows better performance comparing to the orientation towards stator flux vector [14]. Taking this into account and due to easier integration of sensorless control algorithm in previously described control structure, this paper uses sensorless rotor flux oriented control structure shown in Fig. 7. This fact also facilitates comparison analysis between implemented sensored and sensorless algorithms. Open-loop rotor speed estimation (*SPEED_EST*) with advanced rotor flux vector estimation (*FLUX_EST*) has been applied.

B. Estimation of rotor flux components

Regarding selected reference frame, the flux vector components are firstly calculated in term of stator coordinates, and in second step magnitude and phase angle are derived in field orientated coordinates.

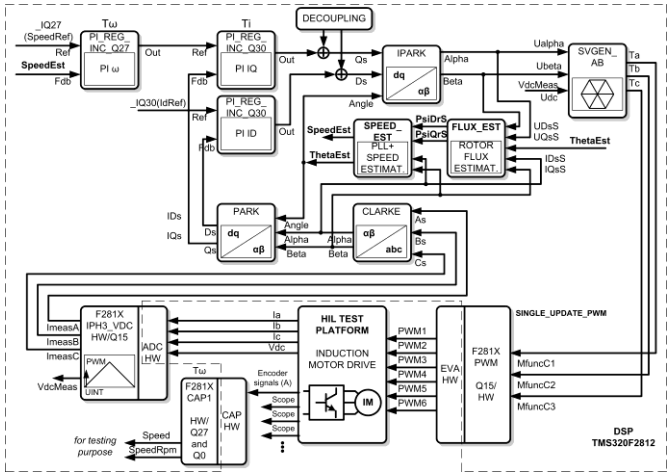


Fig. 7. DSP implementation of rotor-flux oriented sensorless control structure for induction motor drive, with advanced rotor flux estimation (*FLUX_EST*) and open-loop rotor speed estimation (*SPEED_EST*).

Used flux estimator belongs to the class of complex and advanced estimators covering wide range of speed (Fig. 8). Basically, it consists of two models: simple i_s – ω_r open-loop current model defined in field coordinates which has to provide correct estimation in the low speed range, and adaptive u_s – i_s model obtained in stator coordinates for precise estimation in wide speed range [14, 17]. Rotor flux i_s-ω_r current model (superscript i) could be derived based on motor rotor voltage and flux linkage equations in the rotor-field orientated reference frame, where stator current is used as input variable:

$$\frac{d\psi_{rd}^{i}}{dt} = \frac{L_m}{T_r} i_{sd} - \frac{1}{T_r}\psi_{rd}^{i}$$
$$\psi_{rq}^{i} = 0 \qquad (6)$$

Determined rotor flux components has to be transformed in stationary reference frame with inverse Park transformation, to perform correction of adaptive rotor flux voltage model derived in stator coordinates, as depicted in Fig. 8. Stator flux components are then calculated based on the motor stator flux linkage equations:

$$\psi_{s\alpha}^{i} = \frac{L_m}{L_r}\psi_{r\alpha}^{i} + L_\sigma i_{s\alpha}$$
$$\psi_{s\beta}^{i} = \frac{L_m}{L_r}\psi_{r\beta}^{i} + L_\sigma i_{s\beta} \qquad (7)$$

where L_σ represents stator leakage inductance.

Voltage model of rotor flux estimator is based on stator voltage equations in stationary reference frame, where stator flux is simply obtained by integration of stator winding induced electromotive force. Input variables are stator voltages and currents. Stator voltages are not directly measured. They are estimated based on measured dc-link voltage and inverter switching states. Dead-time and switching components for voltage drop compensation scheme is applied. Due to pure integration of input variables, stator voltage and current, compensation terms are included in the model to provide adaptive mechanism for elimination of offset error, erroneous initial values or their disturbances. Adaptive stator flux model is given (superscript u):

$$\psi_{s\alpha}^{u} = \int \left(u_{s\alpha} - R_s i_{s\alpha} - u_\alpha^{comp}\right) dt$$
$$\psi_{s\beta}^{u} = \int \left(u_{s\beta} - R_s i_{s\beta} - u_\beta^{comp}\right) dt \qquad (8)$$

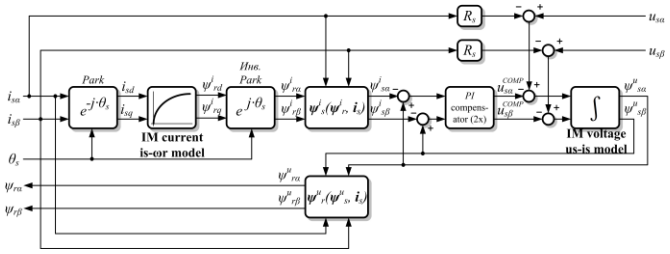


Fig. 8. Block diagram of algorithm for rotor flux estimation.

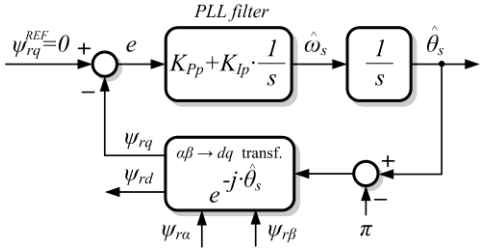


Fig. 9. Block diagram of PLL algorithm implemented in dq-reference frame.

Compensation terms, u_α^{comp} and u_β^{comp}, represents outputs of PI controllers that eliminates the error between the ideal current model (Eq. 6) and voltage model of stator flux:

$$u_\alpha^{comp} = K_{pf}\left(\psi_{s\alpha}^{u}-\psi_{s\alpha}^{i}\right)+K_{if}\int\left(\psi_{s\alpha}^{u}-\psi_{s\alpha}^{i}\right)dt$$
$$u_\beta^{comp} = K_{pf}\left(\psi_{s\beta}^{u}-\psi_{s\beta}^{i}\right)+K_{if}\int\left(\psi_{s\beta}^{u}-\psi_{s\beta}^{i}\right)dt \quad (9)$$

Parameters K_{pf} and K_{if} are determined in the way that current model in adaptive stator flux model dominates in the low speed range, while voltage model prevails in the high-speed range [17]. Finally, outputs of the rotor flux estimator are rotor flux components obtained from motor flux linkage equations in stationary reference frame:

$$\psi_{r\alpha}^{u} = \frac{L_r}{L_m}\left(\psi_{s\alpha}^{u}-L_\sigma i_{s\alpha}\right)$$
$$\psi_{r\beta}^{u} = \frac{L_r}{L_m}\left(\psi_{s\beta}^{u}-L_\sigma i_{s\beta}\right) \quad (10)$$

Determined rotor flux components are later used for rotor flux vector position and rotor speed estimation.

C. Rotor flux vector phase angle estimation

Exact determination of rotor flux vector phase angle, i.e. its position, is necessary for correct and proper transformation of all quantities in the field-rotating reference frame in which control algorithm is implemented. Solution of this problem mainly determines quality of the whole control structure, because error in the phase angle has significant negative influence on the independent control of dq-currents [14].

One of the standard and advanced methods for flux phase angle estimation represents Phase-Locked-Loop (PLL) structure implemented in rotating reference frame [18]. Block diagram of PLL algorithm used in this paper is shown in the Fig. 9. As input values, PLL uses previously determined rotor flux components in stationary reference frame. Rotor flux components are transformed in dq rotating reference frame using estimated rotor flux phase angle at the PLL output.

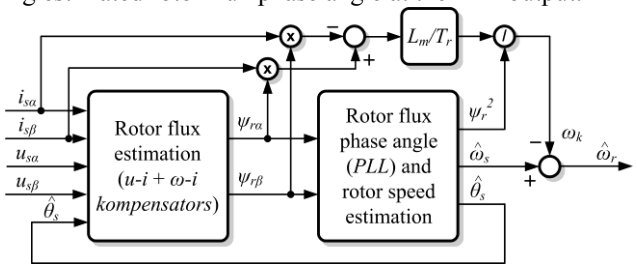


Fig. 10. Open-loop direct rotor speed estimation based on rotor flux vector.

Error signal is formed as a difference between rotor flux q-axis component reference set to 0 and obtained rotor flux q-axis component after transformation. This actually results in rotor flux vector tracking, i.e. in equalization of estimated and actual rotor flux phase angles. PLL filter in the form of PI compensator leads to reducing of error signal to zero value, also for flux frequency step changes. Parameters of PLL filter are selected in a way to provide aperiodical phase angle response with desired bandwidth of PLL control loop ω_{bw} [19]:

$$K_{pp} = \frac{\sqrt{2}}{f_b}\omega_{bw}$$
$$K_{ip} = \frac{1}{2f_b}{\omega_{bw}}^2 \quad (11)$$
$$K_{ip}^{z} = K_{ip}T_p$$

Integral gain of the PLL filter K_{ip} has to be multiplied with PLL sampling loop to obtain corresponding gain K_{ip}^{z} for digital implementation. Selected values used throughout all the experiments in the paper are given in Table II.

D. Open-loop estimation of rotor speed

Rotor flux angular frequency represents the first derivate of rotor flux phase angle, so it yields:

$$\omega_s = \frac{d\theta_s}{dt} = \frac{d\left(\operatorname{arctg}\left(\frac{\psi_{r\beta}}{\psi_{r\alpha}}\right)\right)}{dt} = \frac{\psi_{r\alpha}\frac{d\psi_{r\beta}}{dt}-\psi_{r\beta}\frac{d\psi_{r\alpha}}{dt}}{\psi_{r\alpha}^2} \quad (12)$$

By eliminating rotor currents from the rotor flux linkage equations in the induction motor model [14], and based on voltage equations for rotor winding in stationary reference frame, rotor flux angular frequency could be obtained in the following form:

$$\omega_s = \omega_r + \frac{1}{\psi_r^2}\frac{L_m}{T_r}\left(\psi_{r\alpha}i_{s\beta}-\psi_{r\beta}i_{s\alpha}\right) = \omega_r + \omega_k \quad (13)$$

ω_k represents slip frequency which is directly proportional to motor electromagnetic torque with assumption that rotor flux is maintained on constant value. Rotor speed can be estimated with:

$$\omega_r = \omega_s - \omega_k = \omega_s - \frac{1}{\psi_r^2}\frac{L_m}{T_r}\left(\psi_{r\alpha}i_{s\beta}-\psi_{r\beta}i_{s\alpha}\right) \quad (14)$$

Block diagram of implemented rotor speed estimator is shown in the Fig. 10.

E. Test results

Here are presented the main test results when feedback is closed using estimated speed and the concept described in previous chapter. Figs. 11 and 12, show motor speed, electromagnetic torque and stator current response under the same circumstances in which speed loop was closed with the measured rotor speed. Speed reference is changed in step manner between values ω_r^{REF} = *0,1 – 0,4 p.u.* with motor load

of *1,5 Nm*.

Fig. 11 shows relative values of control variables recorded in the DSP. Average speed settling time of *0,14 s* is not exact the same, but it is very close to the case when speed was measured. q-component of the stator current and corresponding torque oscillations are slightly increased, due to the PLL filter and rotor flux PI compensators in the control feedback path. Moreover, motor line currents are sinusoidal without significant distortion, similar to the case when speed loop was closed using measured rotor speed (Fig. 12).

V. Sensorless Vector Control with Conventional Current Reconstruction Method

A. Conventional current reconstruction method

Constant requirements for reducing cost and increasing reliability of the motor drives lead to the series of research with the aim to reduce number of sensors to its essential minimum. Research in the field proved that it is possible to reduce number of current sensors in three-phase AC drives to

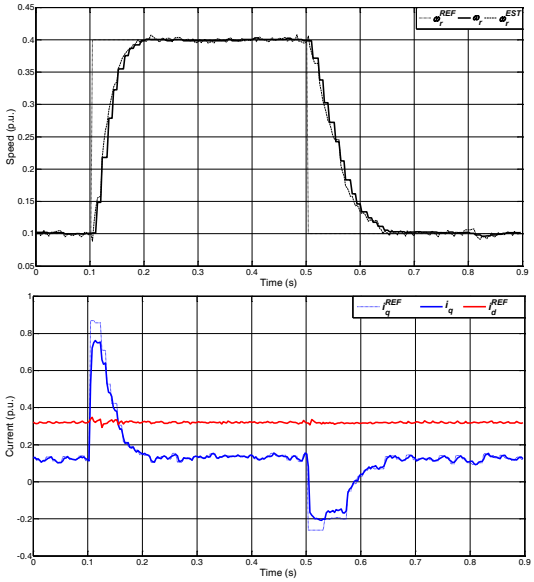


Fig. 11. DSP results: motor speed and dq-currents response for step reference $\omega_r^{REF} = 0,1 / 0,4$ *p.u.* – sensorless case with current measurement.

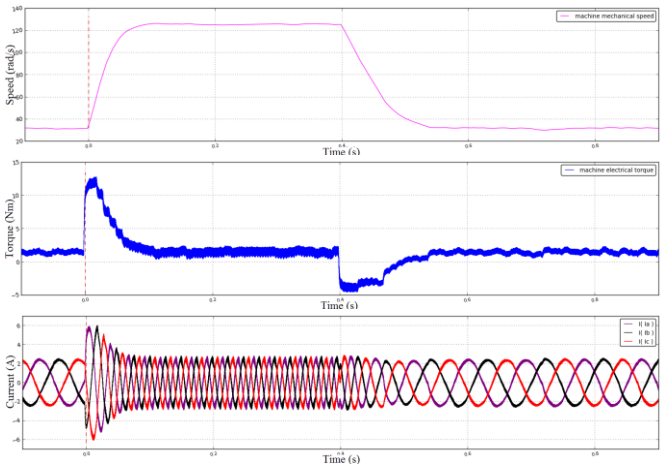


Fig. 12. HIL results: motor speed, torque and stator currents step response for ω_r^{REF}=*0,1-0,4 p.u.* – sensorless case with current measurement.

only one sensor in the dc-link. Block diagram of such drive is shown in the Fig. 13. Among previously described control structures, a core of the control scheme is block with motor phase currents reconstruction (*IABC_RECONS*) and modified switching modulator (*SVGEN_AB2*) with the task to support critical cases in reconstruction mechanism.

Due to the topology of three-phase inverter and selected switching modulation (SVPWM), it is possible to reconstruct motor phase currents from measured dc-link current [20]. In each switching period, dc-link current includes information about two motor line currents while remaining third current could be reconstructed taking into account that sum of the line currents is equal to zero. Fig. 14 shows an example and details of conventional current reconstruction principle, where switching PWM signals *A, B* and *C* for upper inverter switches are arranged defining output voltage vector in the first SVPWM sector. Two dc-link samples are taken in strategic moments (*SAMP1* and *SAMP2*) precisely synchronized regarding the middle of switching PWM period (*TRIG*) and according to the beginning of the active voltage vectors, as shown in Fig. 14. Here, current sample (i_h) during active voltage vector with only one upper switch turned-on is equal to phase current i_a, while current sample ($-i_l$) during active voltage vector with two upper switches turned-on is equal to inverted value of motor phase current i_c. Similar analysis could be performed for other SVPWM sectors that yield to complete current reconstruction algorithm [20].

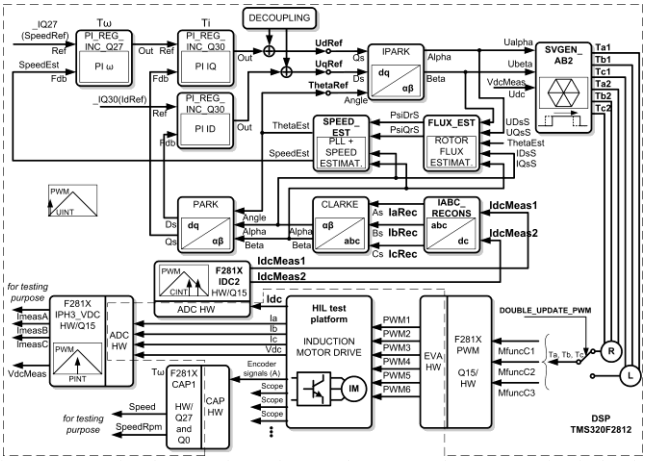


Fig. 13. DSP implementation of sensorless control structure for induction motor drive, with conventional current reconstruction algorithm (*FLUX_EST*) and modified SVPWM modulation (*SPEED_EST*).

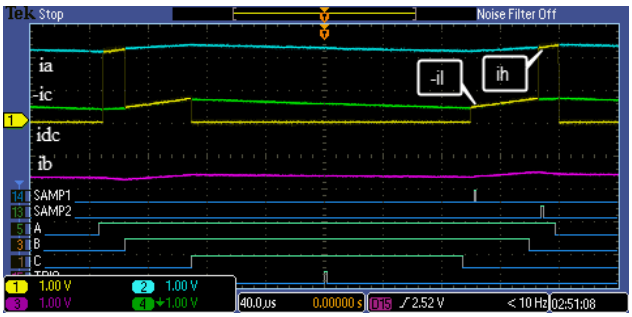
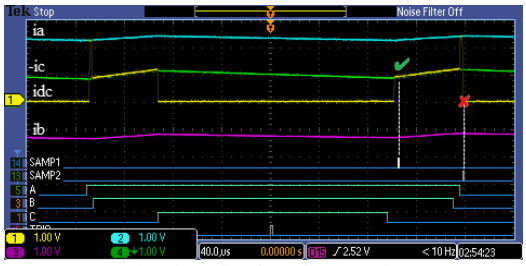


Fig. 14. Conventional dc-link current sampling and line current reconstruction method – example for first SVPWM sector.

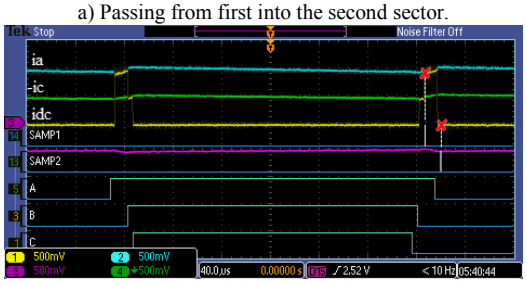
B. Modified SVPWM method

Practical problems with dc-link current sampling, occur when switching PWM period contains narrow active voltage vectors. First critical case represents a situation where the reference voltage vector passes between SVPWM sectors, and when duty cycles values for two inverter legs are almost equal. Fig. 15a shows example of this case, when voltage vector passes between the first and the second sector and when it is possible to reconstruct only one line current, $-i_c$. Line current i_a is unobservable. This is always the case in normal operation due to the reference vector rotation, and it is independent on modulation index value. Second critical situation occurs in the case of small reference amplitudes of output voltage vector, i.e. in the case of small modulation index. This is a usual situation in the case of low reference speed and low motor load torque. PWM duty cycles values for all three inverter legs are almost the same and around 50%. Sampling windows in the frame of both active vectors are not wide enough for reliable dc-link current measurement, so line current information could not be obtained. Fig. 15b shows a case of small amplitude reference voltage vector in the first SVPWM sector. Obviously, first signal *SAMP1* samples line current i_a, instead $-i_c$, while second sampling signal *SAMP2* measure zero value instead current i_a.

Fig. 16 shows results in case of applying original switching scheme without mechanism for obtaining minimal width of active voltage vectors. There is significant reconstructed current waveform distortion in critical intervals, which are useless for achieving vector control with only dc-link current feedback. Abrupt change and large deviation of reconstructed currents (i_a^{REC}, i_b^{REC}, i_c^{REC}) from actual current values (i_a, i_b, i_c) can be noticed in the area between different voltage sectors (*Sector*). To overcome these problems it is necessary to perform one of suggested mechanism for reliable dc-link current measurement by modifying the originally symmetrical PWM voltage patterns sufficiently, in the cases when longer active vectors are needed [6-9, 21].



a) Passing from first into the second sector.



b) Small modulation index in sector 1.

Fig. 15. Critical cases for line current reconstruction method.

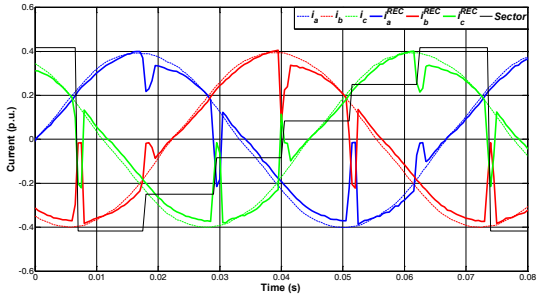


Fig. 16. Result of current reconstruction method without switching pattern modification.

Fig. 17 illustrates the applied solution principles with an example where small modulation index was referenced. PWM signals V_h *(A)*, V_m *(B)*, and V_l *(C)* does not form enough long active vectors for reliable dc-link current reading. Suggested method modifies PWM signals associated with the middle (V_m) and highest (V_h) voltage commands. Both signals are shifted in the right direction to form active vectors with minimal width T_{vector}^{MIN} for reliable dc-link current measurement. Firstly, if needed, PWM signal V_m is right–shifted by time:

$$\Delta T_{vector1} = T_{vector}^{MIN} - (T_m - T_l) \tag{15}$$

Active time intervals of PWM signal V_m during right (lagging) and left (leading) half-periods in PWM cycle should be updated to new values, T_{m2} and T_{m1}, respectively:

$$T_{m2} = T_h + \Delta T_{vector1}$$
$$T_{m1} = T_m - \Delta T_{vector1} \tag{16}$$

Then, second active vector duration has to be calculated and if needed, PWM signal V_h has to be right-shifted. Signal V_h width in lagging PWM half-period has to be extended, and in leading half-period to be reduced, to the new values T_{h2} and T_{h1}:

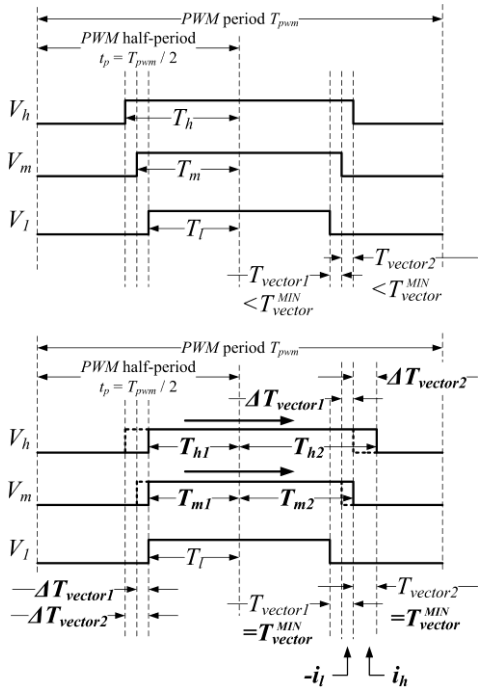


Fig. 17. PWM pattern modification principle used for reliable reconstruction.

$$\Delta T_{vector2} = T_{vector}^{MIN} - (T_h - T_{m2})$$
$$T_{h2} = T_h + \Delta T_{vector2} \quad (17)$$
$$T_{h1} = T_h - \Delta T_{vector2}$$

C. Test results

Figs. 18 and 19 illustrate the operation of conventional current reconstruction method with proposed modified switching pattern, in the closed-loop of described sensorless vector-control structure. Fig. 18 shows dynamic response of motor speed and stator dq-currents for same reference and operating conditions: ω_r^{REF} = *0,1 – 0,4 p.u.* and T_{load} = *1,5 Nm*. There are significant oscillations observed in dq-current components which are not caused only by current ripple on switching frequency, but also due to the current reconstruction mechanism which samples dc-link current in two different instants during PWM period [12]. Its final result is appearance of third and sixth harmonics in dq-current components. Maximal amplitude of the third and sixth harmonics in d-current was 9,4% and in q-current 43,3% of referenced value which contributed to higher distortion and oscillations in motor line current, torque and speed shown in the Fig. 19.

VI. Sensorless Vector Control with Proposed Current Reconstruction Method

A. Proposed current reconstruction method

The basic idea suggested in this paper represents an improvement of the method proposed in [6], which used the line-currents measured in both halves of the naturally symmetrical PWM switching period. The method proposed in [6] is based on sampling of the dc-link current in the center of the active voltage vectors four times during one PWM period and calculation of the two available line-current values by averaging the samples from two matching vector pairs.

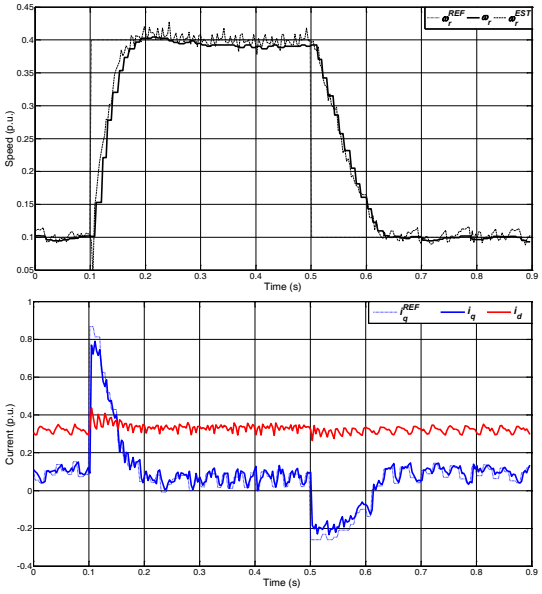


Fig. 18. DSP results: motor speed and dq-currents response for step reference ω_r^{REF} = *0,1 / 0,4 p.u.* – conventional current reconstruction method.

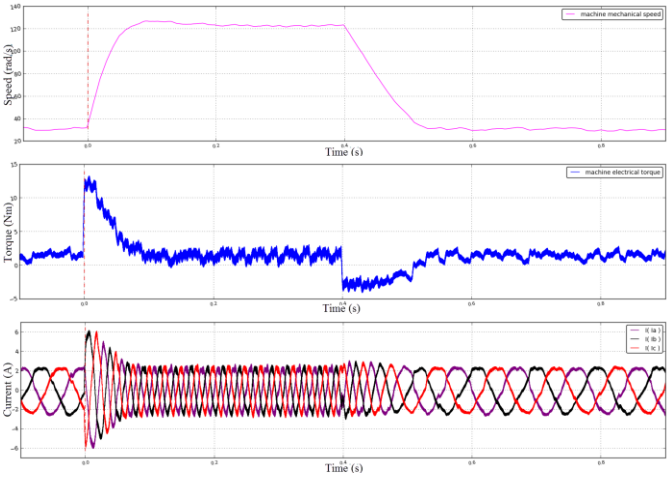


Fig. 19. HIL results: motor speed, torque and stator currents step response for ω_r^{REF}=*0,1-0,4 p.u.* – conventional current reconstruction method.

This approach provides synchronous measurement of all three line-currents, referred to the center of a PWM period. It effectively cancels error due to current ripple in the reconstructed line-currents and eliminates the current samples' mutual phase-shift. Besides its simplicity, this method is completely insensitive to machine parameter variances. However, in [6] the critical cases of a reference voltage vector passing between the six possible active vectors or with a low modulation index are neglected and not considered. The authors in [22] clearly emphasized that during these cases and with the PWM modified scheme used (where PWM signals are not symmetrical), the simultaneously sampled line-currents cannot be acquired. It clearly indicates there is a need to provide an improved procedure for reliably and more accurate measurement of the motor line-currents.

Considering the high PWM switching frequencies, up to 20 kHz, and usually employed electrical motors, one can conclude that there is no need for the very high current control-loop sampling rate at the PWM level. This fact allow us to record line-current information on the lagging (right) side of one PWM period and then on the leading (left) side of the subsequent PWM period and calculate the available line-currents by simple averaging of the corresponding recorded values. In this way, all three estimated line-currents would be referred to the same instant reflecting the average current value in two consecutive PWM periods. The proposed method enables us to improve the PWM pattern control in order to account for critical cases. It represents an extension of the modified PWM pattern explained in Section V.B where under critical conditions, the lagging half-pulse width is shifted to the right and the leading half-pulse width in the subsequent PWM period is shifted to the left in order to create sufficient sampling windows for current measurement (Fig. 21b).

Block diagram of implemented proposed control structure is illustrated in Fig. 20. Key blocks that improve control quality and performances are proposed current sampling block *F281X_IDC4*, *AVERAGING* block for finding inputs for conventional line current reconstruction *IABC_RECONS*, and

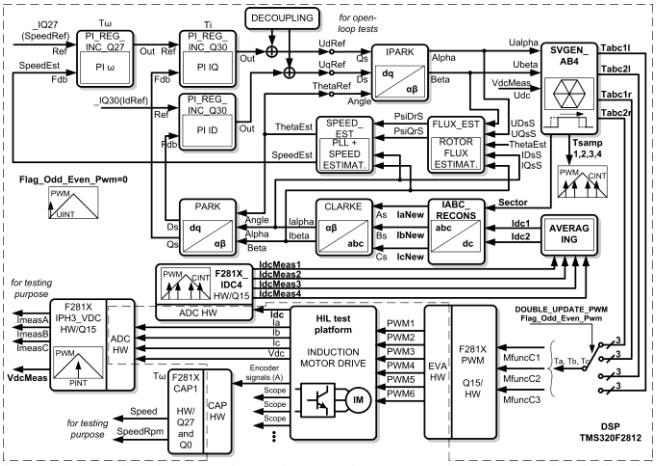
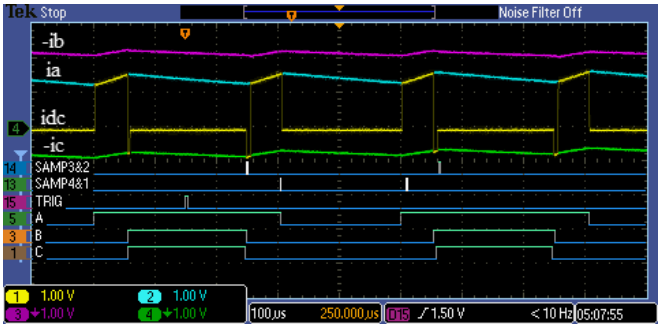


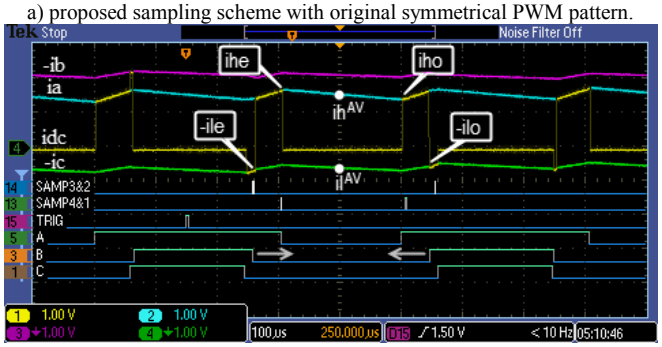
Fig. 20. DSP implementation of sensorless control structure for induction motor drive, with proposed current reconstruction algorithm (*F281X_IDC4+AVERAGING*) and modified modulator (*SVGEN_AB4*).

proposed modified voltage modulator *SVGEN_AB4* that overcomes critical cases in the reconstruction mechanism.

Fig. 21 shows the dc-link current and motor line currents during two consecutive PWM periods and details related to the proposed method. Sampling signals *SAMP1* and *SAMP4* are triggers for measurement of dc-link current in two consecutive PWM periods during matching active voltage vectors defined with only one inverter switch turned-on (here, with PWM signal *A*). *SAMP1* samples dc-link current at the beginning of the active voltage vector, and *SAMP4* at the end of the active vector. Similar, sampling signals *SAMP2* and *SAMP3* are triggers for measurement of dc-link current at the beginning and at the end of matching active voltage vectors defined with two upper switches turned-on (here, with PWM signals *A* and *B*), respectively.



a) proposed sampling scheme with original symmetrical PWM pattern.



b) proposed sampling scheme and modified PWM pattern for improved line current reconstruction.

Fig. 21. Proposed current reconstruction method details.

The line currents at the time instant representing average values in two consecutive PWM periods, can be obtained using simple calculation:

$$i_l^{AV} = -\frac{i_{dc}(SAMP2)+i_{dc}(SAMP3)}{2} = -\frac{i_{lo}+i_{le}}{2}$$
$$i_h^{AV} = \frac{i_{dc}(SAMP1)+i_{dc}(SAMP4)}{2} = \frac{i_{ho}+i_{he}}{2} \quad (18)$$
$$i_m^{AV} = -\left(i_l^{AV}+i_h^{AV}\right)$$

It remains to assign the resultant currents i_h^{AV}, i_m^{AV} and i_l^{AV} to motor line-currents i_a, i_b and i_c depending on the actual sector number as in conventional case.

B. Test results

The first improvements in the reconstructed line-current waveform can be observed for a steady-state operation with ω_r^{REF} = *0,4 p.u.*, T_{load} = *1,5 Nm* and closed-loop operation with proposed current feedbacks, in Fig. 22. Fig. 22a shows actual (measured) line current values, i_a, i_b, and i_c, compared to the reconstructed line currents by proposed scheme, i_a^{NEW}, i_b^{NEW}, and i_c^{NEW}, and by conventional scheme, i_a^{REC} (only phase-*a* current is shown for clarity). Improved reconstructed currents do not include characteristic abrupt changes in its waveforms due to the passing reference voltage vector between SVPWM sectors. Proposed current reconstruction reduces presence of third and sixth harmonic terms in dq-current components by factor of 3, but also the offset from actual values which are noticeable especially in d-current component (Fig. 22b).

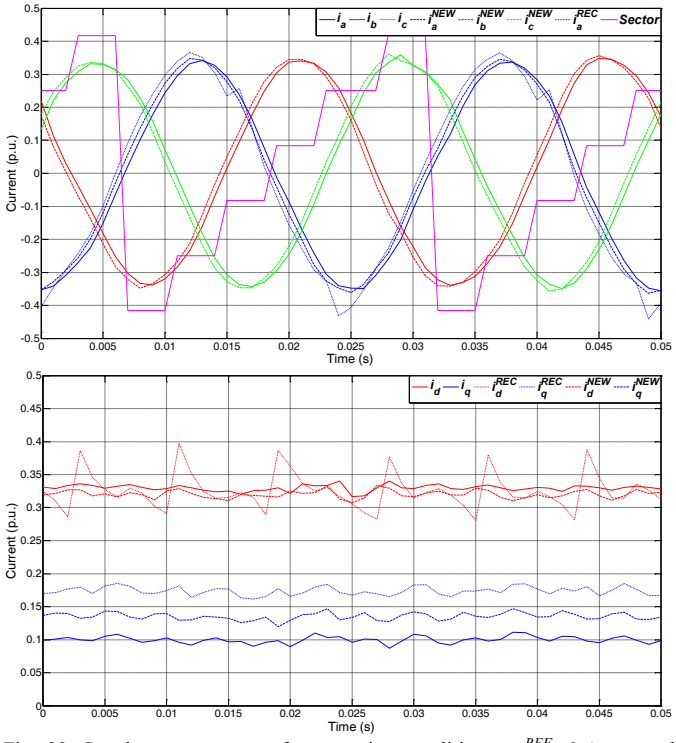


Fig. 22. Steady-state response for operating conditions ω_r^{REF}=*0,4 p.u.* and T_{load}=*1,5 Nm*: a) actual and reconstructed line currents; b) actual and reconstructed dq-currents with proposed (^{NEW}) and conventional reconstruction method (^{REC}).

This can be observed in motor torque and speed, not only in the steady-state, but also in transient intervals, where dynamic response is more stable. Figs. 23 and 24 show dynamic response of motor speed, electromagnetic torque and line currents in the same operating conditions: ω_r^{REF} = *0,1-0,4 p.u.* and T_{load} = *1,5 Nm*. Oscillations are less reduced for low speed reference *0,1 p.u.* because there are more frequent requirements for application of asymmetrical PWM signals due to the low reference voltage amplitude. However, obtained results together with the results in Fig. 18 verify that proposed method provide more stable stationary and dynamic response compared to the conventional current reconstruction method. Proposed control scheme shows almost the same behavior as in the case when direct measured line currents were used (Figs. 11 and 12).

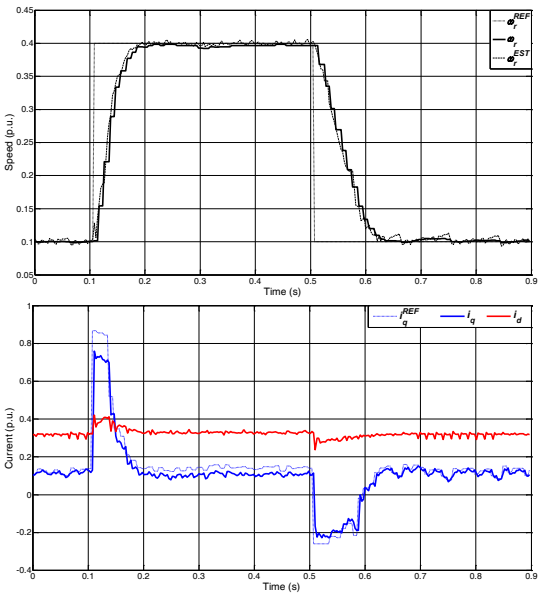


Fig. 23. DSP results: motor speed and dq-currents response for step reference ω_r^{REF} = *0,1 - 0,4 p.u.* – proposed current reconstruction method.

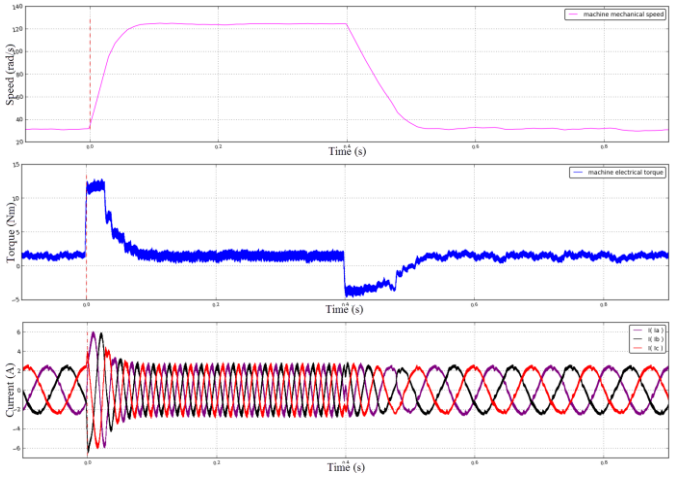


Fig. 24. HIL results: motor speed, torque and stator currents step response for ω_r^{REF}=*0,1-0,4 p.u.* – proposed current reconstruction method.

VII. Conclusion

Application of conventional line currents reconstruction method does not provide acceptable control quality and drive performance. The source of the problem is the distortion of the reconstructed motor currents. Distortion is caused by the nature of the employed method which samples dc-link current in different time instants related to the center of PWM period. Distortion in original abc-domain is reflected in the field-oriented reference frame dq-current components, which are further propagated through complete sensorless control structure. Results are increased oscillations in developed motor torque and speed, which can even cause unstable motor operation during transients.

Proposed solution of this problem does not use standard approach which introduces current filter blocks in the feedback path reducing the dynamic of complete control system. It is also completely independent on the machine model and parameters. It uses averaging of totally four dc-link current samples in two consecutive PWM periods, which significantly reduces the phase error and characteristic third and sixth harmonics in dq-current components. Average dc-link samples are referred to the same time instant which yields to the reconstructed current waveforms which are almost the same as actual measured values.

This paper verifies that proposed method reduces motor torque and speed oscillations to the acceptable level in the case when minimum number of sensors is used, and in conditions where all controller and estimator parameters are set for high-performance response. In future work proposed current reconstruction algorithm will be tested in various shaft-sensorless control structures.

Appendix

TABLE II
Controller Parameters

Symbol	Quantity	Value
f_{pwm}	PWM frequency	2 kHz
T_i	Current loop sampling period	1 ms
T_ω	Speed loop sampling period	10 ms
I_b	Current base value	7,02 A
U_b	Voltage base value	842,55 V
f_b	Frequency base value	100 Hz
ω_b	Angular frequency base value	628,32 rad/s
λ	Current loop dynamic parameter	300
K_{pi}	Current loop proportional gain	0,1357
K_{ii}	Current loop integral gain	0,0403
$K_{p\omega}$	Speed loop proportional gain	8,5716
$K_{i\omega}$	Speed loop integral gain	1,4851
i_q^{MAX}	Speed controller output positive limit	0,82 p.u. (1,45·I_n)
i_q^{MIN}	Speed controller output negative limit	-0,25 p.u.
K_{pf}	Flux compensator proportional gain	0,05
K_{if}	Flux compensator integral gain	0,00111
ω_{bw}	PLL filter bandwidth	300 Hz
K_{pp}	PLL filter proportional gain	26,657
K_{ip}	PLL filter integral gain	0,225

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Operational Transconductance Amplifier in 350nm CMOS technology

Dejan D. Mirković, Predrag M. Petković, Ilija Dimitrijević and Igor Mirčić

***Abstract*—This paper presents transistor level design of operational transconductance amplifier in CMOS technology. Custom designed, circuit is to be built-in into the mixed-signal, switched capacitor circuit. Amplifier targets relatively high slew-rate and moderate open loop gain with megahertz order gain-bandwidth. Adopted architecture is discussed appreciating application in switched capacitor circuits. Circuit behavior is examined through set of simulations. Obtained results confirmed desired behavior. Target technology process is TSMC 350nm.**

***Index Terms*—Integrated circuit, Amplifier, Switched capacitor circuits, CMOS technology**

Original Research Paper
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I. Introduction

OPERATIONAL amplifiers (OA) are considered to be the fundamental parts of analog electronics. Moreover, it is one of the very first circuits with successful tape-out designed in LEDA laboratory in early nineties [1], [2]. OAs appears as inevitable part for analog signal conditioning. Switched capacitor (SC) circuits are not exception. Design covered in this work is meant to be embedded into analog part of the second order ΔΣ analog-to-digital converter (ADC) discussed in [3]. Being part of SC circuits the OA requires relatively high slew-rate and gain-bandwidth. As shown in [4], open loop i.e. DC gain has the smallest influence, comparing to slew-rate and gain bandwidth, on SC circuit characteristics. Therefore moderate open loop gain is sufficient. Because all circuitry will be on-chip, Operational Transconductance Amplifier (OTA) is required. Table I summarizes main OTA design parameters set by the higher order circuit requirements.

Parameters like, input/output dynamic range (DR), common mode (CMRR) and power supply (PSRR) rejection ratios should be as large as possible.

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TABLE I
TARGET OTA PARAMETERS

Parameter	Description	Value
A_0	DC, open loop, gain	> 50 dB
f_{gbw}	Gain-bandwidth	> 120 MHz
SLR	Slew rate	> 120 V/μs

Since TSMC 350nm technology process supports relatively high, 3.3V, power supply voltage DR requirements are expected to be fulfilled.

Circuit supposed to be fully differential which implies utilizing some form of common-mode feedback (CMFB) circuitry. Besides, OTA has to have its own bias point generator in order to provide appropriate transistor operation. Since on-chip capacitors are considered, 2pF differential load capacitance is adopted. This value is also set by higher order circuit requirements concerning kT/C noise of ΔΣ structure explained in [4]. It should be mentioned that target technology process offers Poly-insulator-Poly (PiP) capacitors with 864 aF/μm^2 capacitance per unit area. Hence the value of 2 pF for load capacitance gives reasonably high capacitor area of 2314.81 μm^2 (48.11μm x 48.11μm).

Paper is organized as follows. In second section adopted OTA architecture will be briefly discussed and appropriate subsections will cover circuitry in more details. Third section presents simulation results. Finally, in the fourth section, educative conclusions are drawn and possible improvements are discussed.

II. OTA Architecture

The first step in structural design was to define circuit's architecture. It is well known that cascoding technique is quite often used when high DC gain and PSSR are required without scarifying circuit's dynamics [5]. Although folded cascode (FC) architecture is commonly adopted for building SC circuits; telescopic architecture is chosen for OTA design in this case. Some related work supporting this idea is published in [6], [7]. It is well known that FC provides wider input common-mode range, better input-output common mode relation and high input/output swing [8]. All those advantages imply higher power consumption; lower gain; higher noise and, most importantly in this case, lower speed (i.e. slew-rate and gain-bandwidth). Choosing telescopic architecture means

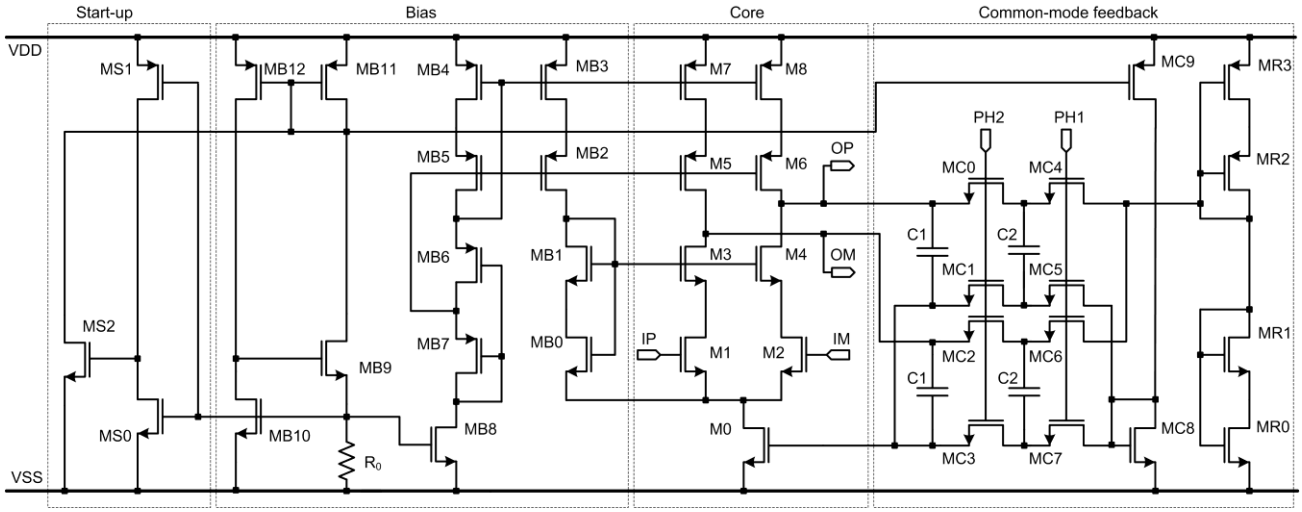

Fig. 1. Telescopic OTA with bias and SC CMFB circuitry.

TABLE II
TRANSISTOR DIMENSIONS

Transistors	width/length [μm/μm]
(M1, M2, M3, M4), (M0, M5, M6, M7, M8)	(128/0.8), (256/0.8)
(MB1, MB8), (MB2, MB3, MB4, MB5, MB7, MB10, MB9),(MB11, MB12), MB0,MB6, MS0, (MS1, MS2)	(128/0.8), (256/0.8), (512/0.8), 24/0.8, 88/0.8, 400/0.8, (4/0.8)
(MC0, MC1, MC2, MC3, MC4, MC5, MC6, MC7, MC8), MC9	(1.6/0.8), 3.2/0.8
(MR1, MR3), MR2, MR0	(2.4/0.8), 7.2/0.8, 0.8/0.8

stricter constraint on input/output common-mode voltage choice. Transistor level schematic of OTA with bias and CMFB circuitry is depicted in Fig. 1. Dimensions of all transistors are summarized in Table II. Design can be partitioned in three sub-blocks namely: Core, Bias with start-up and CMFB.

A. Core

Transistors M0-M8 are the core of the design. Analyzing structure utilizing small-signal model open loop gain is:

$$A_0 \approx g_{m1,2}\left(g_{m3,4}r_{03,4}r_{01,2} \parallel g_{m5,6}r_{05,6}r_{07,8}\right) \quad (1)$$

Cascode configuration by itself provides large DC gain and (1) is expected to meet the DC gain requirements. Being single stage, there is no need for frequency compensation. Stability is also guaranteed by relatively large, 2pF differential load capacitance, C_L. Therefore gain-bandwidth is mainly determined by transconducatance of amplifying devices, $g_{m1,2}$, and load capacitance ratio. Design procedure is as follows. Transconductance of M1 and M2 devices should satisfy the following equation:

$$g_{m1,2} = 2\pi f_{gbw} C_L . \quad (2)$$

For given gain-bandwidth and load capacitance, g_m equals to about 1.5mS. Taking into account fully differential case this value is doubled. In order to properly size amplifying devices set of simulations at room temperature were done. Diagrams shown in Fig. 2, 3 and 4 present obtained results. All those curves are extracted using SPICE [9].

Fig. 2 is created by simulating diode connected device.

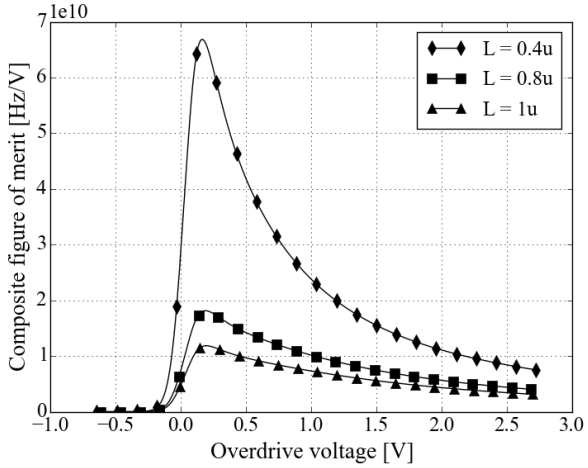

Fig. 2. Composite figure of merit versus overdrive voltage.

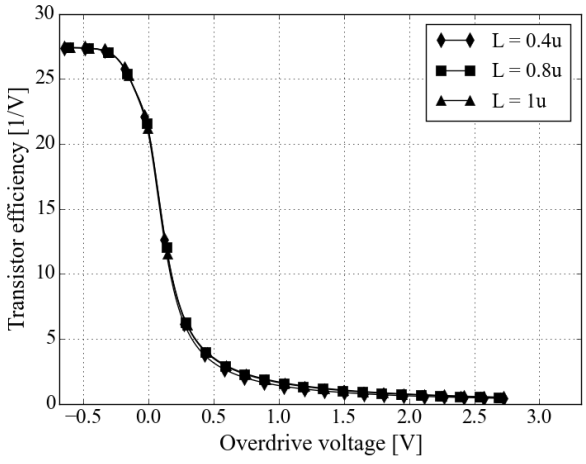

Fig. 3. Transistor efficiency versus overdrive voltage.

It shows composite figure of merit defined as $f_t \times (g_m/I_D)$ versus overdrive voltage, $V_{ov}=V_{GS} - V_{TH}$, where, f_t, is unity current gain frequency and g_m/I_D transistor efficiency. Observing Fig. 2 and Fig. 3 for different channel lengths one can find optimal V_{ov} bias point which compromises between

speed i.e. maximal transistors's operating frequency and efficiency. This value is about 200mV.

Knowing this, the channel current can be extracted. Namely, for overdrive voltage of 200mV Fig. 3 indicates the efficiency of about $10V^{-1}$ which gives the channel current I_D= 300μA.

To pick suitable channel length one should observe Fig. 4 which shows small signal gain, a_{v0}, versus drain-source voltage of the MOS device in target technology for different channel lengths. It is notable that shorter channel lengths give relatively constant a_{v0} in wide dynamic range. On the other hand a_{v0} reduces significantly as length decrees. It is obvious that there is a tradeoff between dynamic range and gain.

If (1) is heavily approximated assuming equal transconductances/resistances, A_0 reduces to $(g_m r_0)^2 = a_{v0}^2$. Picking the L= 0.4μm gives a_{v0} not lower than 20 times in reasonably high dynamic range i.e. 1-3V. Therefore the total gain would be $A_0 \approx 400$ or roughly 52dB. After this value is adopted as good enough the following should be appreciated. Firstly, (1) is heavily approximated and secondly short channel effect is always present. Therefore to mitigate short channel effects, and to ensure gain higher than 50dBs, L= 0.8μm is adopted.

It is also estimated, again using SPICE, that there is a 3.75 μA drain current per 1μm of channel width for chosen transistor efficiency (10) and channel length (0.8μm) in the target technology. Drain current per unit of channel width, I_D/W, versus transistor efficiency is depicted in Fig. 5. Accordingly, for 300μA current the minimal width of amplifying devices is W= 80 μm resulting with width-length ratio of 100. This value sets the initial dimensions and the dimensions of all other transistors are drawn based on it. Eventually, final dimensions end up being larger in order to fully meet requirements given in Table I.

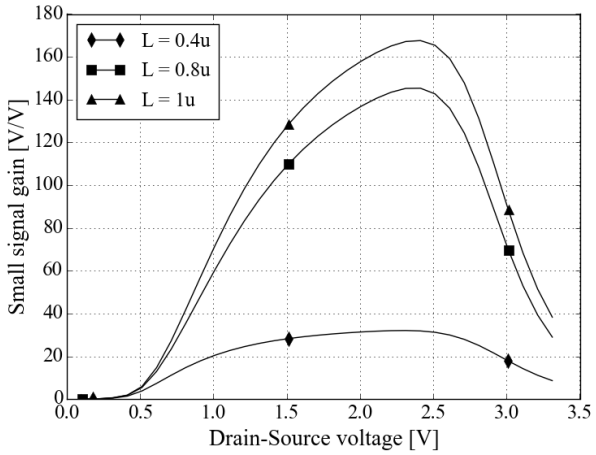

Fig. 4. Small signal gain versus drain-source voltage.

It should be emphasized that these curves are exclusively used to build intuition of how device behaves in various biasing conditions. In other words they serve as guidelines for setting initial design values. Therefore, the designer has the freedom to chose a set of curves which best matches his/hers problem and/or intuition. In this work the most useful ones are covered.

B. Bias with Start-up

Bias circuit is composed of transistors denoted as MB0-MB12 in Fig. 1. Reference current is generated using independent, self biased, V_{TH} reference. This reference uses the fact that sensitivity of the active device voltage to the power supply change is always less than unity. This is governed by square root relation between transistors overdrive voltage and drain current.

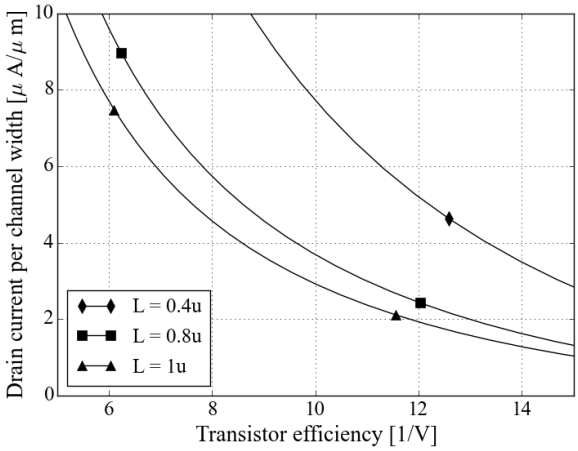

Fig. 5. Drain current per channel width versus transistor's efficiency.

When the circuit is arranged to generate current through an active device according to the overdrive voltage controlled with the same current, result is reference which is for all practical purposes independent of V_{DD}. In this case it is done with transistors MB9-MB12 and resistor, R_0. Practically the gate-source voltage of MB10 equals to voltage drop across R_0 produced by the current trough MB9. Simultaneously it defines drain current value of MB10 which is mirrored back into drain current of MB9 thorough MB11/12 current mirror. This loop provides sustainable reference mainly dependent on R_0 resistance.

From one side current, I_0, in MB9/11 branch is limited by resistor R_0. On the other hand the very same current sets overdrive voltage of MB10. Therefore, equation (3) holds. All values in (3) are referred to transistor MB10.

$$I_0 R_0 = V_{TH} + \sqrt{\frac{2I_0}{\mu_0 C'_{ox}(W/L)}} \tag{3}$$

where μ_0 stands for mobility and C'_{ox} denotes gate oxide capacitance pre unity area. Expressing R_0 from (3), and appreciating relation $g_m^2 = 2\,\mu_0\,C'_{ox}\,(W/L)\,I_0$ (4) arises.

$$R_0 = \frac{V_{TH}}{I_0} + \frac{2}{g_m} \tag{4}$$

Choosing I_0= 600μA (tail source M0), g_m = 6mS (assuming relatively constant overdrive voltage of M0/MB10) and

knowing that V_{TH} for NMOS device in the target technology is about 0.78V, it comes that the value for R_0 is 1.63kΩ. This value is reduced to 1.2kΩ trading power consumption for better dynamics.

Since the reference voltage is self-biased there is a need for start-up circuit to prevent zero current state. Start-up circuit is designed with transistors MS0-MS2. If there is a zero current in the circuit the voltage at R_0 is low. This low state feeds the MS0/1 inverter which turns on MS2 and provides the low potential at the gates of PMOS MB11/12. This condition opens the path for the current to flow from power supply towards R_0. Consequently, voltage at the MB10 gate increases. Inverter triggers once again turning the MS2 off. It is important to emphasis that the size of MS0 should be much greater than the size of MS1. This way the overdrive voltage of MS0 is quite small, allowing inverter to trigger with lower voltage than $V_{DD}/2$. This ensures that inverter drives MS2 to cutoff.

The reset of the bias circuitry (MB0-MB8) serves to distribute generated reference to appropriate points. Transistors MB3-MB5 form high swing cascode current mirror biased with MB6/7 Sooch structure [10]. Transistors MB0 and MB1 are used in similar manner to bias M3/4.

C. Common Mode Feedback

OTA will be used within SC circuit driven with two non-overlapping, clocking signals at f_s sampling rate, named *Phi*1 and *Phi*2. Therefore, CMFB is accomplished with NMOS switches MC0-MC7 and four capacitors (two C_1 and two C_2) [11]. Transistor MC9 mirrors reference current while MC8 converts it into the voltage, V_{Nbias}, appropriate for biasing tail current source i.e. core transistor M0. Desired common-mode voltage is set slightly above $V_{DD}/2$ using sooch voltage divider, MR0-MR3. CMFB voltage, V_{CMFB}, is formed at the gate of core transistor, M0. Circuit's operation can be unveiled by analyzing charge transfer during two, non-overlapping phases. When *Phi*1 signal is active, switches MC0-MC3 are *off* and MC4-MC7 are *on*. In this case total charge on the capacitors is:

$$Q_{Phi1} = 2(V_{CM} - V_{Nbias})C_2 + (V_{OP} - V_{CMFB})C_1 + (V_{OM} - V_{CMFB})C_1. \quad (5)$$

During the second clock phase, *Phi*2 (MC0-MC3 *on* and MC4-MC7 *off*), total charge becomes:

$$Q_{Phi2} = (C_1 + C_2)(V_{OP} - V_{Nbias}) + (C_1 + C_2)(V_{OM} - V_{CMFB}). \quad (6)$$

Since charge in both clock phases has to be the same, net value of V_{CMFB} over two clock phases can be obtained by equating (5) and (6):

$$V_{CMFB} = \frac{V_{OP} + V_{OM}}{2} - V_{CM} + V_{Nbias} = V_{OCM} - V_{CM} + V_{Nbias}, \quad (7)$$

where V_{OCM} is the actual output common-mode voltage. If e.g. V_{OCM} starts to increases comparing to V_{CM} there is a small, positive increment superposed to ideal V_{Nbias} for biasing gate voltage of M0. Since M0 is common source stage in this signal path drain voltage of M0 decreases. Voltage drop at M0's drain is further transferred through two common-gate stages M1/2 and M3/4 opposing the initial V_{OCM} increase. Inverse reaction takes place if V_{OCM} deviates from V_{CM} in other direction. In this way negative feedback is formed which, over time, averages V_{OCM} to V_{CM}.

To determine adequate values for C_1 and C_2 capacitance two tradeoffs should be analyzed.

The first tradeoff puts bound on C_1 value. This capacitance is lumped together with OTA's load capacitance during active phase *Phi*1. Actually, OTA is only used during this phase for amplifying the input signal. At the same time desired common-mode voltage is sampled at C_2. This implies that C_1 capacitance value should be smaller than C_L in order not to deteriorate OTA dynamics. On the other hand its value should also be large enough to differ from MOS parasitic caps (particularly C_{gd}), otherwise stored charge, i.e. voltage, on it will not be preserved during the sampling period. Using SPICE analysis, C_{gd} capacitance of M5/6 and M3/4 output transistors is estimated to about 40fF, contributing in total with 80fF to the output node of OTA. Therefore, 500fF is adopted for C_1 as a tradeoff between MOS parasitic and loading effect of the OTA output.

Second tradeoff addresses C_2/C_1 ratio. During phase *Phi*2 the output common-mode voltage is corrected by tying C_1 and C_2 in parallel. Then the charge stored on these two capacitors will redistribute among each other equating the voltage on them. As a result the final voltage on parallel capacitance at the end of phase *Phi*2, V_{eq}, will be:

$$V_{eq} = \frac{k}{k+1}(V_{CM} - V_{Nbias}) + \frac{1}{k+1}(V_{OCM} - V_{CMFB}), \quad (8)$$

where $k = C_2/C_1$. Fig. 6 shows output common-mode voltage versus time for different values of k and sampling frequency f_s = 16.77 MHz.

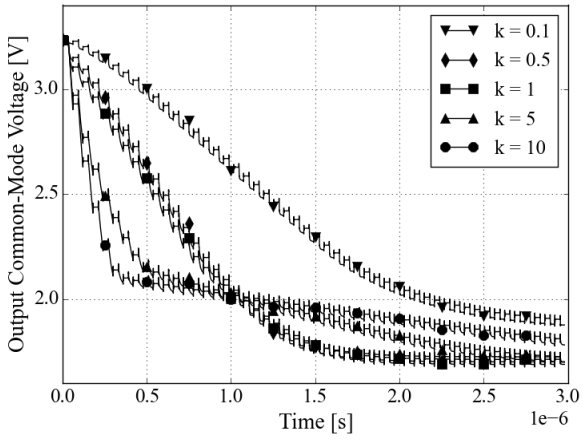

Fig. 6. Settling of output common-mode voltage.

The amount of CMFB voltage is tuned with C_2/C_1 ratio. First term in (8) represents well defined, fixed value, increment which is added to the unregulated, second term.

For $k > 1$ (i.e. $C_2 > C_1$) first term dominates, increments are larger and the output common-mode stabilization is expected to be obtained sooner. However these large increments usually force output to slew resulting output to actually settle later. For $k < 1$ increments are smaller and output common-mode stabilization comes later in time but in more controlled manner. One can clearly see that there is a tradeoff between settling of output voltage around desired common-mode value, slewing and the amount of CMFB applied. As a result of this tradeoff k=1 i.e. C_2 = 500fF is chosen. Also, it can be concluded that k= 0.5 gives similar response and even smaller value for C_2 capacitance (250fF). Still, this value approaches parasitic capacitances jeopardizing first tradeoff mentioned earlier.

III. Simulation Results

Circuit's behavior is examined through set of various simulations in SPICE. Results for nominal PVT (Process, Voltage, Temperature) conditions at room temperature are summarized in Table III.

TABLE III
SIMULATED OTA CHARACTERISTICS

Param.	Description	Condition	Value
A_0	DC, open loop gain	open loop/closed loop[a]	57.6 dB
Φ_M	Phase margin	open loop/closed loop	83 °
f_{GBW}	Gain-bandwidth	open loop closed loop	140 MHz 126 MHz
SLR	Slew rate	closed loop, excitation:	190 V/μs
t_S	Settling time	pulse, ±(*ICMR*/2) V, 100kHz	16.6 ns
V_{OMAX}	Maximum output swing	closed loop, excitation: sine, ± 3.3 V, 1MHz	± 1.83 V
PSRR	Power supply rejection ratio	open loop, from V_{DD} open loop, from V_{SS}	215 dB 218 dB
CMRR	Common-mode rejection ratio	open loop, from V_{CM}	240 dB
ICMR	In. common-mode range	open loop closed loop	4 mV 2.54 V
OCMR	Out. common-mode range	open loop closed loop	1.92 V 2.74 V
V_{OCM}	Out. common-mode voltage	open loop/closed loop	1.7 V

[a]Unity gain feedback configuration

As can be seen from Table III, target design requirements concerning open loop gain, gain-bandwidth and slew rate are met. It can be also noted that circuit is slightly overdesigned. This is to leave some margin for PVT variations and noise which will inevitable arise at layout/physical level.

Even open loop analysis confirms stability it is of curtail importance to check circuit's closed loop behavior. This is done by using famous Middlebrook method, where instead open loop, total loop gain is examined [11]. Results are graphically presented in Fig 7.This method is considered to be the most trustable when examining stability of feedback systems. It is also favorable because there is no need to break feedback loop hence bias points are not corrupted.

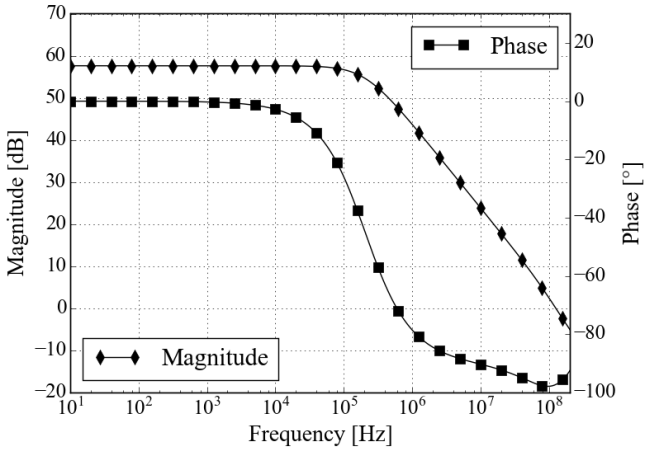

Fig. 7 Total loop gain (Magnitude and Phase) versus frequency.

Usually leading CAD vendors, implement this method into its simulation software (e.g. Cadence® Spectre, *iprobe* component in conjunction with *stb* simulation directive). Nevertheless, diving into the [12] one can build its own SPICE deck for implementing the method.

Good circuit dynamics are paid with burning extra power. Total power of the circuit is quite high and it is estimated to P_{TOT}= 9.77mW. Since fully differential, power-supply and common-mode rejection ratios are quite high as expected. Usage of high swing bias cascodes resulted with satisfactory output swing.

IV. Conclusion

This paper presents one design example of OTA circuit considering CMOS 350nm technology process. Designed circuit is to be integral pat of ΔΣ ADC. Adopted architecture is discussed with emphasis on individual sub-blocks namely: Core, Common-Mode Feedback and Bias with start-up. Design procedure of each sub-block is given, as well. For this purpose a set of useful curves is extracted using SPICE giving the insight into MOS device behavior in target technology process. Important design tradeoffs are drawn based on those curves. Transistor level simulation results are presented and discussed. Based on these results one can conclude that circuit meets severe dynamic requirements while preserving stability. Consequently power consumption is increased hence design could be further optimized in this direction.

Acknowledgment

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Instructions for Authors

First A. Author, Second B. Author, and Third C. Author

***Abstract*—These instructions give you guidelines for preparing papers for ELECTRONICS journal. Use this document as a template if you are using Microsoft *Word* 6.0 or later. Otherwise, use this document as an instruction set. The electronic file of your paper will be formatted further. Define all symbols used in the abstract. Do not cite references in the abstract. Do not delete the blank line immediately above the abstract; it sets the footnote at the bottom of this column.**

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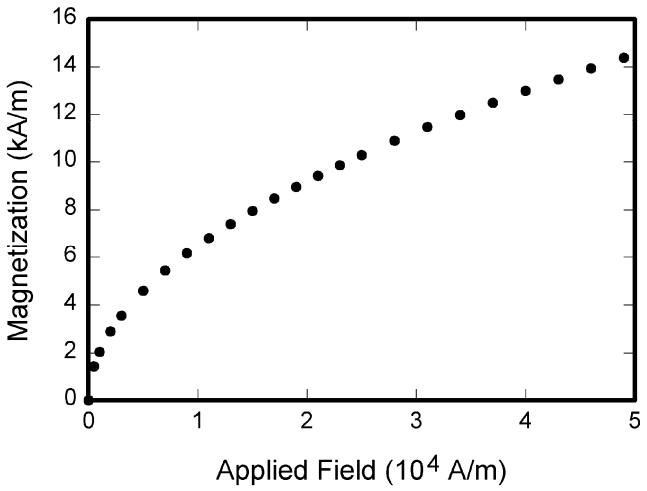

Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

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Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). **This applies to papers in data storage.** For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception is when English units are used as identifiers in trade, such as "3½-in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

TABLE I
Units for Magnetic Properties

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb = 10^{-8} V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T = 10^{-4} Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 = 10^{-3} J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	$1 \rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	$1 \rightarrow 4\pi \times 10^{-7}$ H/m = $4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	$1 \rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a] Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

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Because we will do the final formatting of your paper, you do not need to position figures and tables at the top and bottom of each column. In fact, all figures, figure captions, and tables can be at the end of the paper. Large figures and tables may span both columns. Place figure captions below the figures; place table titles above the tables. If your figure has two parts, include the labels "(a)" and "(b)" as part of the artwork. Please verify that the figures and tables you mention in the text actually exist. **Please do not include captions as part of the figures. Do not put captions in "text boxes" linked to the figures. Do not put borders around the outside of your figures.** Use the abbreviation "Fig." even at the beginning of a sentence. Do not abbreviate "Table." Tables are numbered with Roman numerals.

Color printing of figures is not available Do not use color unless it is necessary for the proper interpretation of your figures.

Figure axis labels are often a source of confusion. Use words rather than symbols. As an example, write the quantity

"Magnetization," or "Magnetization *M*," not just "*M*." Put units in parentheses. Do not label axes only with units. As in Fig. 1, for example, write "Magnetization (A/m)" or "Magnetization ($A \cdot m^{-1}$)," not just "A/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K."

Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) × 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

B. References

Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use "Ref. [3]" or "reference [3]" except at the beginning of a sentence: "Reference [3] shows ... ." Please do not use automatic endnotes in *Word*, rather, type the reference list at the end of the paper using the "References" style.

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Capitalize only the first word in a paper title, except for proper nouns and element symbols. For papers published in translation journals, please give the English citation first, followed by the original foreign-language citation [8]. All references **must be** written in Roman alphabet.

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Define abbreviations and acronyms the first time they are used in the text, even after they have already been defined in the abstract. Abbreviations such as IEEE, SI, ac, and dc do not have to be defined. Abbreviations that incorporate periods should not have spaces: write "C.N.R.S.," not "C. N. R. S." Do not use abbreviations in the title unless they are unavoidable (for example, "IEEE" in the title of this article).

[1]It is recommended that footnotes be avoided (except for the unnumbered footnote with the receipt date and authors' affiliations on the first page). Instead, try to integrate the footnote information into the text.

D. Equations

Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). First use the equation editor to create the equation. Then select the "Equation" markup style. Press the tab key and write the equation number in parentheses. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Use parentheses to avoid ambiguities in denominators. Punctuate equations when they are part of a sentence, as in

$$\int_0^{r_2} F(r,\varphi)\, dr\, d\varphi = [\sigma r_2 / (2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\, |z_j - z_i|)\, \lambda^{-1} J_1(\lambda r_2)\, J_0(\lambda r_i)\, d\lambda \,. \tag{1}$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature, but T is the unit tesla). Refer to "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ... ."

E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm × 0.2 cm," not "0.1 × 0.2 cm^2." The abbreviation for "seconds" is "s," not "sec." Do not mix complete spellings and abbreviations of units: use "Wb/m^2" or "webers per square meter," not "webers/m^2." When expressing a range of values, write "7 to 9" or "7-9," not "7~9."

A parenthetical statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.) In American English, periods and commas are within quotation marks, like "this period." Other punctuation is "outside"! Avoid contractions; for example, write "do not" instead of "don't." The serial comma is preferred: "A, B, and C" instead of "A, B and C."

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VI. Some Common Mistakes

The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A

graph within a graph is an “inset,” not an “insert.” The word “alternatively” is preferred to the word “alternately” (unless you really mean something that alternates). Use the word “whereas” instead of “while” (unless you are referring to simultaneous events). Do not use the word “essentially” to mean “approximately” or “effectively.” Do not use the word “issue” as a euphemism for “problem.” When compositions are not specified, separate chemical symbols by en-dashes; for example, “NiMn” indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas “Ni–Mn” indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones “affect” (usually a verb) and “effect” (usually a noun), “complement” and “compliment,” “discreet” and “discrete,” “principal” (e.g., “principal investigator”) and “principle” (e.g., “principle of measurement”). Do not confuse “imply” and “infer.”

Prefixes such as “non,” “sub,” “micro,” “multi,” and “ultra” are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the “et” in the Latin abbreviation “*et al.*” (it is also italicized). The abbreviation “i.e.,” means “that is,” and the abbreviation “e.g.,” means “for example” (these abbreviations are not italicized).

An excellent style manual and source of information for science writers is [9].

VII. Editorial Policy

Each manuscript submitted is subjected to the following review procedure:

- It is reviewed by the editor for general suitability for this publication
- If it is judged suitable, two reviewers are selected and a single-blinded review process takes place
- Based on the recommendations of the reviewers, the editor then decides whether the particular paper should be accepted as is, revised or rejected.

Do not submit a paper you have submitted or published elsewhere. Do not publish “preliminary” data or results. The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

Every paper submitted to “Electronics” journal are single-blind reviewed. For conference-related papers, the decision to accept or reject a paper is made by the conference editors and publications committee; the recommendations of the referees are advisory only. Undecipherable English is a valid reason for rejection.

VIII. Publication Principles

The contents of “Electronics” are peer-reviewed and archival. The “Electronics” publishes scholarly articles of archival value as well as tutorial expositions and critical reviews of classical subjects and topics of current interest.

Authors should consider the following points:

1) Technical papers submitted for publication must advance the state of knowledge and must cite relevant prior work.
2) The length of a submitted paper should be commensurate with the importance, or appropriate to the complexity, of the work. For example, an obvious extension of previously published work might not be appropriate for publication or might be adequately treated in just a few pages.
3) Authors must convince both peer reviewers and the editors of the scientific and technical merit of a paper; the standards of proof are higher when extraordinary or unexpected results are reported.
4) Because replication is required for scientific progress, papers submitted for publication must provide sufficient information to allow readers to perform similar experiments or calculations and use the reported results. Although not everything need be disclosed, a paper must contain new, useable, and fully described information. For example, a specimen’s chemical composition need not be reported if the main purpose of a paper is to introduce a new measurement technique. Authors should expect to be challenged by reviewers if the results are not supported by adequate data and critical details.
5) Papers that describe ongoing work or announce the latest technical achievement, which are suitable for presentation at a professional conference, may not be appropriate for publication in “Electronics”.

IX. Conclusion

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

Appendix

Appendixes, if needed, appear before the acknowledgment.

Acknowledgment

The preferred spelling of the word “acknowledgment” in American English is without an “e” after the “g.” Use the singular heading even if you have many acknowledgments. Avoid expressions such as “One of us (S.B.A.) would like to thank ... .” Instead, write “F. A. Author thanks ... .” **Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.**

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